Harnessing ML and Agentic AI for Co-packaged Optics Co-optimization in 3D Heterogeneous Integration

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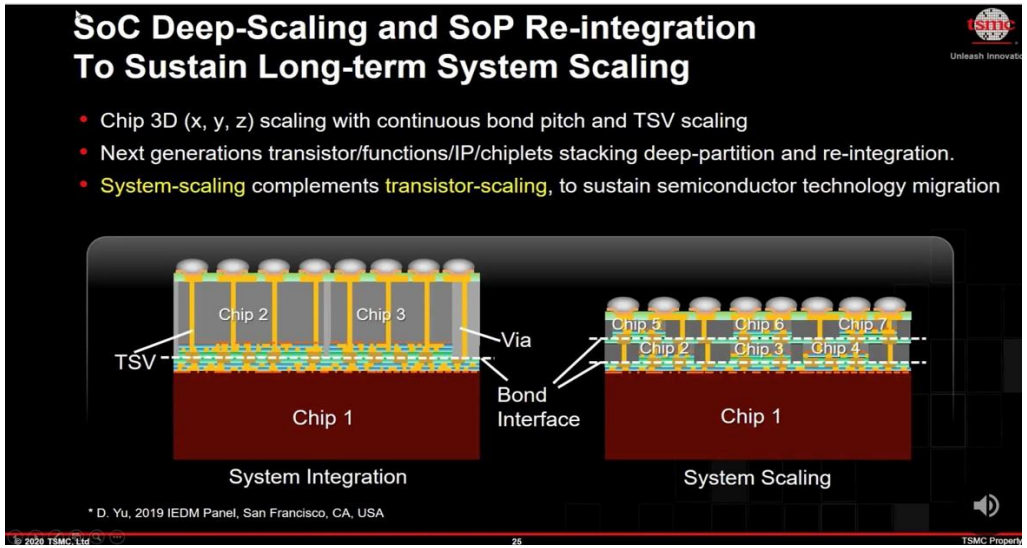
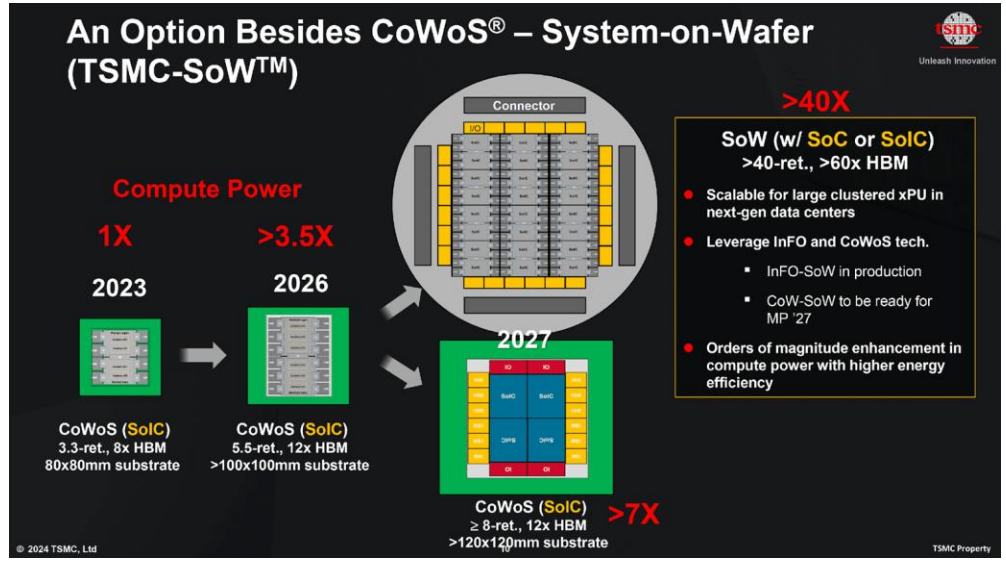
EDPS, 2025

Aggressive System Scaling with 3DHI Requires Multiphysics Solution

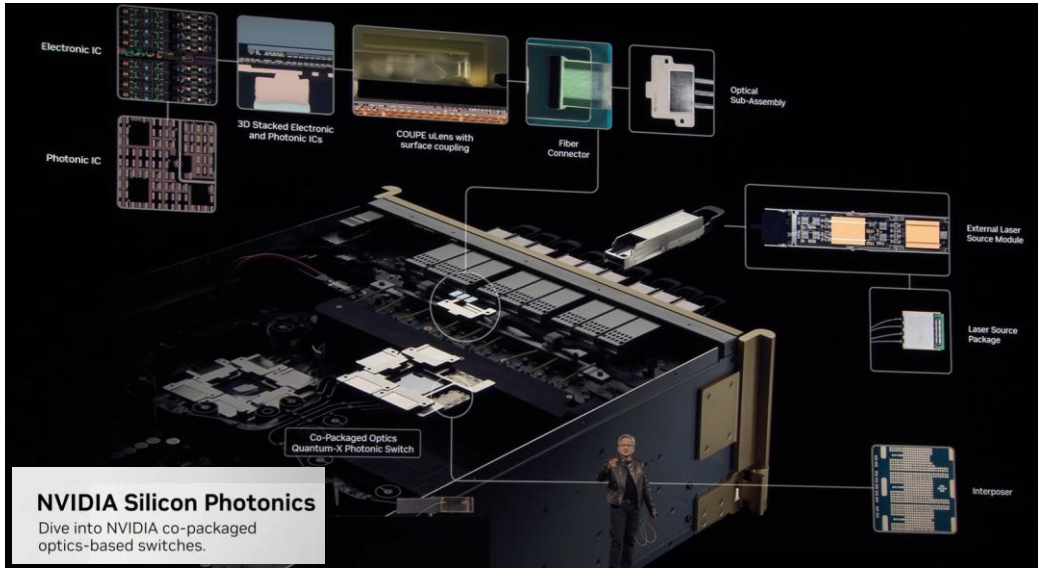




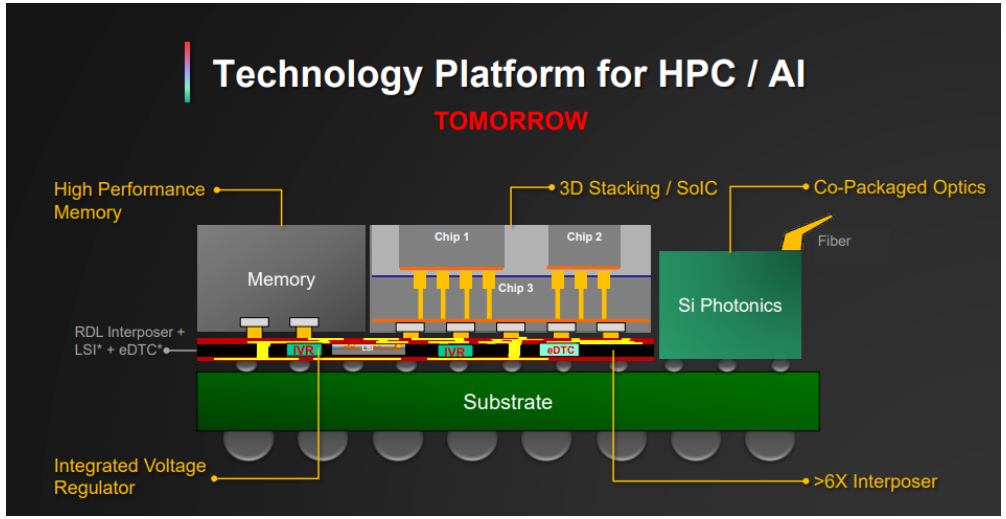
Courtesy of TSMC, 2024

SoIC innovative bump-less bonding

Doug Yu, TSMC, ECTC keynote, 2020
Focusing on PPAT



Jensen Huang, Nvidia CEO, GTC Keynote, March 2025

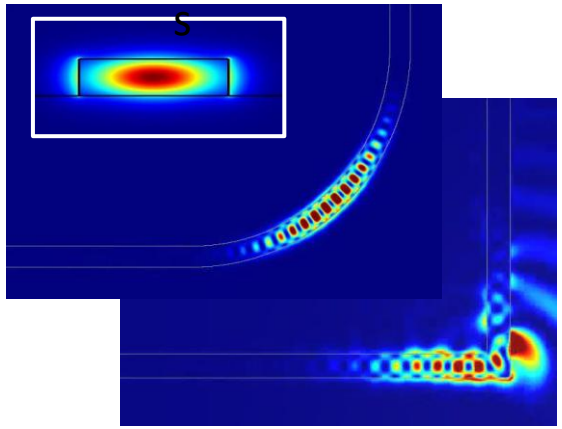


Kevin Zhang, TSMC, ISSCC keynote, 2024

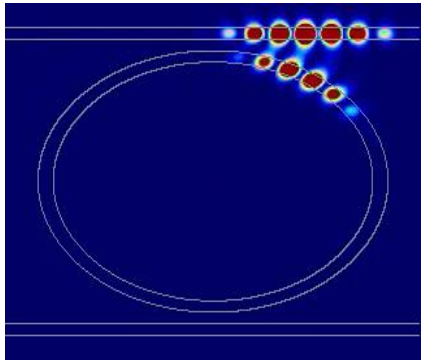
Silicon Photonics in Co-Packaged Optics (CPO)

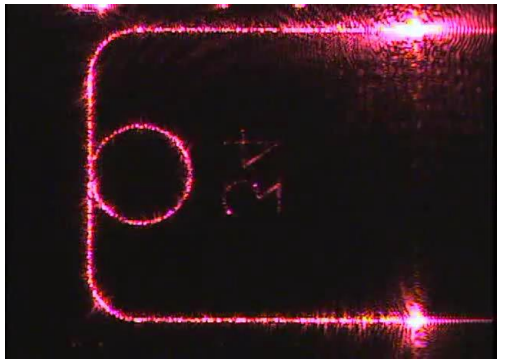
- Light (photons) propagating inside a Silicon-On-Insulator (SOI) waveguide

Waveguide



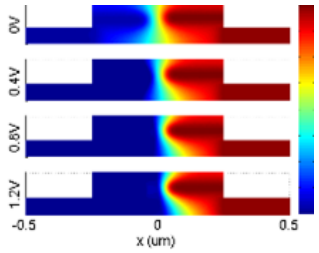
Microring resonators

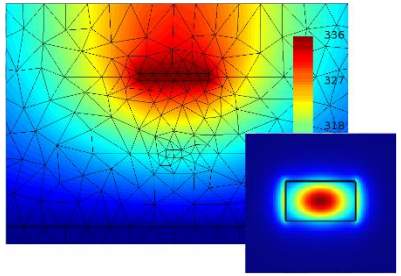




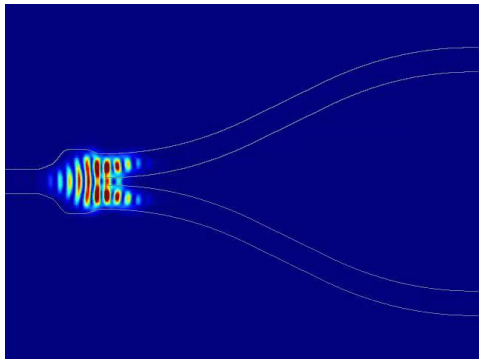
Measurement Data, Di Liang, U. of Michigan

Electrical/thermal phase control

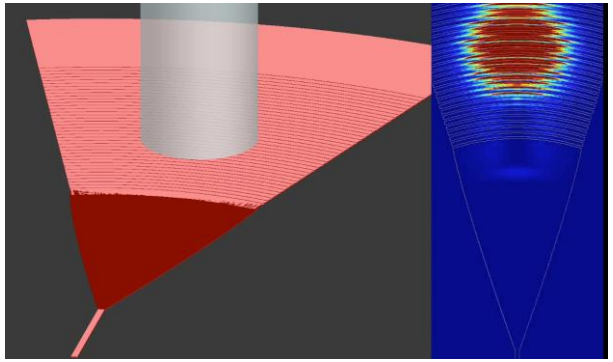




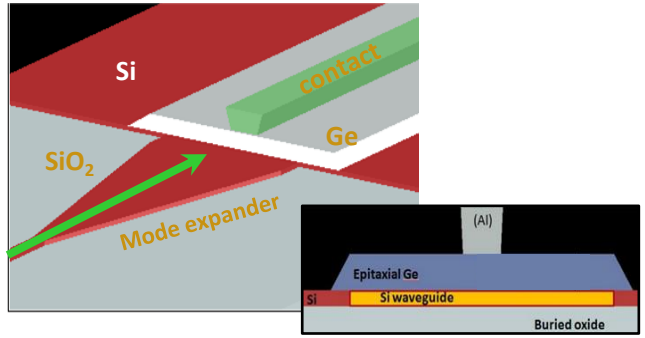
Waveguide coupling/splitting



Fiber-waveguide coupling



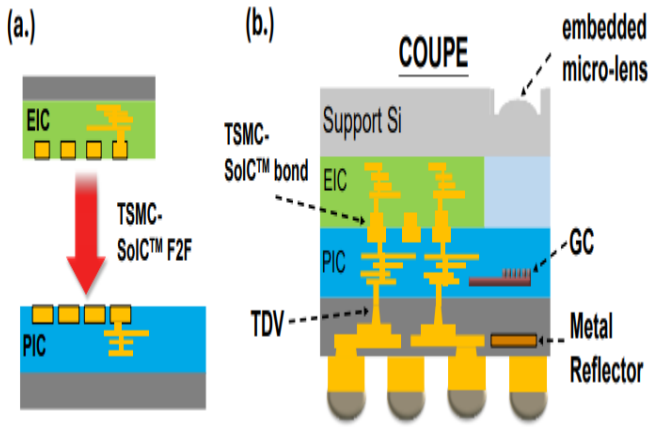
Photodetector



"TSMC COUPE™ Photonic Integrated Circuit Co-Design with Custom Verilog-A and PDK TMI Models Using Synopsys Tools", P. Samadian, TSMC OIP 2025

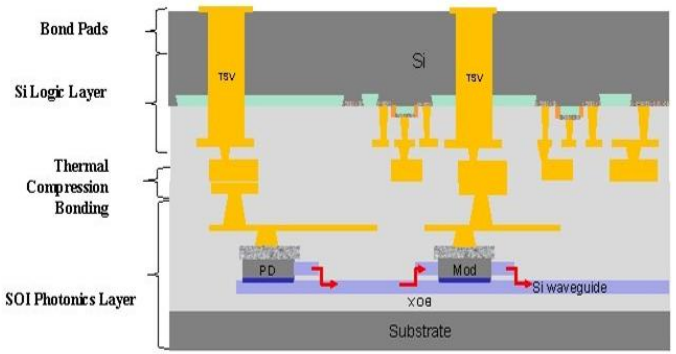
Ansys part of SYNOPSYS®

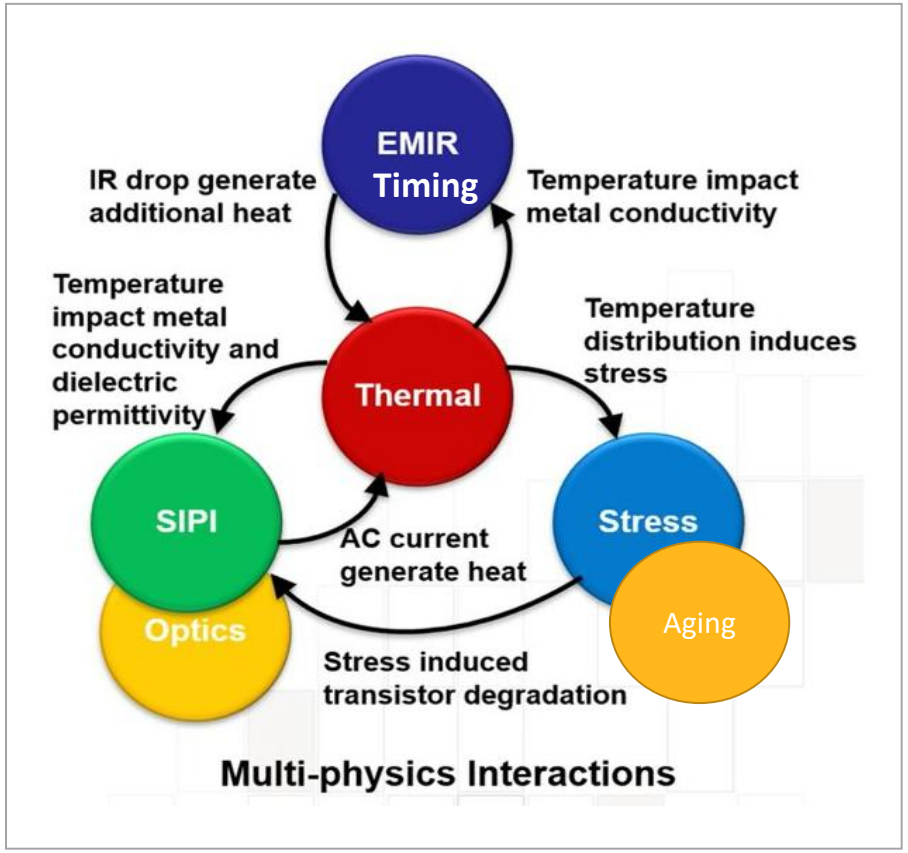
Significant Multiphysics Challenge in CPO with TSMC COUPE



"Optical and Electrical Characterization of a Compact Universal Photonic Engine", TSMC, ECTC 2025

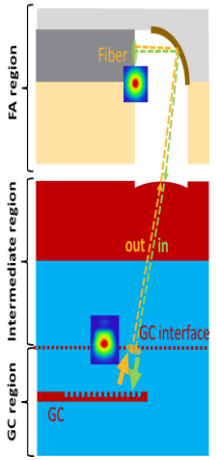
Cross die electromagnetics



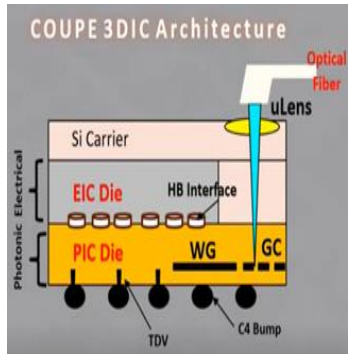


Courtesy of TSMC

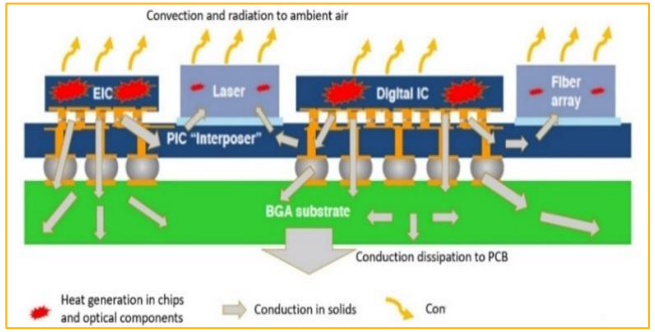
Optical I/O and photonic device simulation



Increased IR drop & electromigration



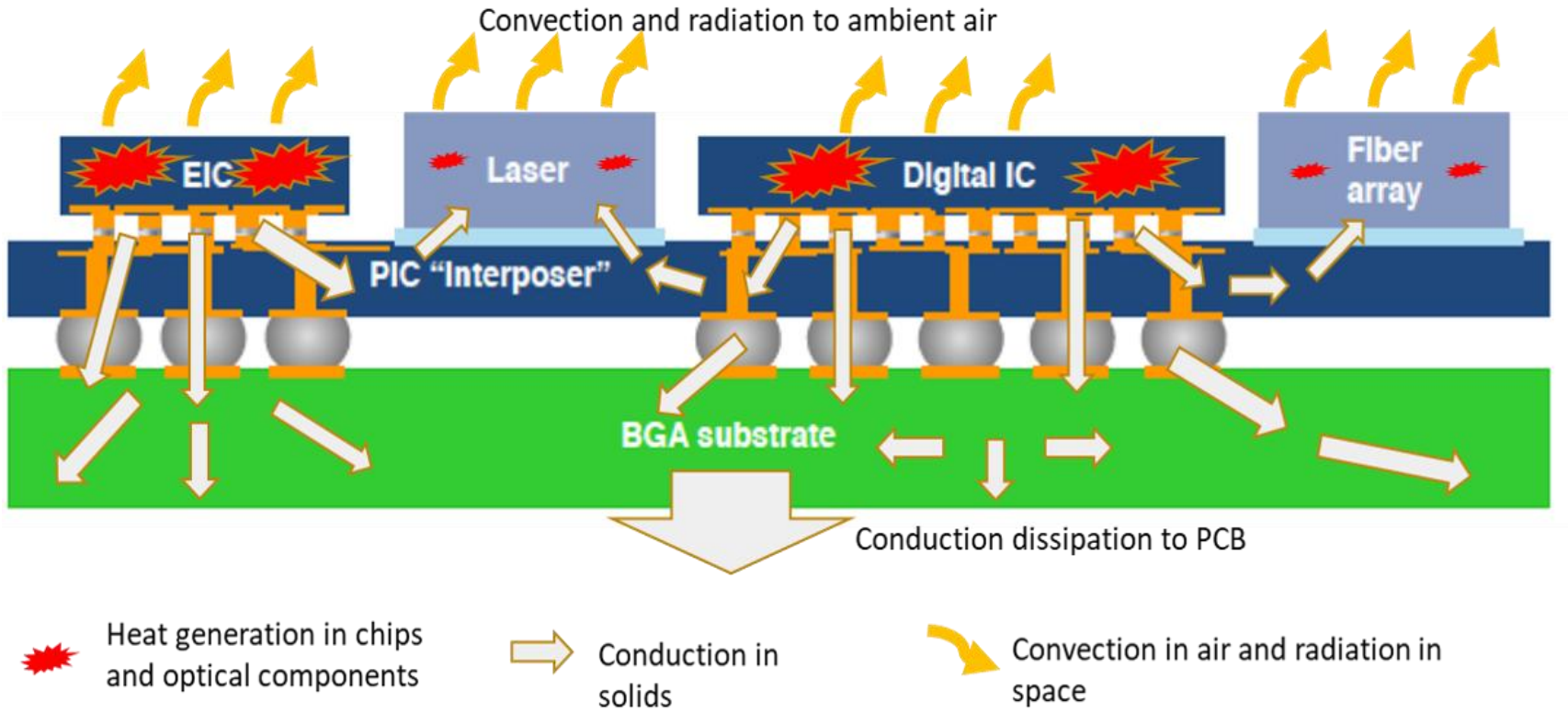
Coupled Thermal and Stress



Ansys part of SYNOPSYS®

Challenge: Thermal Simulation is Critical for Silicon Photonics

- Solving for Digital IC and EIC on heat generation
- Solving for PIC Package: heat generation, dissipation, and thermal couplings of chips and optical components



Full 3DIC thermal simulation inc. heaters

↓

Temperature map in the Si Interposer layer

↓

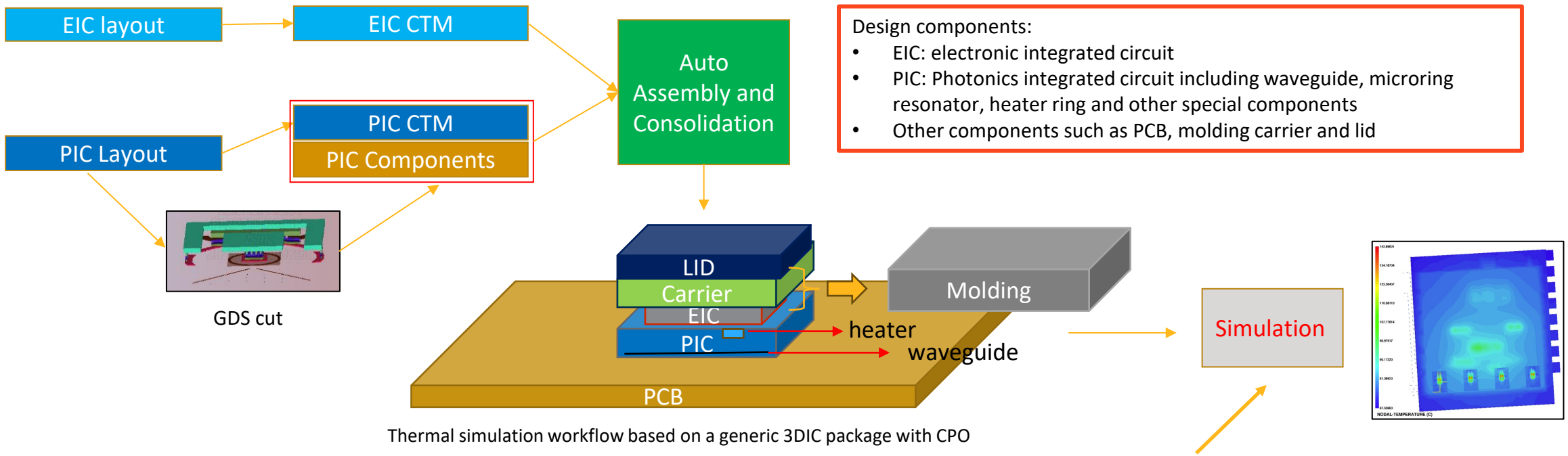
Update local temperature of each photonic device

↓

Run photonic circuit simulation

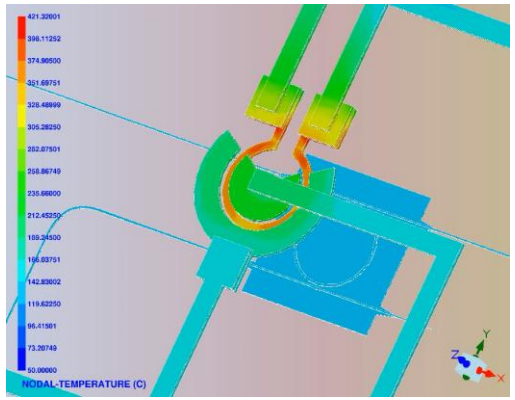
"Electronic-Photonic IC Co-Design with Signal/Power Integrity and Thermal Simulation for Silicon Photonic 3D IC", J. Youn, J. Pond, N. Chang, et al., best paper candidate, DesignCon 2021
"Towards an Automated Workflow for Link-level Exploration and Optimization in the Domain of All-to-all Optical Networks", L. Ramini, A. Alam, Design Track, DAC, 2022
"A PVT-robust Design with Electronic/Photonic Co-simulation Engine for Microring-based DWDM 3D Silicon Photonics", C. Hong, A. Alam, J. Pond, et al., Design Track, DAC, 2024

Thermal Integrity Workflow: Overview



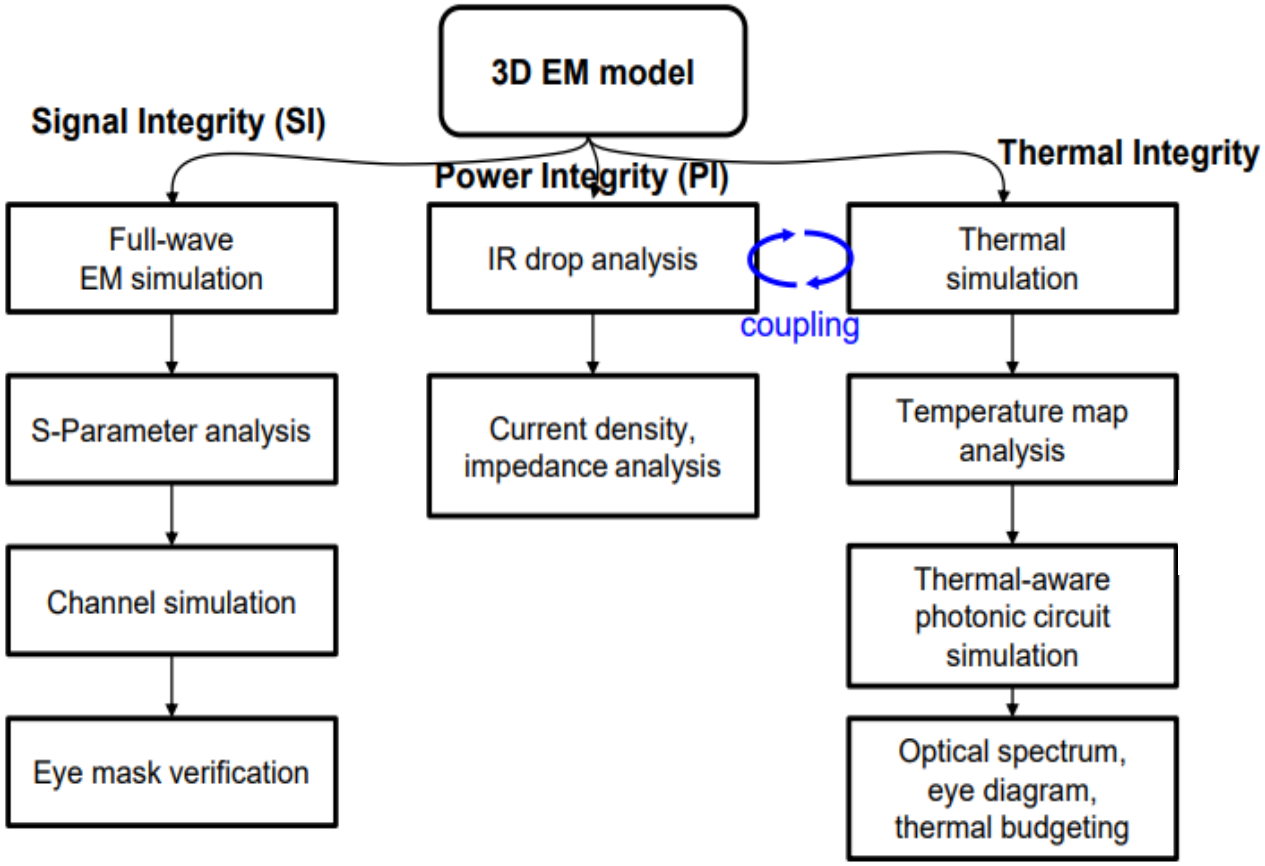
Thermal simulation workflow based on a generic 3DIC package with CPO

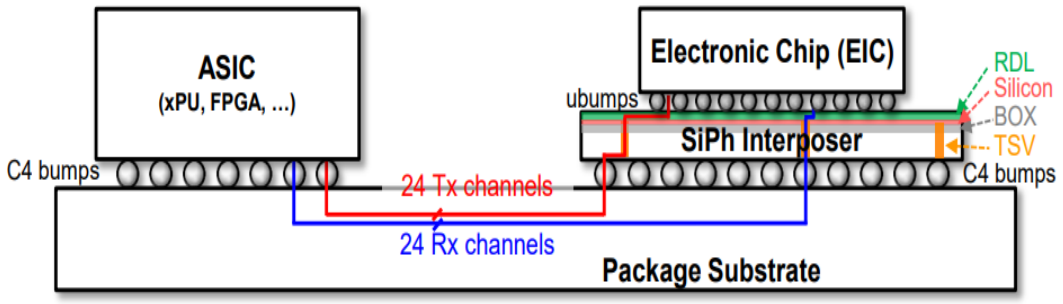
- Highlights
  - Computationally efficient due to use of CTMs
  - Accurate thermal map for PIC by preserving geometries of critical photonic components
  - Automated flow for stacking/aligning multi-die package

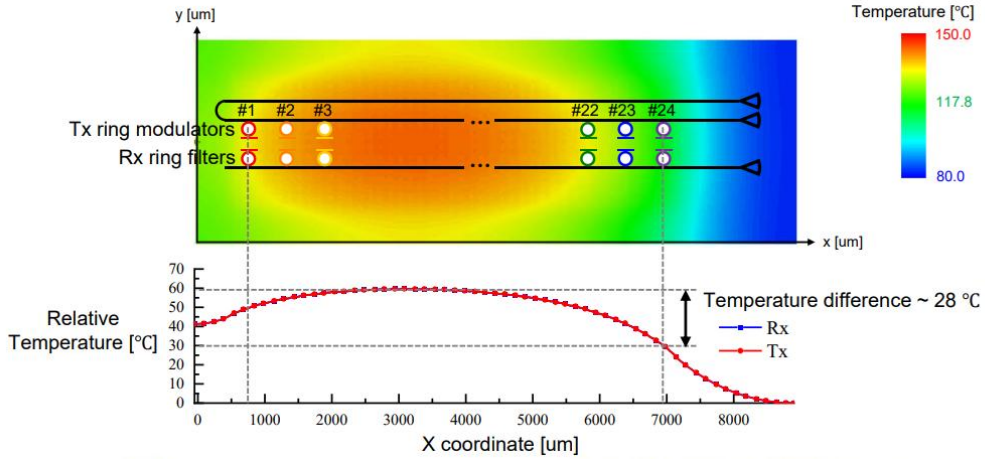


CPO Thermal Simulation

Electronic-Photonic 3DHI Co-design Methodology



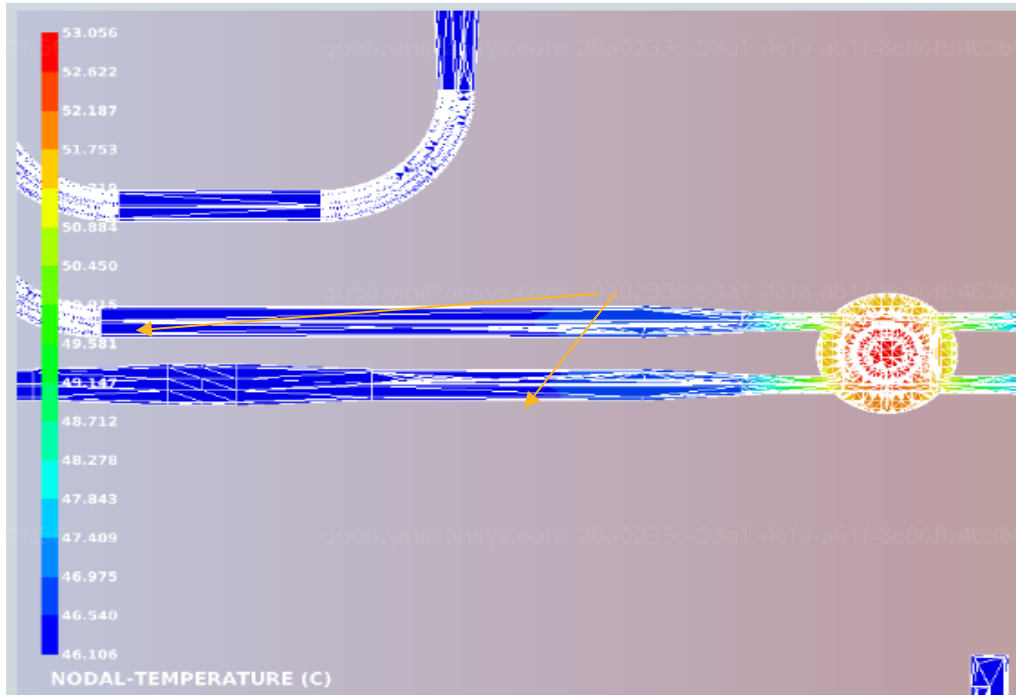




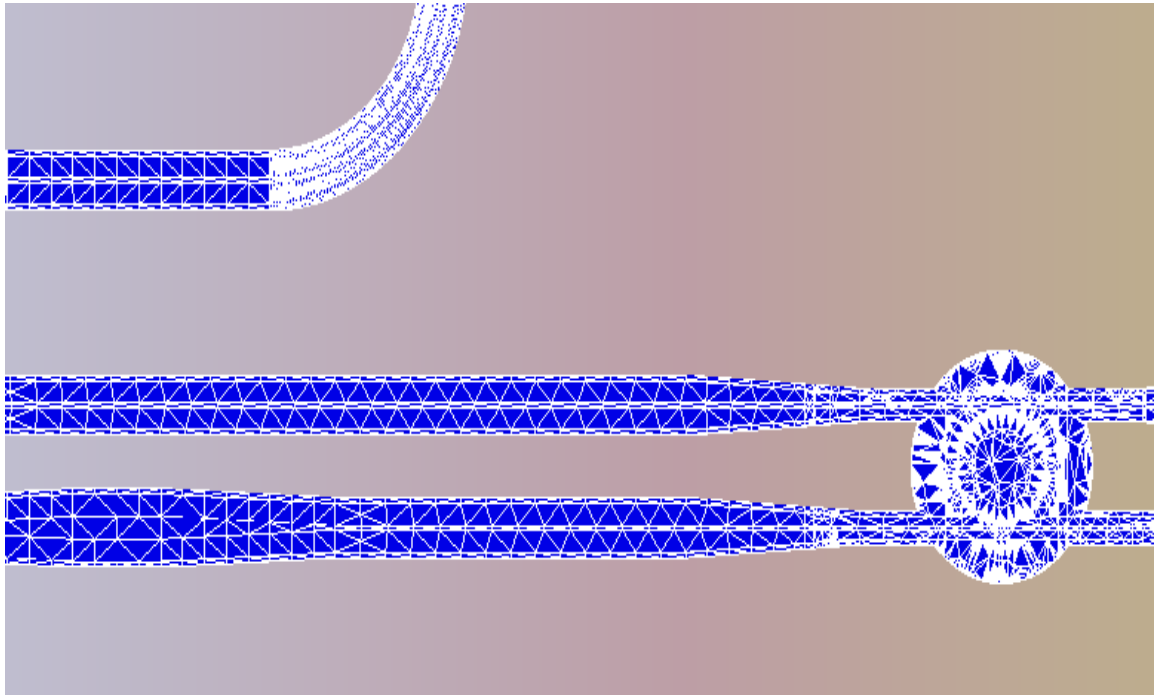
"Electronic-Photonic IC Co-Design with Signal/Power Integrity and Thermal Simulation for Silicon Photonic 3D IC", J. Youn, J. Pond, N. Chang, et al., best paper candidate, DesignCon 2021

Challenge on Optimized Mesh for Waveguide Structures

- To ensure the accuracy, mesh complicated layout to ensure good quality of FEA (finite element analysis)

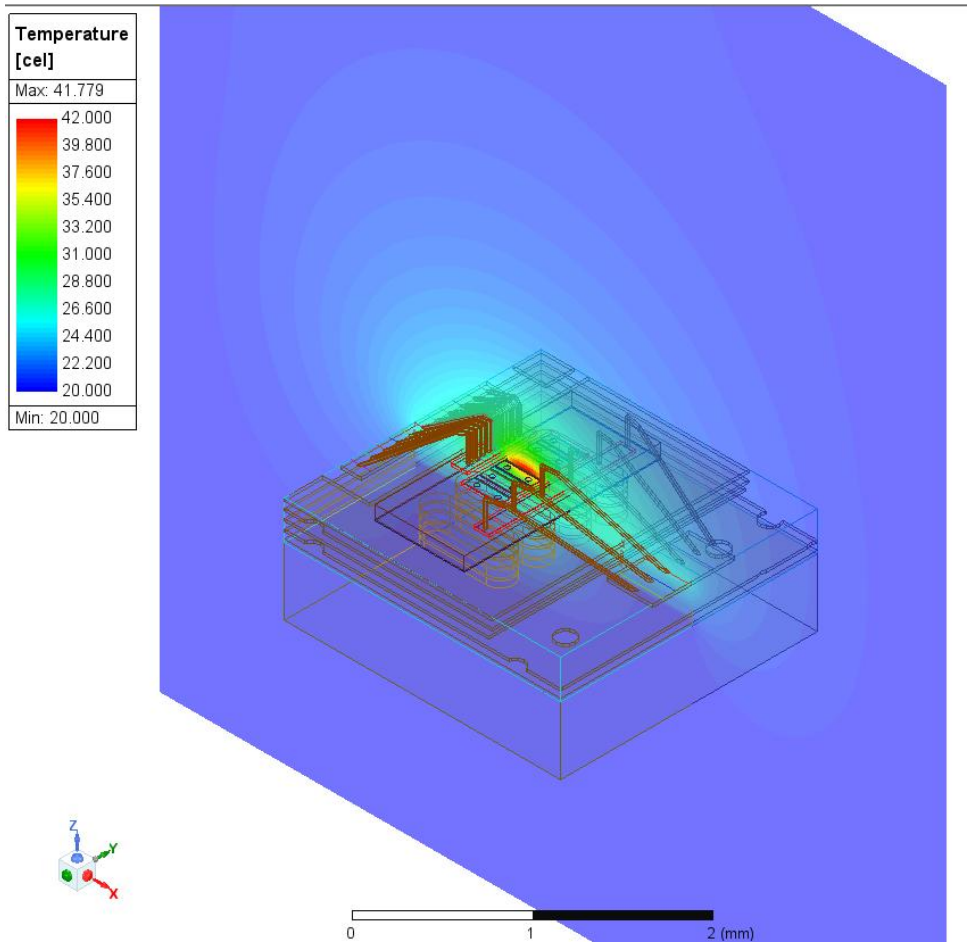


Irregular shapes with non-optimized mesh

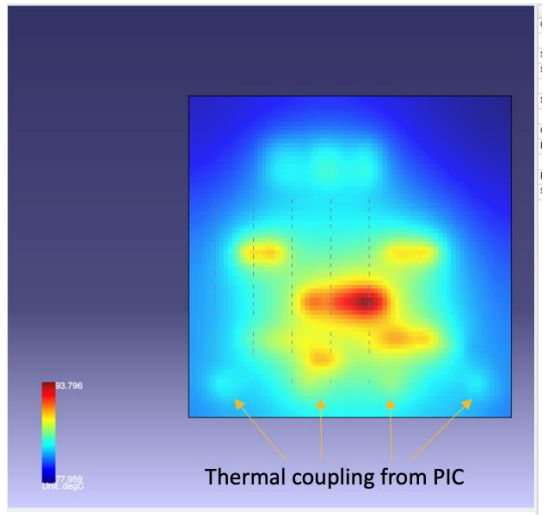


Optimized mesh result

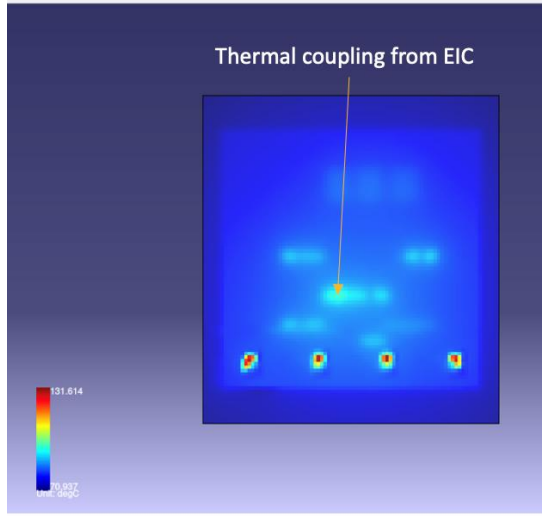
3DHI CPO Thermal Simulation Result w/ PIC and EIC Coupling Result



3DHI CPO Thermal Simulation Result



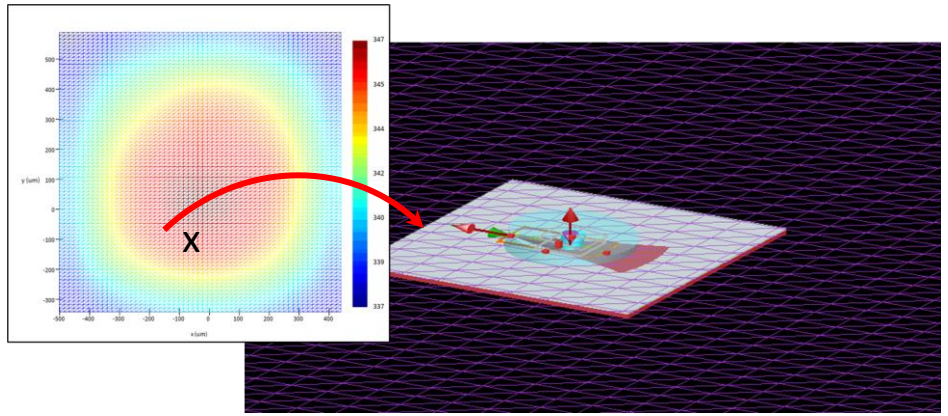
EIC



PIC

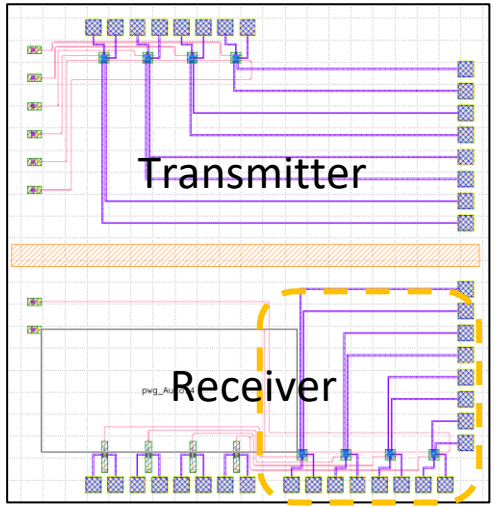
Thermal-Aware PIC Design

- Import temperature maps from thermal simulations into the photonic circuit simulator
- Use thermally aware compact models (e.g., ring resonators in receivers)
- Capture resonance shifts from thermal cross-talk
- Assess package temperature impact on performance (e.g., grating coupler spectrum shift)

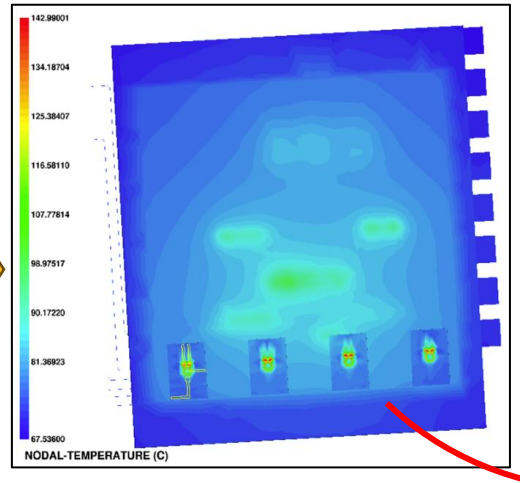


Importing temperature map into FDTD simulation of a grating coupler

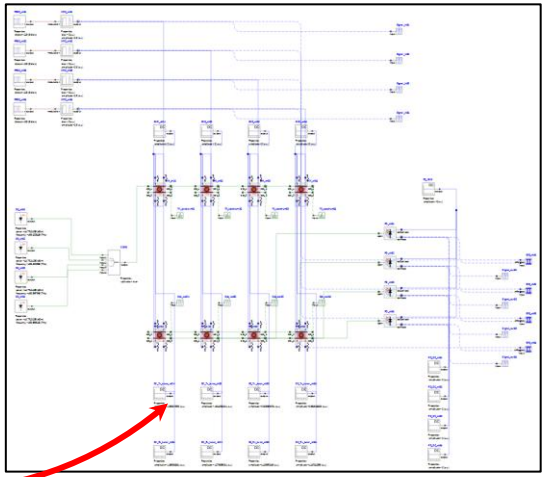
Layout of 4-channel WDM example circuit in PIC

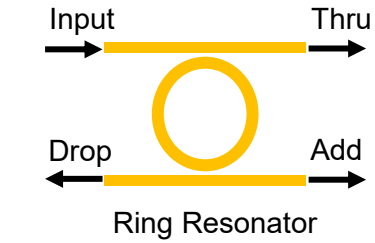


PIC temperature map of WDM receiver with thermal crosstalk from EIC

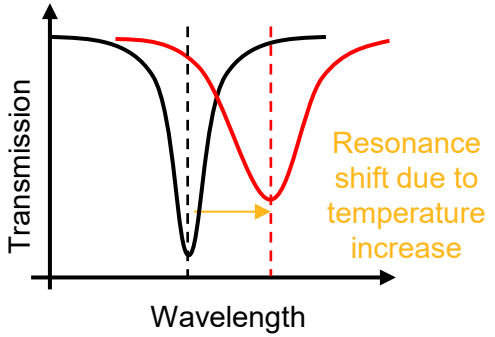


Schematic of 4-channel WDM circuit





Ring Resonator



"Accurate Thermal Simulation of 3DIC Package with Co-Packaged Optics", A. Alam, et al, DAC 2025

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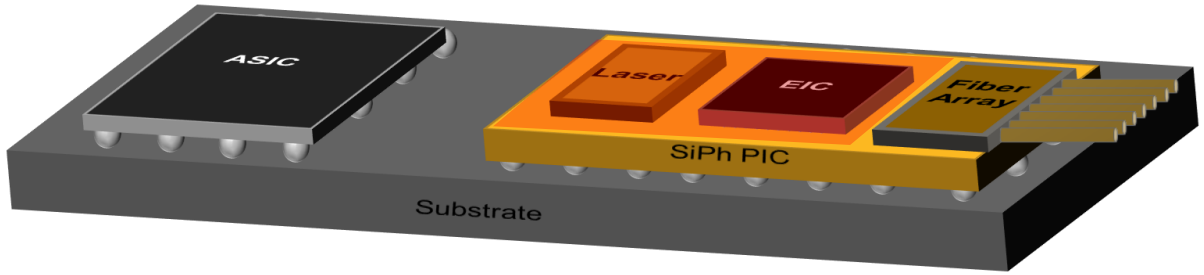
Comprehensive Multiphysics Solutions for CPO Needed

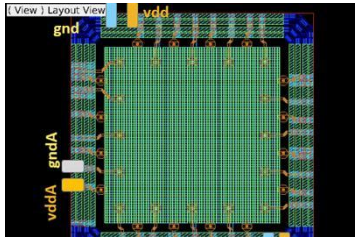
Thermal Management

RHSC / Totem / RHSC-ET / Icepak / Lumerical



ESD Analysis

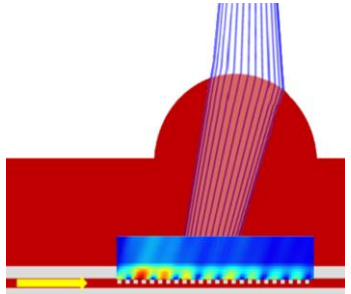
Pathfinder SC



Thermal Aware

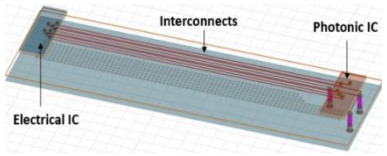
Optical Input/Output

Lumerical / Zemax



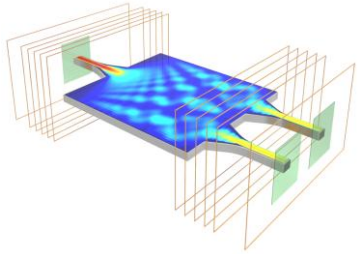
Signal Integrity

RaptorX / HFSS / Lumerical



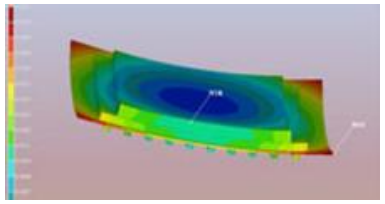
Photonic Components

Lumerical



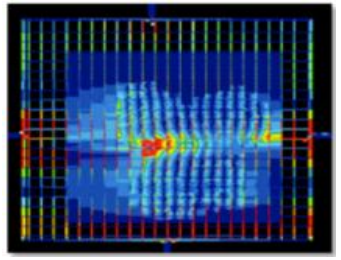
Structural Integrity

Mechanical / RHSC ET



EMIR

Totem / RHSC



Structural Aware

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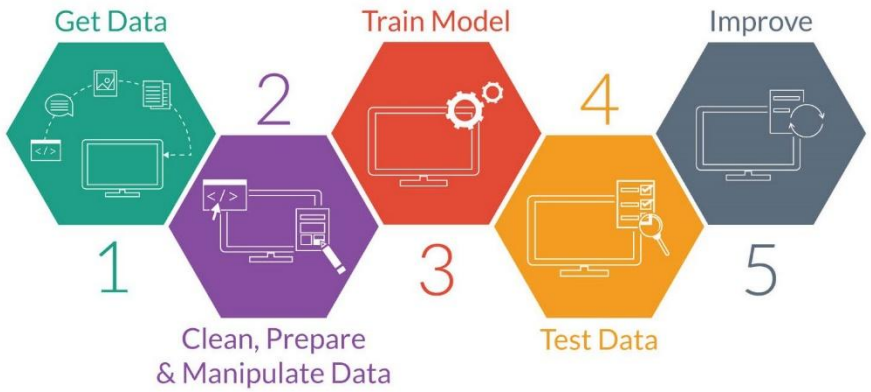
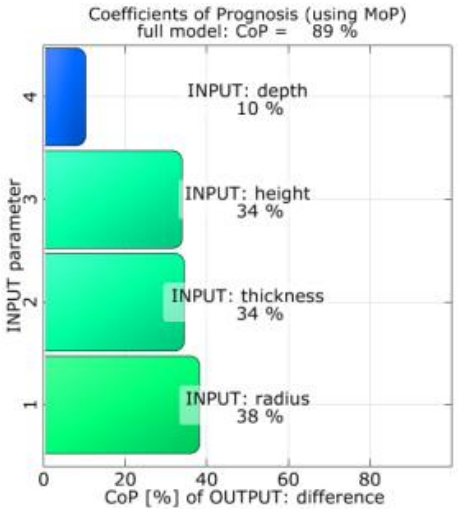
Auto-ML Framework Needed for System Technology Co-optimization

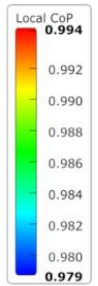


Adaptive Meta-Model of Optimal Prognosis (AMOP) for scalar values:

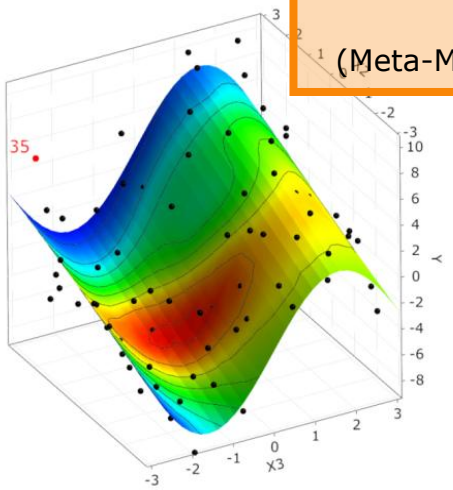
- Objective measure of prognosis quality = Coefficient of Prognosis (CoP)
- Determination of relevant parameter subspace
- Determination of optimal approximation model
- Approximation of solver output by fast surrogate model without over-fitting
- Evaluation of variable sensitivities

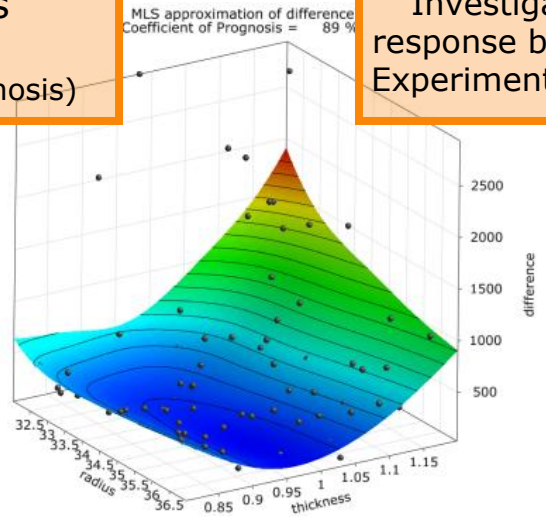
Calculate forecast quality using **CoP** (Coefficient of Prognosis)





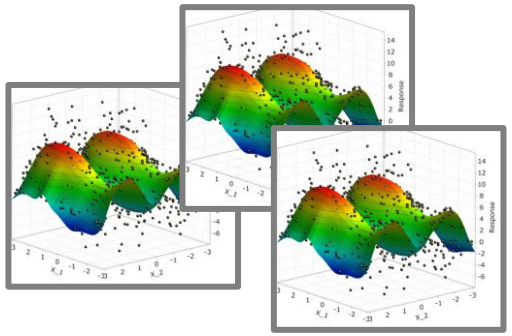
The winner is … **MOP** (Meta-Model of Prognosis)





Investigate response by response based on Design of Experiments (DOE) sampling

Generate competing meta-models



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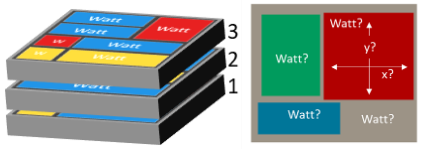
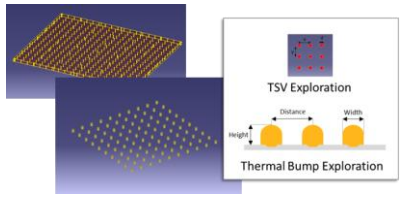
ML-Based Power & Thermal Design Space Exploration for System Technology Co-optimization (STCO)

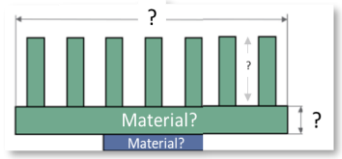
CTM, other power source



Die/pkg/pcb/tsv/bump model



Heatsink, Boundaries model



✓ **Bill of Material**
✓ **Architecture**

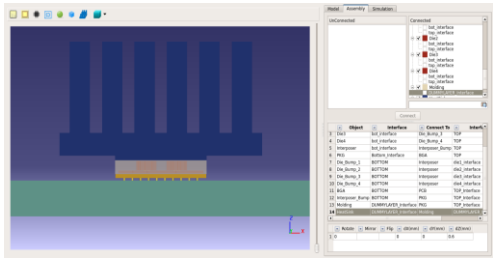
✓ **Performances**
✓ **Cost**

Exploration module
Power, Heatsink, BC

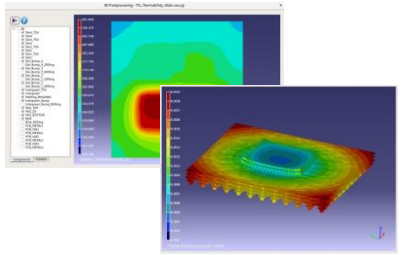
Goals setting
Max T°, Gradient, Warpage…

/ML Optimizer

Model Assembly → Static, Transient → Temp contour, Thermal Stress, …



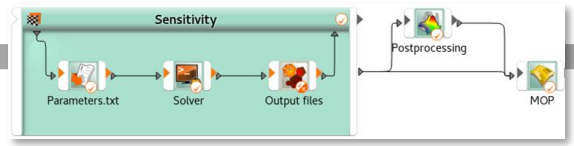
Thermal/ Stress Solvers



Results Postprocessing
✓ **Warpage**
✓ **T°$_{Max}$** (EM)
✓ **ΔT°** (Timing)

/ML Optimizer

Sensitivity Analysis

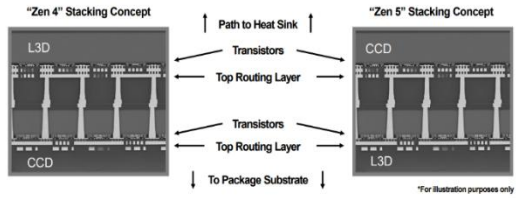


Variable Sweeping

ML-based Meta-model Training

"Zen 5" AMD 3D V-Cache™

- Thermal benefits when L3D moved below the CCD
- +500MHz Base and +200MHz Boost Frequency[4] vs. "Zen 4" 3D V-Cache™



T. Singh, et al., AMD, ISSCC, 2025

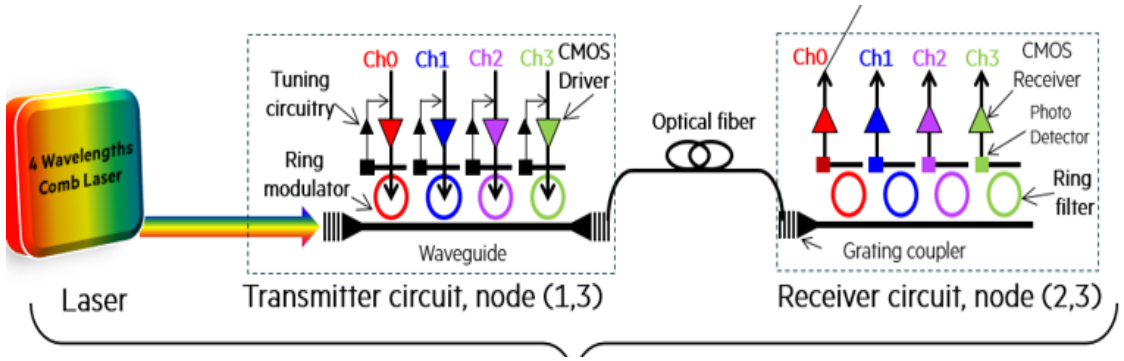
- Examples of desired system technology co-optimization
  - TSV pitch and placement for better thermal management, dynamic IR drop, and EM
  - Thermal-aware chiplet/block placement to minimize vertical thermal coupling
  - Warpage/stress sensitivity for analog and thermal-aware STA in global timing paths
  - Thermal-aware EMAG analysis, signal integrity, and SiPh performance optimization

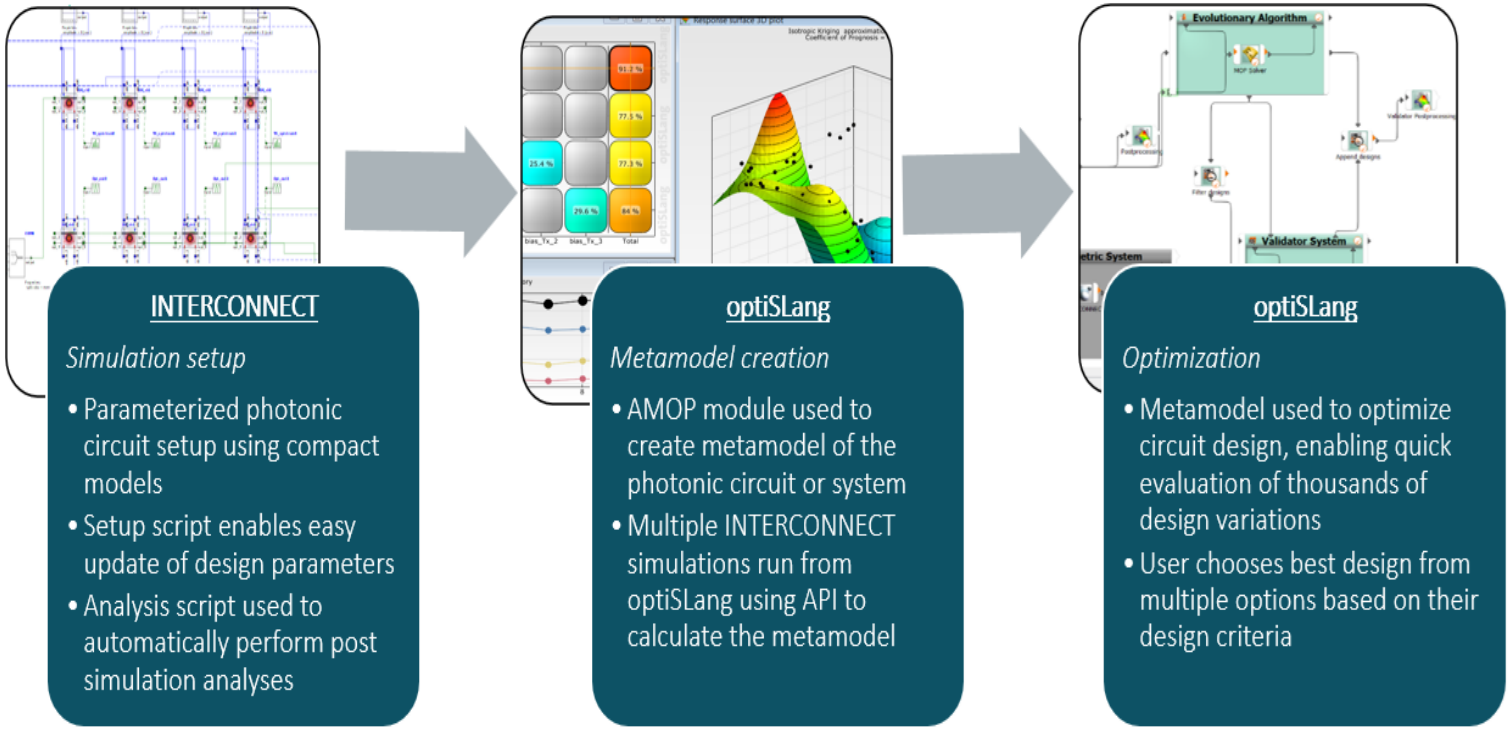
Ansys part of SYNOPSYS®

Efficient PIC Co-optimization with Automatic ML-based Workflow

- **Problem:** Photonic transceivers need to deliver faster data rate with low bit-error-rate (BER)
- **Solution:** AI/ML assisted optimization workflow for photonic integrated circuits with Ansys optiSLang and INTERCONNECT
- **Results:**
  - Reduces design cycle
  - Improve eye quality and BER
- **Collaboration Partner:**

Hewlett Packard Enterprise

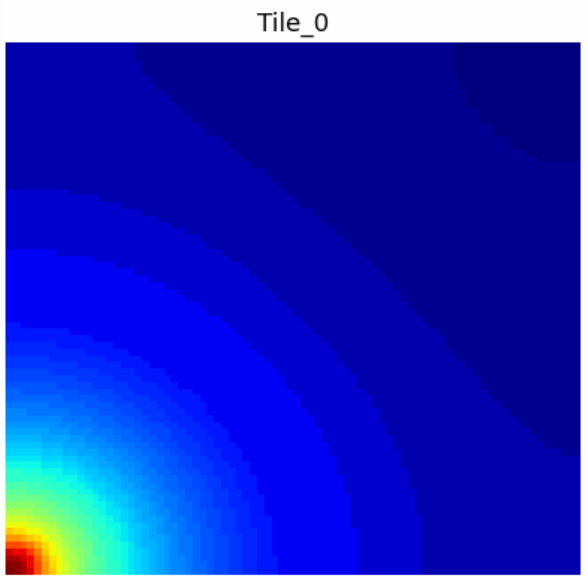




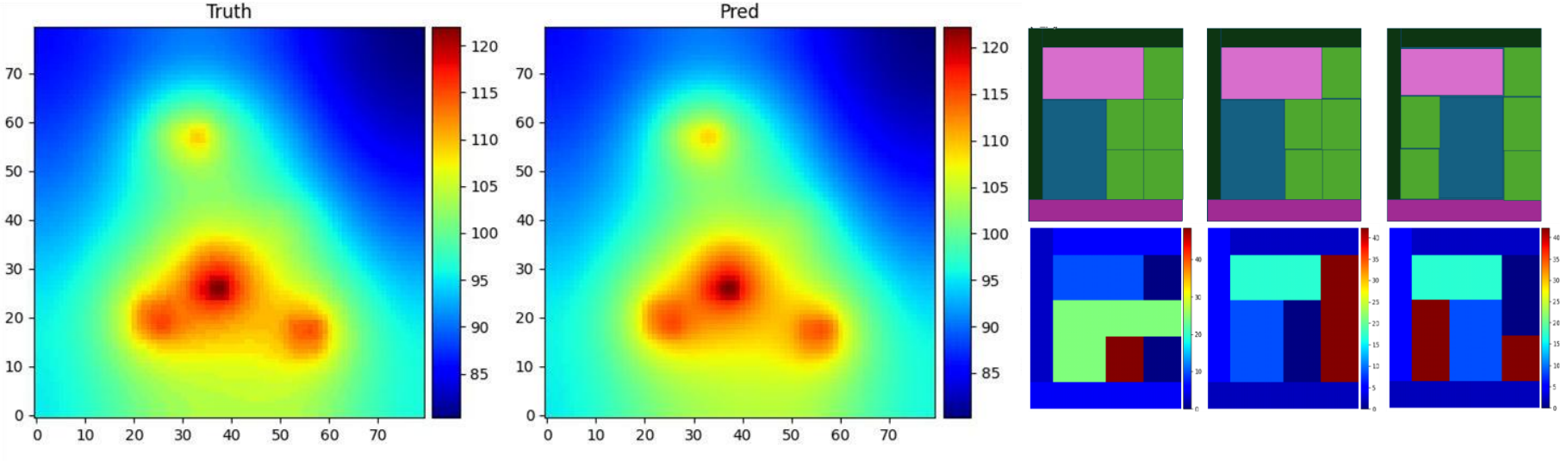
"Towards An Automated Workflow for Link-level Exploration and Optimization in the Domain of All-to-all Optical networks", L. Ramini, et al, DAC 2022

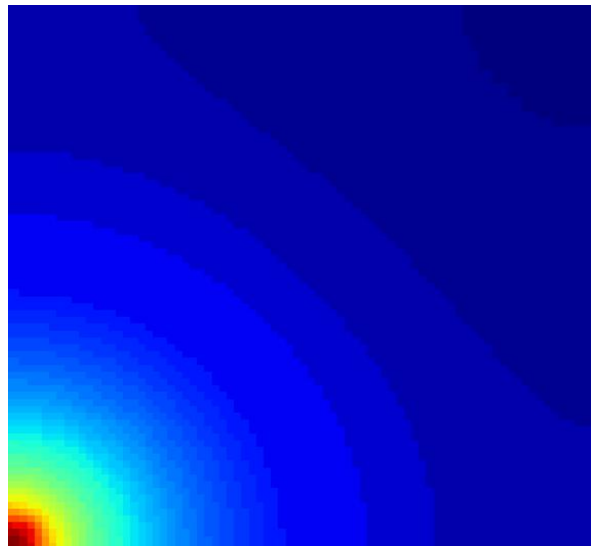
Parallel Per-tile Activated ML Thermal Solver for Solving Arbitrary Power Pattern with FNO of PhysicsNeMo

- Training data: Finite amount of single tile heating cases
- NN Input: Single tile heating power map
- NN Output: Single tile heating thermal profile with FNO model
- Post processing: Linear superposition of thermal responses
- Validation with numerical solver: error rate < 0.5%
- Supports both static and transient simulations, and successfully applied in DARPA Thermonat project



Single tile heating (Inference in parallel, took <3s)





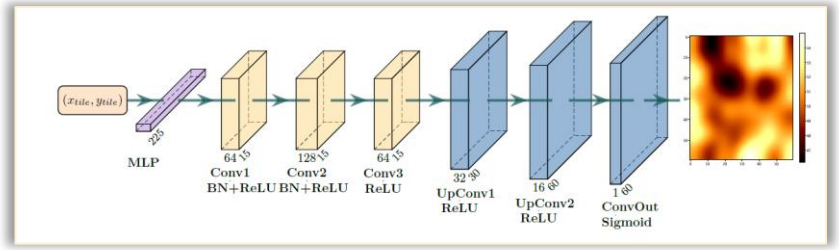
Superposition

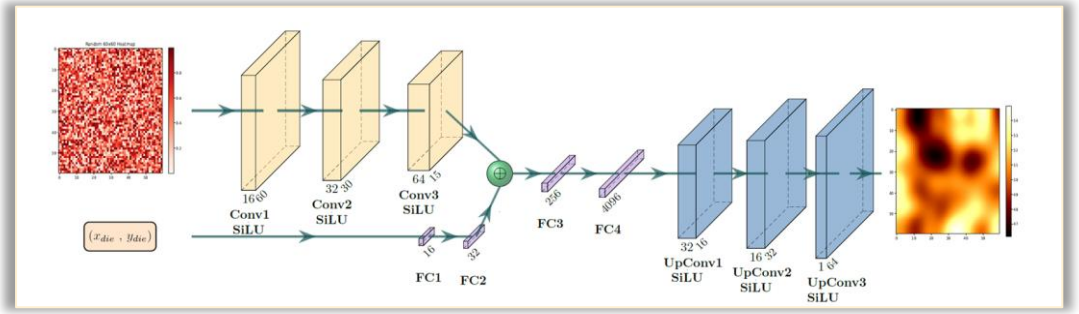
"Parallel Per-tile Activation with Linear Superposition of Thermal Response for Solving Arbitrary Power Pattern in 3DIC Thermal Simulation", H. He, N. Chang, et al., MLCAD, 2024

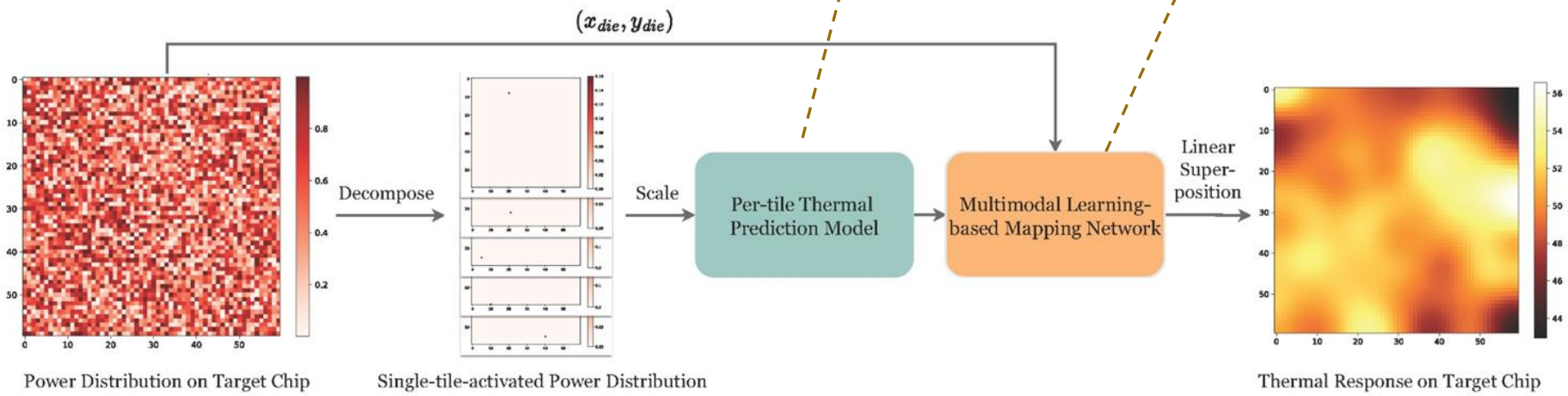
"Invited Paper: Solving Fine-Grained Static 3DIC Thermal with ML Thermal Solver Enhanced with Decay Curve Characterization", H. He, N. Chang, A. Kumar, et al., ICCAD, 2023

Multimodal Learning-Based Thermal Solver for 3DICs with Arbitrary Power Distributions and Chip Dimensions

- Handles diverse power distributions and chip dimensions without additional data collection or model retraining
- Requires far fewer and a fixed-size training dataset to maintain accuracy
- Achieves 150× faster runtime and uses only 0.023% of the memory compared to an FEM solver
- Delivers an average prediction error of just 3.72% in real-world scenarios

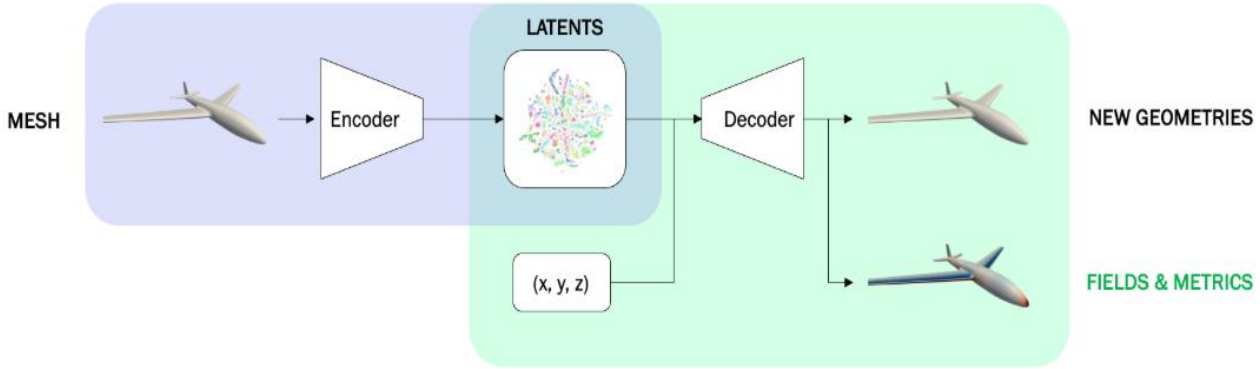






"Multimodal Learning-Based Thermal Solver for 3DICs with Arbitrary Chip Dimensions and Power Distributions", Z. Lu, A. Kumar, N Chang, et al, MLCAD 2025

Building Foundation Model for 3DHI Thermal Simulation



Large Physics Foundation Model from PhysicsX based on 25M pre-trained cases

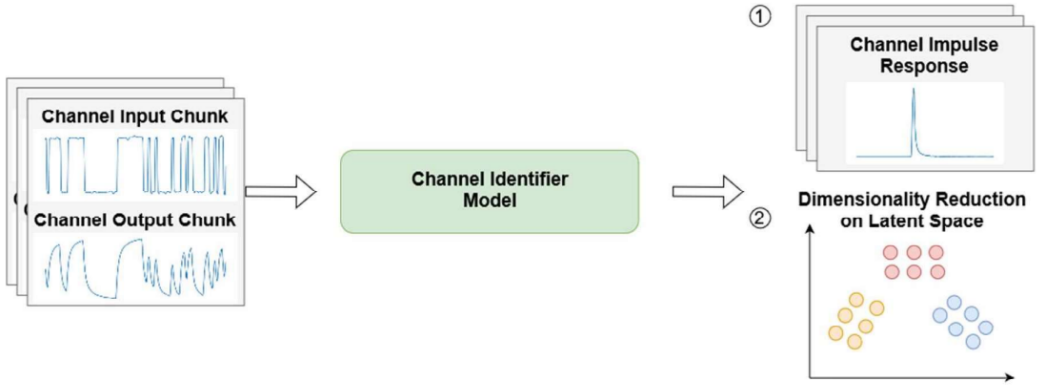


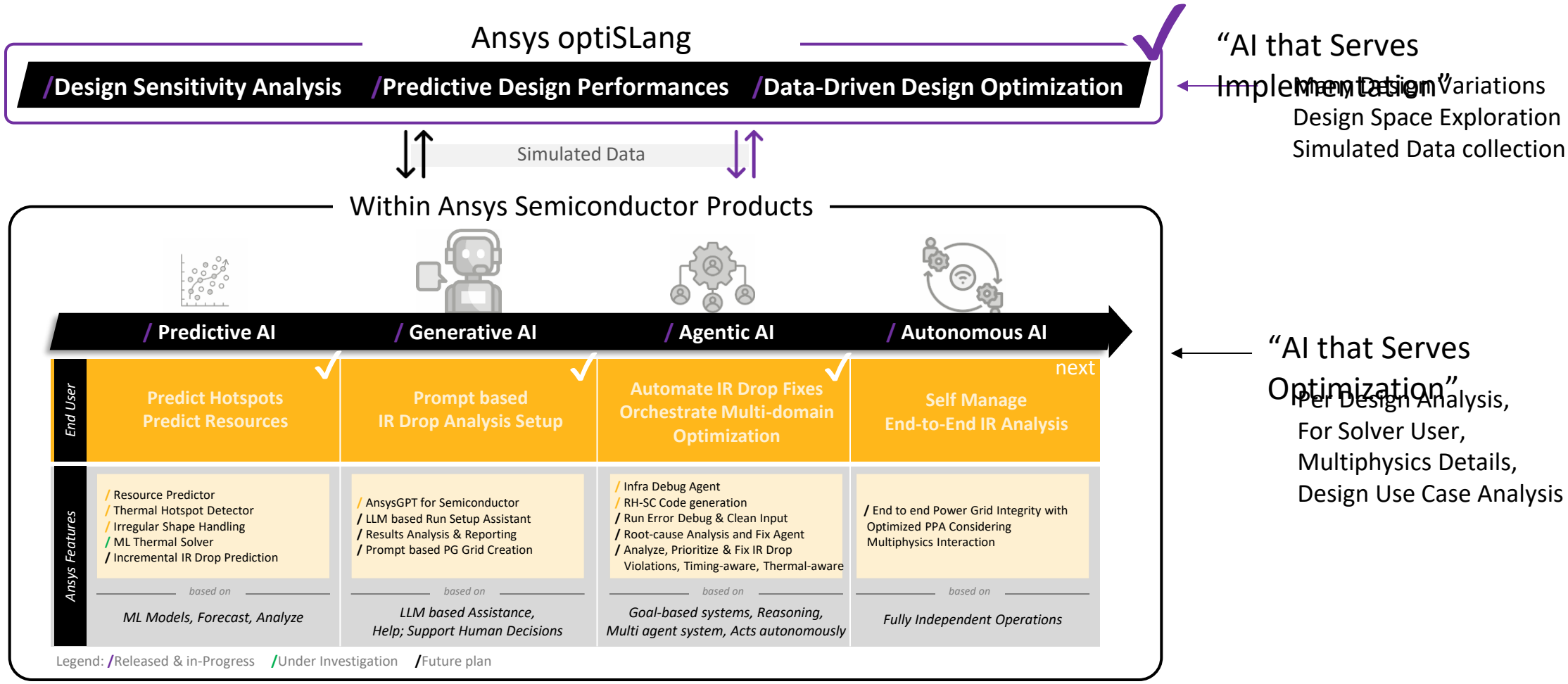
Figure 1. High-level overview of the proposed method. Channel waveforms are used to predict the channel's impulse response and the latent space of the model identifies channel properties.

SI/PI Foundation Model from HPE

PhysicsX - Building Beyond Human Imagination with Foundation Models for Geometry and Physics
"Foundational Model Approach for SI/PI Analysis Using Large Language Model Techniques", P. Kashyap (HPE), C. Cheng (HPE) , et. al, DesignCon, 2025

- Proposal for building Foundation model for thermal integrity in 3DHI
  - Supports arbitrary chiplet sizes and custom power maps
  - Accounts for process-node and design specific parameters (i.e. conductivity, thickness, metal density, HTC)
  - Combines minimal simulations with foundation model for fast and accurate thermal prediction
  - **Applications:** thermal-aware placement, early physical architecture exploration

Agentic AI Roadmap for Semiconductor



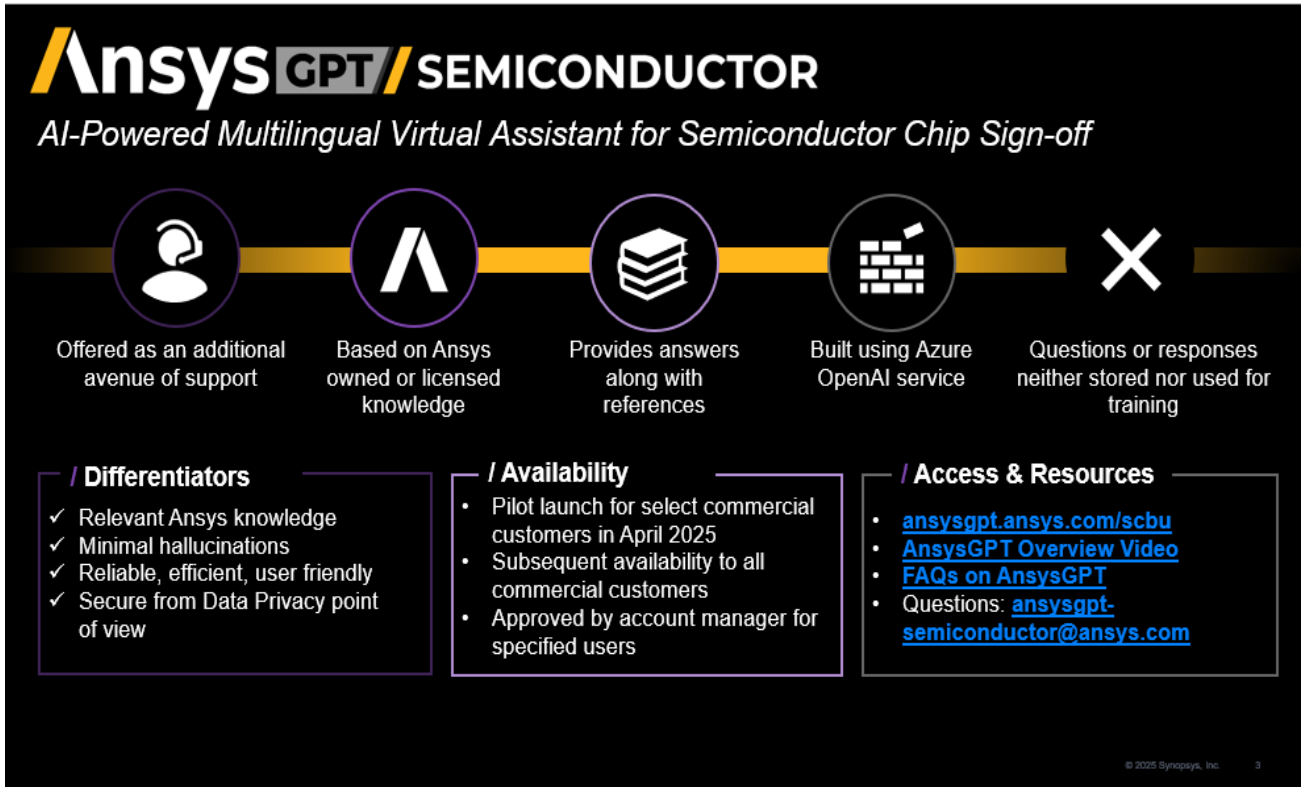
"AI that Serves Implementation"

- Many Design Variations
- Design Space Exploration
- Simulated Data collection

"AI that Serves Optimization"

- Per Design Analysis,
- For Solver User,
- Multiphysics Details,
- Design Use Case Analysis

Embedded Ansys Engineering Copilot including AnsysGPT for Semiconductor



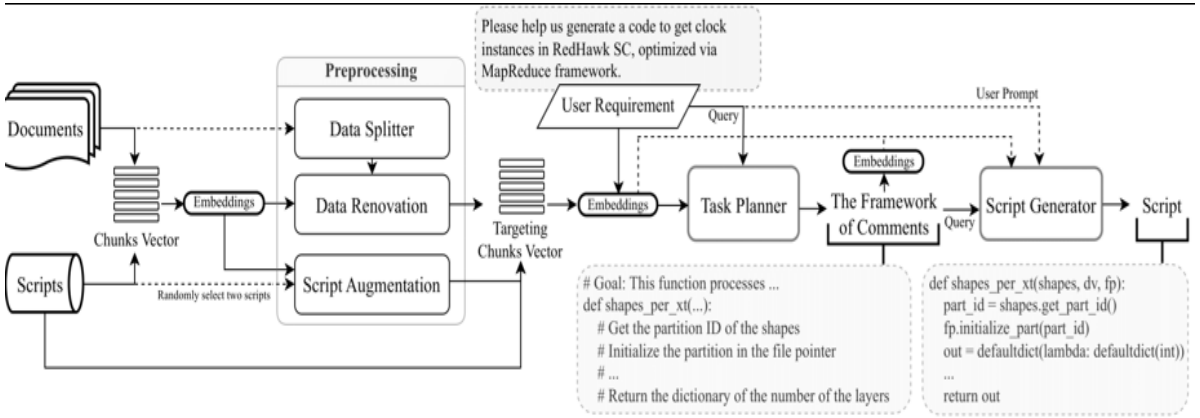
- Embedded chat window in RH-SC
  - Access AnsysGPT for Semiconductor
  - Security & Privacy, no customer data leaves the workflow

- Engineering Copilot
  - Seamless Integration & UX
  - User Interaction in workflow automation or providing debugging/diagnosis
  - Tools integration in Agentic AI workflow

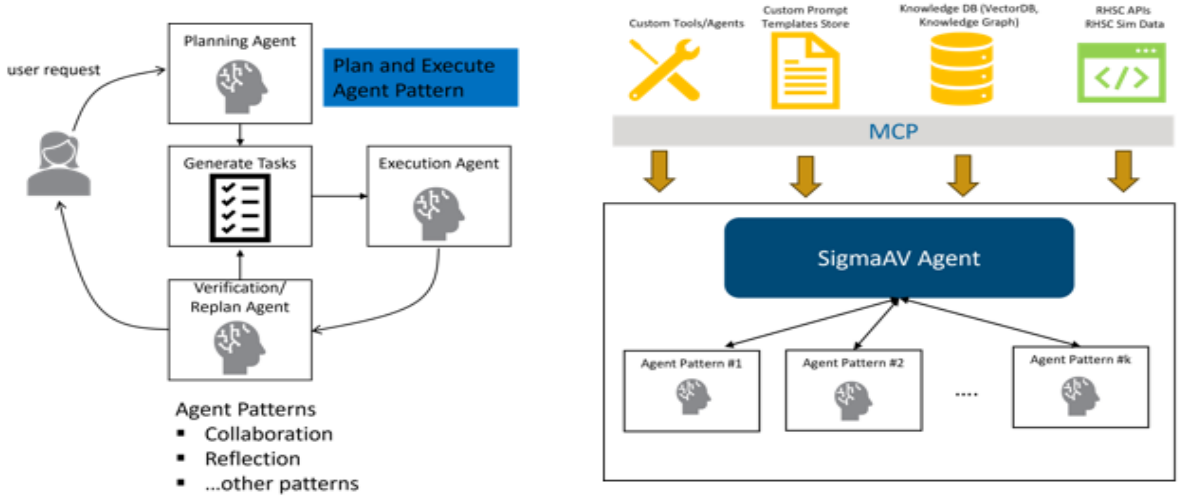
Beyond AnsysGPT: Agentic AI Enabled RH-SC Copilot for Advanced Analysis

- Three levels of Agentic AI workflows
  - Interactive Q&A (AnsysGPT)
    - Embedded Q&A with guided workflows
    - RAG-based, zero hallucination, with safety guardrails
  - MapReduce Code Generation via GenAI (CodeGen)
    - Generates code based on user prompts via GenAI
    - Produces well-structured, commented code with adaptive feedback for auto-correction
  - Collaborative Multi-agent AI Workflow (Debug/Diagnosis Assistant)
    - Provides HPC issues debugging for RH-SC on SeaScape
    - Enables SigmaAV diagnosis by analyzing logs, aggressor-victim interactions, timing criticality, and PG grid robustness using a multi-agent AI workflow
    - Enables multi-agent communication via MCP protocol

MapReduce Code Generation

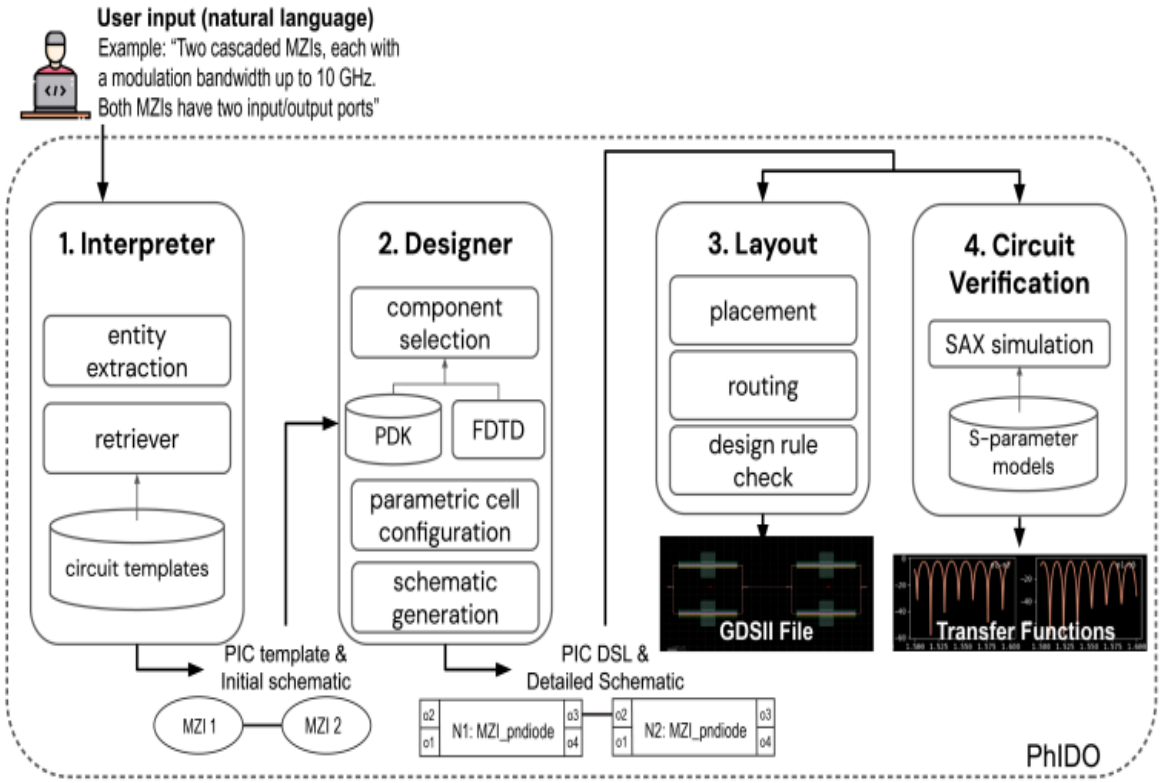


Collaborative Multi-Agent AI Workflow



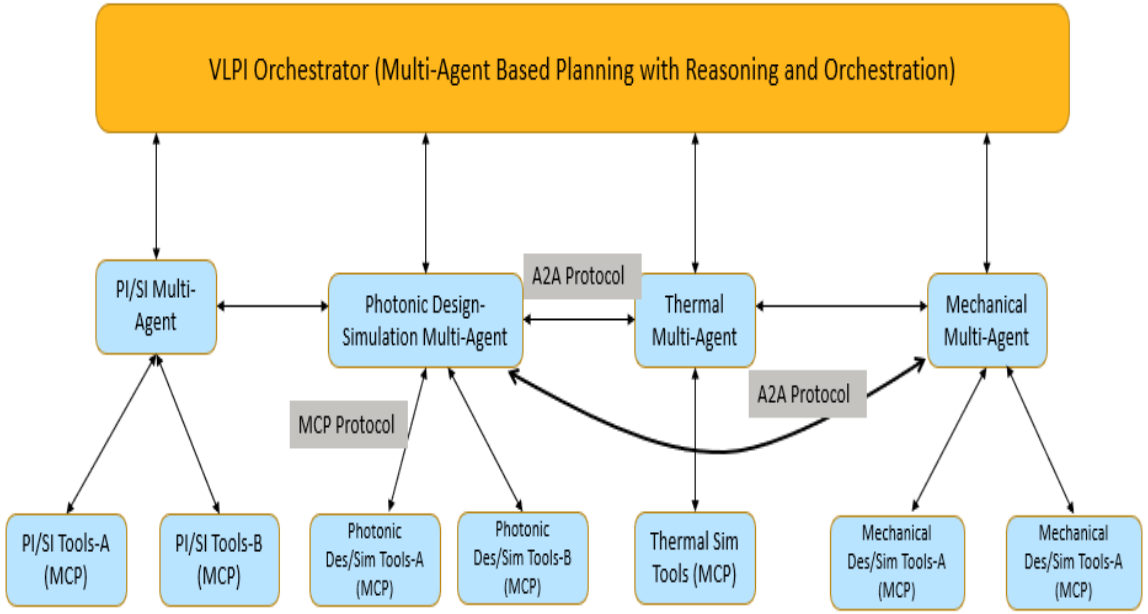
"Novel Preprocessing Technique for Data Embedding in Engineering Code Generation Using Large Language Model", Y. Lin, A. Kumar, N. Chang, et al., ISLAD, 2024
"Harnessing LLMs for Advanced EDA Platforms : Code Generation and Beyond", A. Kumar, EDPS, 2024

Vision: Leveraging Agentic AI for Very Large Photonic Integration Design (VLPI)



PhIDO is a multi-agent framework for PIC design automation

"AI Agents for Photonic Integrated Circuit Design Automation", A. Sharma, arXiv, 2025



- **Our proposed VLPI orchestrator for performing root-cause analysis**
  - **Detect**: Identify issues (e.g. high temperature on microring)
  - **Query**: Retrieve related causes and mitigations from knowledge graph (KG)
  - **Reason**: Combine data + KG to find root cause
  - **Report**: Output clear explanation with recommended fixes

Both Design and physical verification with diagnosis can be accelerated through Agentic AI Technology

Acknowledgement

- Thanks to Lang Lin, Jie Yang, Haiyang He, Wenbo Xia, Fangwen Cheng, Chris Ortiz, Jerome Toublanc, Tianhao Zhang, Owen Lin, Zelin Lu, Wei You, Pantha Sarker, Ahsan Alam, Zeqin Liu, Parya Samadian, Di Liang, and Sanjay Gangadhara for many discussions on CPO and fast ML-based thermal simulations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