# Following the 'Signals' –
## Overcoming Challenges from Transistor to AI Data Centers with EDA, CAE, and AI Solutions

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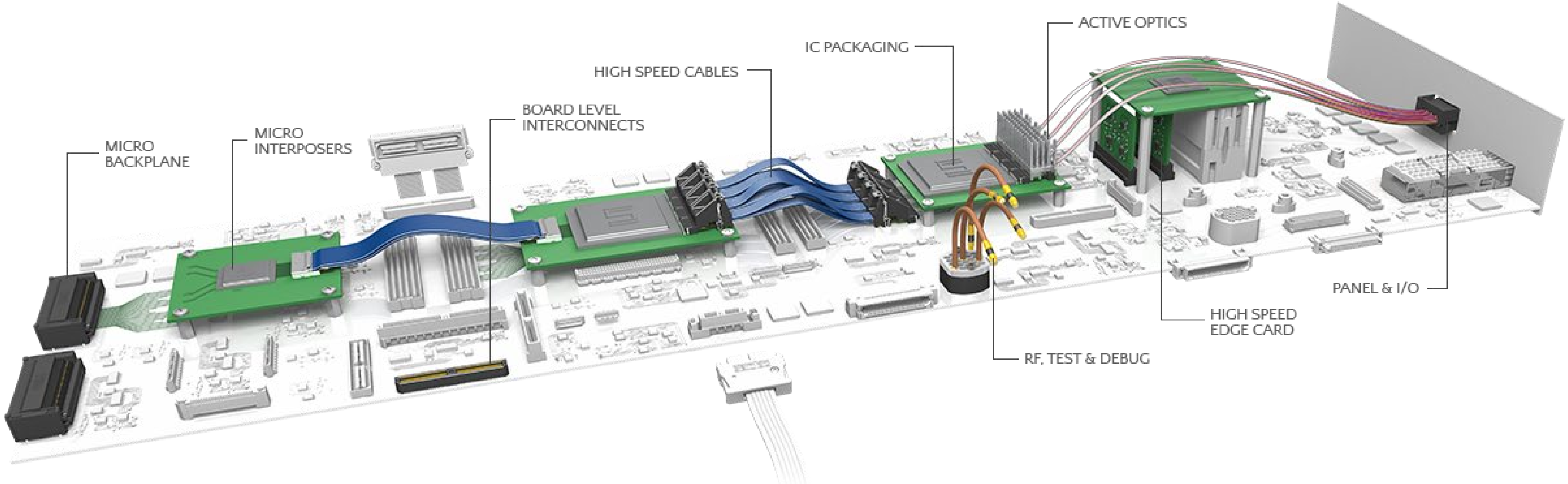
**Sr. Director, Keysight R&D**

# Agenda

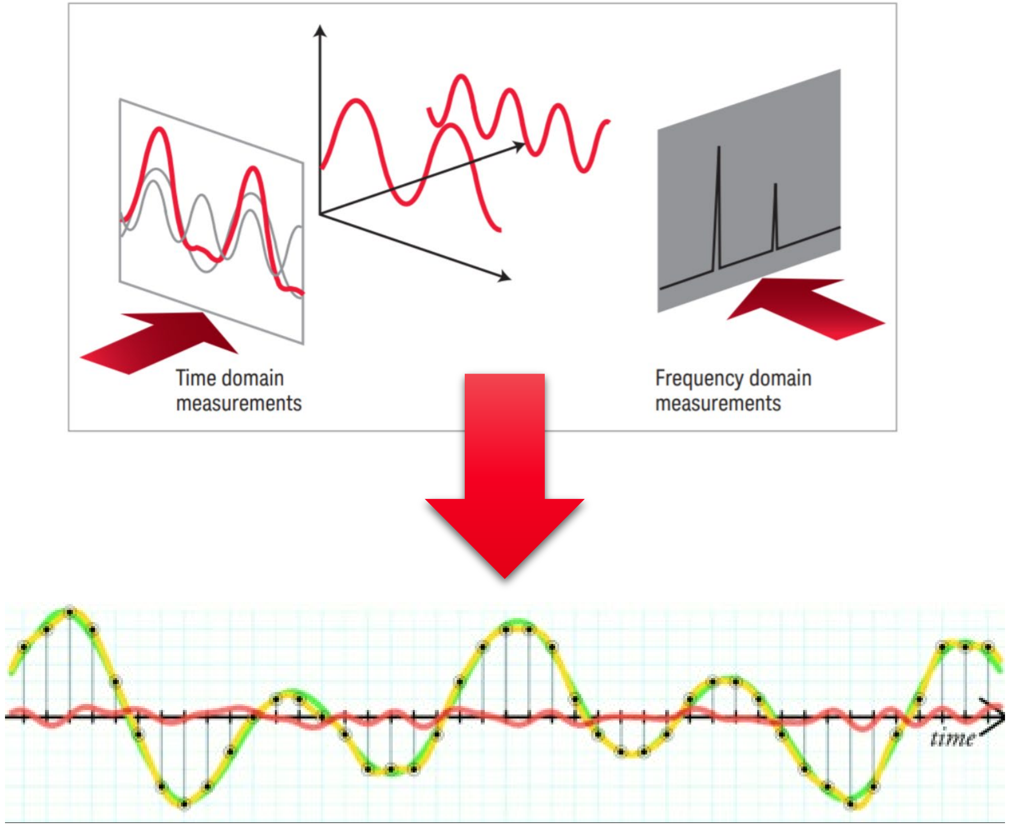
## Follow the ‘Signal’



- Transistor Level
- Circuit Level
- System Level
- Package/Board/3DIC
- Datacenter Level
- Network Level

# Definition of ‘Signal’

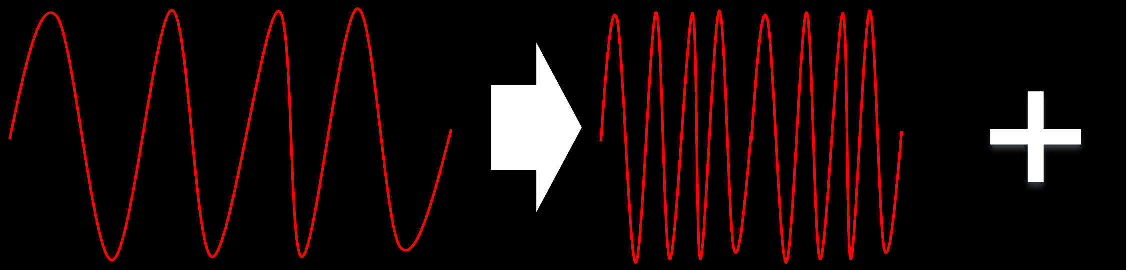
- An **electrical signal is a form of energy transmission through electric charges**
  - movement or flow of electrical energy, carrying information from one point to another
- **Analog signals:**
  - vary continuously in time and amplitude
- **Digital signals:**
  - discrete values, typically representing binary '0s' and '1s'

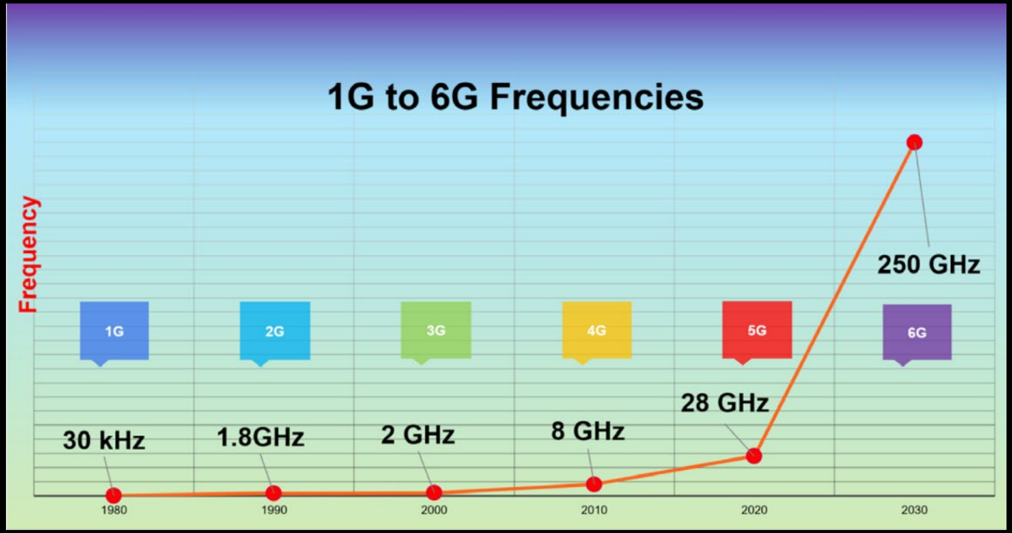


Original Signal
Quantized Signal
Quantization noise

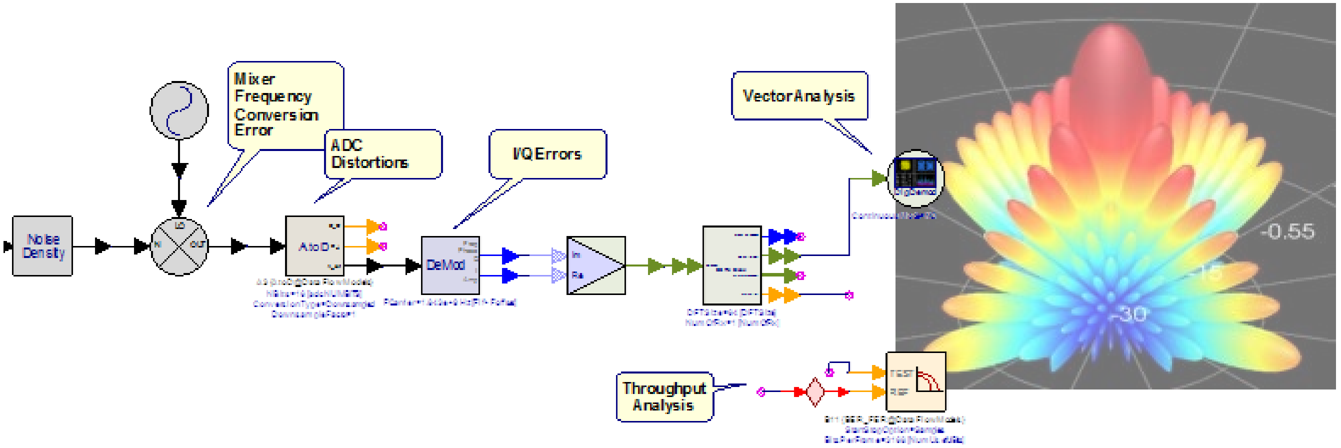
# High Frequencies Drive

…Higher Frequencies

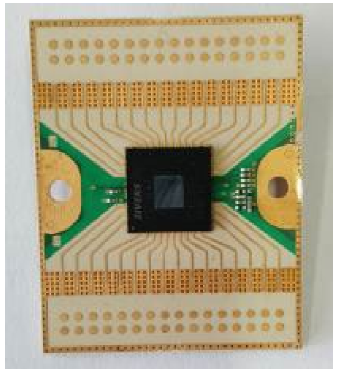


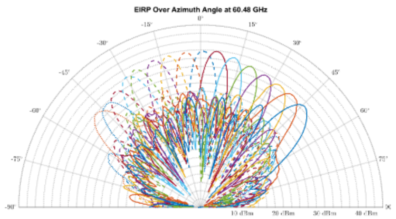


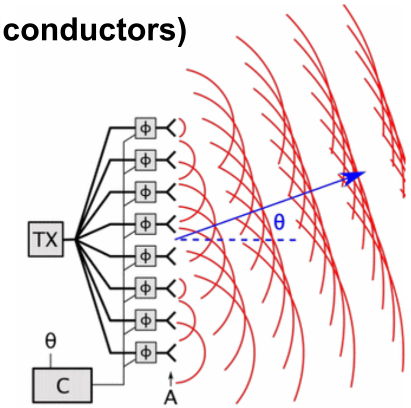
# New Engineering Challenges



WLAN 802.11ad transceiver (courtesy of Sivers Semiconductors)

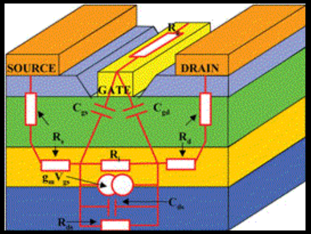




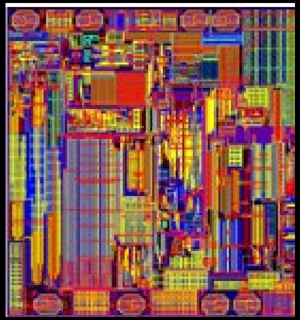


Wikipedia

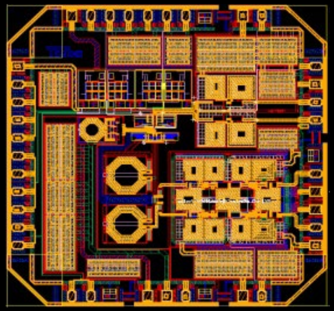
# Signal challenges at every layer of the Technology Stack



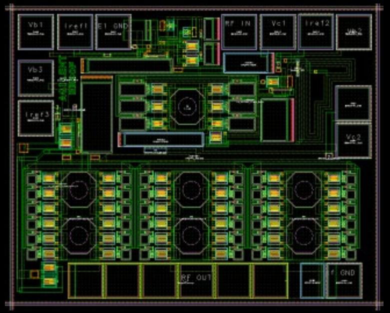
Primitive Devices



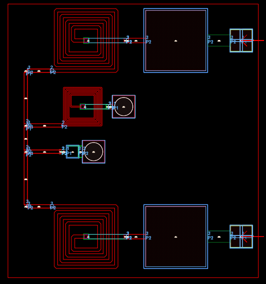
Analog / Mixed Signal IC (Si)



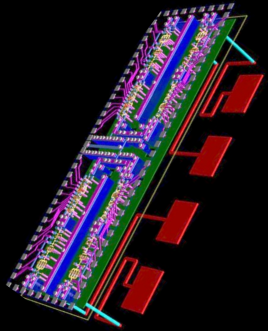
RFIC (Silicon)



RFIC (Non-Si)

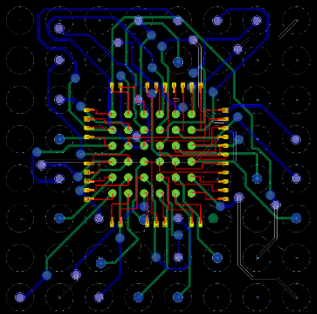


MMIC

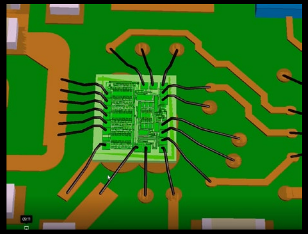


3DIC / 3DHI

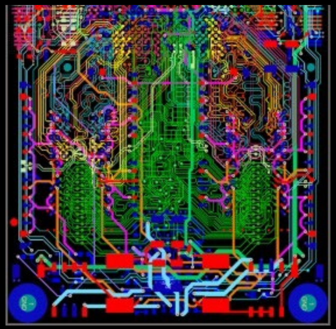
Signal complexity increases



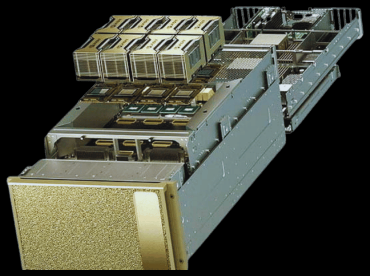
Small Scale Package



Wiring



Large Scale PCB



System

Server

Network

# Transistor Level

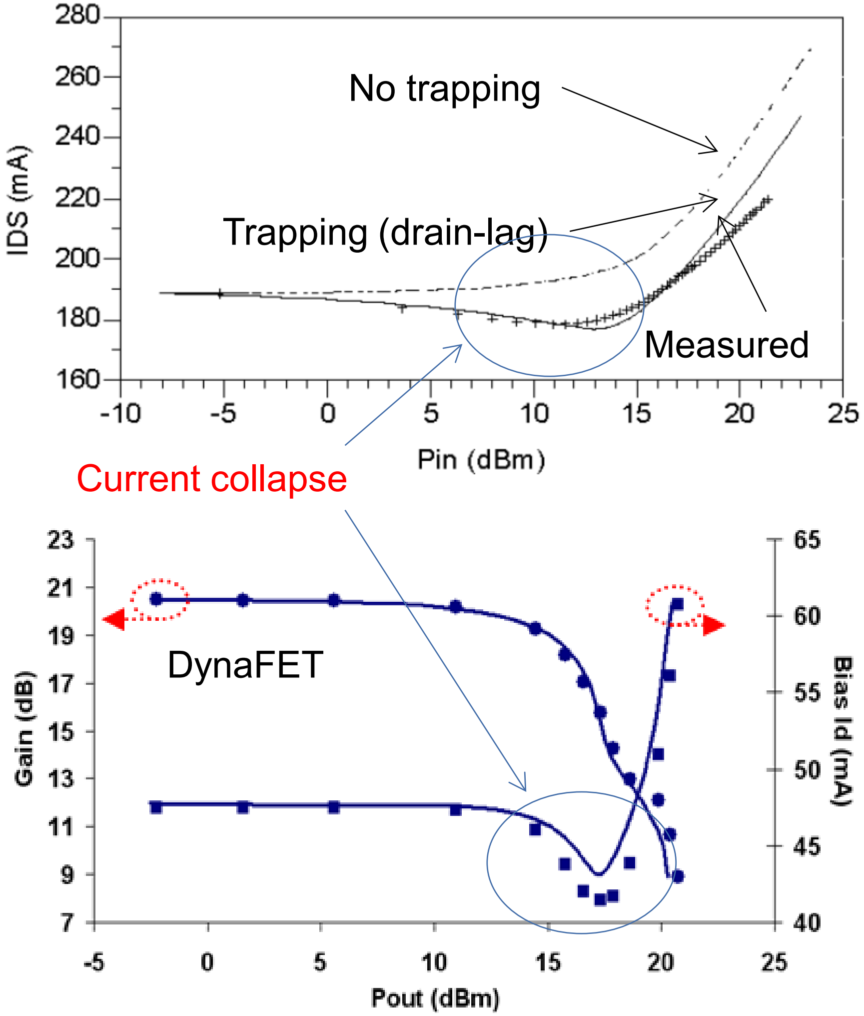
## Key Challenges

- Smaller technology nodes, higher frequencies, and new materials make model **extraction increasingly intricate** and data-intensive
- Every new technologies exhibits new artifacts and physical effects, **model accuracy increasingly difficult** for a large performance range
- More demand for **efficient Power PAs** for RF & MMIC ( e.g. Gallium Nitride (GaN) )

# Transistor Level - Customer Problem

## PA design accuracy challenges – e.g. GaN

- **New effects causing model inaccuracies**
  - Gain Compression, PAE, Intermodulation and Load Pull data show inaccurate behaviors in PDKs vs. Designs
  - Large discrepancy between DC, small and large signal results also typical in PDKs.
    - Especially true for III-V technologies like GaN → dynamic effects of trapping are still not accurately modeled by existing compact models
  - Some models like Angelov for GaN may allow some trade-off of DC, S-parameter and large-signal at specific bias-points
- Inability to predict current collapse (increase of PAE), knee-effect / drain-lag → reduction of the RF output signal as input power increase



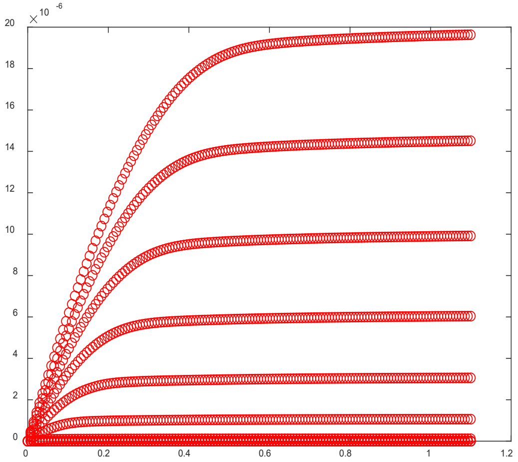
*Gallium Nitrate (GaN) - Jardel, De Groote et al., 2007*

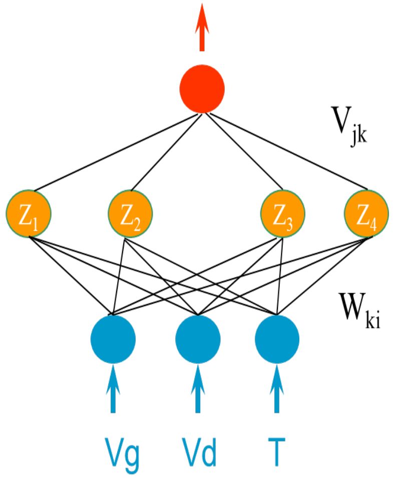
# Transistor Level – Data driven Model solutions

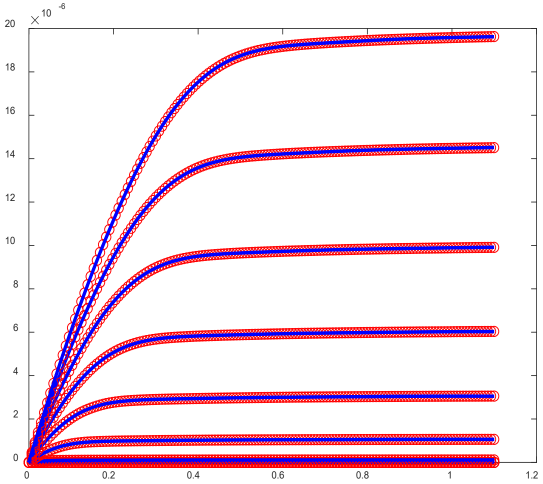
Advanced Design System

IC-CAP

$$I_d = I_d^{ANN}\left(Vg, Vd, T, W, L\right)$$



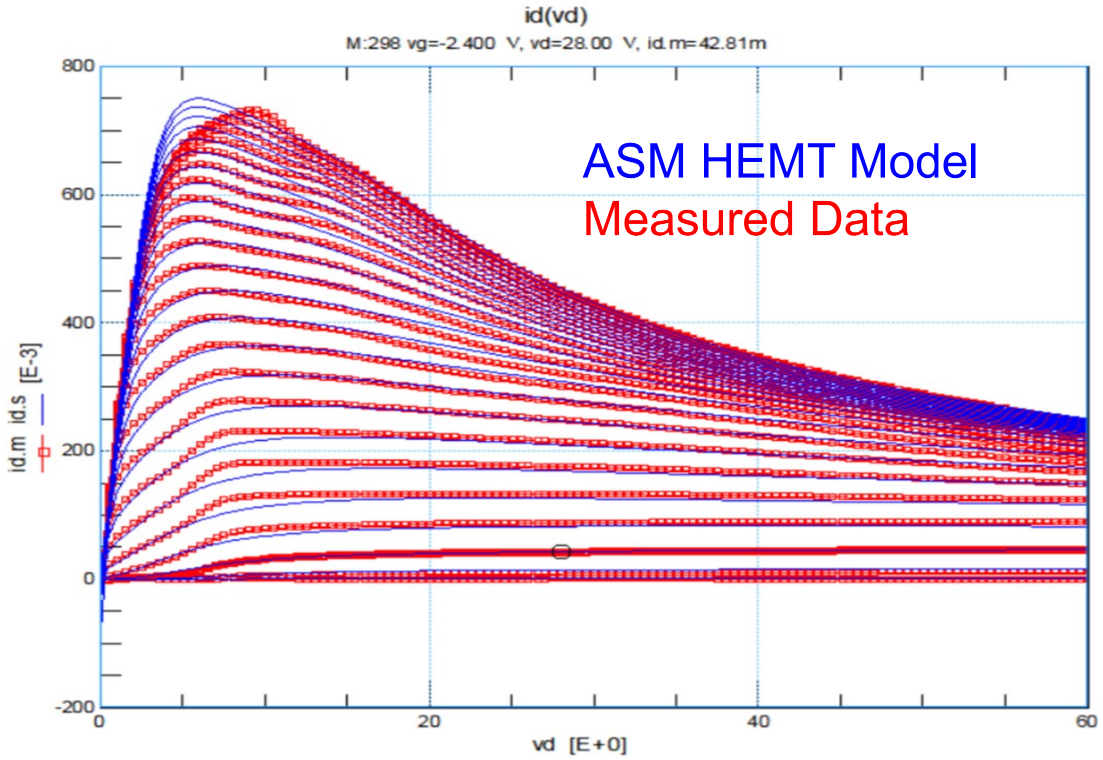




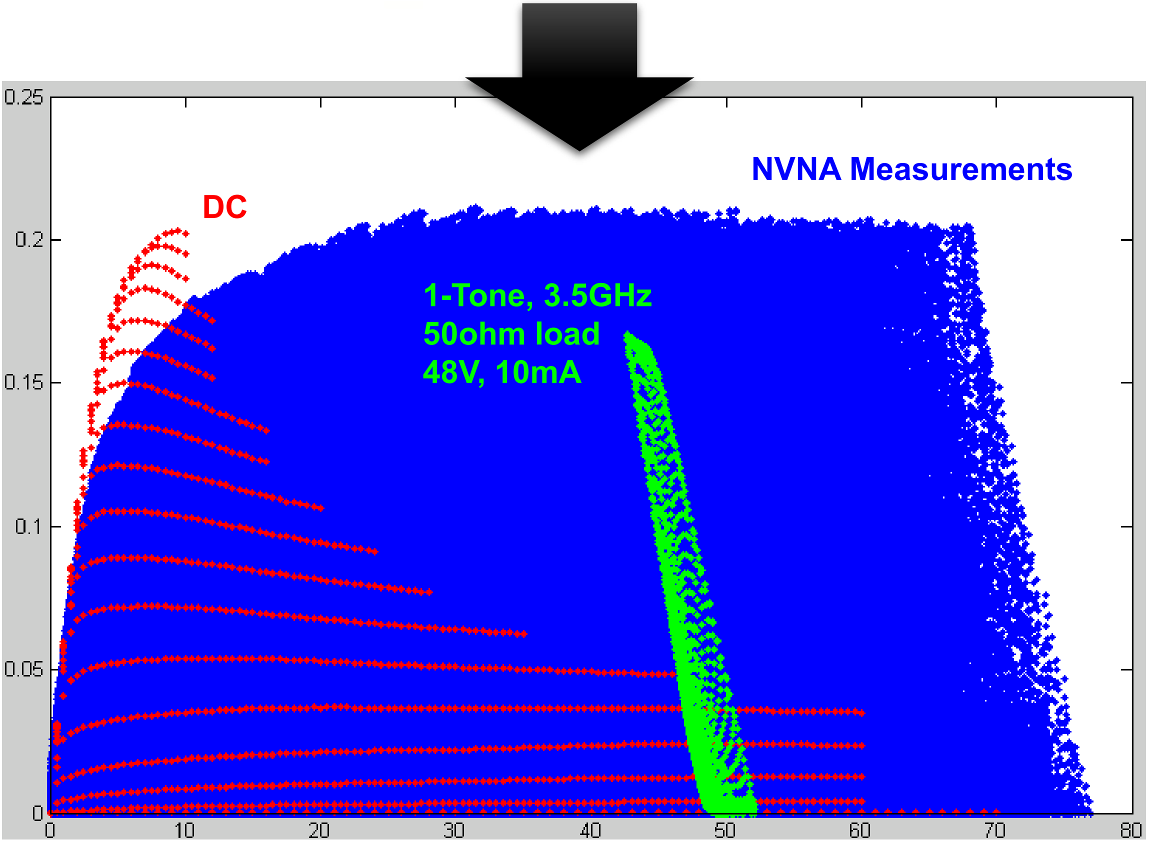
Data → ANN → Model

# “If the design doesn’t work, it’s the Models fault”

## Much faster I-V modeling with improved accuracy



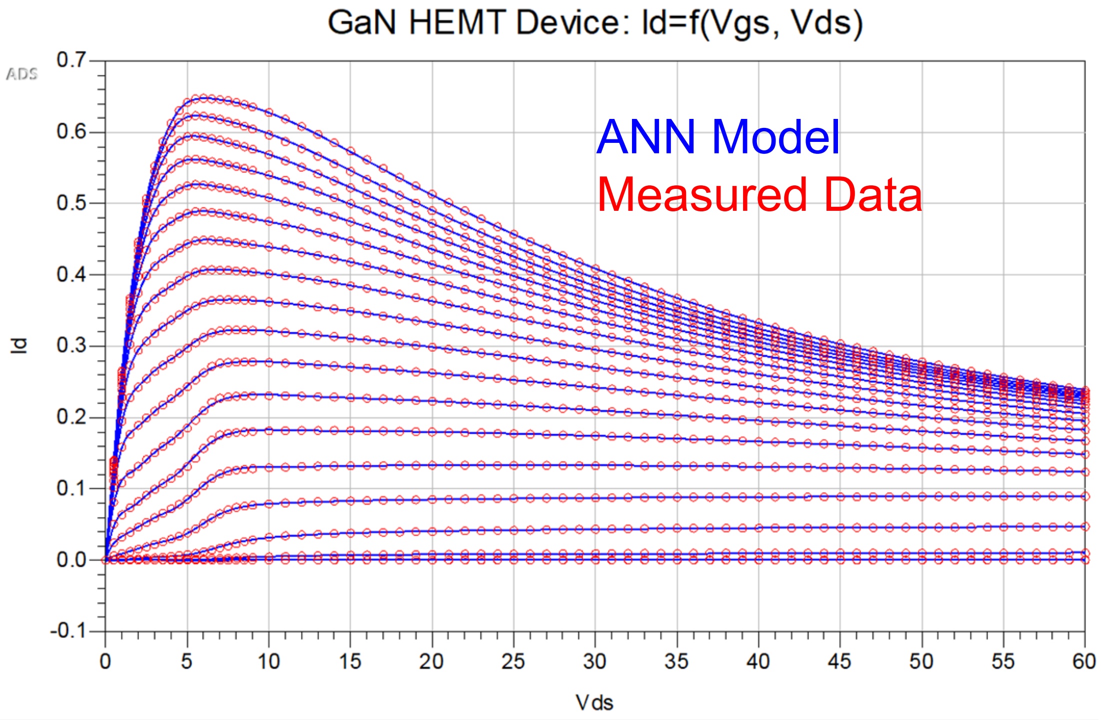
$$I_d = \frac{\mu_{eff}}{\sqrt{1+\theta_{sat}^2\psi_{ds}^2}} \frac{W}{L} C_g N_f \left[V_{go} - \left(\frac{\psi_s+\psi_d}{2}\right) + V_{th}\right] \psi_{ds}(1+\lambda V_{ds})$$

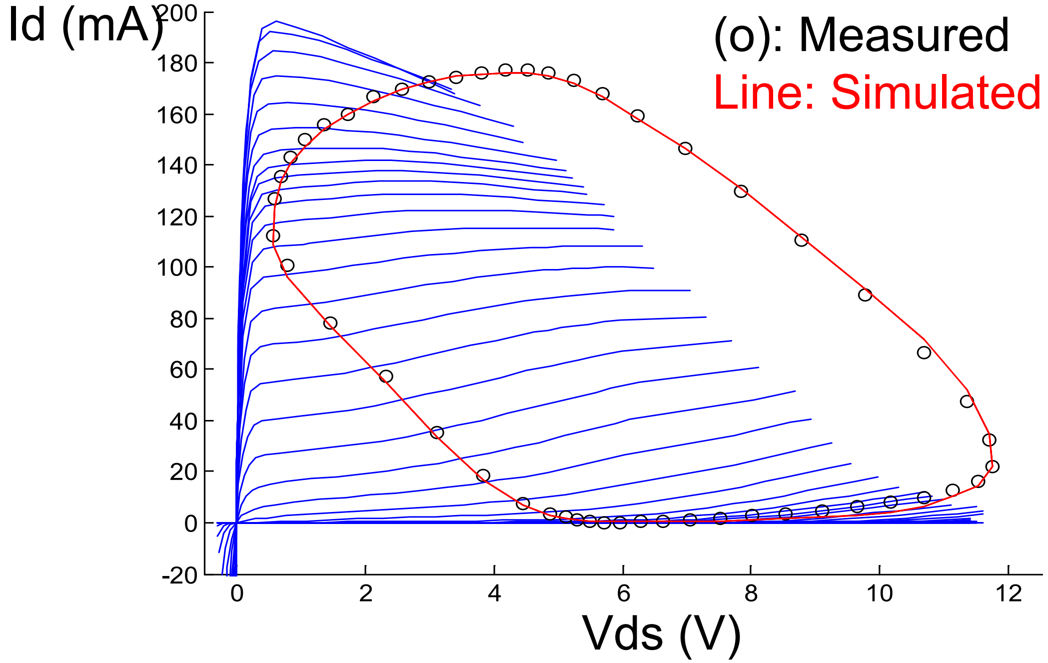


J. Xu, S. Halder, F. Kharabi, J. McMacken, J. Gering,
and D. E. Root, ARFTG Conf. June, **2014**, Tampa

# “If the design doesn’t work, it’s the Models fault”

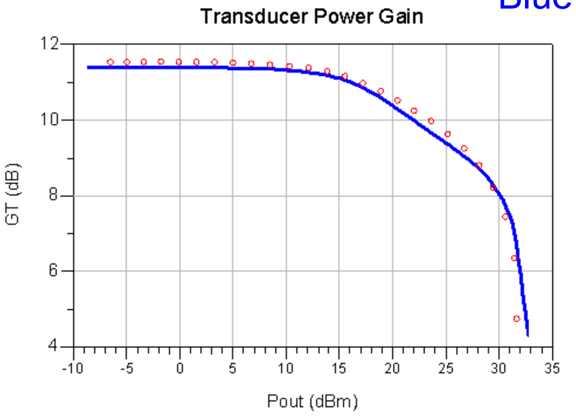
**Much faster I-V modeling with improved accuracy**

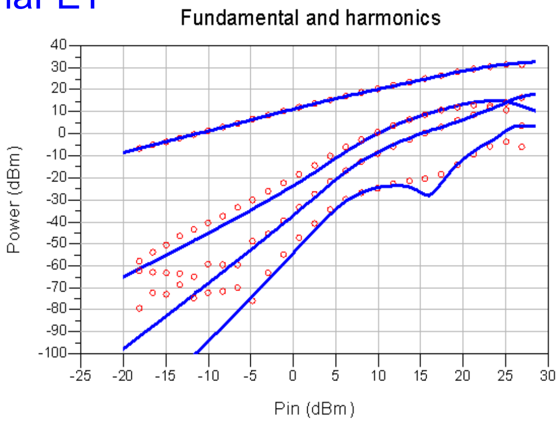




Red: Measured

Blue: DynaFET



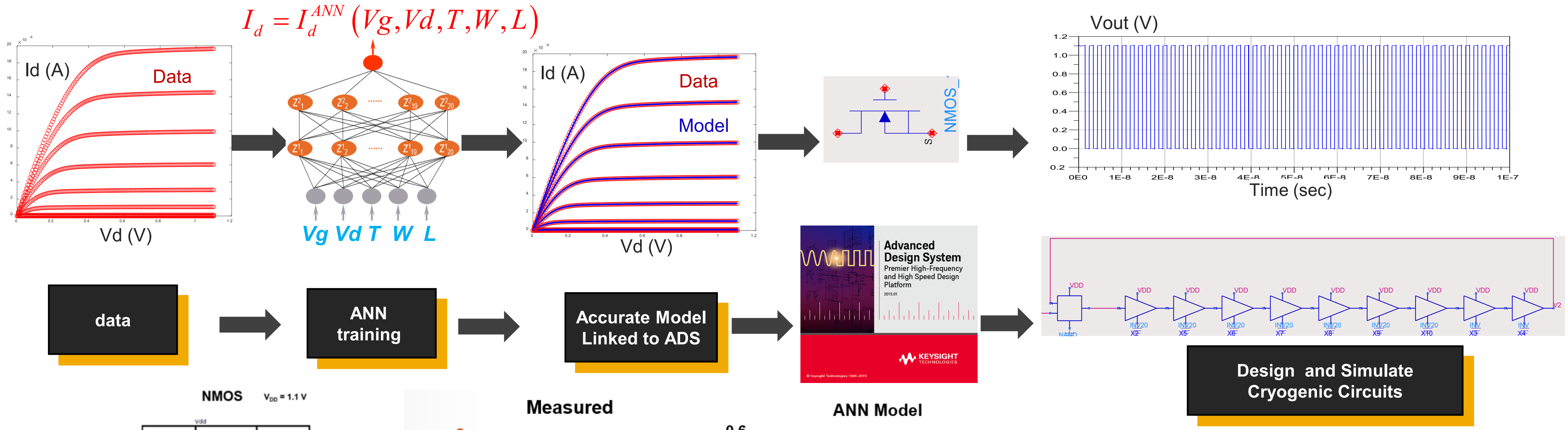


> *“I just spent four months trying to extract the ASM model **to the same data** set and you **got better results** in two minutes!”*

# Cryogenic CMOS Modeling

**Enabling circuit simulations for quantum control applications**

$$I_d = I_d^{ANN}\left(Vg, Vd, T, W, L\right)$$



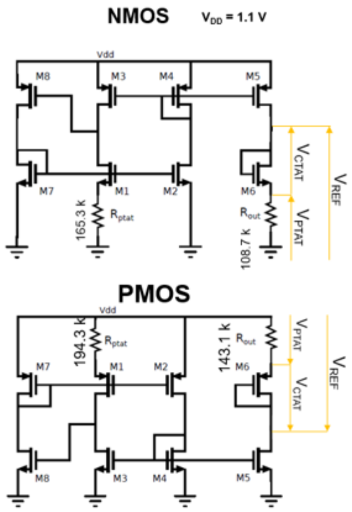
**data**

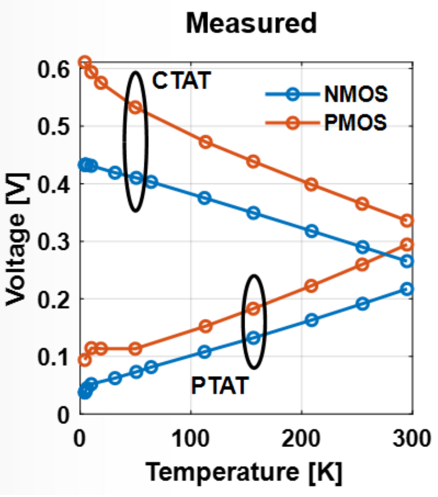
**ANN training**

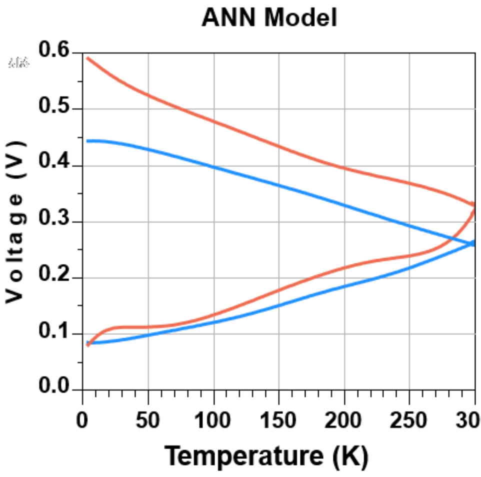
**Accurate Model Linked to ADS**

**Design and Simulate Cryogenic Circuits**

Voltage Reference Circuits



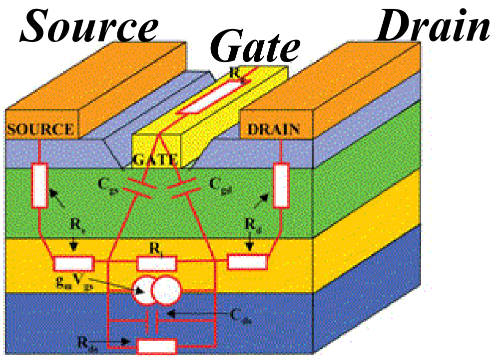


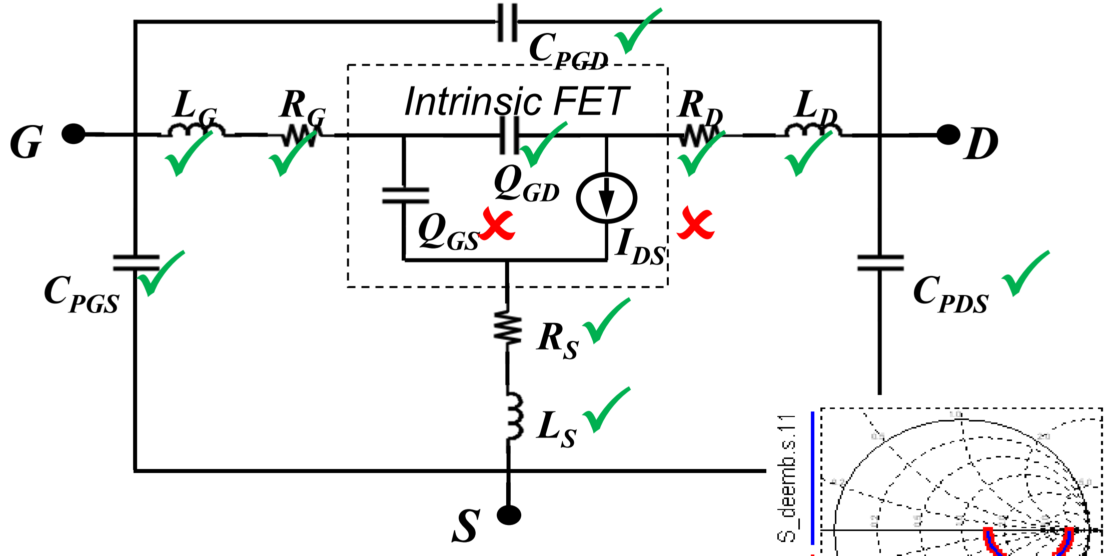


*P. A. 't. Hart, J. van Staveren, F. Sebastiano, J. Xu, D. E. Root and M. Babaie*, "**Artificial Neural Network Modelling for Cryo-CMOS Devices**," 2021 IEEE 14th Workshop on Low Temperature Electronics (WOLTE), 2021, pp. 1-4, doi: 10.1109/WOLTE49037.2021.9555438.

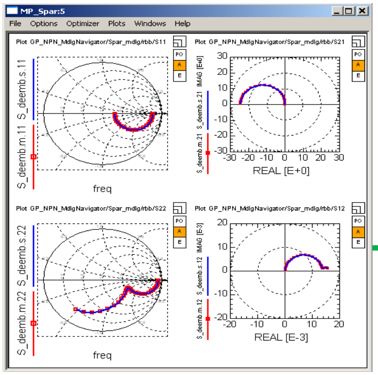
KEYSIGHT

# Nonlinear building blocks for device models – Hybrid modeling solution

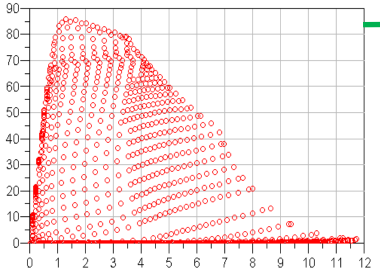




**VNA**



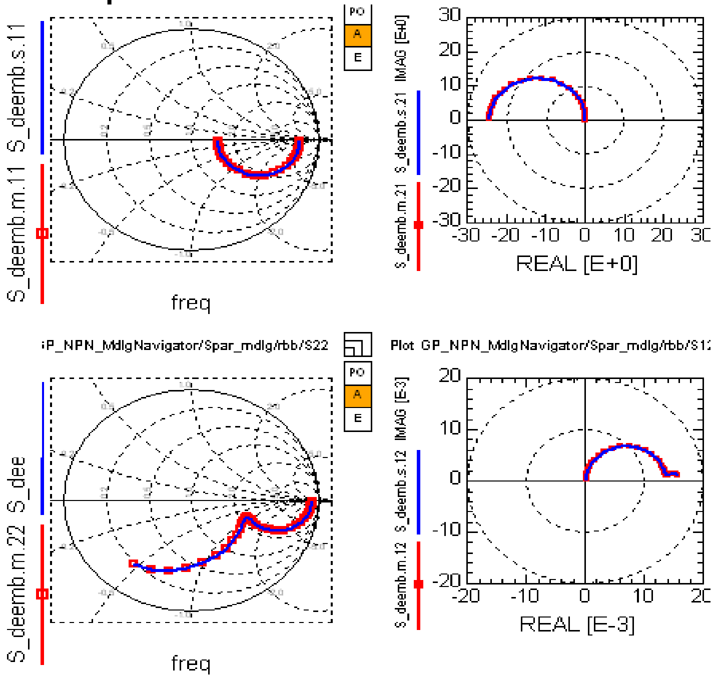
**DC**



**ANN Training**

$$Q_{GS} = f_{ANN}(V_{GS}, \omega)$$

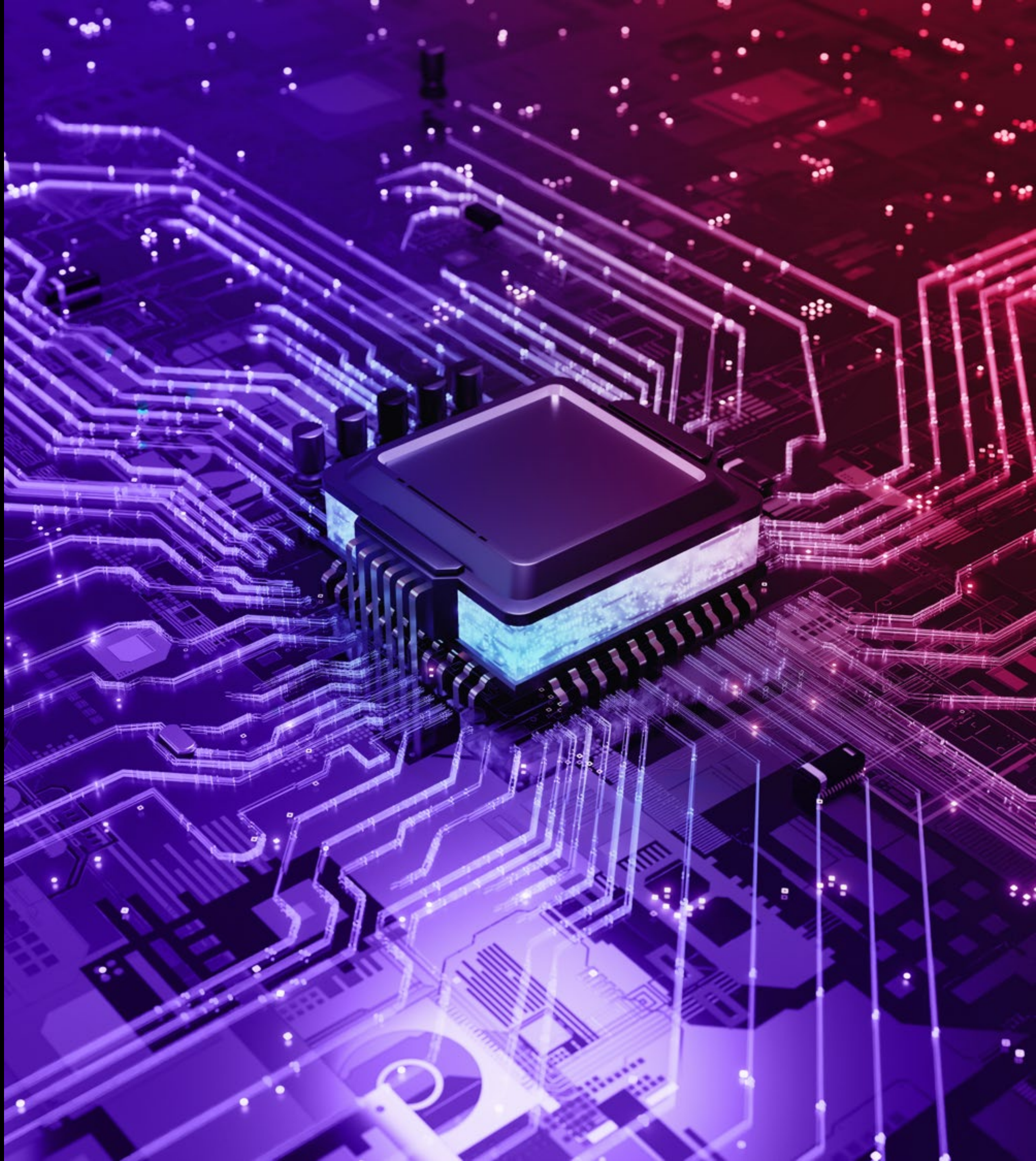
$$I_{DS} = f_{ANN}(V_{GS}, V_{DS}, \omega)$$



# Circuit & Package Level

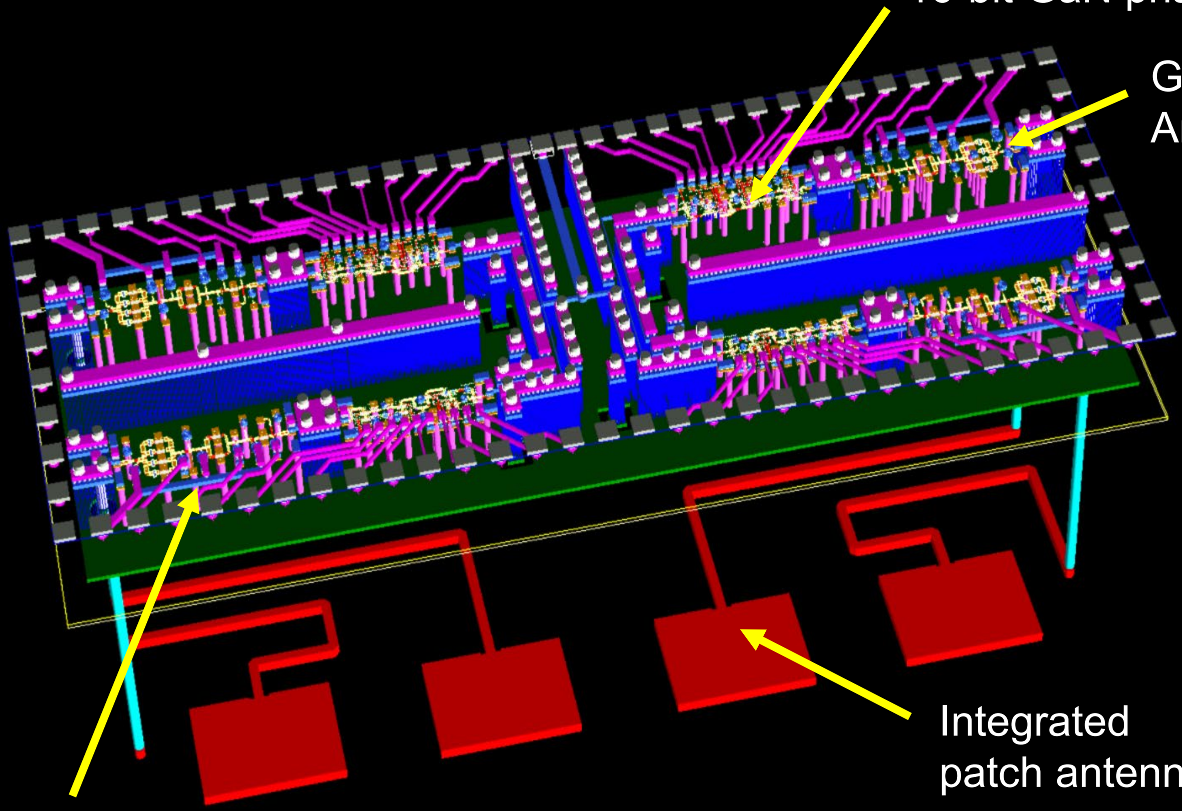
## Key Challenges

- Increasing complexity around system integration, including mixed fabrication technologies – heterogenous integration (3DIC / 3DHI)
- Assembling multi-technology structures and performing simulations across technology boundaries
- Multi-physics are increasingly relevance for overall performance



# High Frequencies Drive → New Engineering allenges

3DHI example of a 28 GHz Front-End module
(4 PA + Phase Shifter flip-chipped)



16-bit GaN phase shifter

GaN Power
Amp

Integrated
patch antenna

Fan Out

## Co-Simulation Needs

- IC, Package and board-level **EM** interactions
- IP manufacturing **variations**
- **Electro-thermal** effects like self-heating

# System-in-Package (SiP) – Integration Overview

**YOLE Intelligence Report: *Status of the Advanced Packaging Industry 2024***

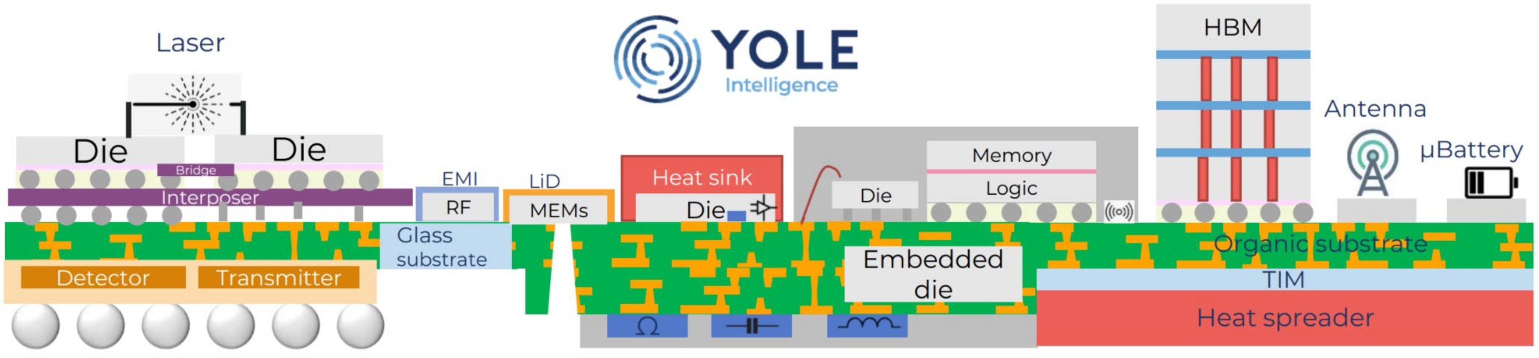
## SiP is an integration of different components (active or passive) using a packaging solution

### Common SiP components

- Chiplet
- Memory/logic die
- Embedded die
- Passive component
- Sensors
- MEMS
- Optical component
- Filters
- Switches
- Duplexers
- Amplifier

### Advanced packaging solutions

- Substrate
- Interposer
- Bridge
- TSV
- Bump/pillar
- Hybrid bond



### Packaging solutions
### Mainly for power and RF applications

- EMI
- Thermal interface material
- Heat sink
- Heat spreader

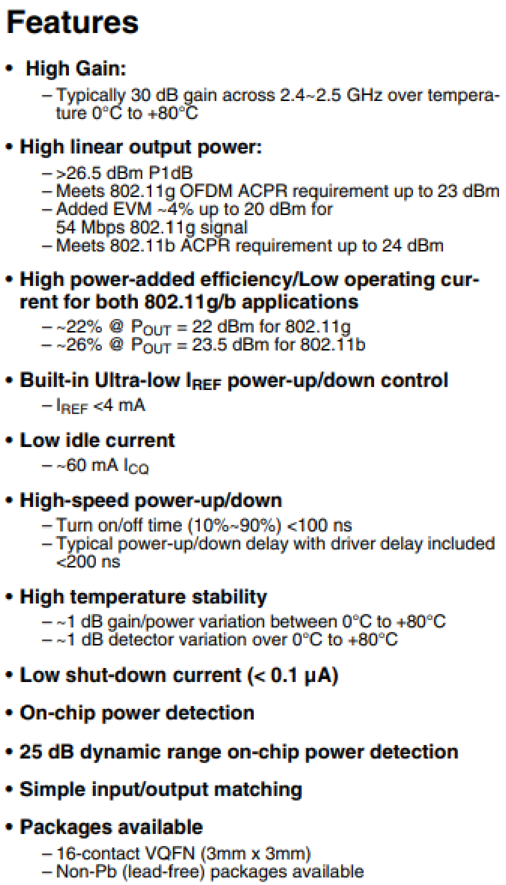
### Other SiP components (for selected applications)

- Antenna
- Photonic
- Laser
- Detector
- Transmitter
- Micro–cooler
- Micro-battery

This diagram does not show the actual dimensions and construction – only an illustration of possible integration in a SiP.

# Harder Specifications

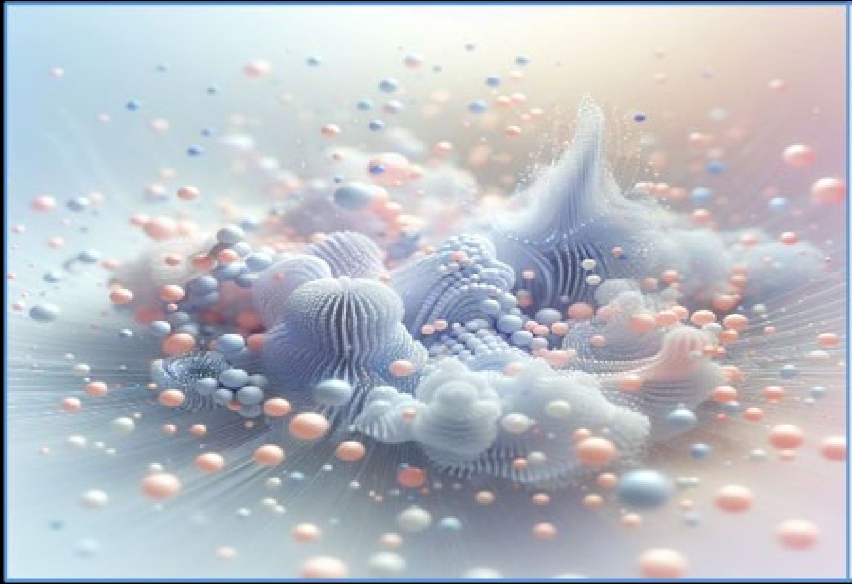
## Example of Microchip SST12LP14



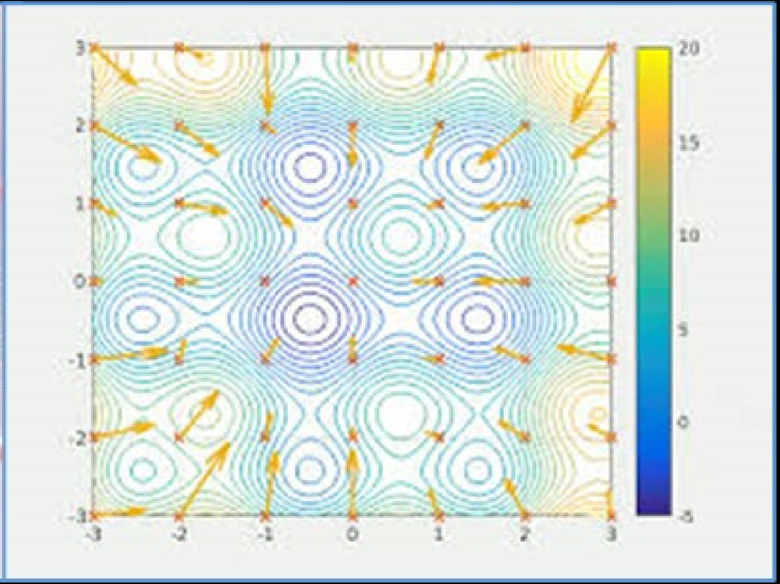
### Features

- **High Gain:**
  - Typically 30 dB gain across 2.4~2.5 GHz over temperature 0°C to +80°C
- **High linear output power:**
  - >26.5 dBm P1dB
  - Meets 802.11g OFDM ACPR requirement up to 23 dBm
  - Added EVM ~4% up to 20 dBm for 54 Mbps 802.11g signal
  - Meets 802.11b ACPR requirement up to 24 dBm
- **High power-added efficiency/Low operating current for both 802.11g/b applications**
  - ~22% @ $P_{OUT}$ = 22 dBm for 802.11g
  - ~26% @ $P_{OUT}$ = 23.5 dBm for 802.11b
- **Built-in Ultra-low $I_{REF}$ power-up/down control**
  - $I_{REF}$ <4 mA
- **Low idle current**
  - ~60 mA $I_{CQ}$
- **High-speed power-up/down**
  - Turn on/off time (10%~90%) <100 ns
  - Typical power-up/down delay with driver delay included <200 ns
- **High temperature stability**
  - ~1 dB gain/power variation between 0°C to +80°C
  - ~1 dB detector variation over 0°C to +80°C
- **Low shut-down current (< 0.1 µA)**
- **On-chip power detection**
- **25 dB dynamic range on-chip power detection**
- **Simple input/output matching**
- **Packages available**
  - 16-contact VQFN (3mm x 3mm)
  - Non-Pb (lead-free) packages available

# Enlarge Optimization Space



Representation of a search domain of an optimizer



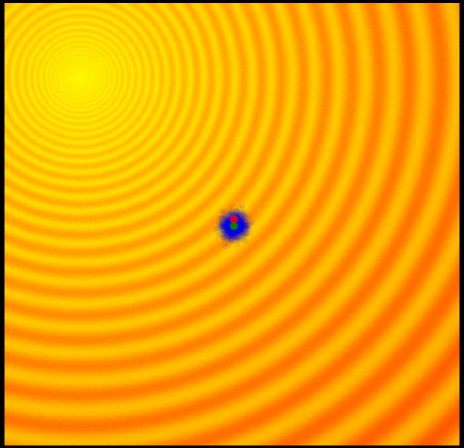
Contour plots of an optimization domain. A lot of local minima to get trapped into…

# ML Optimization – a new generation of algorithms

## Breakthrough techniques unlock a proven concept

### Challenge

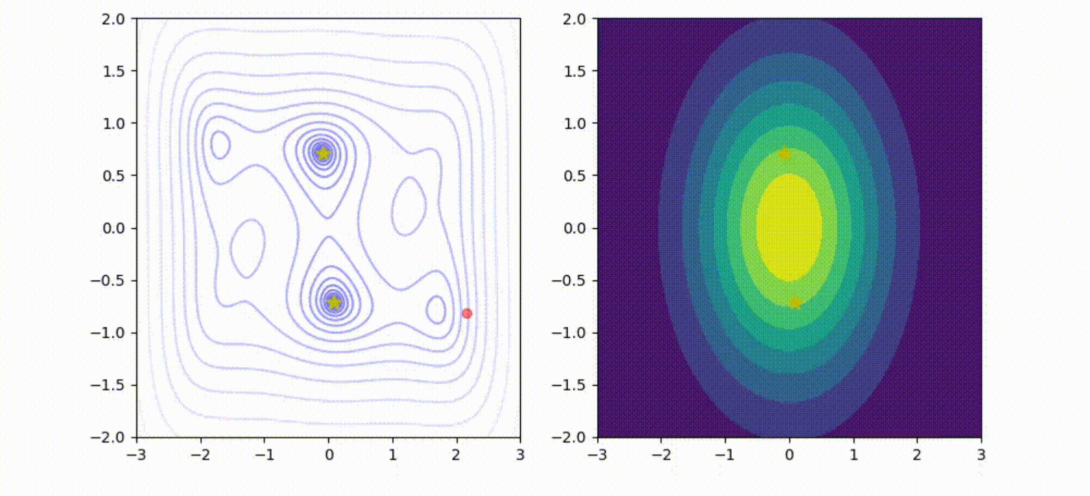
- **Conventional optimizers** struggle when handling more than **20 variables** and/or objectives/goals
- Result: Users need to work around limitations.
  → **Manually break** into many smaller problems



*Older fixed Gaussian distributions try within a circle of predictions*

### Solution

- Use new AI/ML-driven optimization techniques:
  - Expanded capacity to **handle 40+ parameters**, **multi-objectives**
- Able to automate complex processes, accelerating workflow
  - Creation of **Agents** and **Agentic workflows**



*AI/ML approaches are smart and adaptive, supporting higher optimization dimensions*

# AI/ML – a new generation of algorithms

**ML Optimizers especially shine when:**

- There is **no historical data** — cannot apply supervised/unsupervised Machine Learning algorithms
- **Limited** number of **iterations** (less than 10K) — cannot apply Reinforcement learning
- Can utilize **Deep Learning** (**DL**) approaches

**Re-enforcement Learning (RL) algorithms:**

- **Transfer learning** capabilities with accelerated learning
- Can be **combined** with **DL** as pre-training
- Simultaneously processes hundreds of design configurations using proprietary **multi-thread** technology

IC-CAP 2025 ML Optimizer

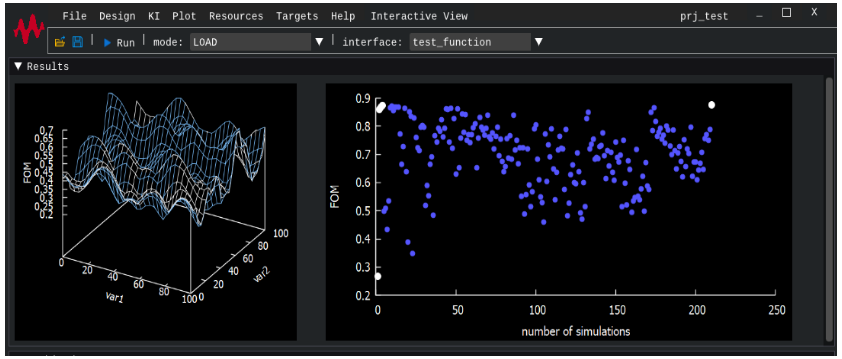
**< 10 Parameters** → with ML → **40 + Parameters**

*Zijian Song et al.*,
"Automating Compact Model Parameter Extraction: Industry-Grade Implementation and Benchmarking of Machine Learning-Driven Derivative-Free Algorithms", 2024 IEEE NAFEMS

ADS 2024 Worst-Case Bit-Pattern Generator for Eye Diagram

**14x Simulation Speed Up**

*Majid Ahadi Dolatsara*,
"Worst-Case Bit-Pattern Generator for Eye Diagram Analysis of Non-LTI High-Speed Channels", 2024 Signal Integrity Journal



mode: LOAD
interface: test_function

Nexus.AI

# ML Optimization – Applied to Complex Verifications

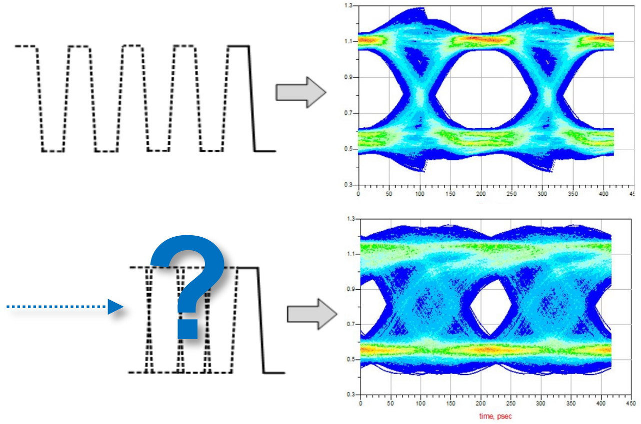
## Example: Worst-case Eye Pattern for HSD/Signal Integrity applications

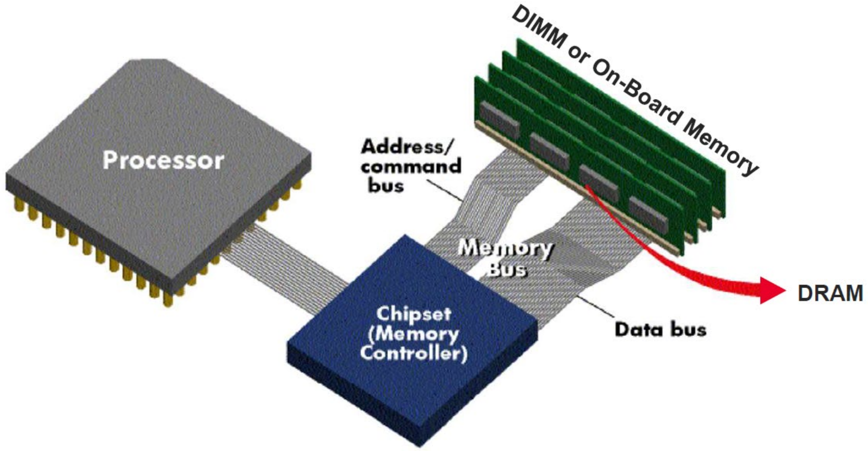
ML Optimization toward a maximal aggressor waveform

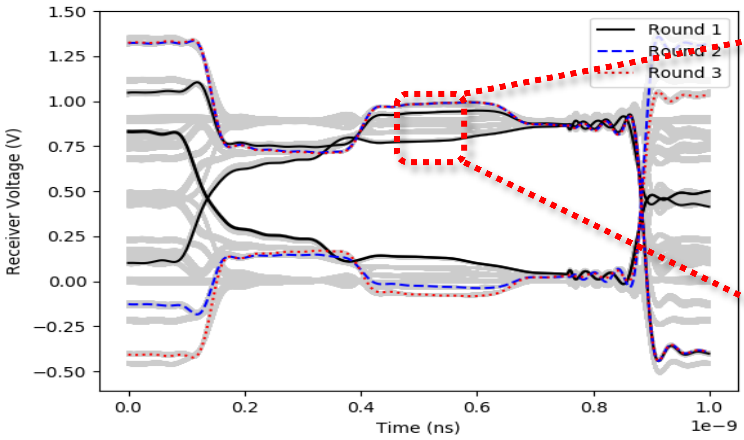
- Finds the **worst-case Eye Diagram**, using << shorter bit sequence, in the fewest # of Transient search simulations
- *Result*: Dramatic simulation speed-ups with optimized waveform

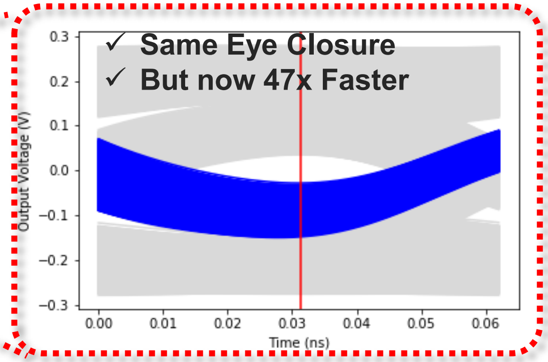
ML optimization for the Equalizers to clean up Eye Closure in ADS

*M. Ahadi, et. al., IEEE TEMC, V. 63. N. 1, 2020*









✓ Same Eye Closure

✓ But now 47x Faster

| | Eye height (mV) | Eye width (ps) | Number of bits |
|---|---|---|---|
| **Worst-eye** | 639 | 745 | 5,760 |
| **Transient Eye** | 639 | 744 | 1,000,000 |

# System Level - Wireless

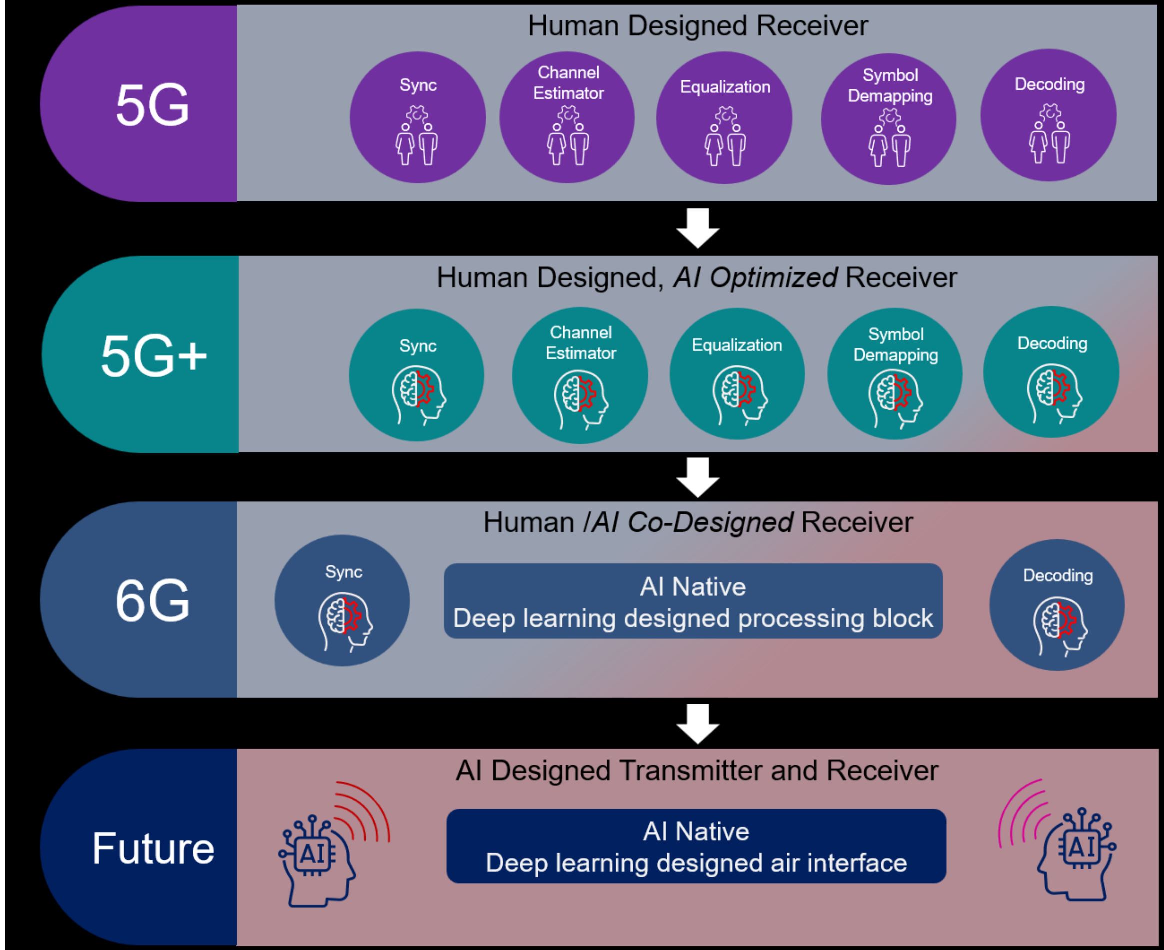
## Key Challenges

- High-fidelity modeling requires **system architecture**, DSP / **baseband algorithm** development, and **RF system design**
- Accurate digital twin system models **require integrated scenario- modeling** and network simulation

# AI is Transforming the 6G Air face

## New development environments needed to enable 6G

- 6G is **transitioning** from fixed/allocated assets to optimized, **reconfigurable Physical Layer** (**PHY**)
- **Systems** are increasingly **autonomous**, using advances in AI/ML
- **RF Hardware** will need to accommodate **dynamic adaption**: Freq, BW, MIMO, more



5G
Human Designed Receiver
Sync | Channel Estimator | Equalization | Symbol Demapping | Decoding

5G+
Human Designed, *AI Optimized* Receiver
Sync | Channel Estimator | Equalization | Symbol Demapping | Decoding

6G
Human /*AI Co-Designed* Receiver
Sync | AI Native Deep learning designed processing block | Decoding

Future
AI Designed Transmitter and Receiver
AI Native Deep learning designed air interface

Initial Set of 3GPP AI/ML Use Cases and Work Items: 3GPP TR 38.843

**Channel feedback**

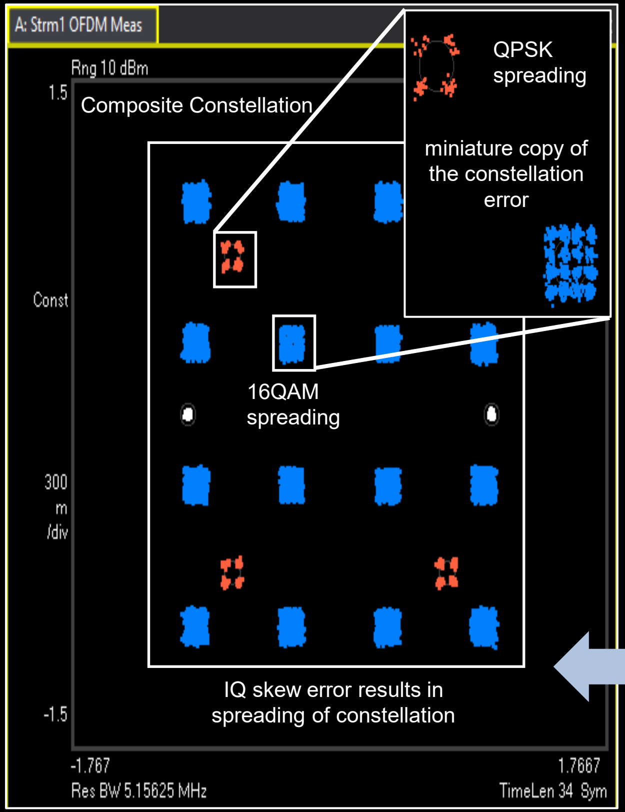
**Beam management**

**Precise positioning**

KEYSIGHT

# 6G AI/ML Air Interface Research Enabled by Keysight EDA

## Digital Twin for 6G Communications – Integrated Baseband, RF, and THz Channel + AI Receiver

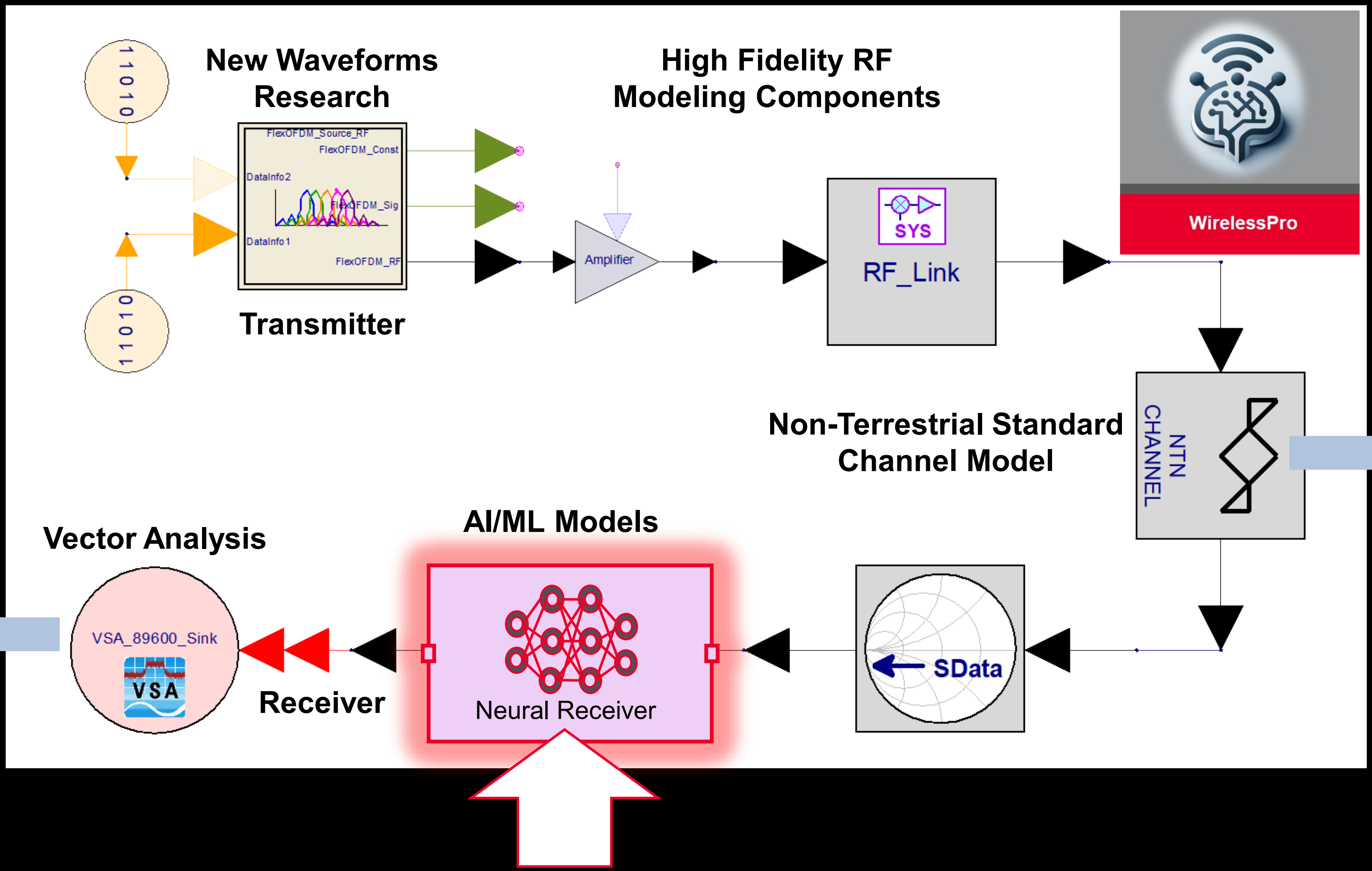


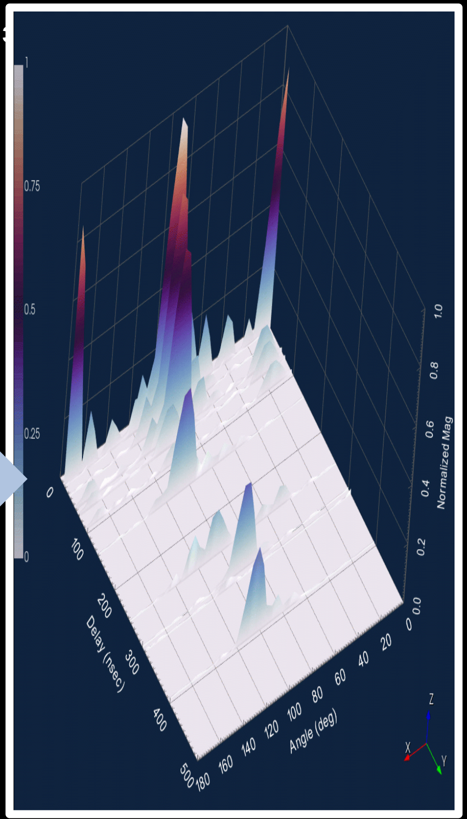
QPSK spreading

miniature copy of the constellation error

16QAM spreading

IQ skew error results in spreading of constellation

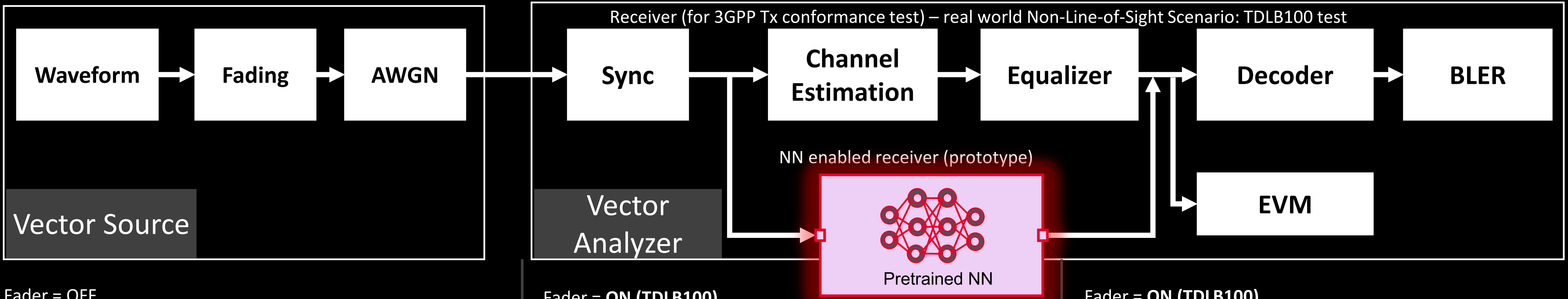




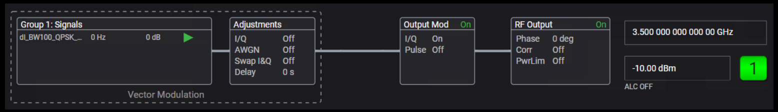
KEYSIGHT

Data Generation, NN Model Training and System Verification

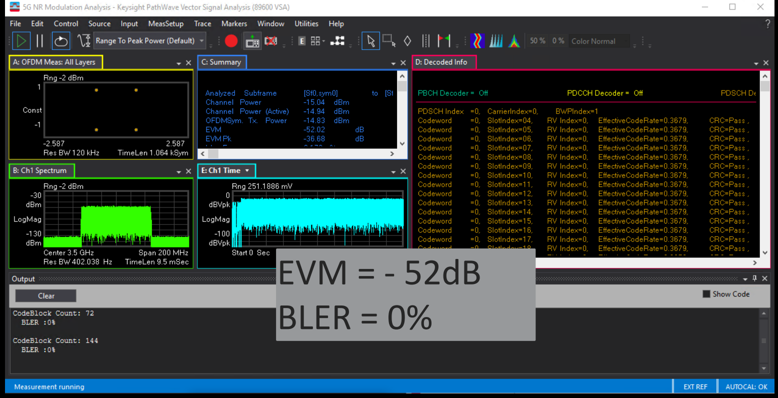
# Wireless NN Receiver Deployed in a Real Hardware System


Waveform
Fading
AWGN
Vector Source
Receiver (for 3GPP Tx conformance test) – real world Non-Line-of-Sight Scenario: TDLB100 test
Sync
Channel Estimation
Equalizer
Decoder
BLER
NN enabled receiver (prototype)
EVM
Vector Analyzer
Pretrained NN

Fader = OFF
AWGN = OFF


Group 1: Signals
dl_BW100_QPSK_... 0 Hz 0 dB
Adjustments
I/Q Off
AWGN Off
Swap I&Q Off
Delay 0 s
Vector Modulation
Output Mod On
I/Q On
Pulse Off
RF Output On
Phase 0 deg
Corr Off
PwrLim Off
3.500 000 000 000 00 GHz
-10.00 dBm
ALC OFF

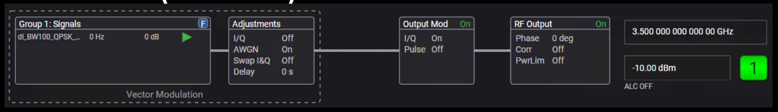
## Receiver (for 3GPP **Tx conformance test**)


EVM = - 52dB
BLER = 0%

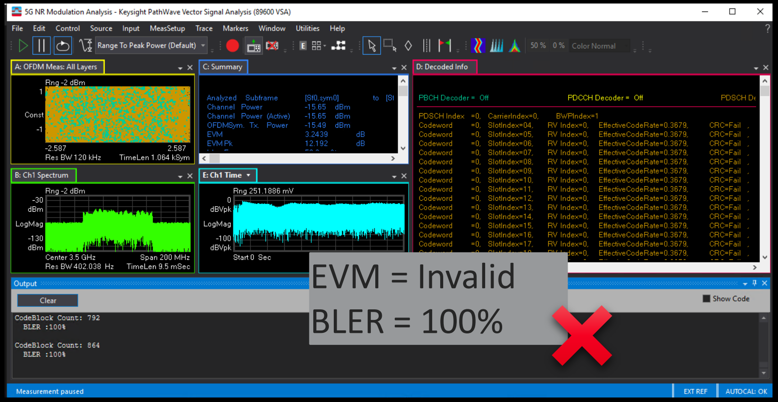
```
CodeBlock Count: 72
  BLER :0%

CodeBlock Count: 144
  BLER :0%
```

Measurement running

Fader = **ON (TDLB100)**
AWGN = **ON (SNR 20dB)**


Group 1: Signals
dl_BW100_QPSK_... 0 Hz 0 dB
Adjustments
I/Q Off
AWGN On
Swap I&Q Off
Delay 0 s
Vector Modulation
Output Mod On
I/Q On
Pulse Off
RF Output On
Phase 0 deg
Corr Off
PwrLim Off
3.500 000 000 000 00 GHz
-10.00 dBm
ALC OFF

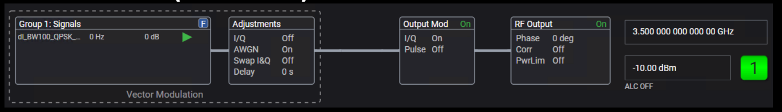
## TDLB100 conformance test – No NN


EVM = Invalid
BLER = 100% ✗

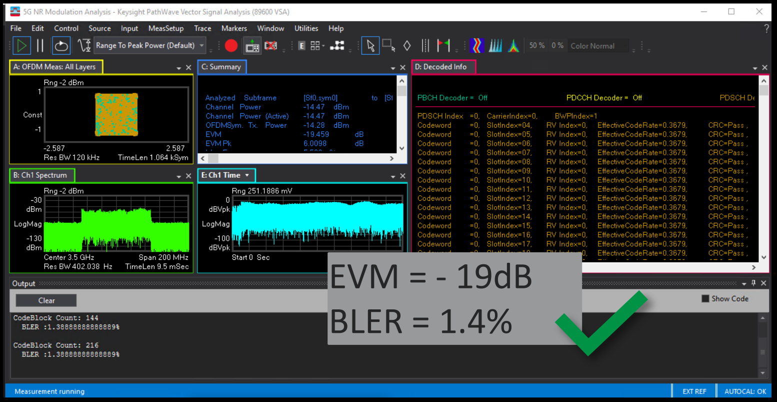
```
CodeBlock Count: 792
  BLER :100%

CodeBlock Count: 864
  BLER :100%
```

Measurement paused

Fader = **ON (TDLB100)**
AWGN = **ON (SNR 20dB)**


Group 1: Signals
dl_BW100_QPSK_... 0 Hz 0 dB
Adjustments
I/Q Off
AWGN On
Swap I&Q Off
Delay 0 s
Vector Modulation
Output Mod On
I/Q On
Pulse Off
RF Output On
Phase 0 deg
Corr Off
PwrLim Off
3.500 000 000 000 00 GHz
-10.00 dBm
ALC OFF

## NN enabled receiver


EVM = - 19dB
BLER = 1.4% ✓

```
CodeBlock Count: 144
  BLER :1.38888888888889%

CodeBlock Count: 216
  BLER :1.38888888888889%
```

Measurement running

**ONNX (Open Neural Network Exchange) model** (Training data: CF=3.5GHz, BW=100MHz, Channel CDLB100-20, AWGN: -5-20 dB, 300K batch)

# System Level - Wired

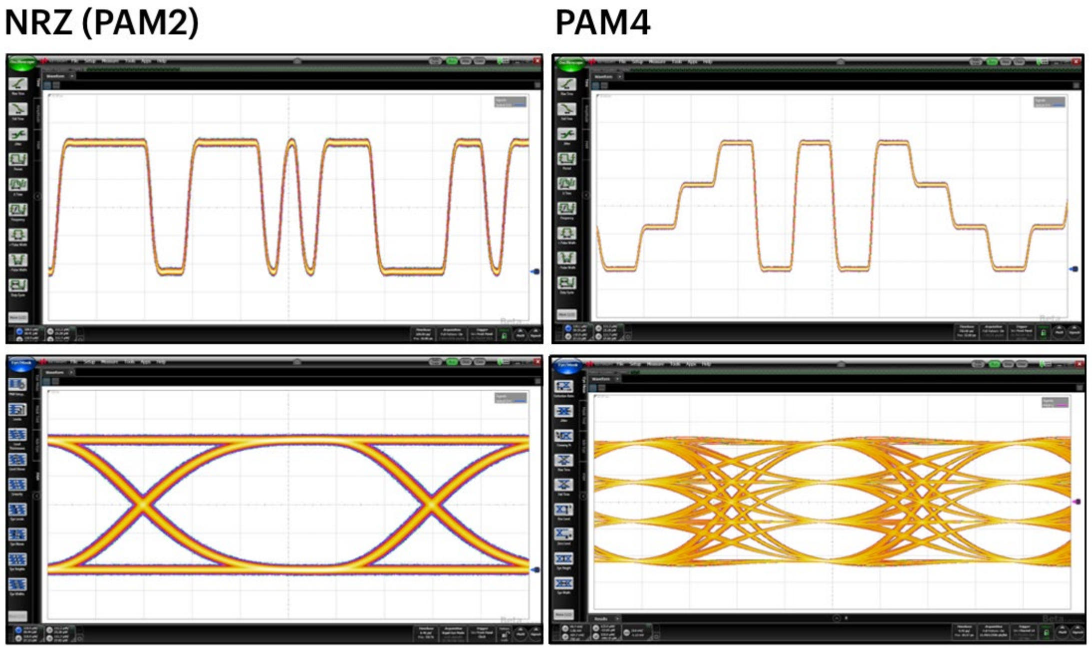
## Key Challenges

- **Metal interconnects** have **reached** their speed and capacity **limits**
- Datacenters need to **connect thousands** of **GPUs** to scale for AI load
  - **HPC** speed up **scales logarithmic**, **latency** is **critical**
  - **Ethernet standards** are **evolving** to support larger bandwidth and Bitrates for AI workload

# Modulation Schemes Evolve

## Advanced Modulation and Coding Challenges

- PAM2 (NRZ) backbone of PCIe Gen1-5 & Ethernet 802.3 – 100G
  - Better noise margins but lower bandwidth
- PAM4 standard for **200G, and 400G Ethernet, PCIe Gen 6**, and **future Gen 7**
  - Signals use **four amplitude/voltage** levels, **doubling the data rate (Bits)** in the same bandwidth as NRZ
- PAM4 requires sophisticated signal integrity management due to reduced noise margins



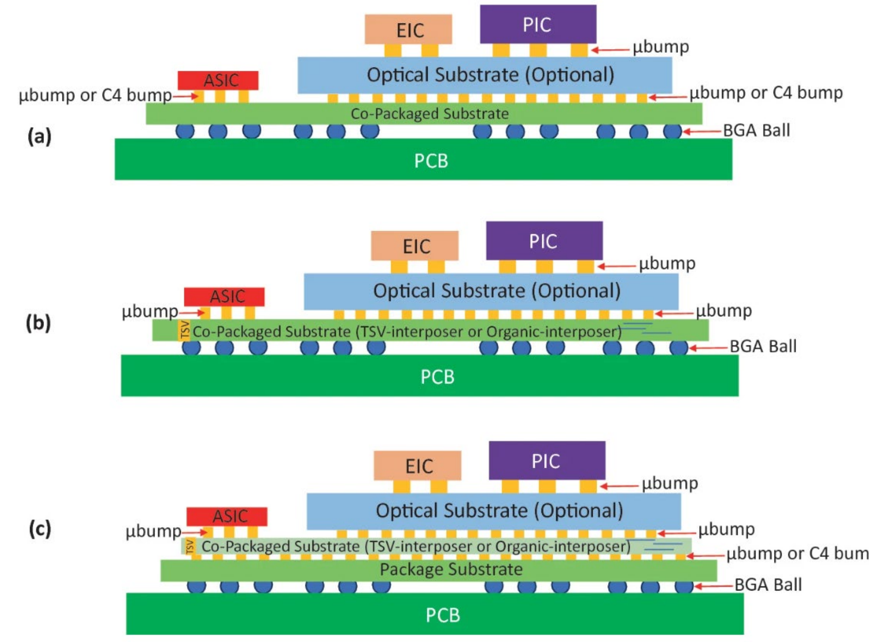
NRZ (PAM2)

PAM4

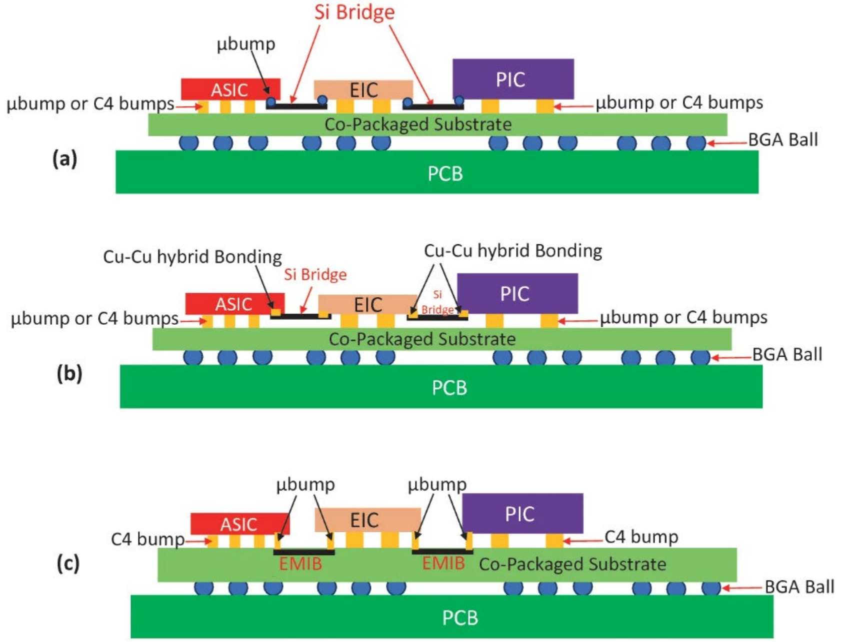
| Feature | PAM2 (NRZ) | PAM4 |
|---|---|---|
| **Bits per symbol** | 1 | 2 |
| **Voltage levels** | 2 | 4 |
| **Noise margin** | High | Lower |
| **Complexity** | Low | High |
| **Use cases** | PCIe Gen 1–5, USB | PCIe Gen 6+, 400G Ethernet, Data Centers |

# Technology integration needed to support HPC and PAM4 requirements

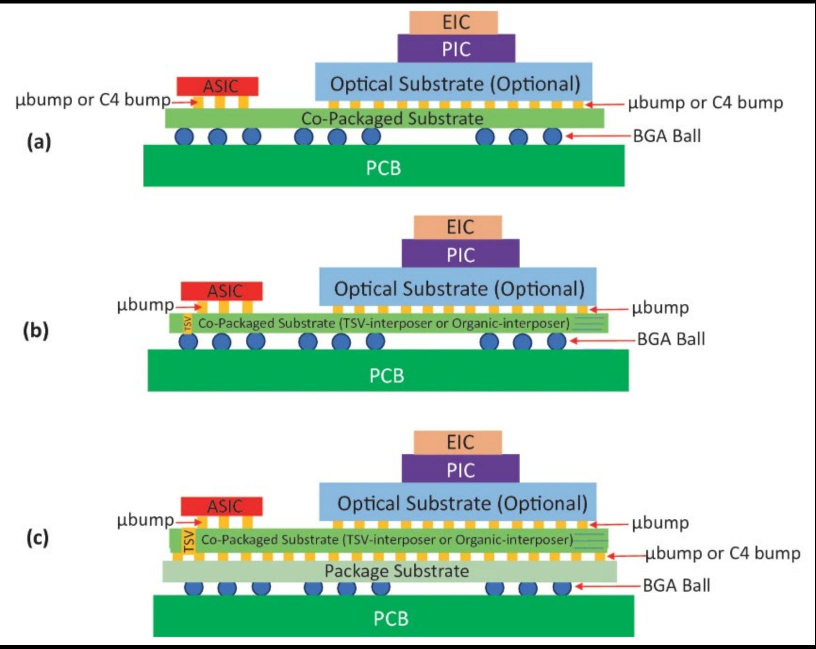
## 2D Heterogeneous Integration of ASIC Switch, PIC and EIC



## 2D Heterogeneous Integration of ASIC Switch, PIC and EIC with Bridges



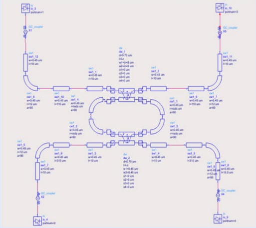
## 3D Heterogeneous Integration of ASIC Switch, PIC and EIC



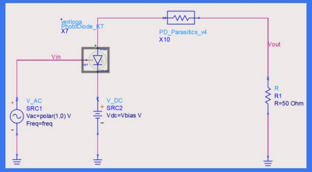
# Photonic Design Solutions - Challenging

## Models & Design

Micro Ring Resonators & Modulator

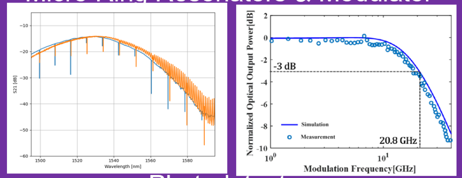


Photodetectors

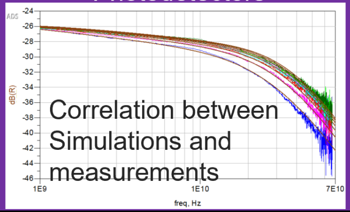


## Design & Test Validations

Micro Ring Resonators & Modulator



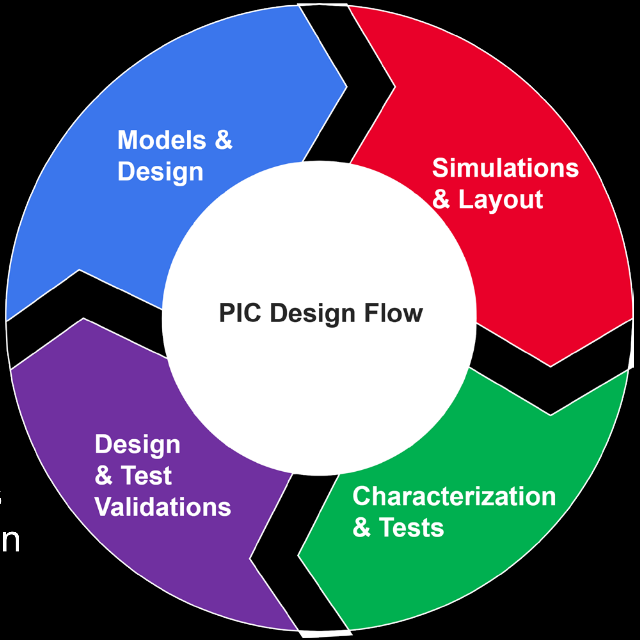
Photodetectors



Correlation between Simulations and measurements

Photonic Model

Photonics Verification solutions



Models & Design

Simulations & Layout

PIC Design Flow

Design & Test Validations

Characterization & Tests

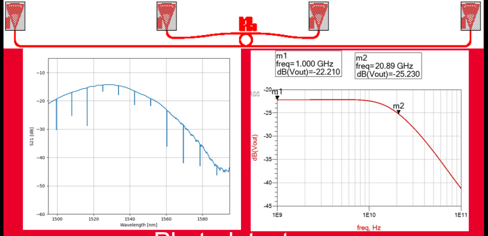
RF simulation technology and flexible workflows

Photonic Characterization Capabilities

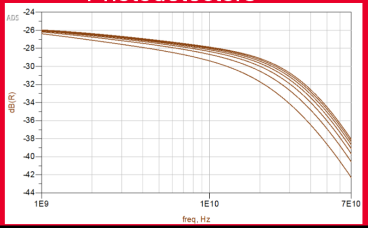
E-O-E design, simulation and measurement flow

## Simulations & Layout

Micro Ring Resonators & Modulator



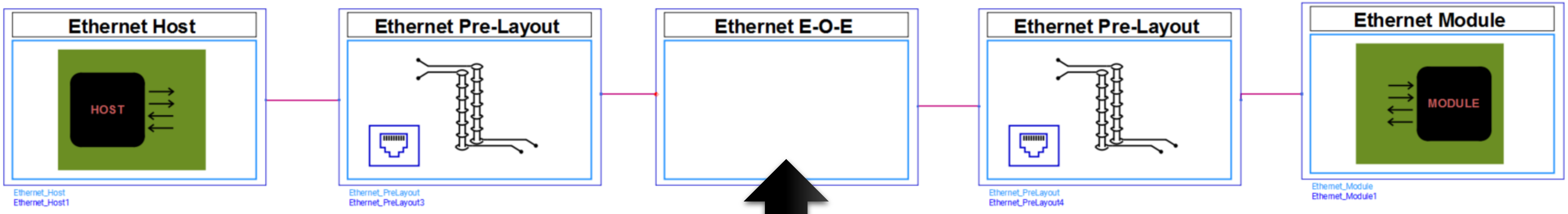
Photodetectors

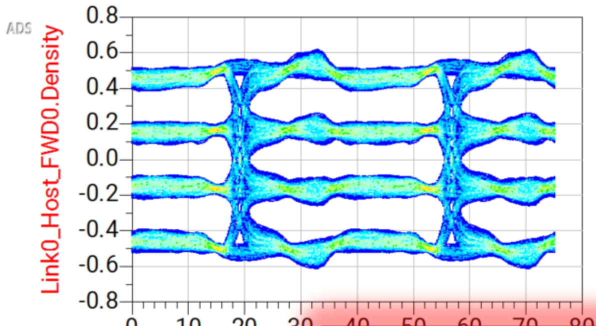


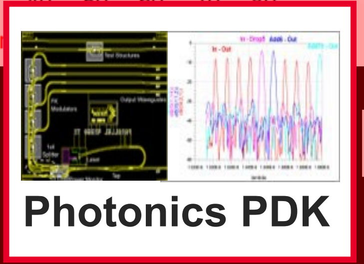
## Characterization & Tests

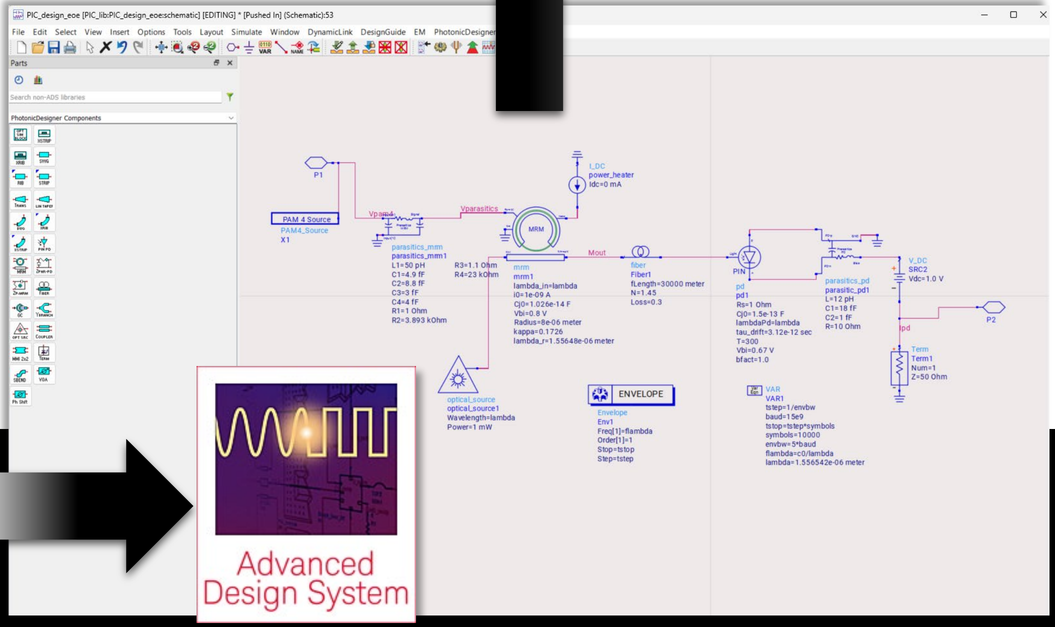
# E-O-E simulation for digital standards: Ethernet, PCIe

## Example workflow









PAM4_Source
X1

parasitics_mrm
parasitics_mrm1
L1=50 pH
C1=4.9 fF
C2=8.8 fF
C3=3 fF
C4=4 fF
R1=1 Ohm
R2=3.893 kOhm
R3=1.1 Ohm
R4=23 kOhm

I_DC
power_heater
Idc=0 mA

mrm
mrm1
lambda_in=lambda
i0=1e-09 A
Cj0=1.026e-14 F
Vbi=0.8 V
Radius=8e-06 meter
kappa=0.1726
lambda_r=1.55648e-06 meter

fiber
Fiber1
fLength=30000 meter
N=1.45
Loss=0.3

pd
pd1
Rs=1 Ohm
Cj0=1.5e-13 F
lambdaPd=lambda
tau_drift=3.12e-12 sec
T=300
Vbi=0.67 V
bfact=1.0

parasitics_pd
parasitic_pd1
L=12 pH
C1=18 fF
C2=1 fF
R=10 Ohm

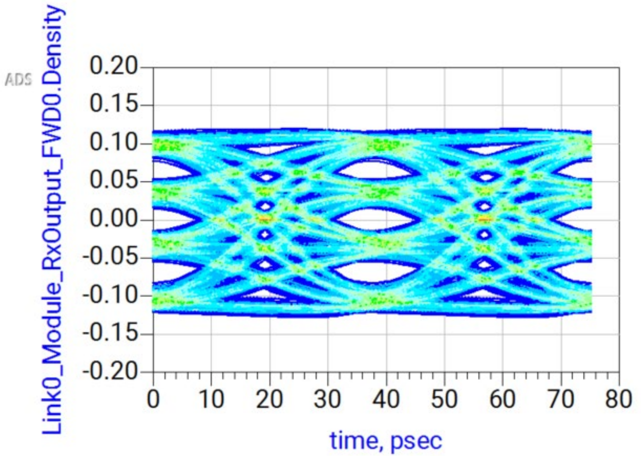
V_DC
SRC2
Vdc=1.0 V

Term
Term1
Num=1
Z=50 Ohm

optical_source
optical_source1
Wavelength=lambda
Power=1 mW

Envelope
Env1
Freq[1]=flambda
Order[1]=1
Stop=tstop
Step=tstep

VAR
VAR1
tstep=1/envbw
baud=15e9
tstop=tstep*symbols
symbols=10000
envbw=5*baud
flambda=c0/lambda
lambda=1.556542e-06 meter

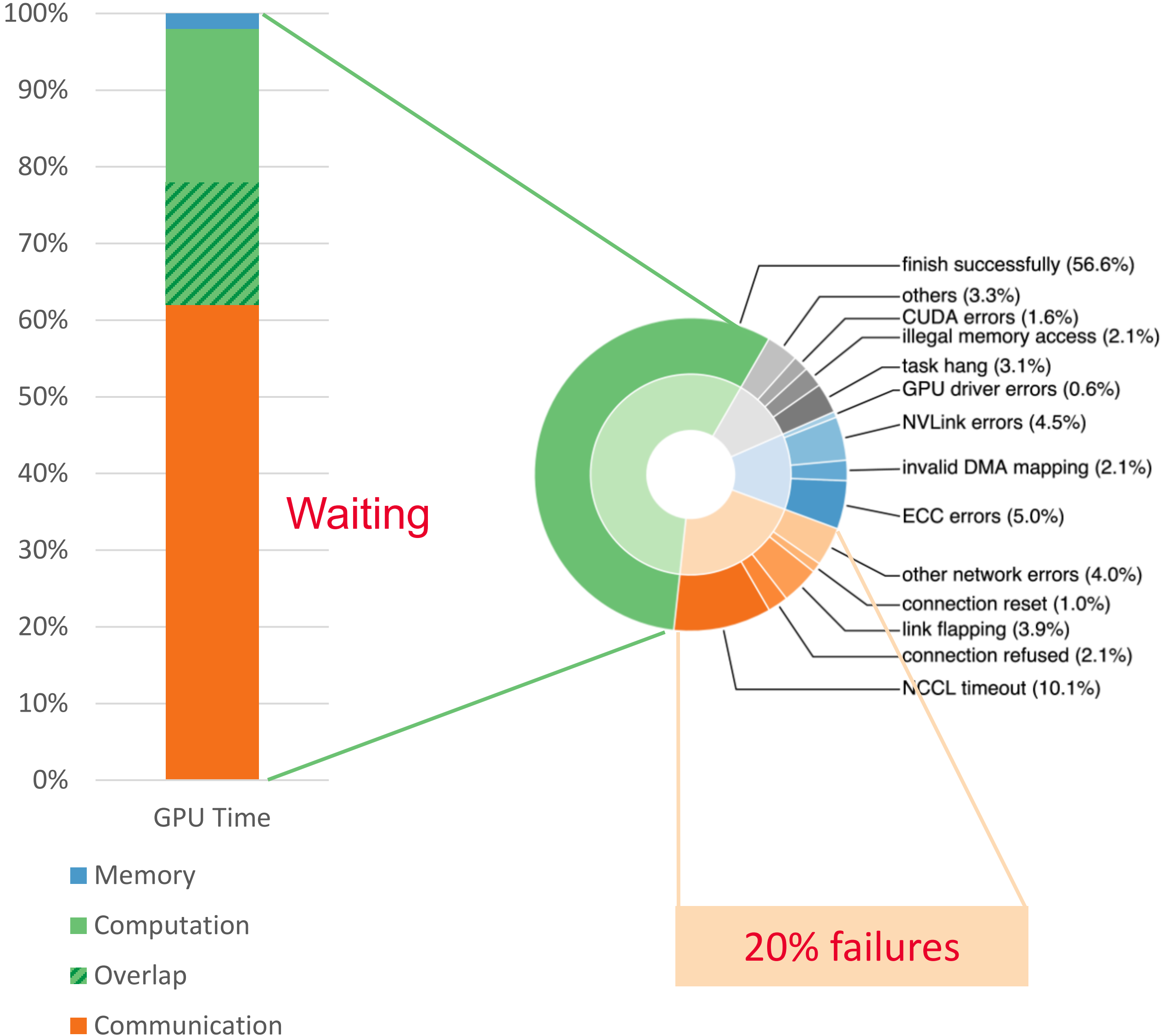


# Datacenter Level

## Key Challenges

- High networking bandwidth for **AI/ML workloads**
- **Cost to test network** designs and parameters
  - GPU Availability
  - Unique test engineering skillset for AI networks
- Time-to-market to validate **AI Clusters**

*Vision transformer example. Source: https://github.com/facebookresearch/HolisticTraceAnalysis/*



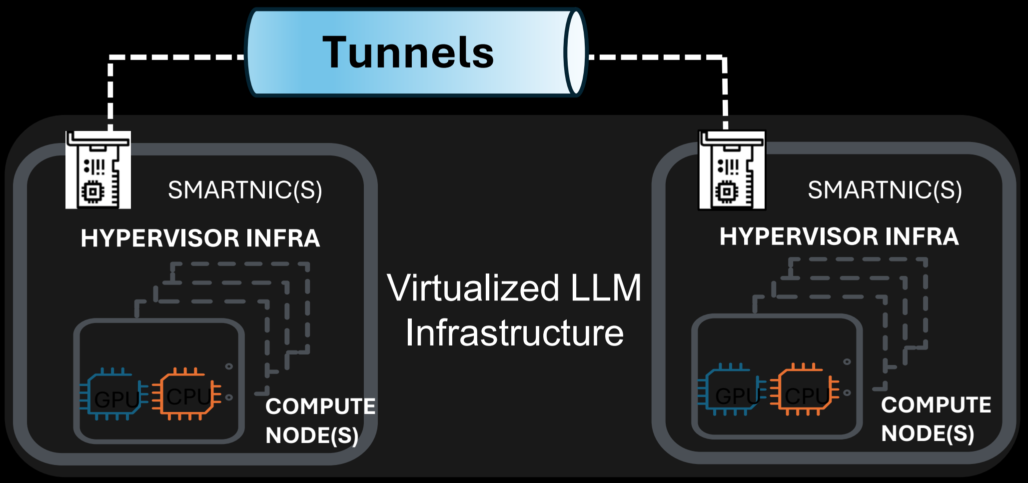
*Source: Unicron: Economizing Self-Healing LLM Training at Scale, Tao He[1], Xue Li[1], Zhibin Wang[1,2], Kun Qian[1], Jingbo Xu[1], Wenyuan Yu[1], Jingren Zhou[1] [1]Alibaba Group, [2]Nanjing University*

KEYSIGHT

# Operation of AI ML Network Infrast re

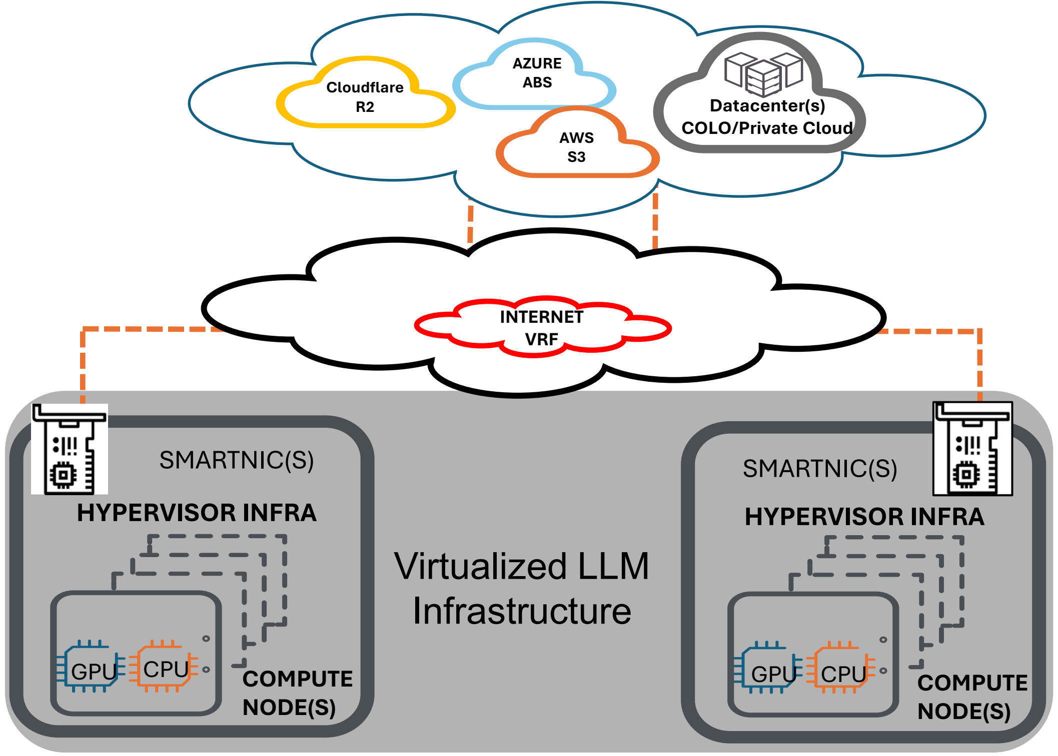
**Backend Data Center for AI Models Training**
East-West Traffic Test Demands –

- **Distributed** GPU/CPU architectures
- Collective communications & parallel **processing** among GPU nodes
- Hyper-virtualized **infrastructures** for multi tenancy
- Immense **performance needs** for lossless connectivity and minimum tail-end latency

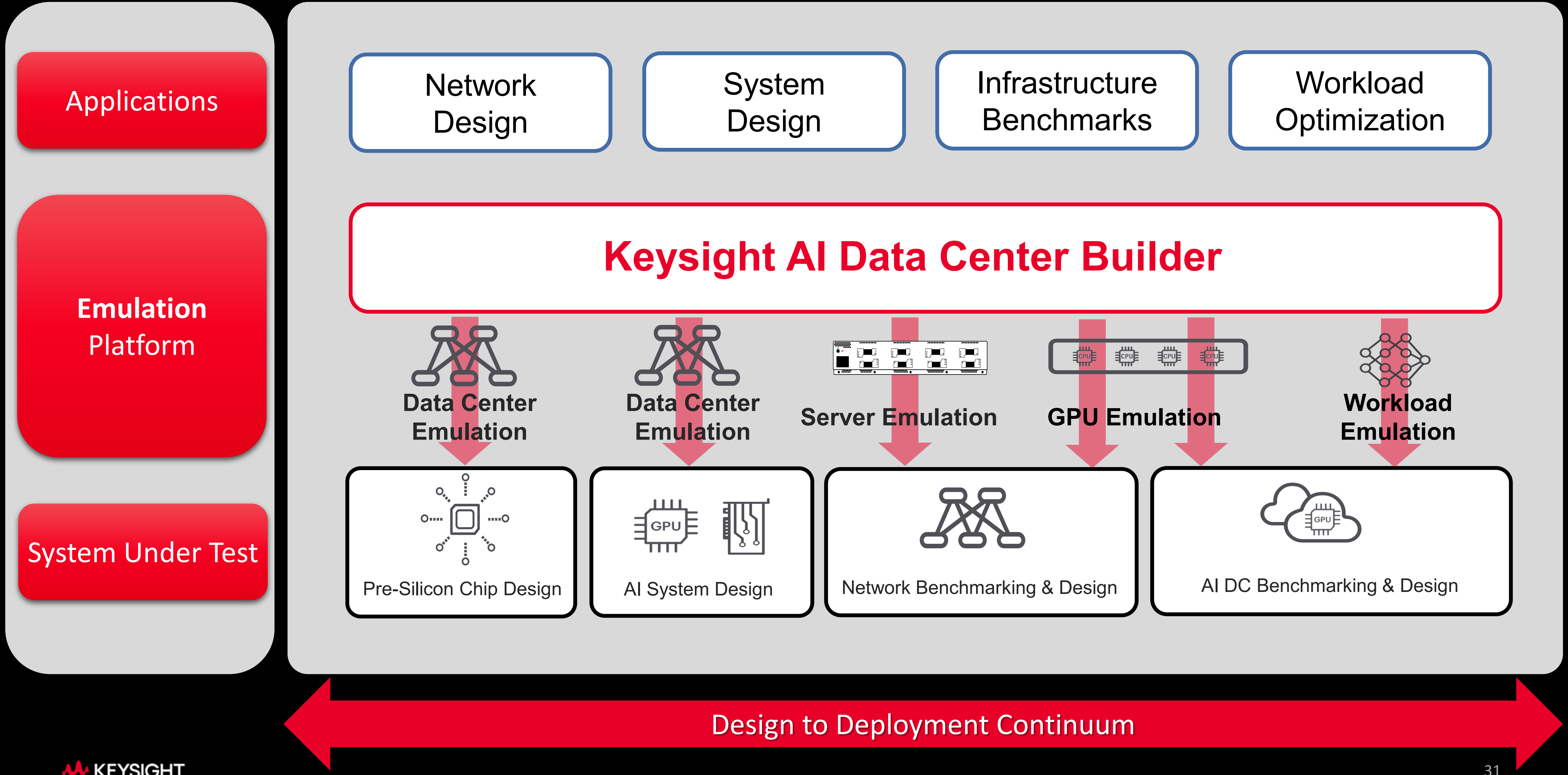


**Front-end Data Center for Inference Workloads**
North-South Network Traffic Test Demands -

- **GPUs** need **high-speed access** to block/remote **storages**
- Provisions to **secure data (encrypted)** in **motion**
- **Ultra-low latency** demands



# Product lifecycle & Use case Coverage



**Applications**

**Emulation Platform**

**System Under Test**

Network Design

System Design

Infrastructure Benchmarks

Workload Optimization

**Keysight AI Data Center Builder**

**Data Center Emulation**

**Data Center Emulation**

**Server Emulation**

**GPU Emulation**

**Workload Emulation**

Pre-Silicon Chip Design

AI System Design

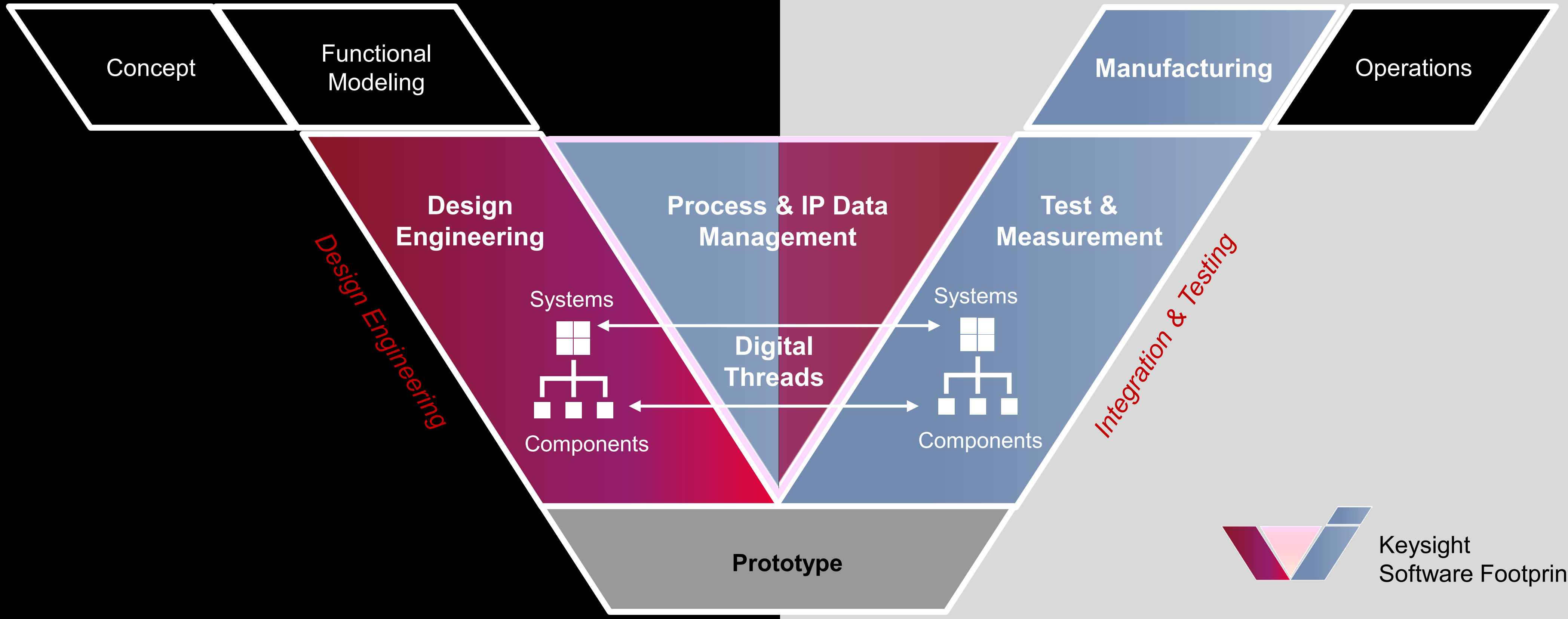
Network Benchmarking & Design

AI DC Benchmarking & Design

Design to Deployment Continuum

# Summary - End-to-End Workflow

# Design solutions with users in mind



Concept

Functional Modeling

Manufacturing

Operations

**Design Engineering**

**Process & IP Data Management**

**Test & Measurement**

Design Engineering

Systems

Components

**Digital Threads**

Systems

Components

Integration & Testing

**Prototype**

Keysight
Software Footprint

DIGITAL TWINS

PHYSICAL SYSTEMS

# Thank you