LIGHTMATTER

Future Compute Platforms through Silicon Photonics and Advanced Chiplet Packaging

Sandeep Sane, Ph.D.
Senior Director, Head of Packaging Technologies

$850M RAISED

Fidelity
Google Ventures
Sequoia
Spark Capital
Viking
T. Rowe Price
Matrix Partners
SIP Capital
MIT
Stanford

3
OFFICES

Mountain View (HQ)

Boston

Toronto

300
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Founder, CEO

Darius Bunandar, PhD
Founder, Chief Scientist

Thomas Graham
Founder

Simona Jankowski
CFO

Ritesh Jain
SVP, Engineering & Ops

Bob Turner
SVP, Sales & Solution Arch

Sujatha Wagle
VP, Supply Chain Ops

Beth Keil
SVP, People

Steve Klinger
VP, Product

Boon Tan
VP, Product Engineering

Colin Sturt
General Counsel

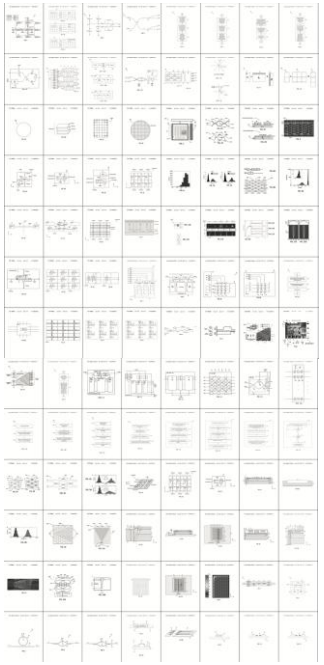
Kaushik Patel, PhD
VP, Photonics & Si Eng

Praveen Kukkamalla
VP, Sales

Kurt von Hausen
VP, Cloud Services Sales

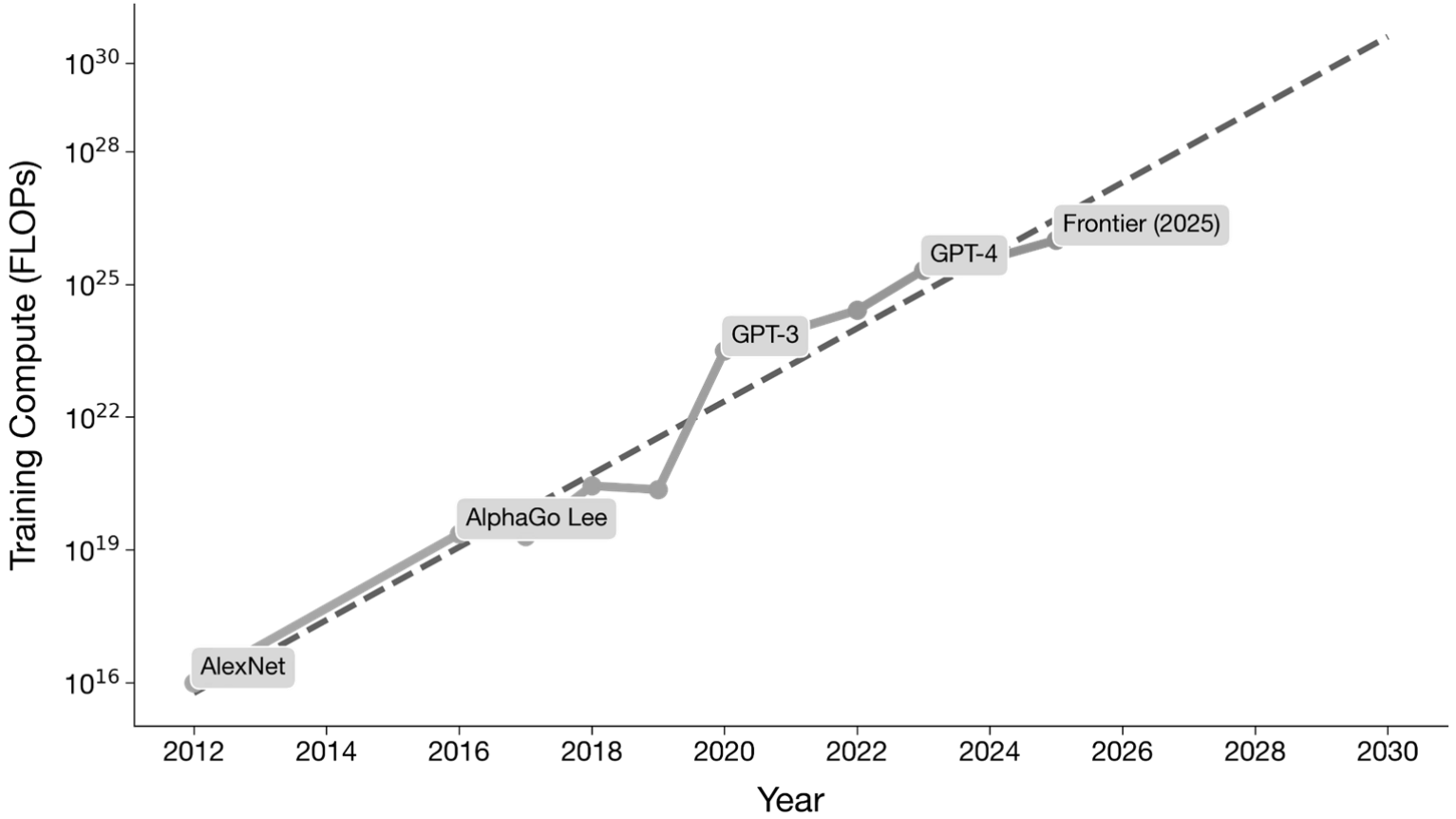
Israel Kandarian
Head of Creative Marketing

311
PATENTS

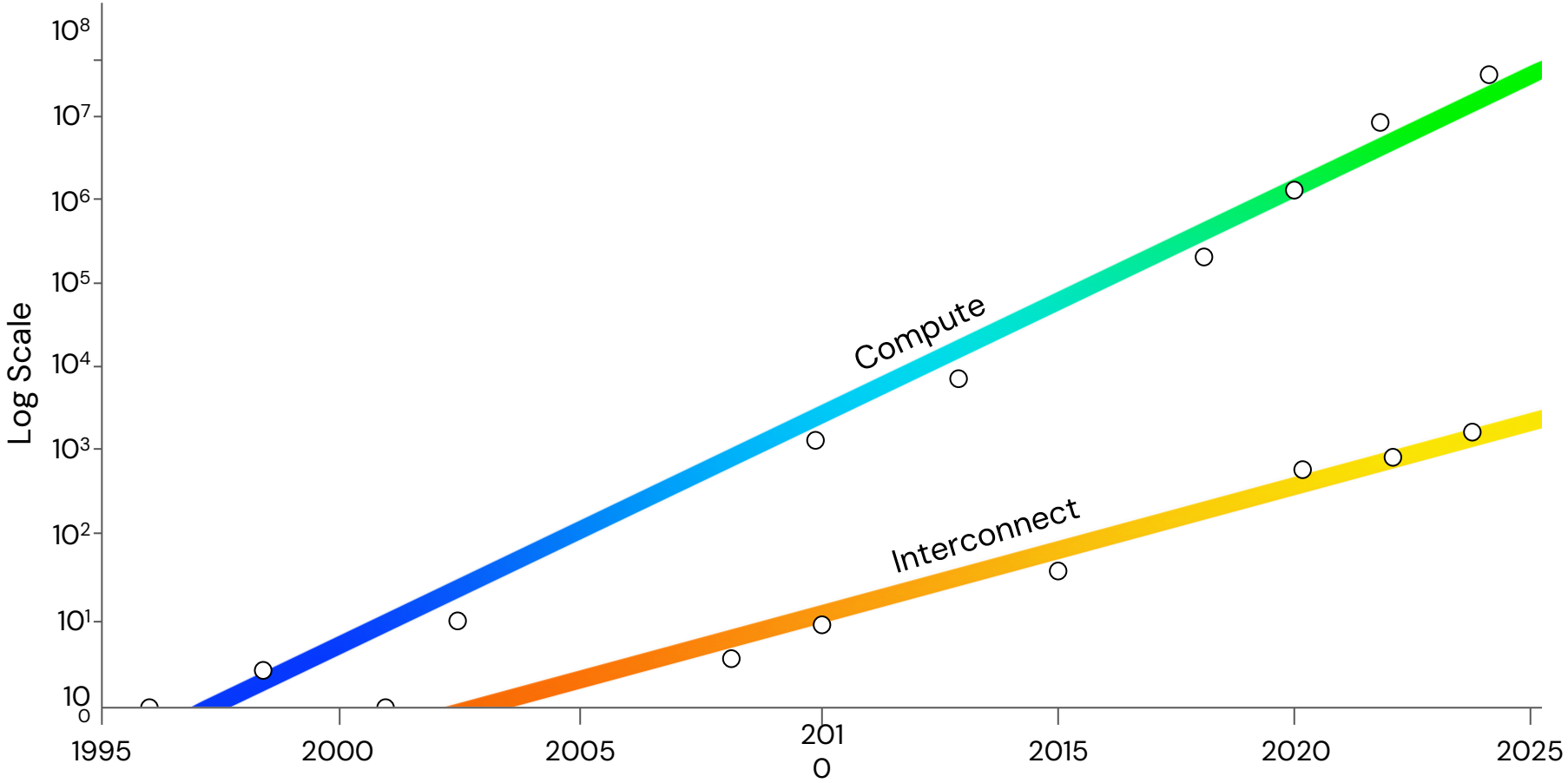


Granted & Pending

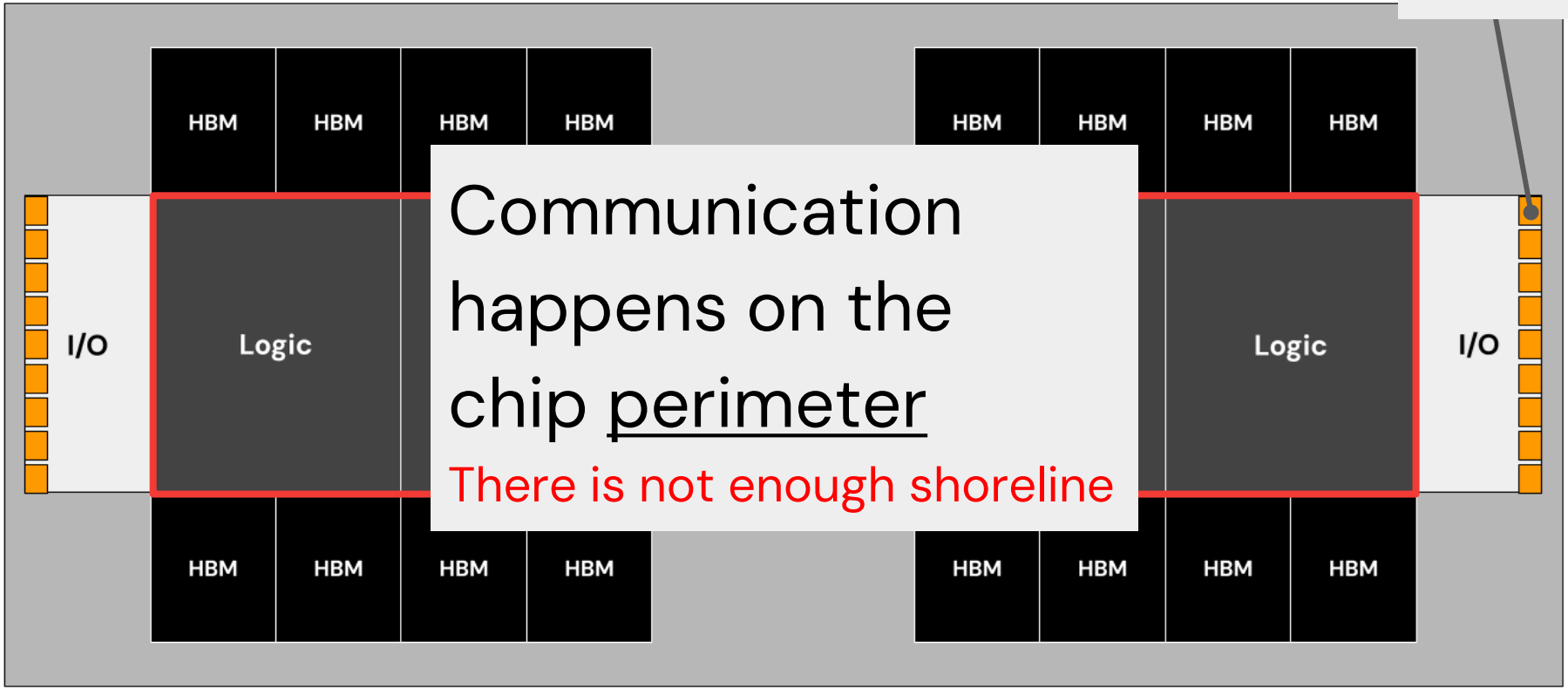
10^9 Growth in a Decade



Interconnect Progress Is Too Slow



Challenge: Package Area and Shoreline



A new paradigm is needed

Photonics Evolution: Moving Closer to the Chip

Bandwidth

100x

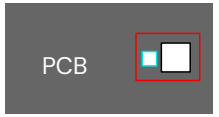
10x

1x

3D Photonic Interposer

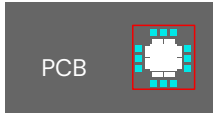
- ASICs 3D stacked on PIC
- Advanced package, OCS
- ~2.5 pJ/bit

3D Co-Packaged Optics (CPO)



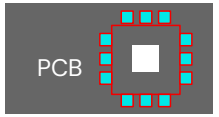
- 3D stacked PIC/EIC chiplet
- Standard pkg, UCIe
- ~3 pJ/bit

2D Co-Packaged Optics (CPO)



- I/O chiplet (PIC+EIC)
- In-package, XSR SerDes
- ~6-10 pJ/bit

Near Package Optics (NPO)



- Pre-packaged OE (PIC+EIC)
- LR SerDes, Re-timer
- ~8-15 pJ/bit

Power Efficiency

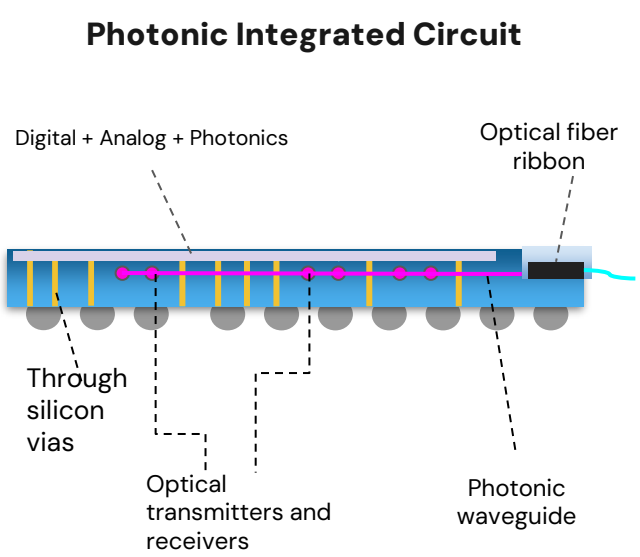
Highest

Lowest

Copper, Pluggables

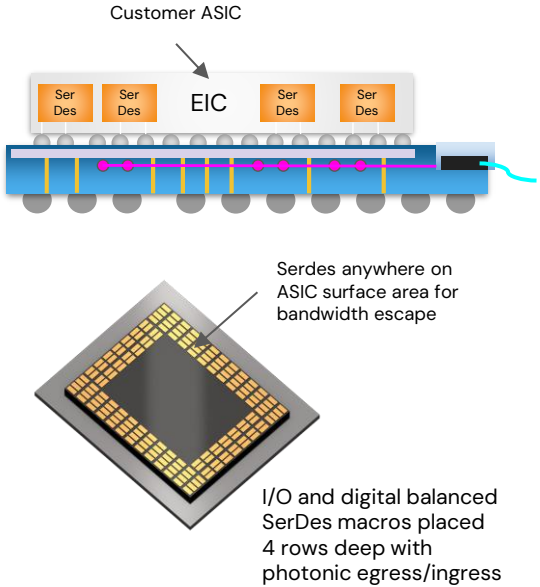
Photonic Integrated Circuit: PIC
Electronic Integrated Circuit: EIC
Optical Engine (OE) = PIC+EIC

Passage ™ : 3D Photonic Interposer

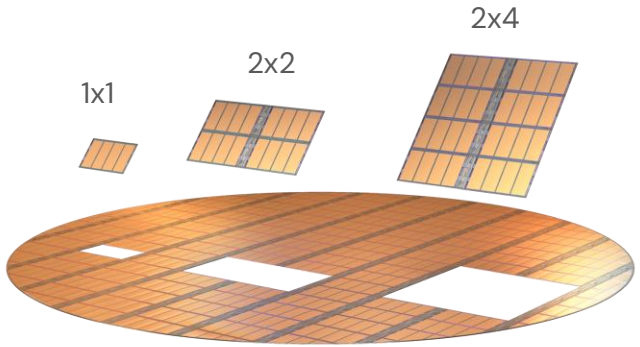


Passage Cross Section

(note: digital/analog can be integrated in top die; FAB choice dependent)



Passage value (3D integration) and density

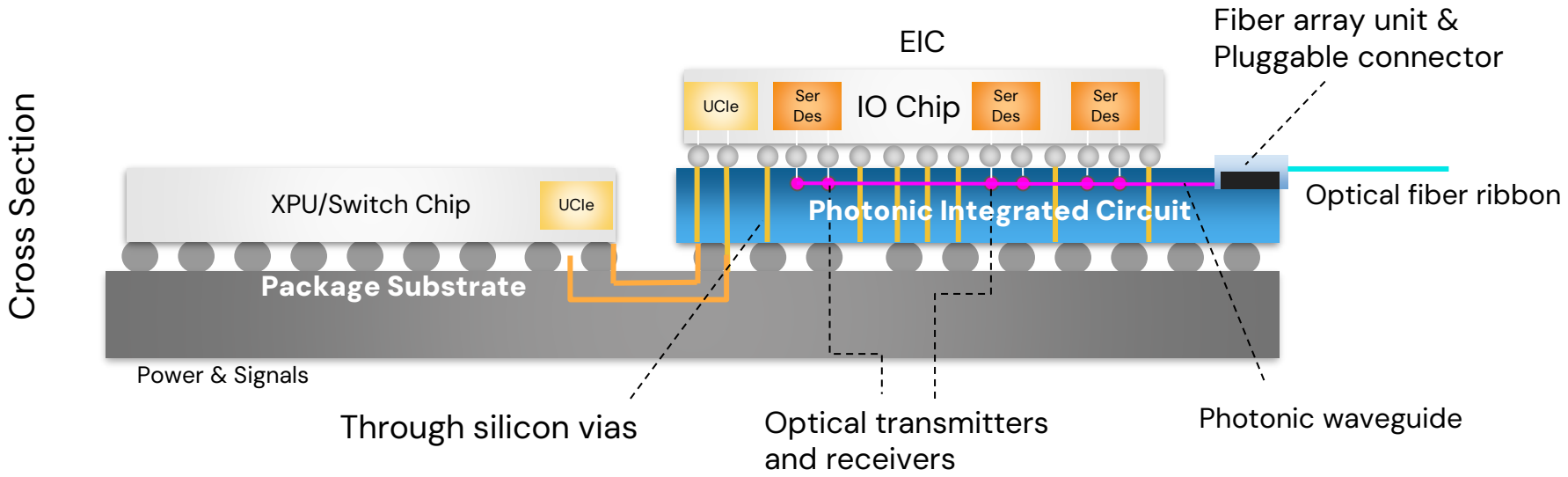


Passage scalability from single to multi-reticle

Built on 3D packaging technology and a Chip-on-Wafer assembly flow

3D CPO Requires Compact Optical Modulators and Receivers

Standard Package Example

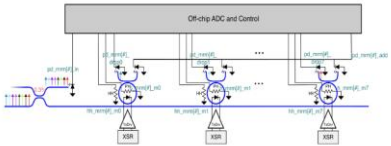


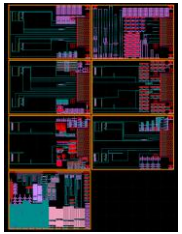
Standard processes today

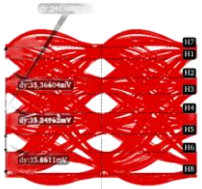
- Bump pitch: ~120 µm
- Bump size: ~80 µm
- **Area for a transmitter/receiver: 0.015 mm²**

Engineering Capabilities: Rings → Racks

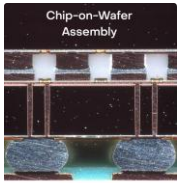
DEVICES

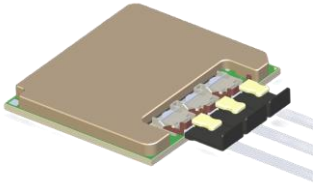


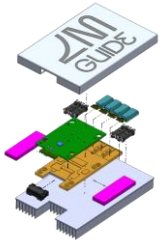




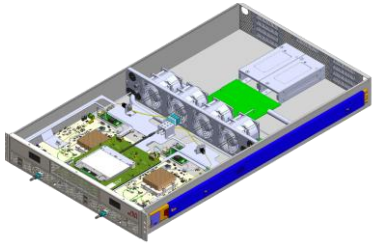
CHIPS

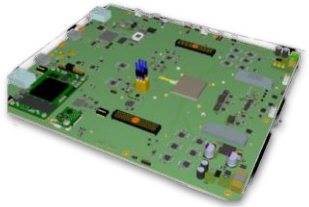




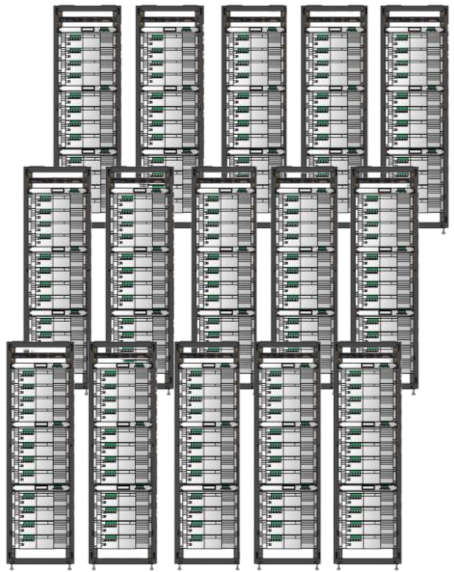


SYSTEMS





DATACENTER



Enabling All Link Architectures

MULTIPLE ROADMAP GENERATIONS HERE TODAY

STANDARDS COMPLIANT

OR

CUSTOM ADVANCED

Bandwidth	Modulation	Number of Wavelengths	Transmission Type	WDM Type
56 Gbps	NRZ	16	Bi-directional	DWDM
56 Gbps	NRZ/PAM4	16	Uni-directional	DWDM
112 Gbps	PAM4	16	Uni-directional	DWDM
224 Gbps	PAM4	4	Bi-directional	CWDM
224 Gbps	PAM4	4	Uni-directional	CWDM

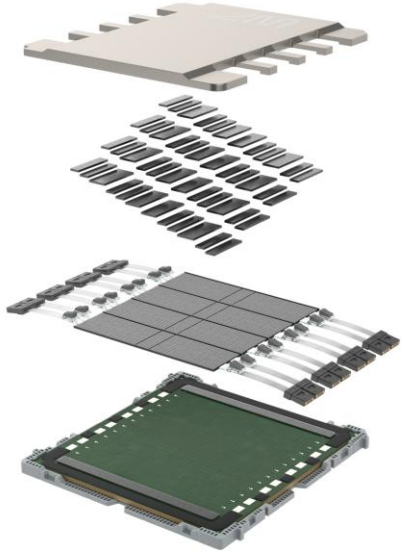
800 Gbps and 1600 Gbps per fiber already available. Leapfrog with Lightmatter.

Passage L-Series

3D CPO

Available 2026

Passage M-Series



Photonic Interposer

Available Now

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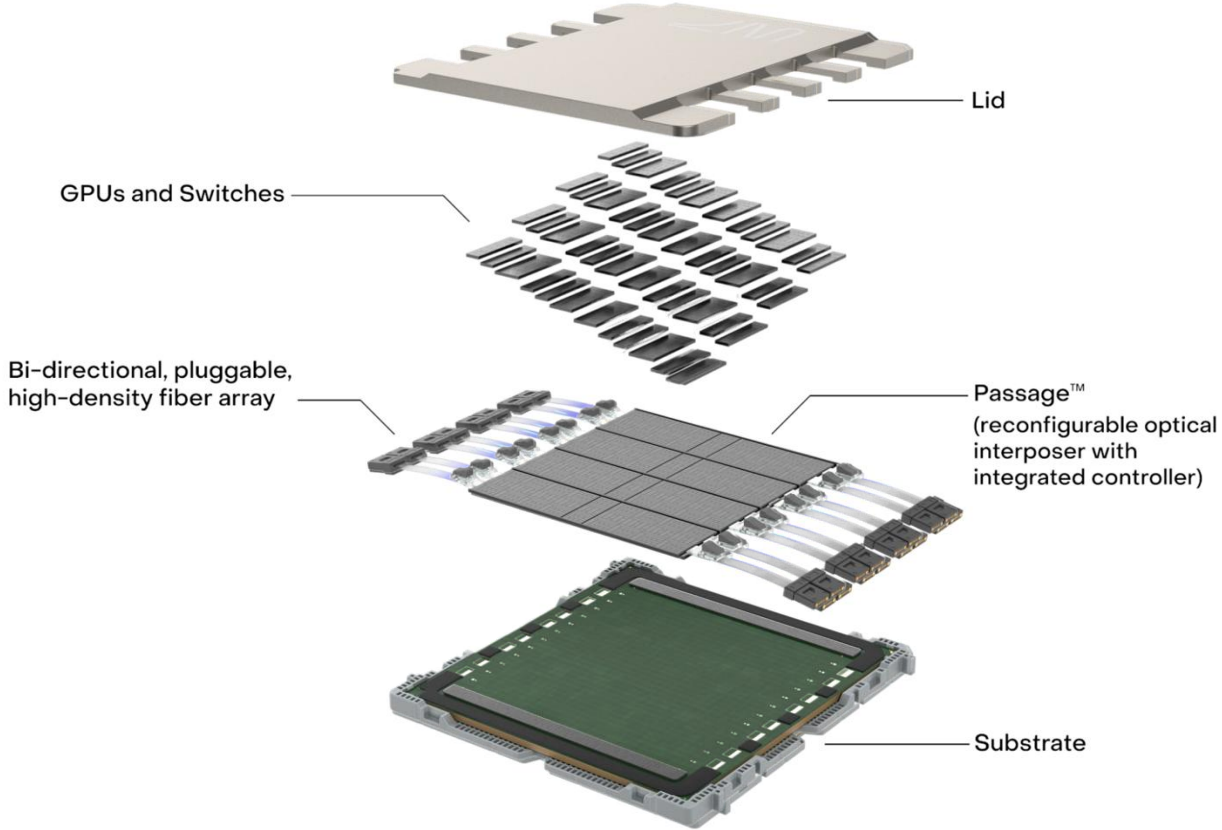
Passage™ M Series: Multi-Reticle PIC



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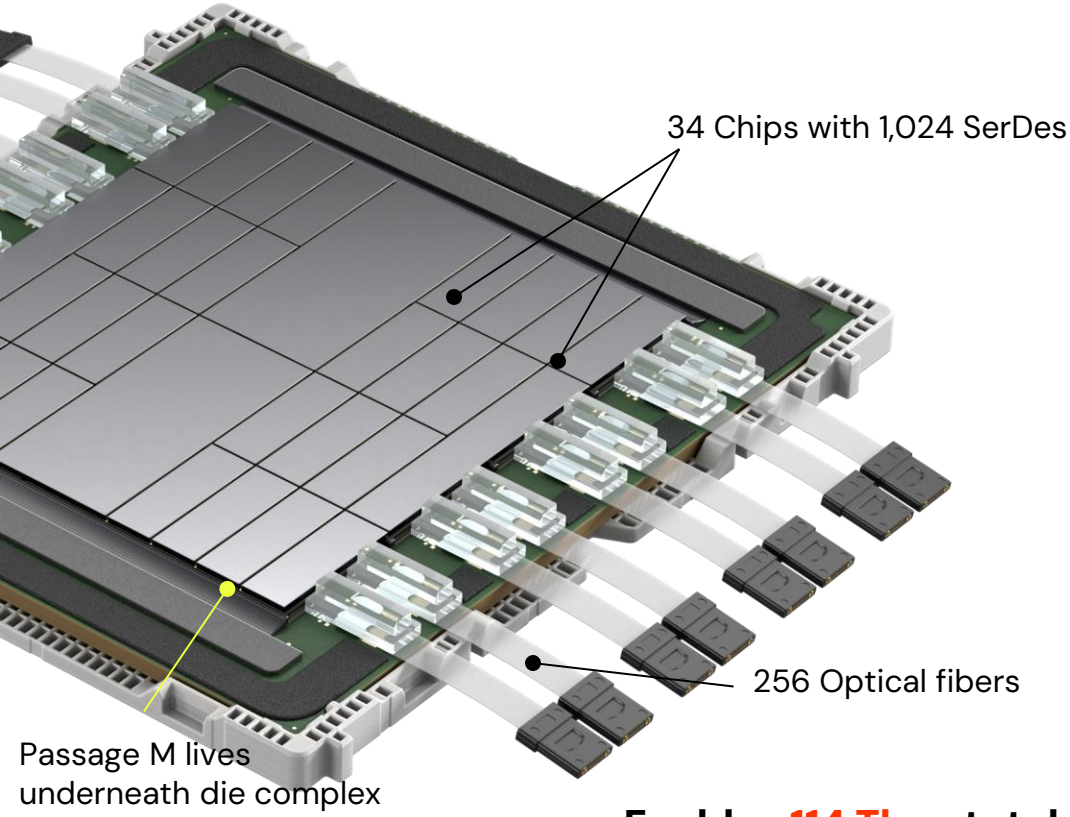
Passage™ M Series

Photonic interposer reference platform



Specifications	
Bandwidth (Tx + Rx)	Up to 114 Tbps
# of SerDes	1024
Silicon die Complex	4,000 mm^2
Power delivery	>1.4 W/mm^2 density
Fibers	256
Redundancy	Optical circuit switching
Substrate Form Factor	91x85mm

Enables 114 Tbps total bandwidth.

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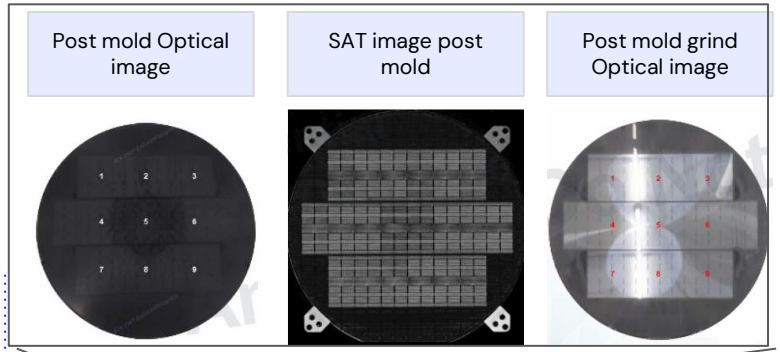
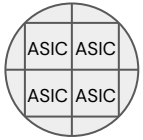
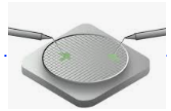
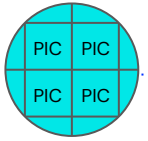
M1000 How it's built.







ASIC



Wafer Test

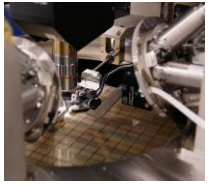
TSV Reveal

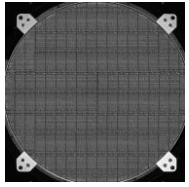
RDL and bumping

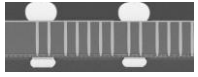
CoW reflow: PIC wafer (TSV) to ASIC attach

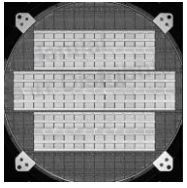
Wafer level underfill, mold and grind

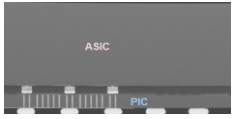
Wafer dicing

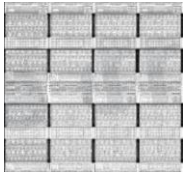


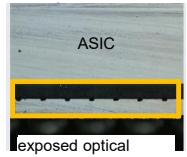












exposed optical waveguide in the PIC

System

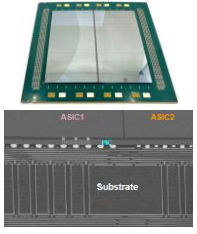
Final Electro-optical test

Fiber attach with real time optical test

Package e-test (Known good PKG)

Heat sink attach

Post substrate attach reflow



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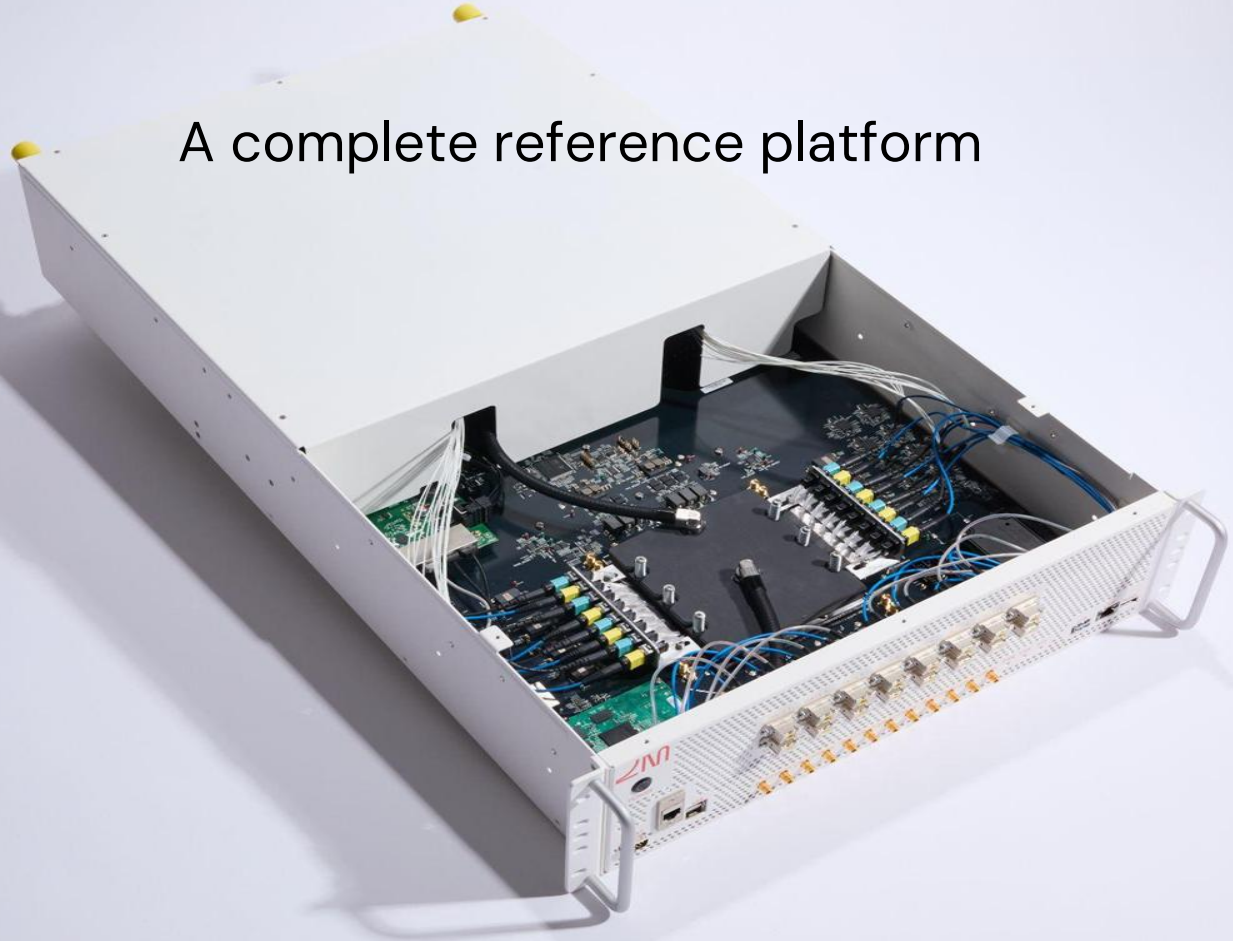
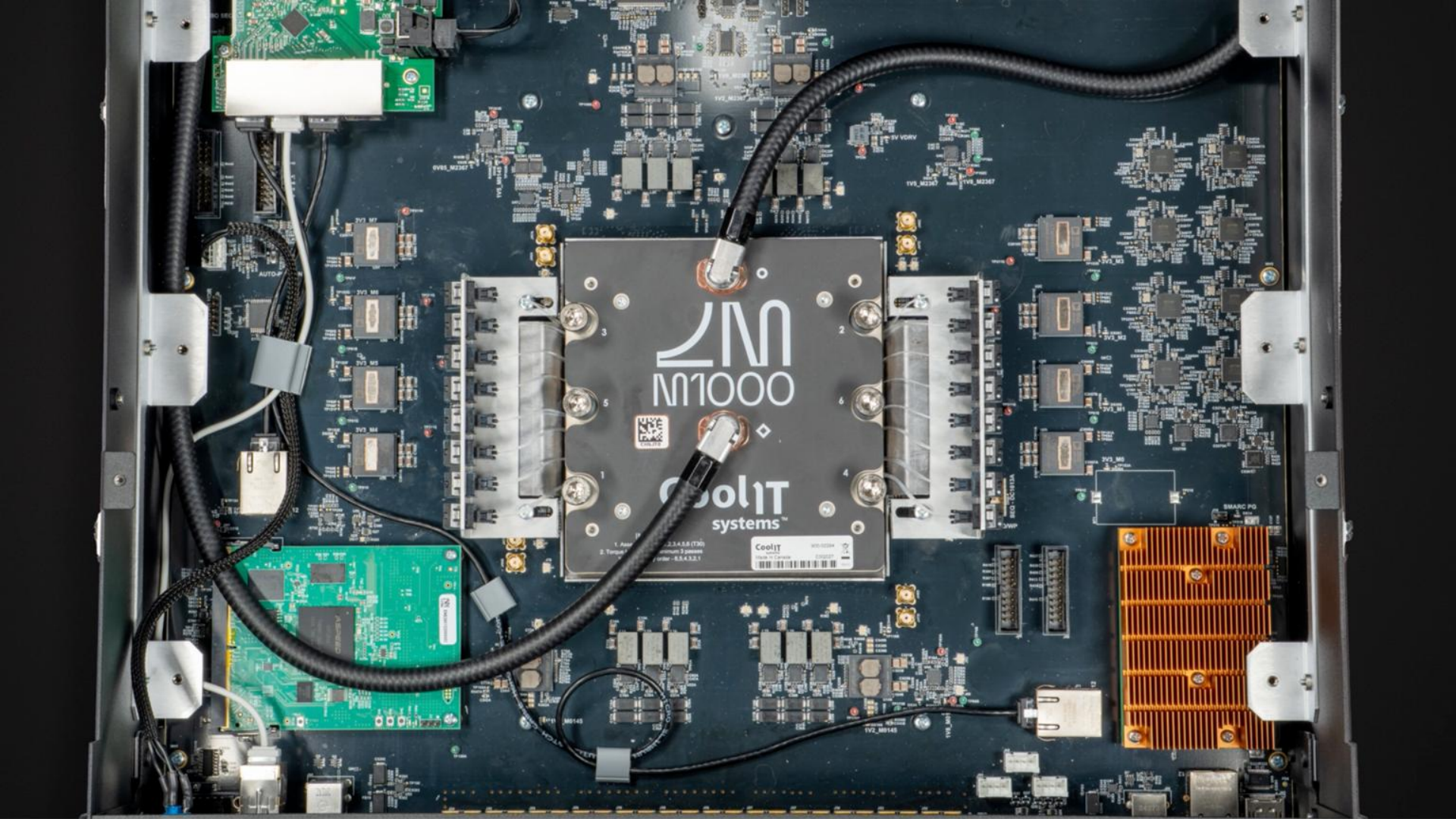
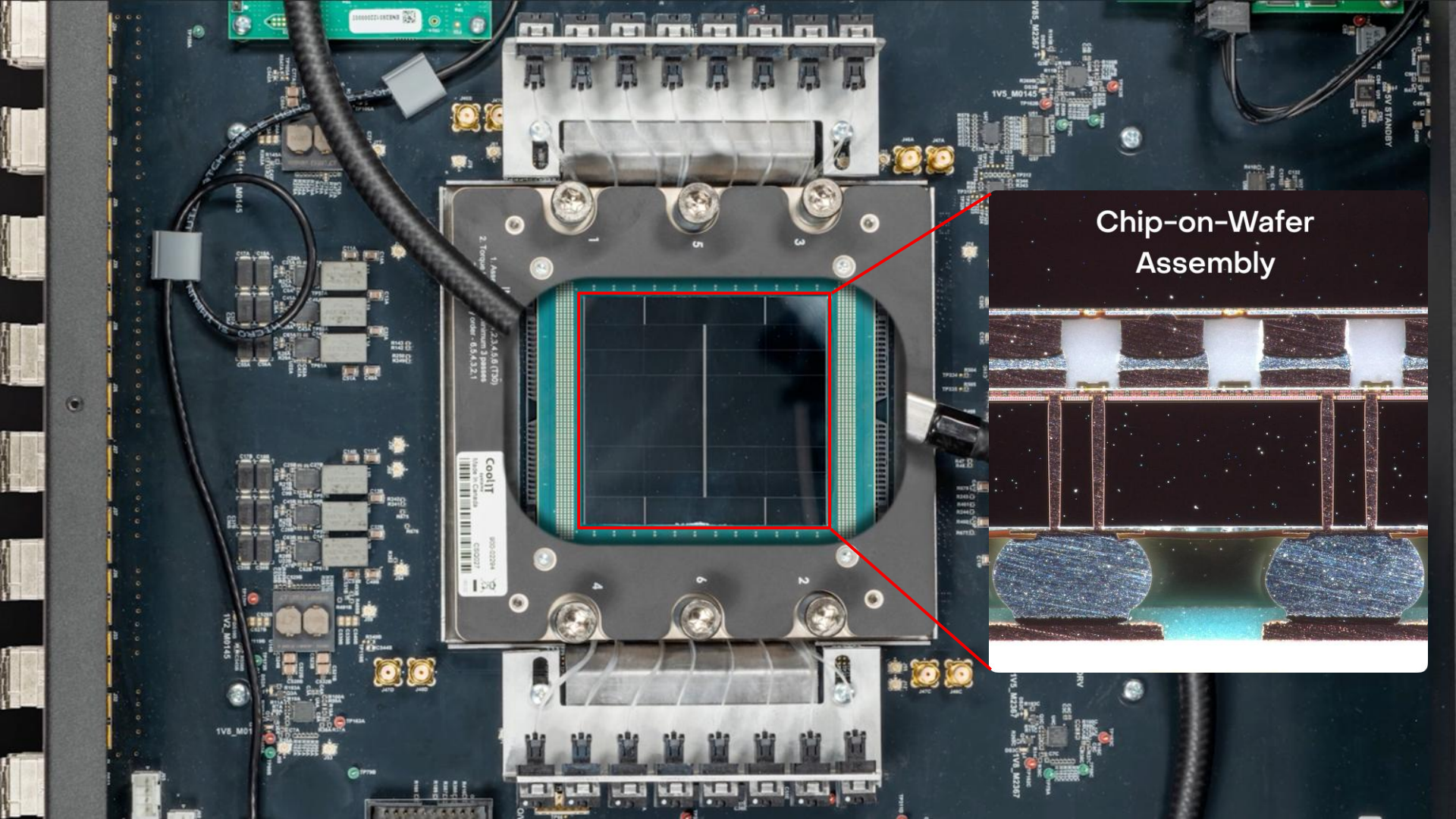
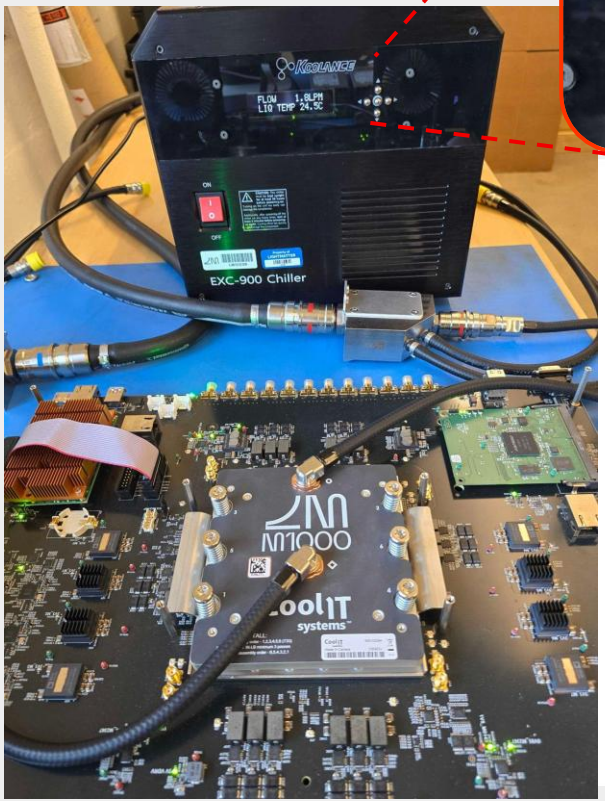
A complete reference platform

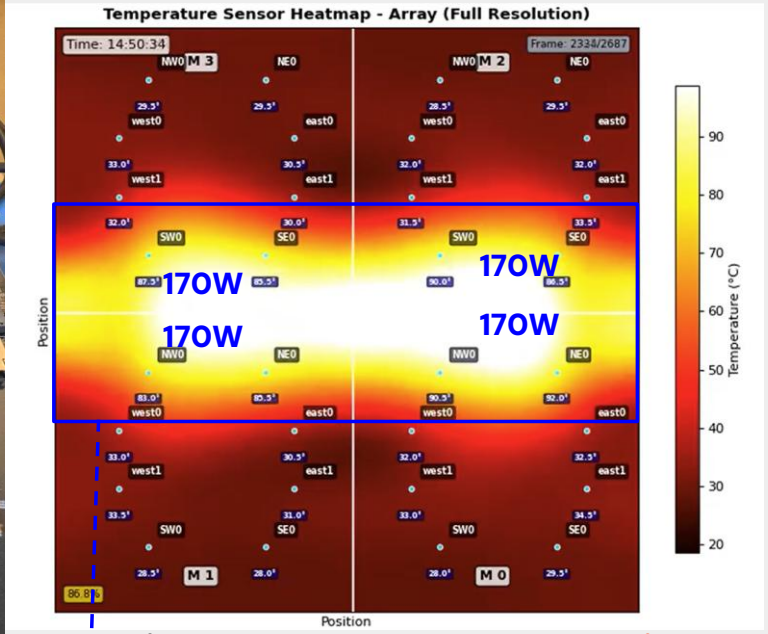



M1000
CoolIT
systems


Chip-on-Wafer
Assembly

Power delivery and thermal load

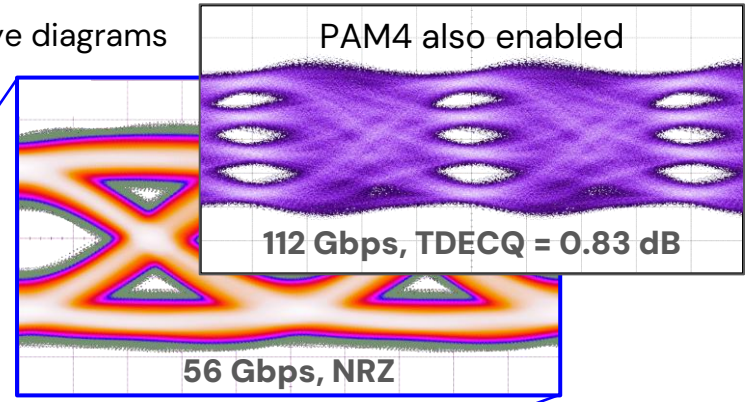




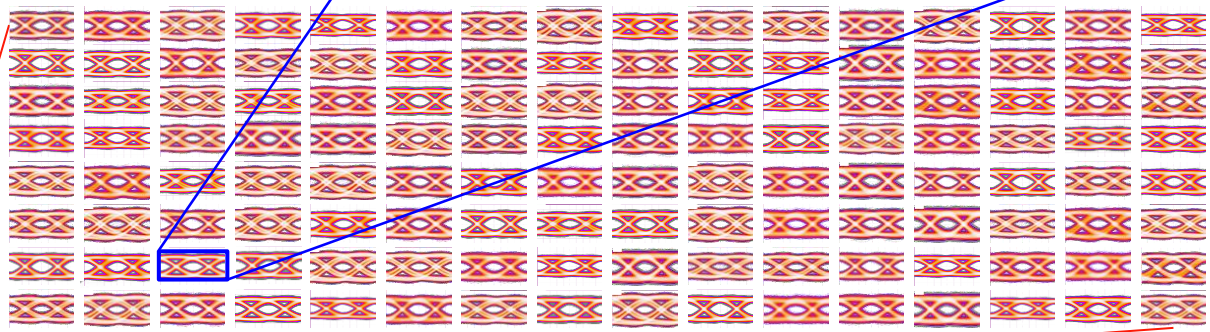
369mm² thermal test chip, power density 1.47W/mm².
Passage TSVs support >2.5A/mm².

Bandwidth density leadership

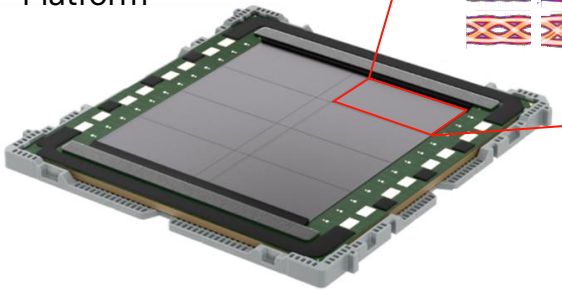
SerDes eye diagrams



128 SerDes per tile



Passage M1000 Platform



LM Packaging, Test, Quality and Reliability Methodology

Concept/Development

- SI/PI
- Substrate Design
- Design for manufacturing/Reliability
- Thermal analysis
- Mechanical Design/Analysis
- Optical Analysis

Assembly/Test

- 2D and 3D Heterogeneous Integration & process dev.
- Wafer Electrical Sort and Optical Characterization
- Wafer and component test points through the process flow

Reliability/Validation

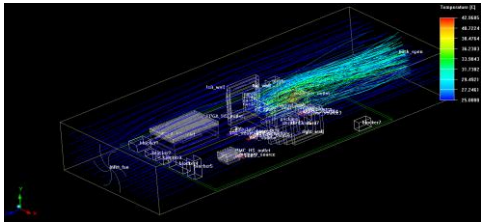
- Electrical and Compliance Tests – ESD, Latch Up, EMI/EMC
- Package/Environmental – TC, UHAST, HTS, S/V, Fiber Integrity
- Operational – HTOL
- Failure rate and Lifetime prediction

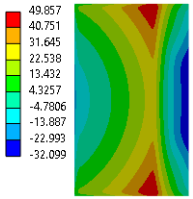
Analysis and Lab Validations

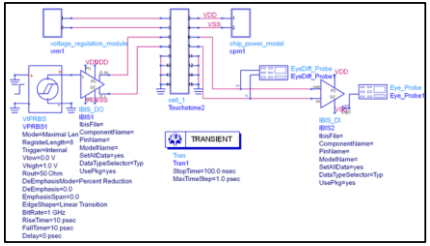
Deliver an **error free** and **high quality design**
Model **validation** with lab experiments
Scale **reliable** solutions to High Volume Manufacturing

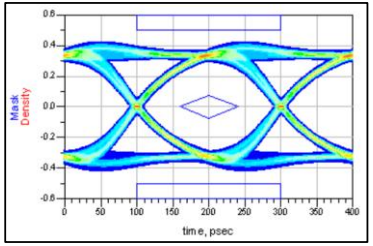
Capture Multi-Physics Interactions

Optical Design	• Waveguide mode analysis • Coupling efficiency • Link budget analysis.
Signal Integrity	• Insertion loss • Return loss • Crosstalk analysis
Mechanical Design	• Stress and strain analysis • Warpage and shock/vibration analysis.
Thermal Design	• Airflow simulation • Thermal analysis from silicon to rack level
VR / Power Integrity	• IR drop analysis • AC/Impedance analysis • Transient analysis





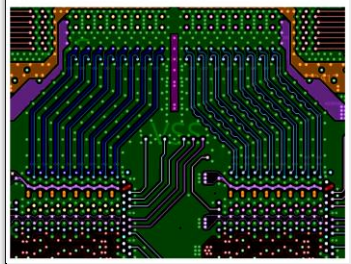


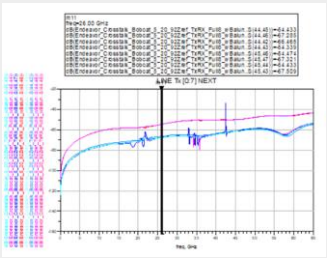


SI, PI + Packaging Design

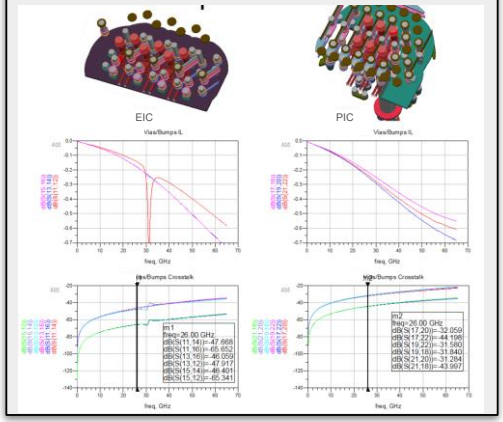
Line Side Routing

D2D TX (9F)



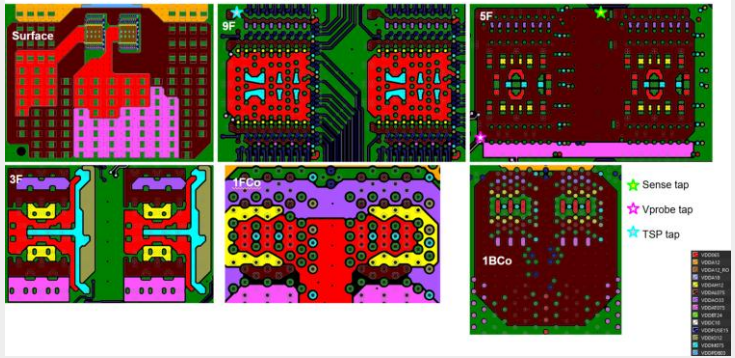


Bump & uVia XTALK optimization

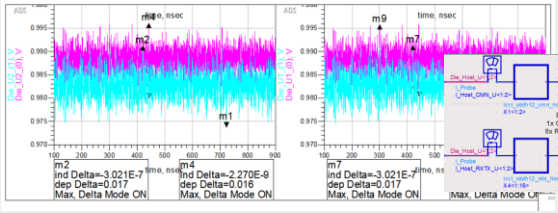


Power Integrity

VDDAL075 (H/L AVDDL) - Layout



H/L AVDDL - Mission Mode Results

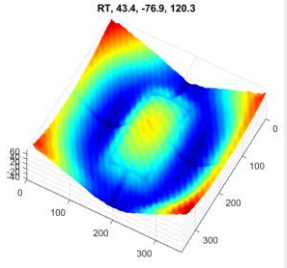


Thermal, Mechanical, and Optical Analysis

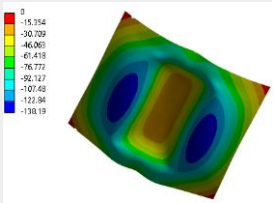
Mechanical Analysis

Warpage analysis for to optimize fiber attach manufacturing

Model

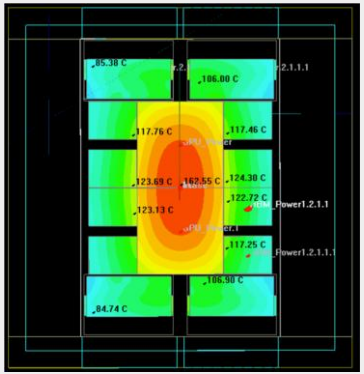


Measurement



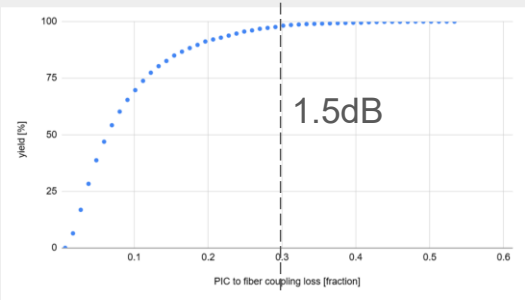
Thermal Analysis

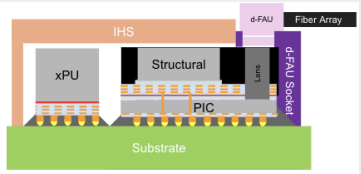
Heat transfer based design rule definition for 3D Heterogeneous Integration



Optical Analysis

Zemax + Lumerical analysis to define manufacturing tolerance to meet yield

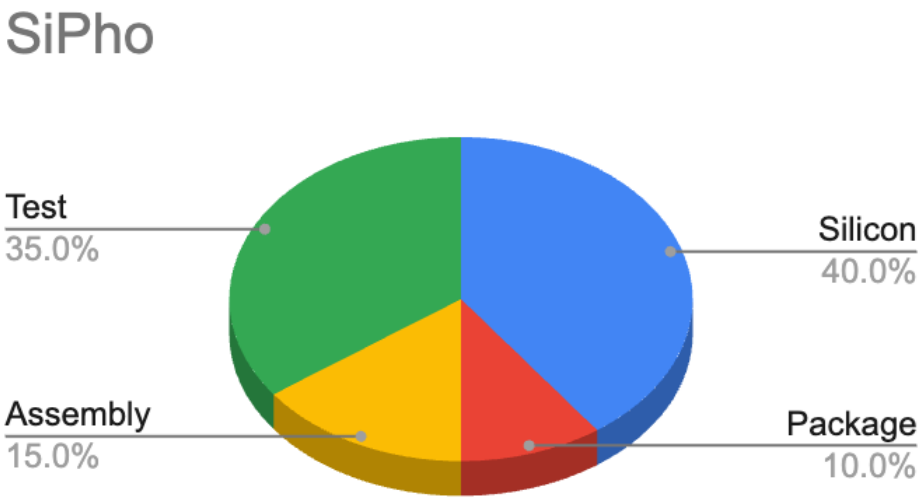




LIGHTMATTER

SPAT Costs and the Need for continued Innovation

Silicon, Package, Assembly, Test



Note: Graph shown for demonstration purposes only

For SiPho Relative Packaging, Assembly and Test (PAT) cost % is increasing

PAT cost challenges in SiPho:

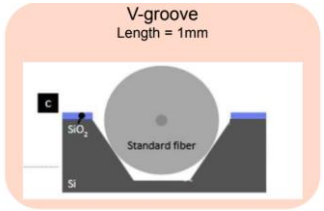
1. In assembly: fiber attach yields

1. In test: test times are much higher

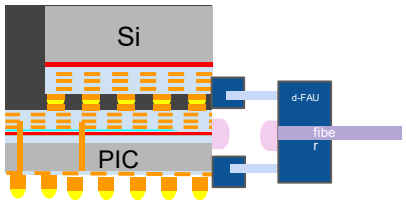
DFM/DFT-driven product architecture is must for high volume SiPho manufacturing and cost reduction

Fiber Attach Methods

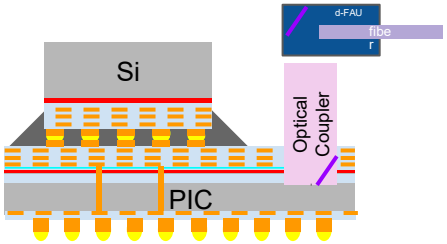
Traditional FAU



Lens based edge attach



Wafer Level Optical coupler

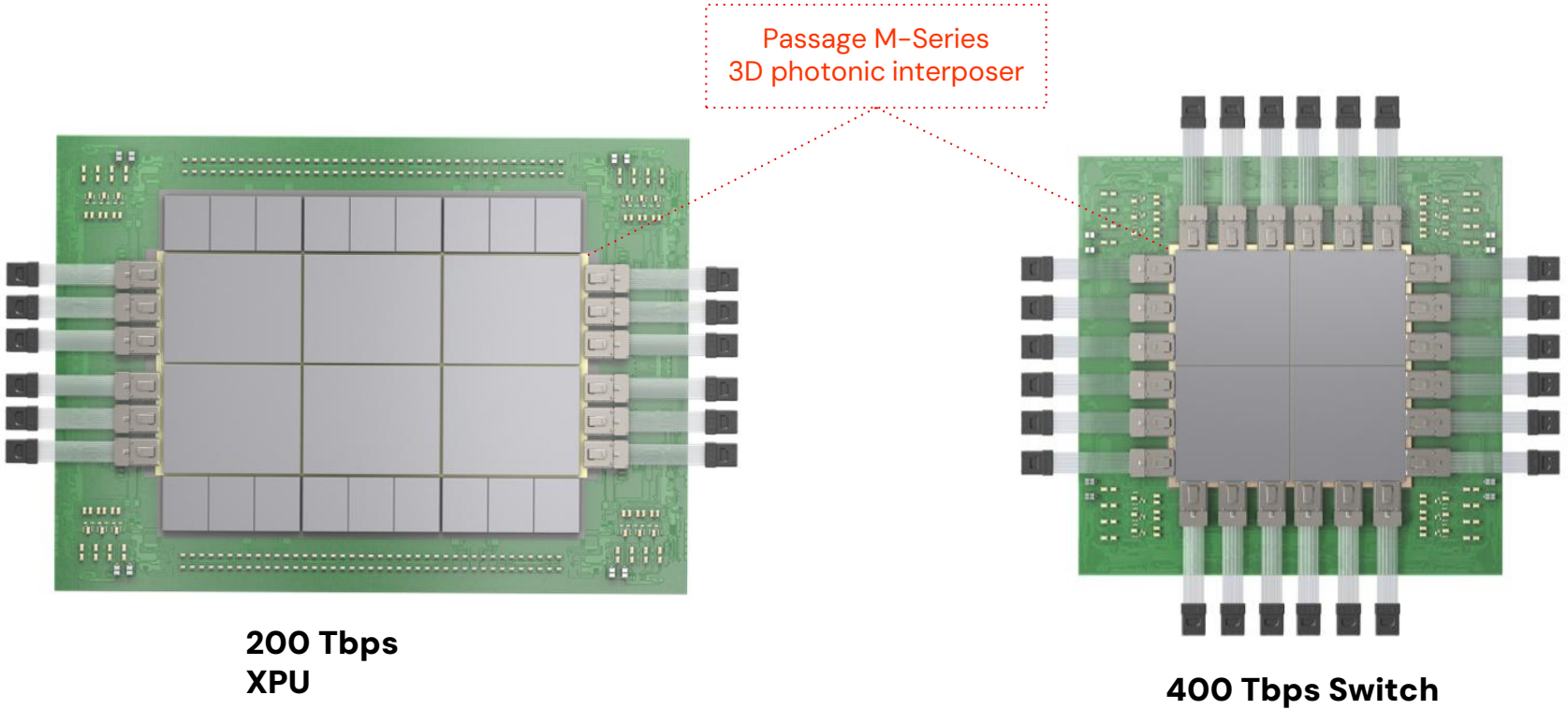


V-Groove based Fiber Attach Methods	**Lens based: Detachable fiber attach**	**LM Focus: Detachable fiber attach**
Package level assembly (interface on die edge)	Package level assembly (interface on die edge)	Wafer level assembly and test compatible
Not compatible with 3D Arch	**Compatible with 3D Package Arch**	**Compatible with 3D Package Arch**
XPU to OE D2D: Standard Package	**XPU to OE D2D: Standard & Adv. Package**	**XPU to OE D2D: Standard & Adv. Package**
Passive or Active alignment	Active alignment	Passive or Active alignment
Test with FAU after package assembly	Test with FAU after package assembly	Test with FAU at wafer level
FAB: GF only	FAB: GF & TSMC	FAB: GF & TSMC
Serviceability: No	**Serviceability: Yes**	**Serviceability: Yes**
Limited scalability to HVM ($$$)	Scalability to HVM ($$)	HVM scalable solution ($)

LM driving strong ecosystem partnership to bring detachable FAUs to HVM scale

3D Interposer scale-up and out to 1M nodes

The M1000 revolution



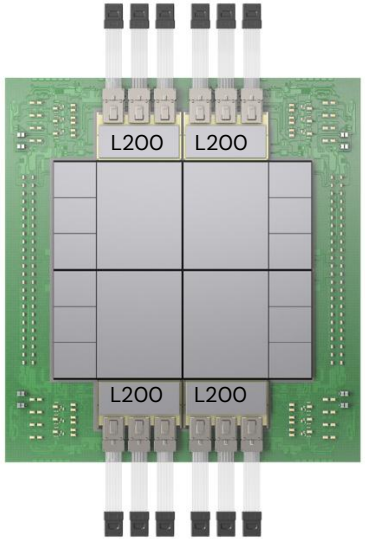
Lightmatter 3D CPO Product and Ecosystem

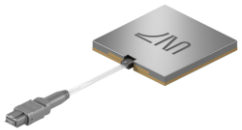
Customer ASIC with UCIe IP	**Multiple fabs**
Passage™ EIC (partners)	tsmc
LIGHTMATTER Passage™ PIC	tsmc, Tower Semiconductor
Detachable Fiber Coupler	**Multiple Suppliers**

Guide™ Light Engine (16λ, 100 mW/fiber)

ASE

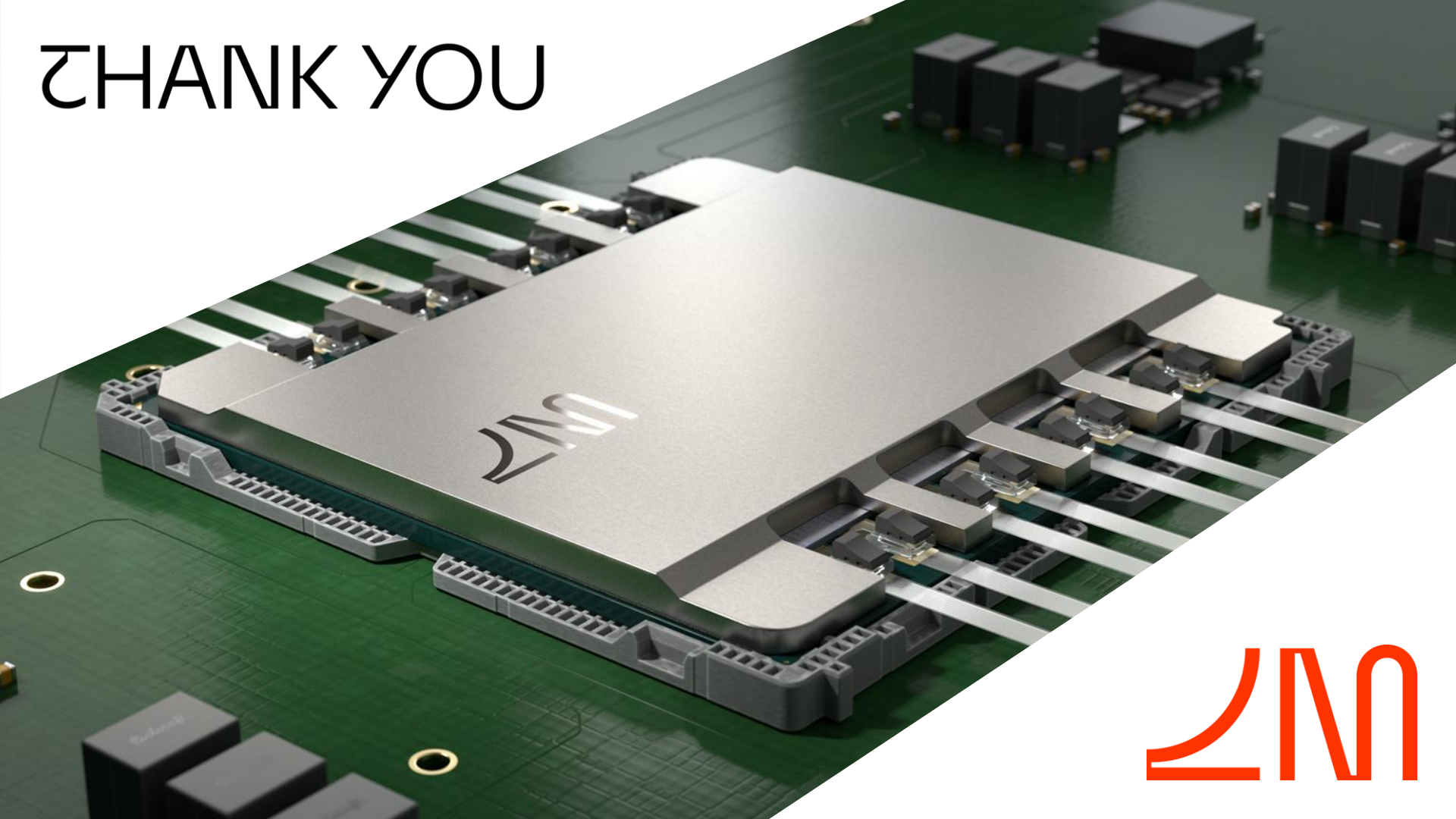
Amkor Technology

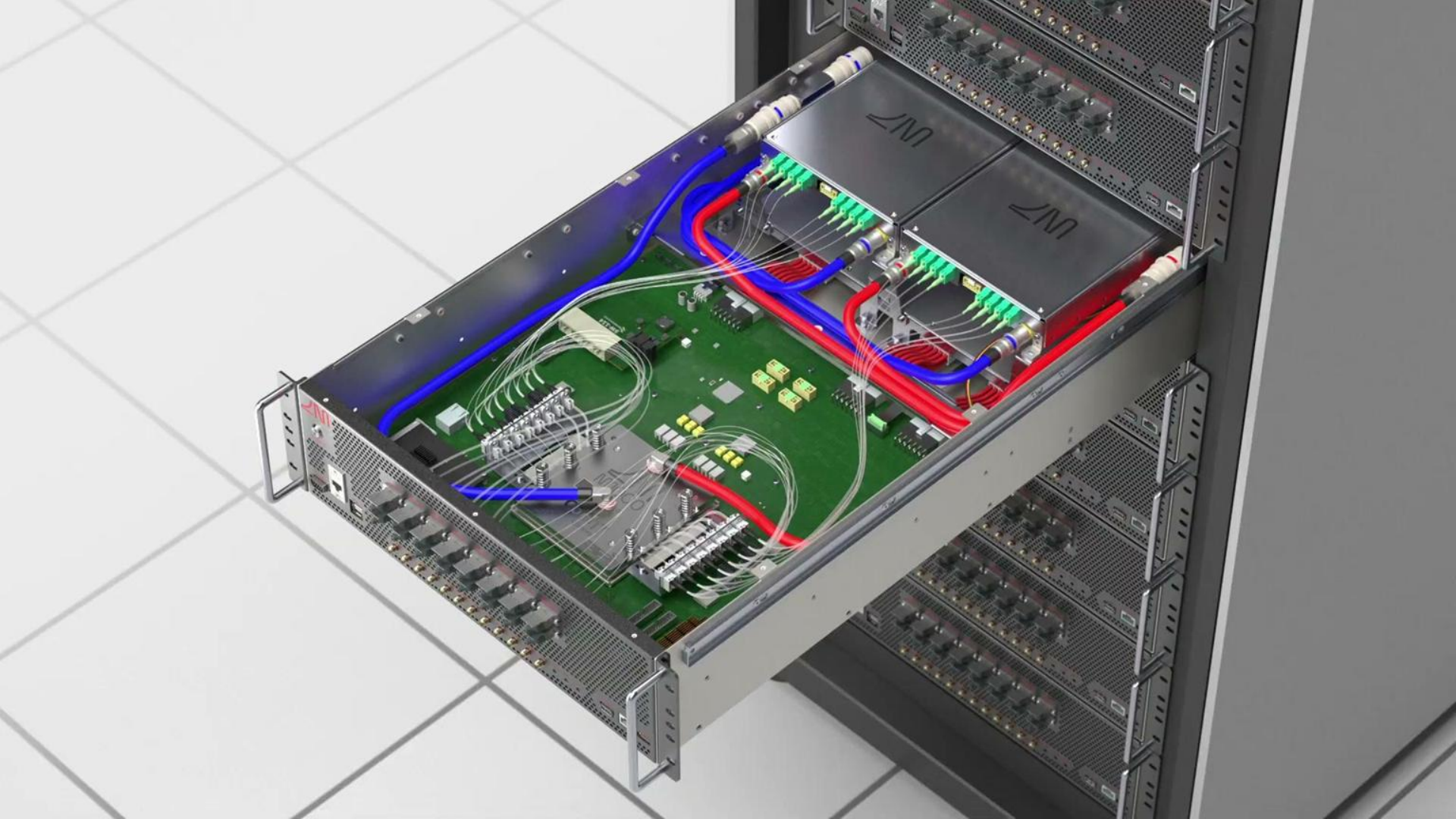




- Global ecosystem
- High-volume readiness
- Quality and reliability

THANK YOU





backup