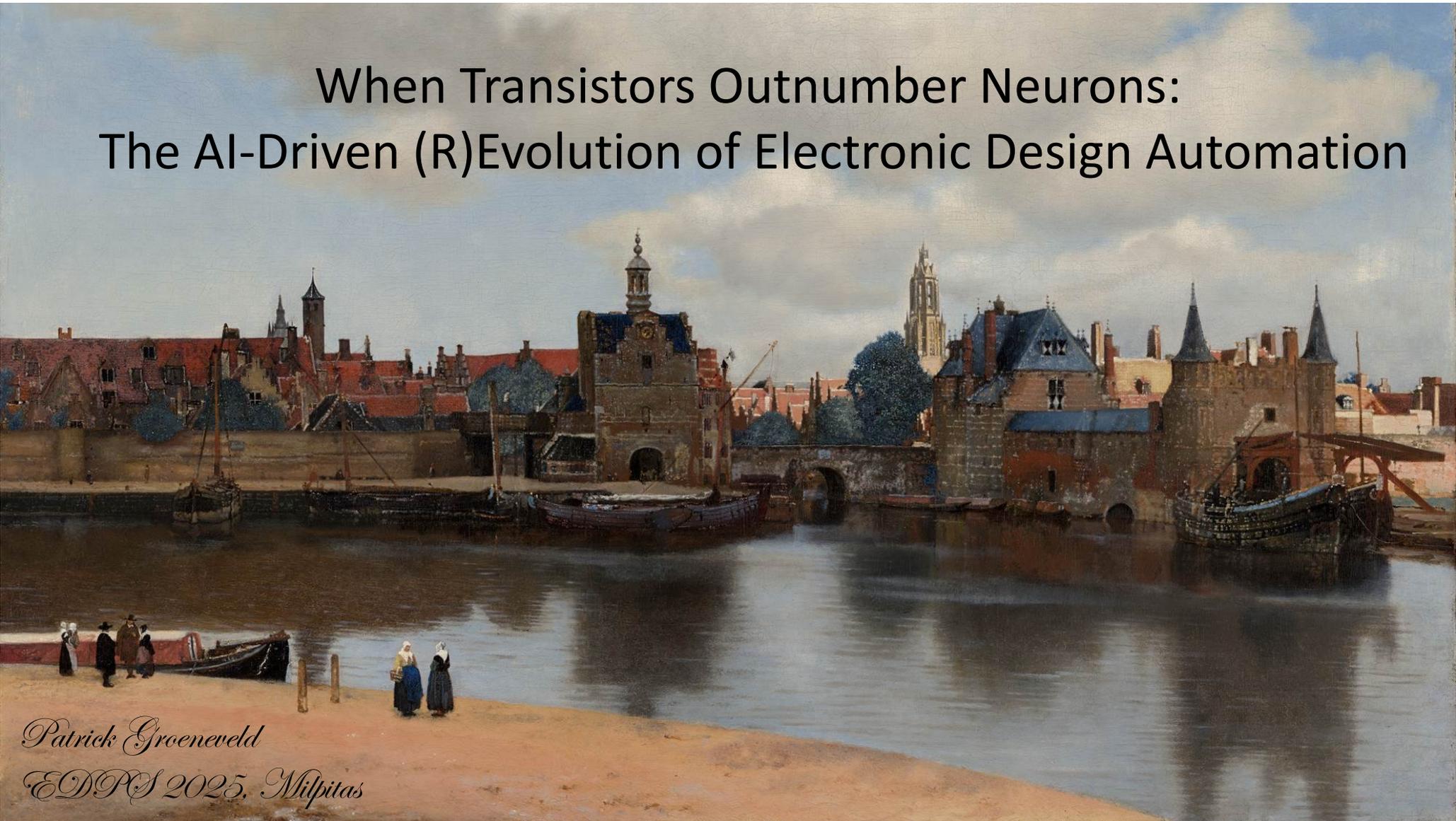


When Transistors Outnumber Neurons: The AI-Driven (R)Evolution of Electronic Design Automation



Patrick Groeneveld

EDPS 2025, Milpitas



Johannes Vermeer. View of Delft 1660



Imagine:
If the Wires on a 3nm Mobile SoC
were as wide as 2-lane Roads...

IC Wire pitch at 3nm: 24nm
2-lane Road width: 10m (30feet)
Scaling factor = 435Million

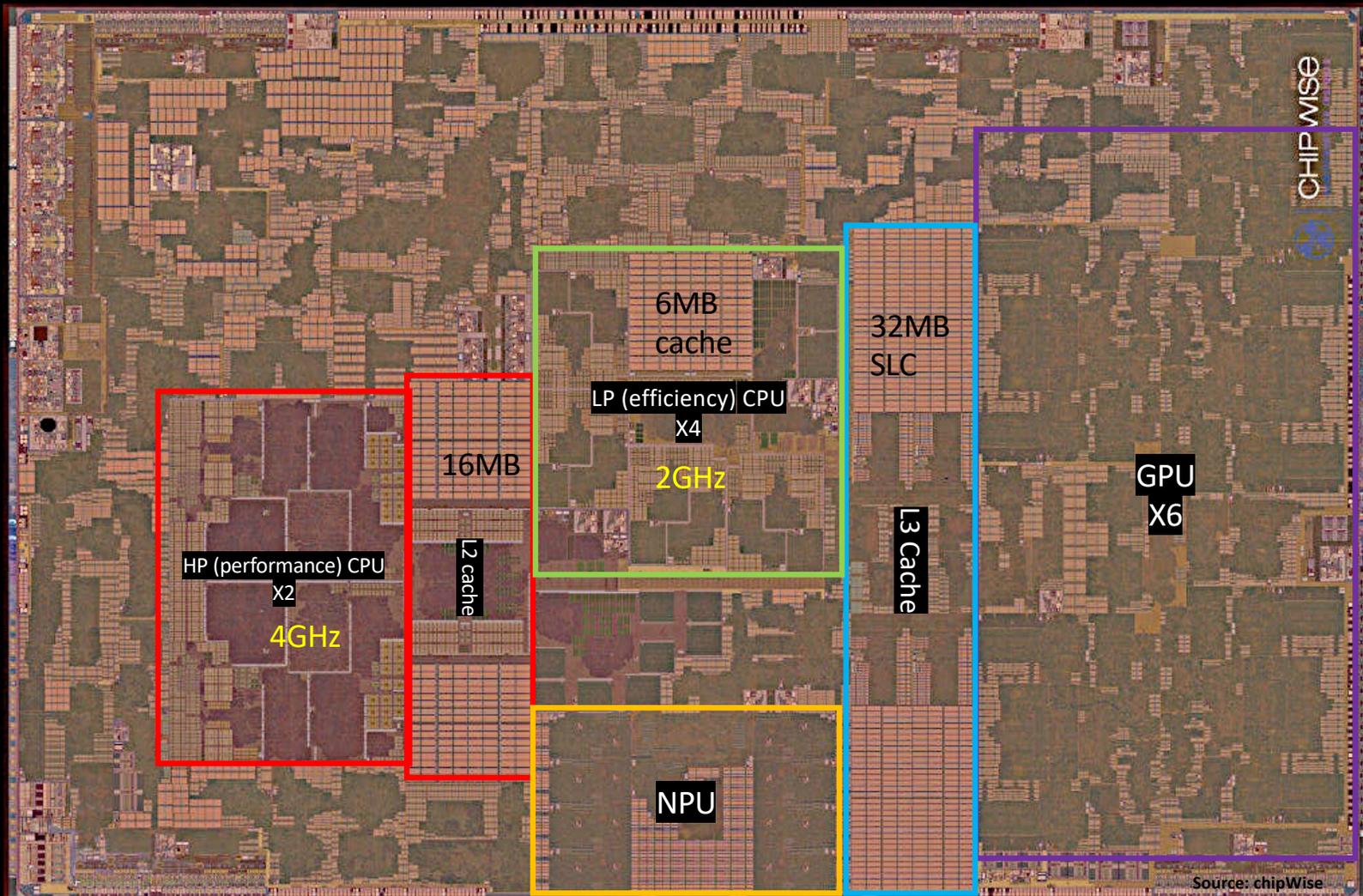
Scaled up, the wire is a road.
The **A19 Pro Chip (iPhone 17)** contains:
~18 million miles wires in 12 layers.
Connecting
~20 Billion transistors
~1.2 Billion standard cells
Consumes ~2 GigaWatt

The **USA** contains
2.7 million miles of
paved roads in 1 layer.
Connecting
0.31 Billion people
0.26 Billion cars
0.14 Billion homes
Consumes ~400 GigaWatt

2700miles/4350km

Apple A19 SoC in iPhone 17

September 2025



Moore's Law Ending?



MIT Technology Review

Intelligent Machines

The End of Moore's Law?

The current economic boom is likely due to increases in computing speed and decreases in price. Now there are some good reasons to think that the party may be ending.

by Charles C. Mann May 1, 2000

The New York Times

SCIENCE

Incredible Shrinking Transistor Nears Its Ultimate Limit: The Laws of Physics

By WILLIAM J. BROAD FEB. 4, 1997

nature news home news archive specials opinion features news blog

comments on this story

Published online 24 June 1999 | Nature | doi:10.1038/news990624-1

The end of the road for silicon?

Philip Ball

The writing is on the wall for silicon chips, according to research published in the [24 June issue of Nature](#). By the year 2012, miniaturization of microelectronics will have reached its limit, and computer power will be unable to increase any further without drastically rethinking the whole basis of silicon electronics.

- Stories by subject
- Technology
 - Chemistry

MIT Technology Review

Intelligent Machines

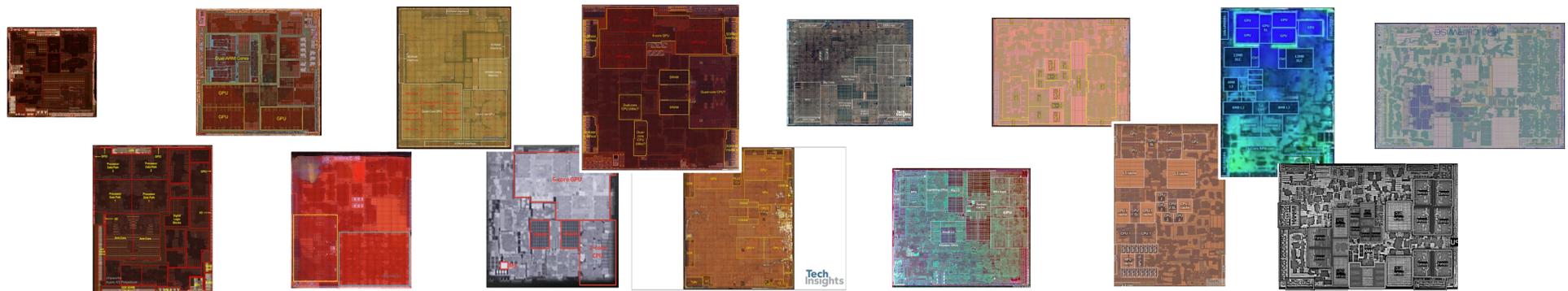
Moore's Law Is Dead. Now What?

Shrinking transistors have powered 50 years of advances in computing — but now other ways must be found to make computers more capable.

by Tom Simonite May 13, 2016

15 Generations of Apple Mobile System-on-Chips

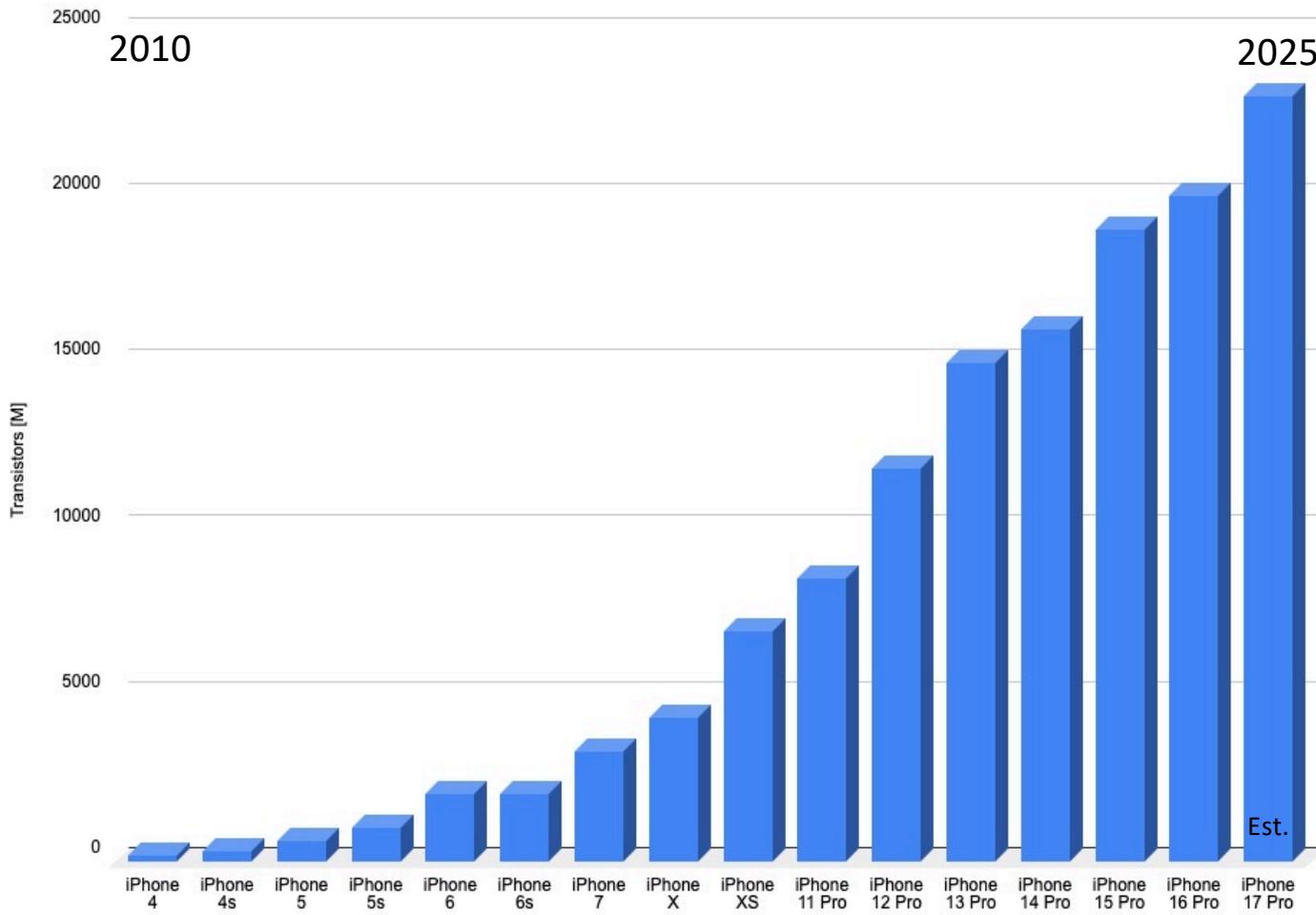
Chip	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18
Year	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Device	iPhone 4	iPhone 4s	iPhone 5	iPhone 5s	iPhone 6	iPhone 6s	iPhone 7	iPhone 8 & X	iPhone Xs	iPhone 11	iPhone 12	iPhone 13	iPhone 14	iPhone 15	iPhone 16
Node	45nm Samsung	45nm Samsung	32nm Samsung	28nm Samsung	20nm TSMC	16nm TSMC	16nm TSMC	10nm TSMC	7nm TSMC	7nm TSMC	5nm TSMC	5nm TSMC	4nm TSMC	3nm TSMC	3nm TSMC
Area [cm ²]	0.52	1.25	0.96	1.03	0.89	1.05	1.25	0.88	0.83	0.98	0.88	1.08	1.14	1.03	1.05



Die photos:
chipworks/TechInsights/Angstomiconics

7
Data source: wikipedia

16 years of iPhone SoC: Transistor count



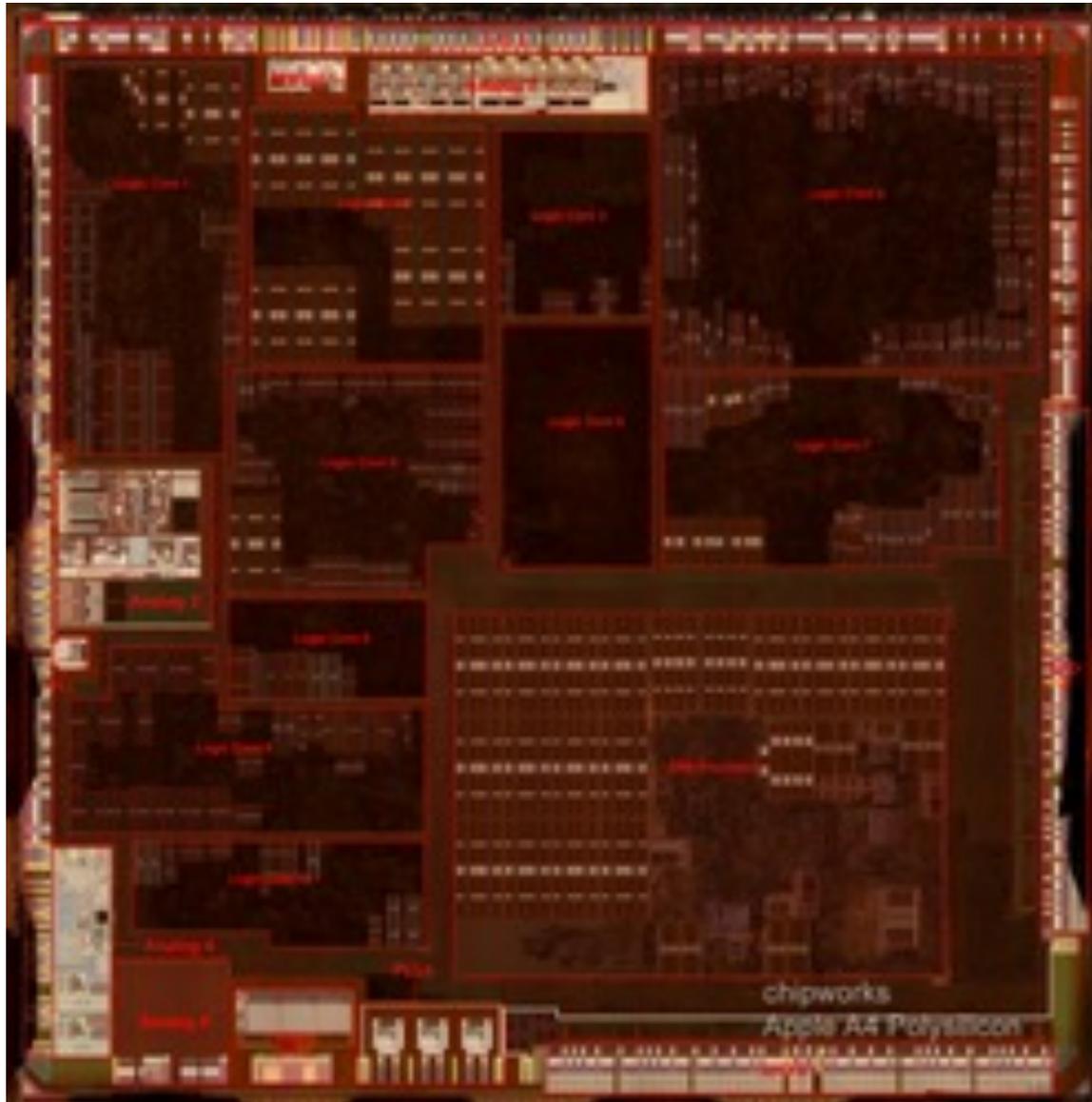
iPhone SoC
scale

2010

iPhone 4

45nm Samsung

A4 SoC



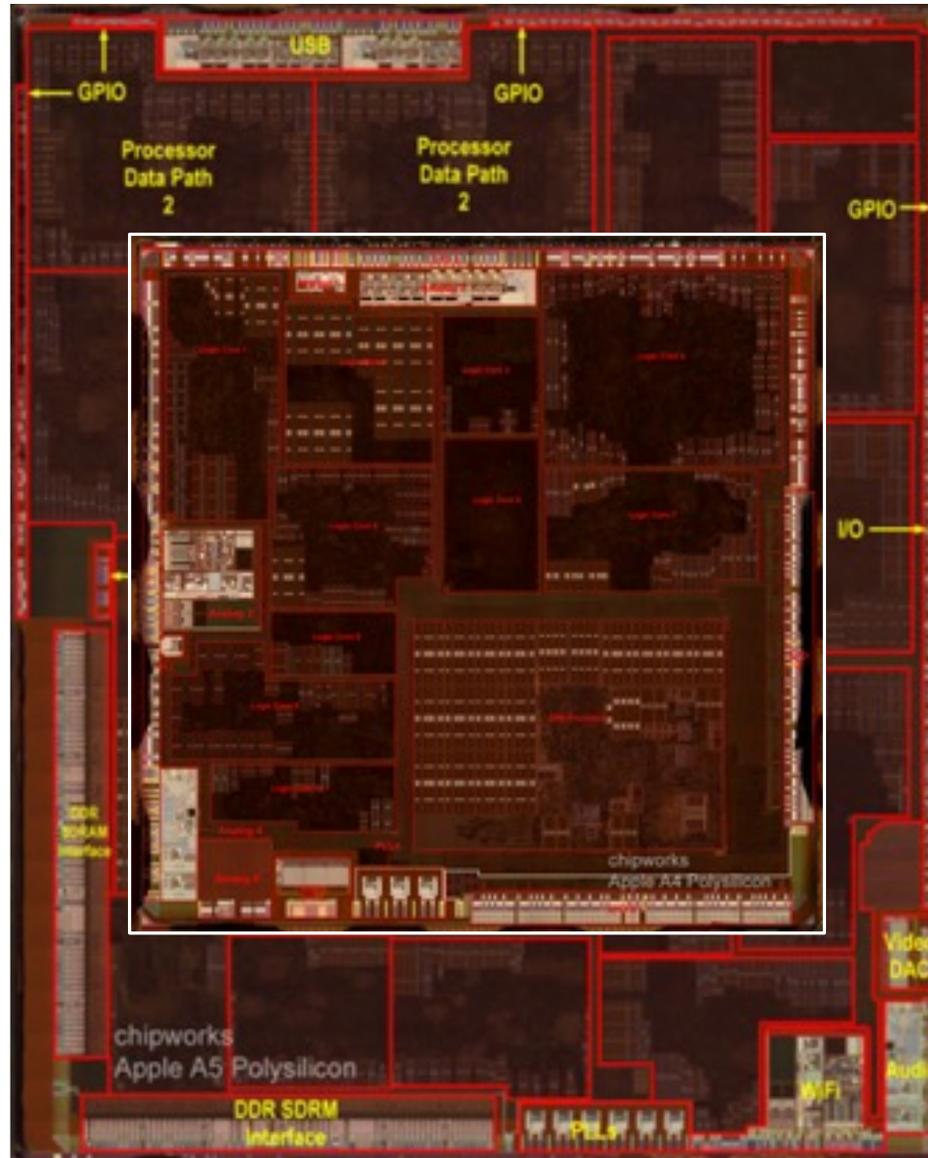
Die photos:
chipworks/TechInsights/Angstometrics
Data source: wikipedia

2011

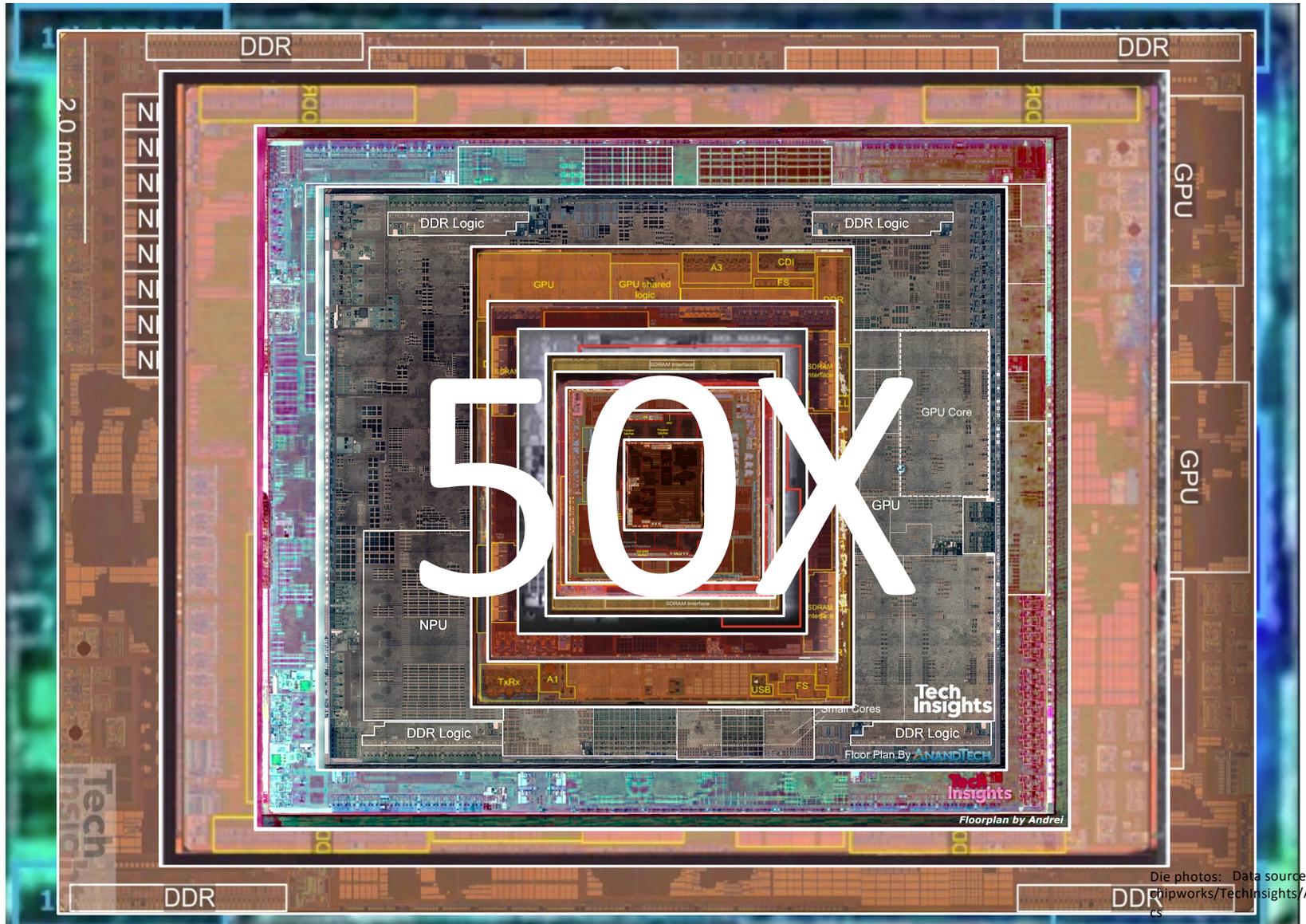
iPhone 4s

45nm Samsung

A5 SoC



Die photos:
chipworks/TechInsights/Angstometrics
Data source: wikipedia



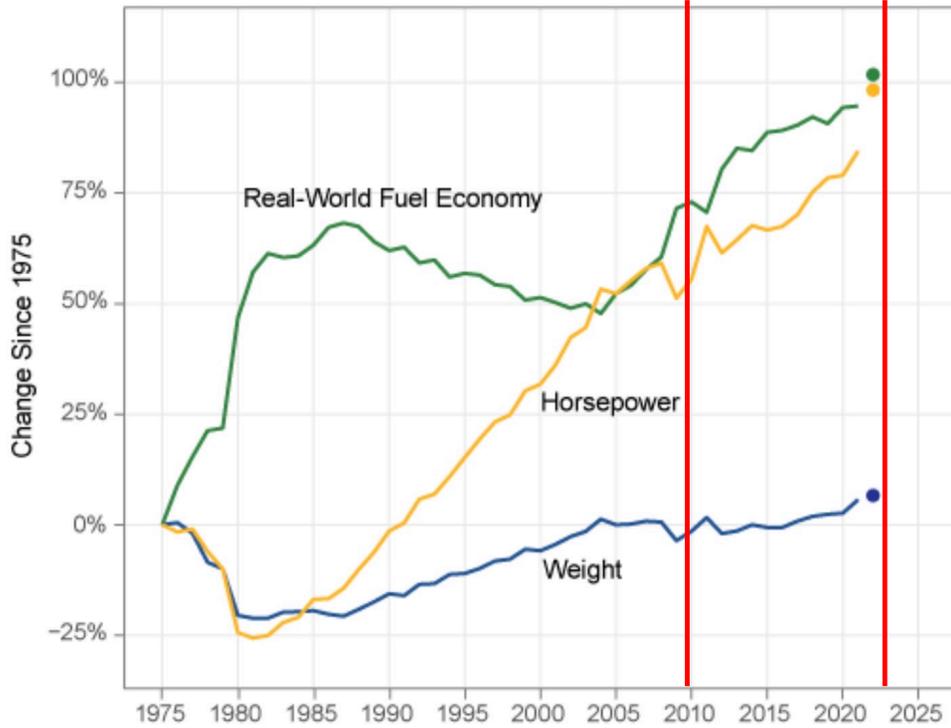
Die photos: Data source: wikipedia
chipworks/TechInsights/Angstromi
cs

Automotive Progress vs SoC Progress, Same Period



1.2X

2010 2023

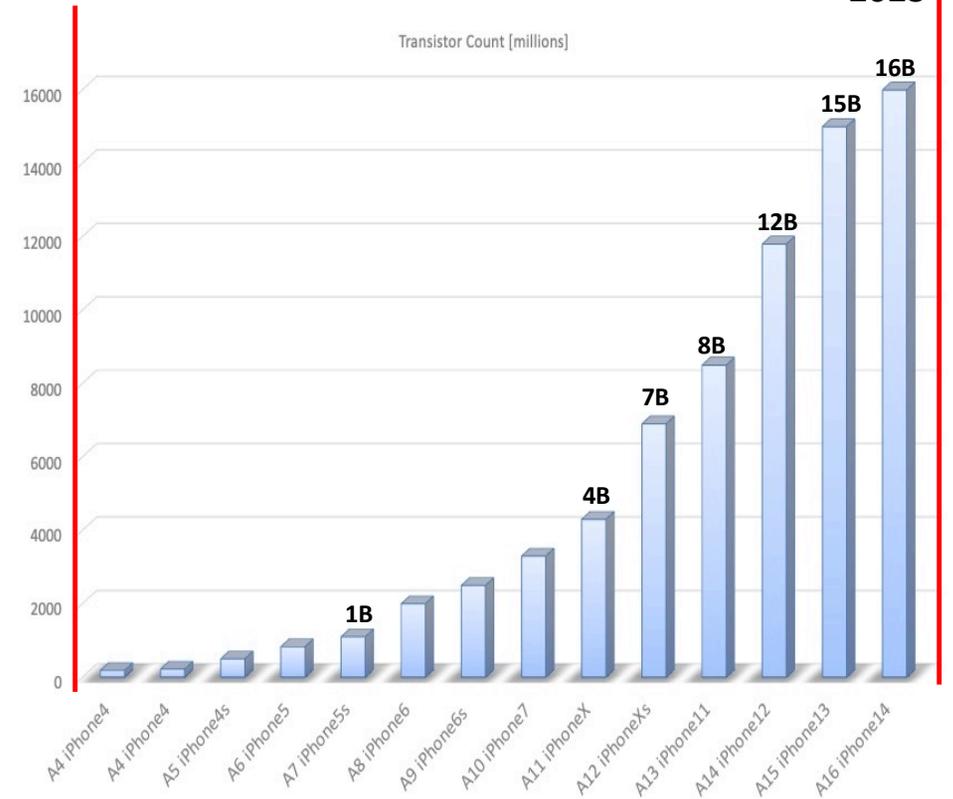


2010

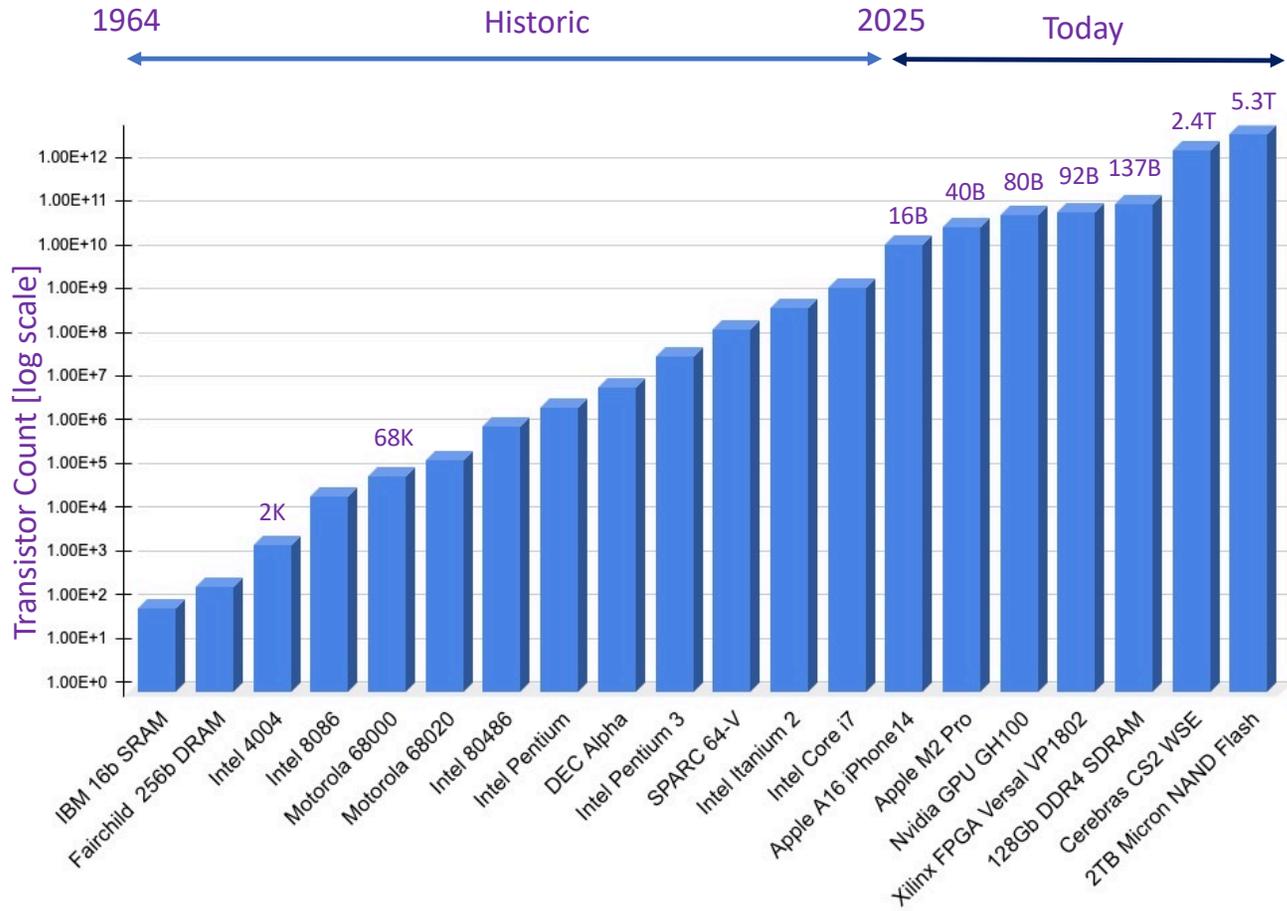
50X



2023



60 Years of Relentless Scaling



Cerebras CS-2: 2.4T



Largest Flash: 5.3T

Micron's 232-layer NAND

The foundation for a new wave of end-to-end technology innovation

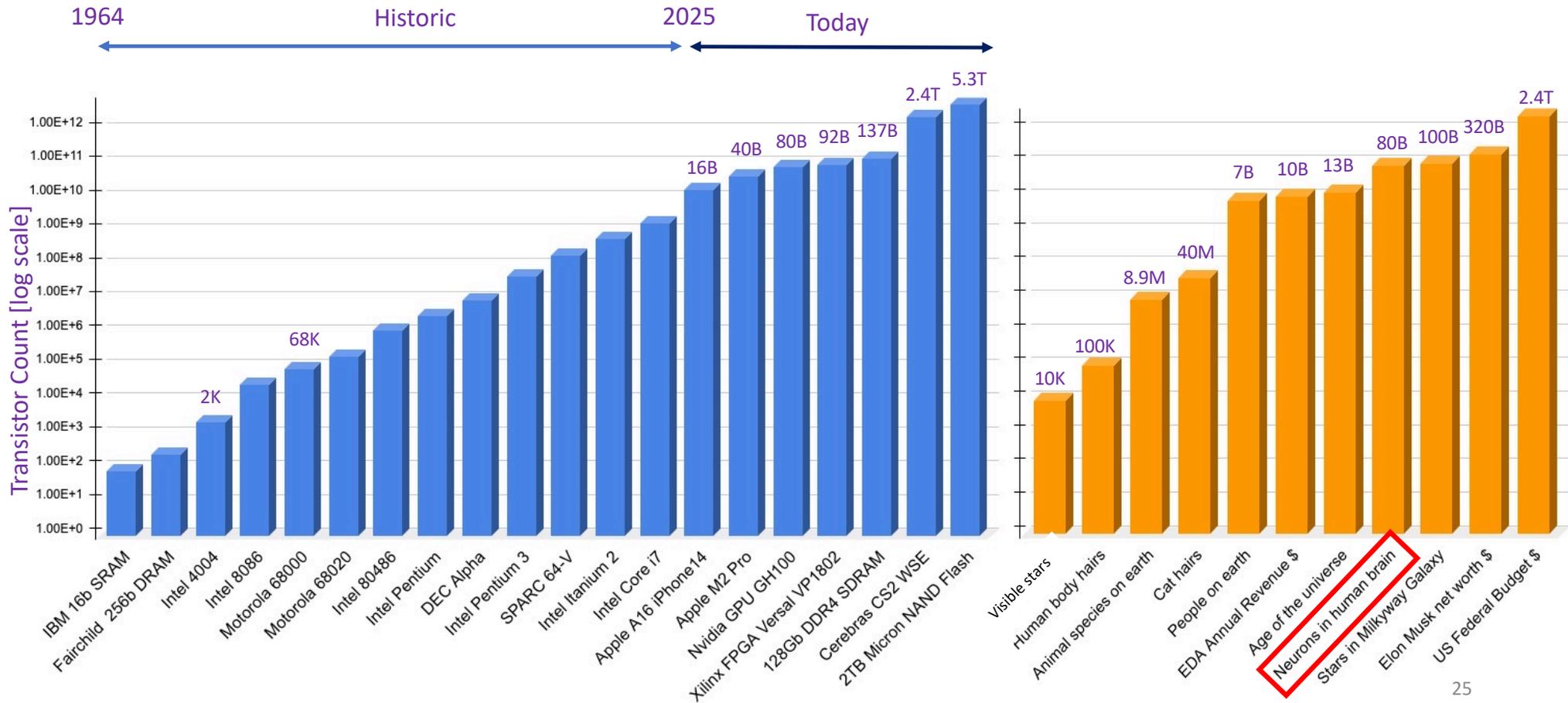
- Highest layer count
- Most bits/mm²
- Fastest I/O speed

Built on the proven technologies pioneered in Micron's industry-leading 176-layer NAND

Micron 3D NAND Evolution

Generation	Density (Gb/mm ²)	Layers
1	~1	~10
2	~2	~20
3	~4	~40
4	~8	~80
5	~16	~160
6	~32	~232

Microelectronics: Mindboggling Scale

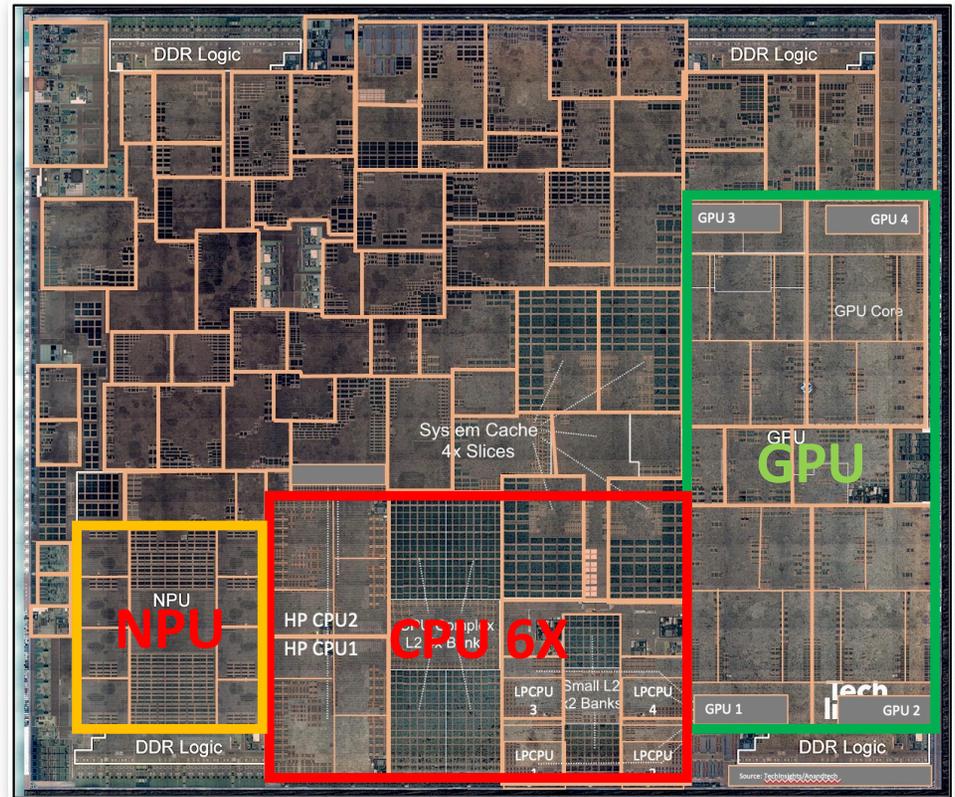
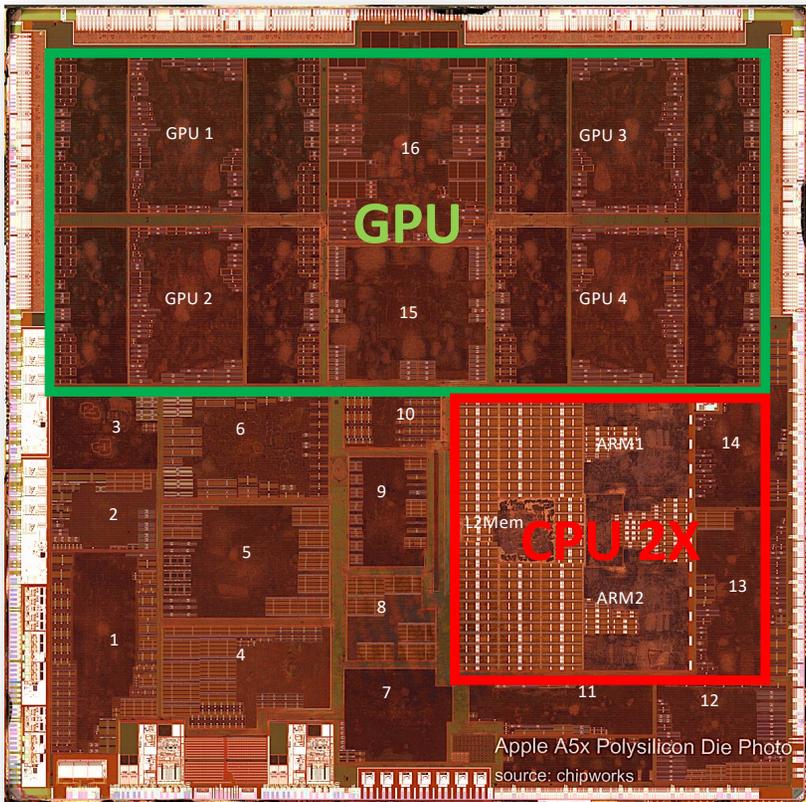


How was “Moore’s Dividend” Reinvested?

2012: A5 SoC (0.7B Transistors)



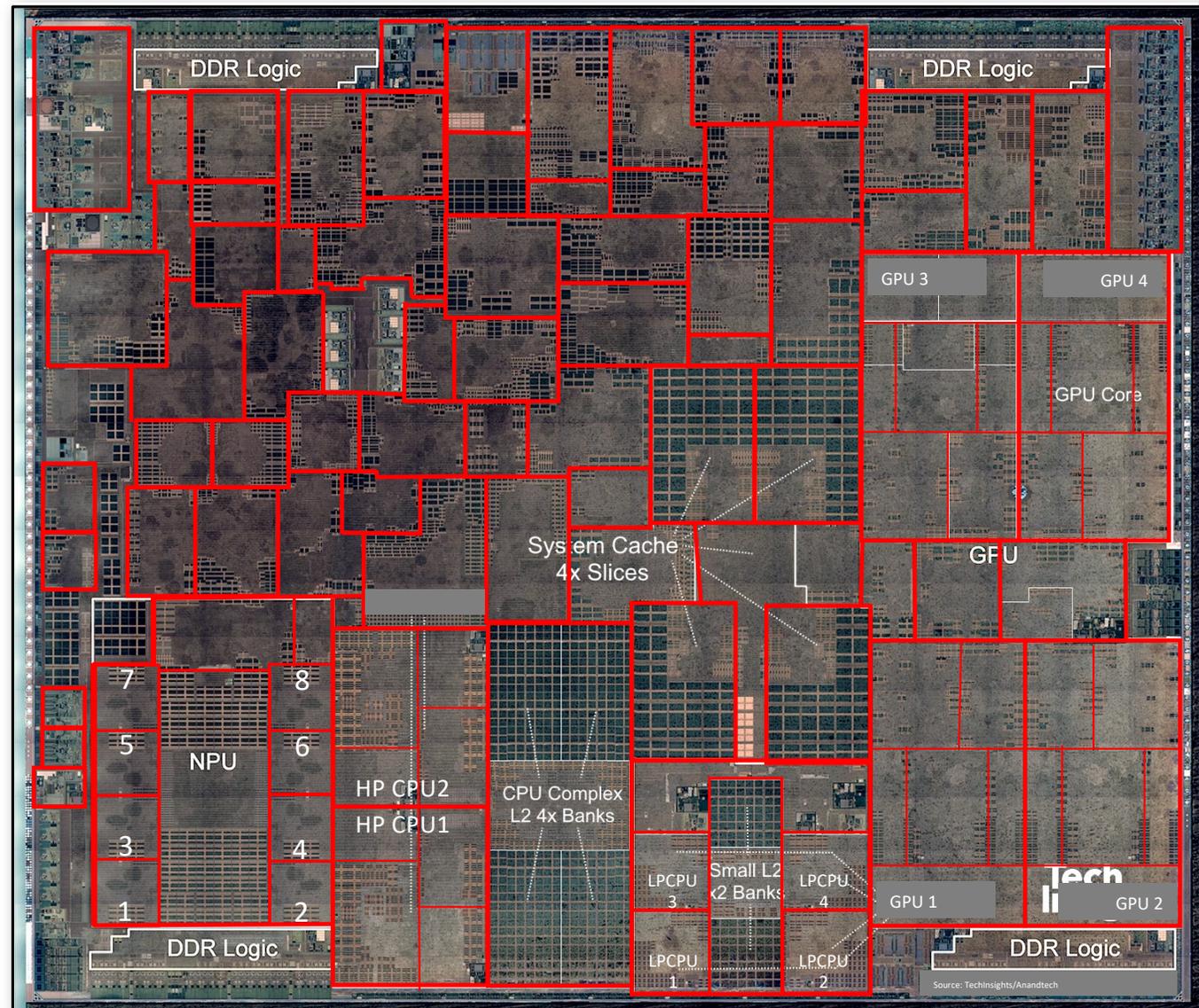
2018: A12 SoC (7B Transistors)



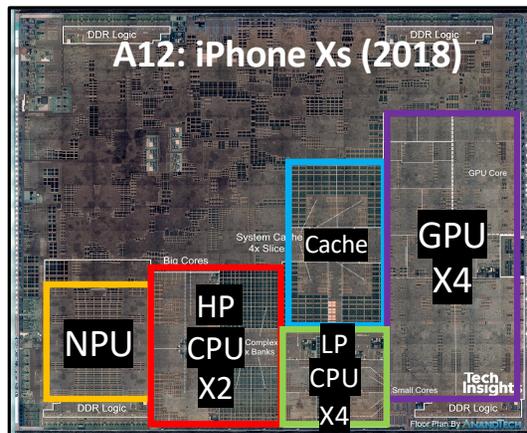
Apple A12

- 7nm TSMC FinFet
- $9.89 \times 8.42 = 83.27 \text{ mm}^2$
- 6.9 Billion transistors
- 4 **GPU** cores (~18%): 9 Blocks
- 6 **CPU** cores (~14%): 13 Blocks
 - 4 'Tempest' Low Power CPU cores
 - 2 'Vortex' High Performance CPU cores
 - L2 & L3 caches
- 8 **NPU/TPU** cores (~7%) 4 Blocks
- DDR (~3%) 1 block
- Misc (~57%): 50 Unique Blocks

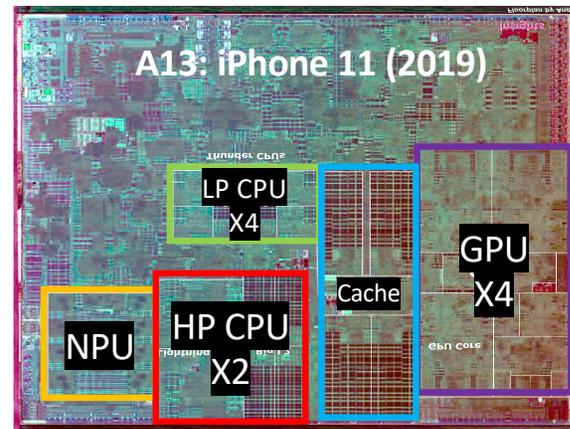
- Total: ~75 unique blocks
- ~5 Watt peak



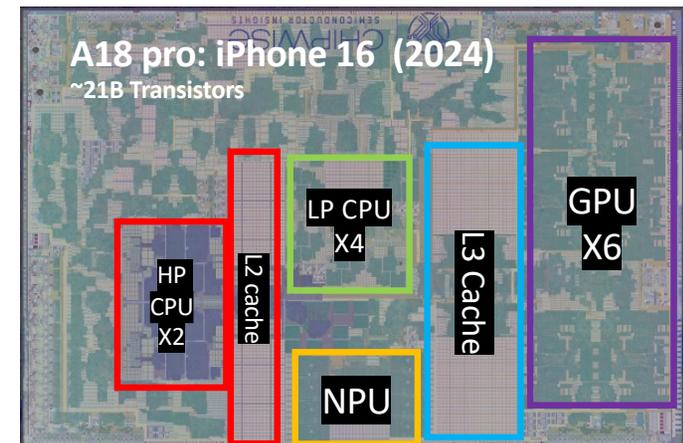
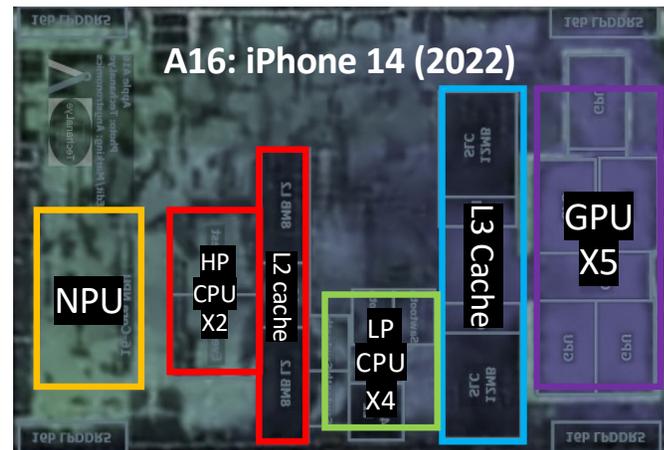
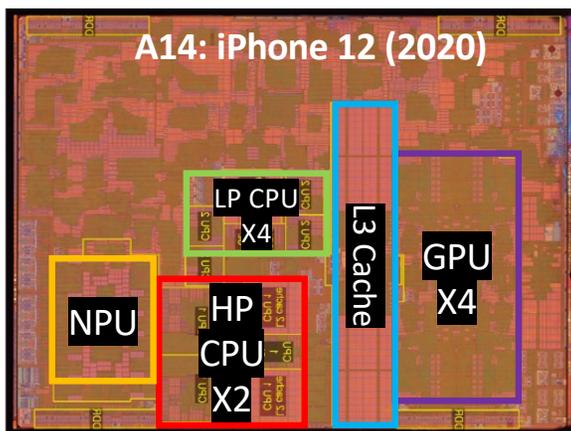
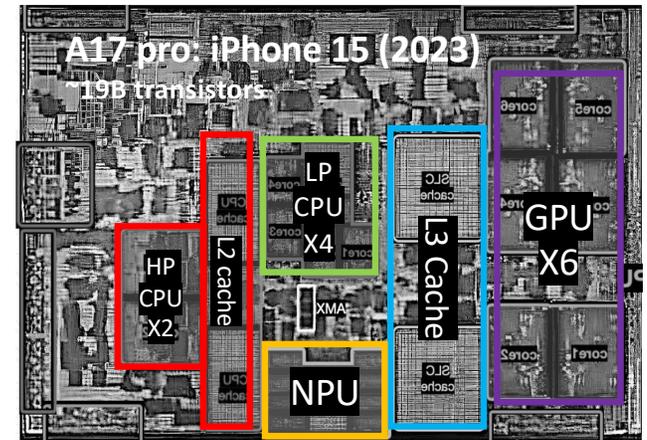
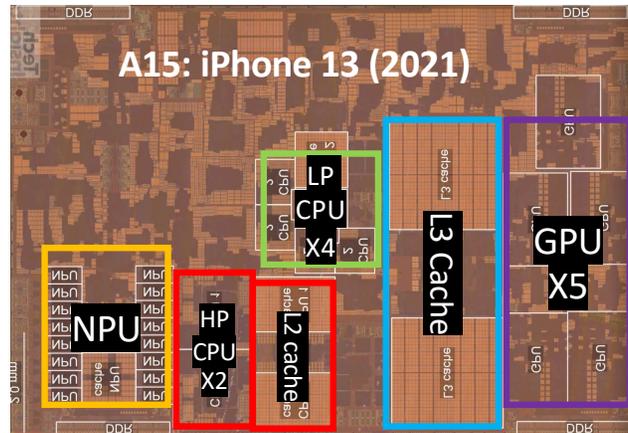
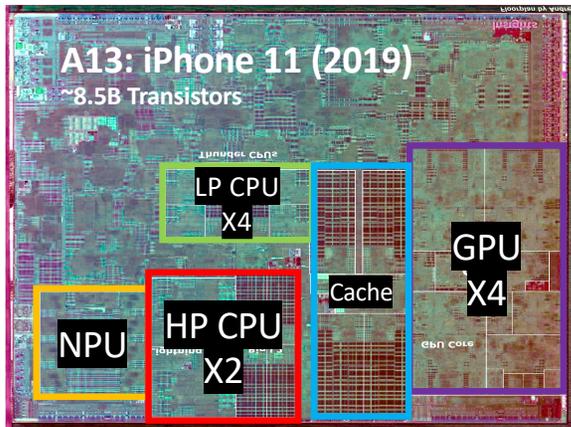
Tracking the changes 2018-2025



7B transistors

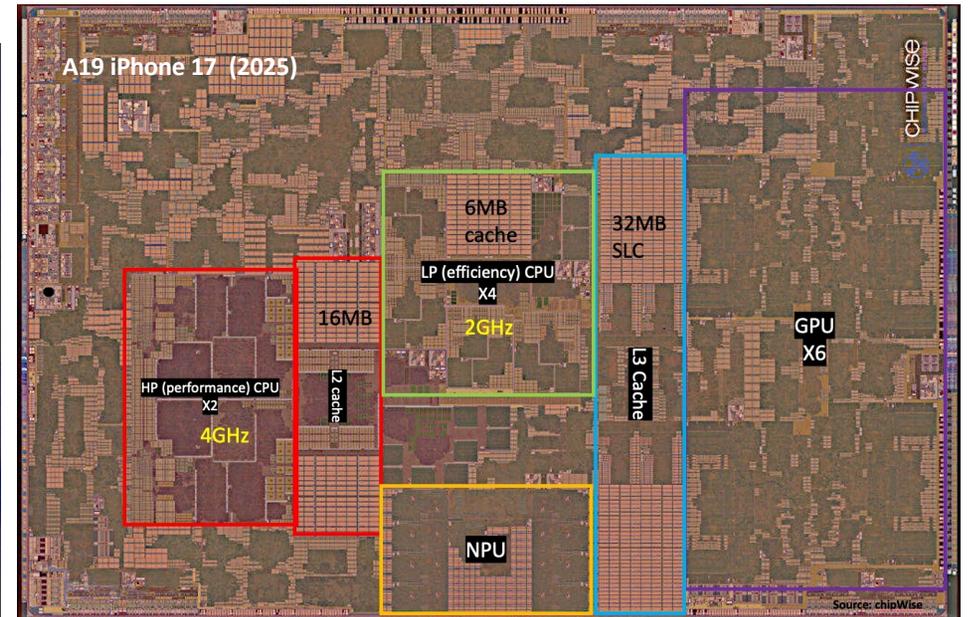
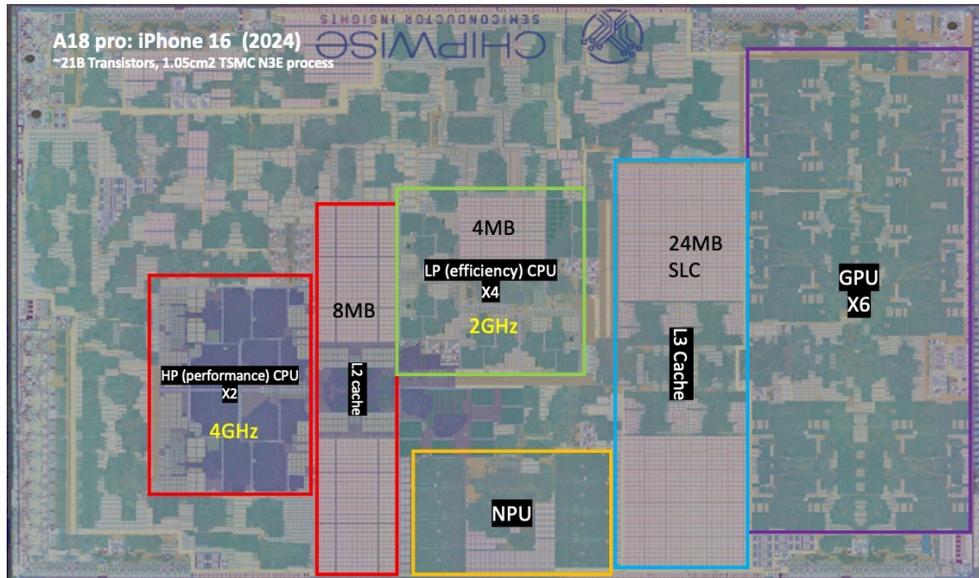


The Past 6 Years of Apple Mobile SoCs



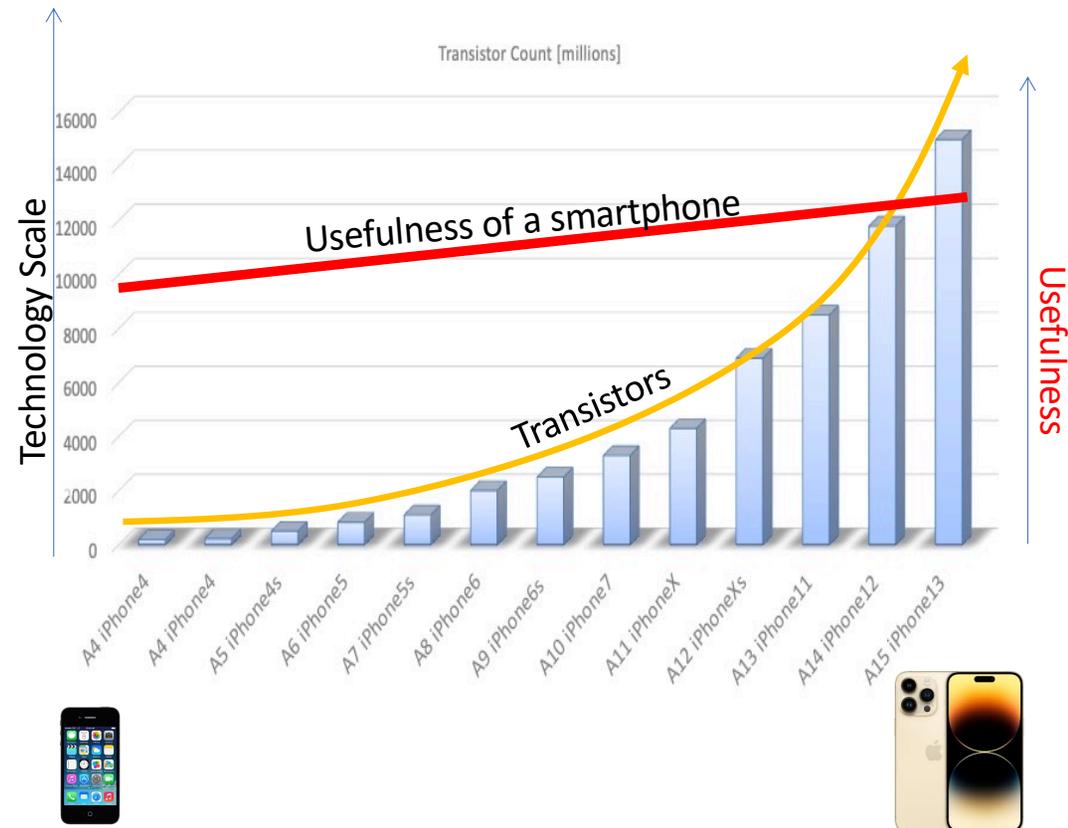
Sources: TechInsights/Anandtech/Angstromics/chipWise

iPhone 16 vs iPhone 17: incremental



Claassen's Law

**“The Perceived Usefulness
of a new product is an
underlying technology’s
logarithmic function”**
Theo Claassen, Philips Semiconductor (now: NXP), 1999

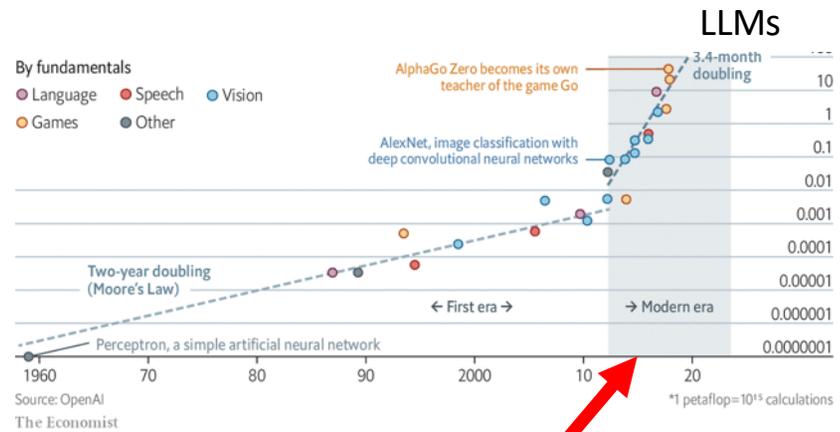


AI hardware needs “More than Moore”

Moore’s Law Transistor Supply:
transistors doubling every ~24 months



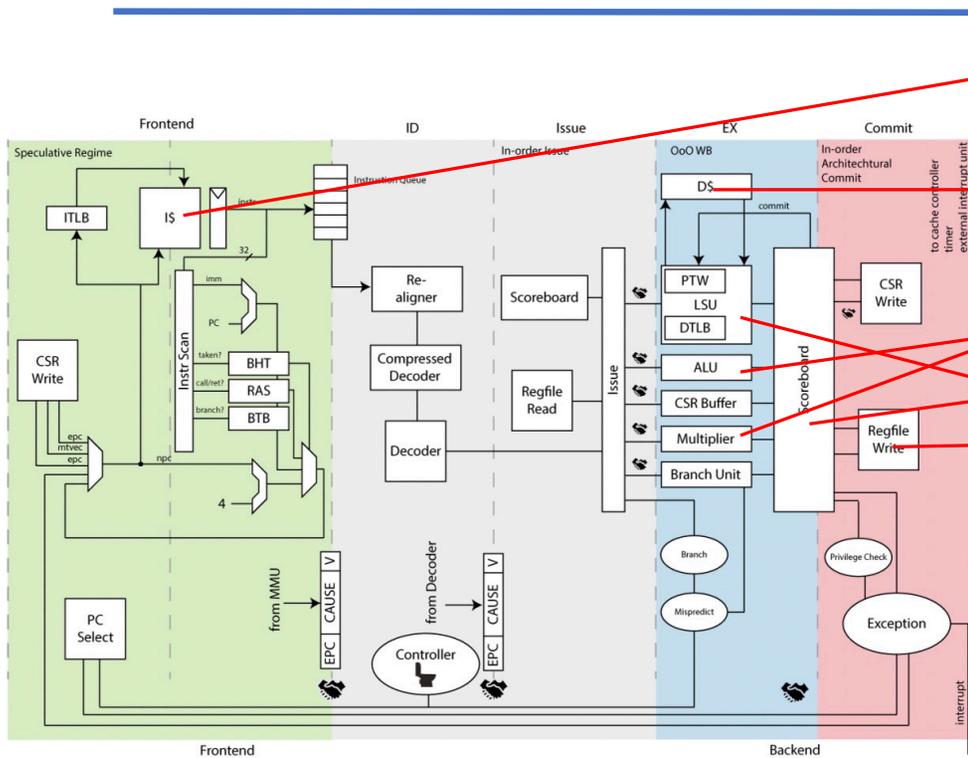
Computational Demand from AI / Machine Learning
doubling every ~5-7 months



Mid-2010's:
Unleashes Machine Learning / AI
Based on brute force
Floating-point multiply-add

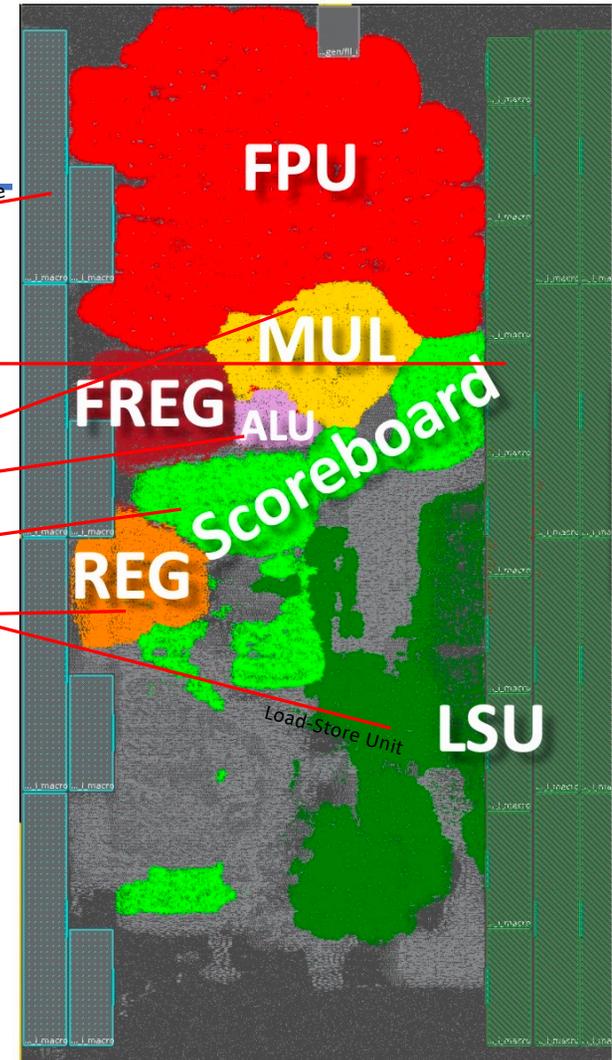
Beyond CMOS: Analog, Optical, Carbon Nanotube?

EDA: From Concept to Chip, *Fully Automated*



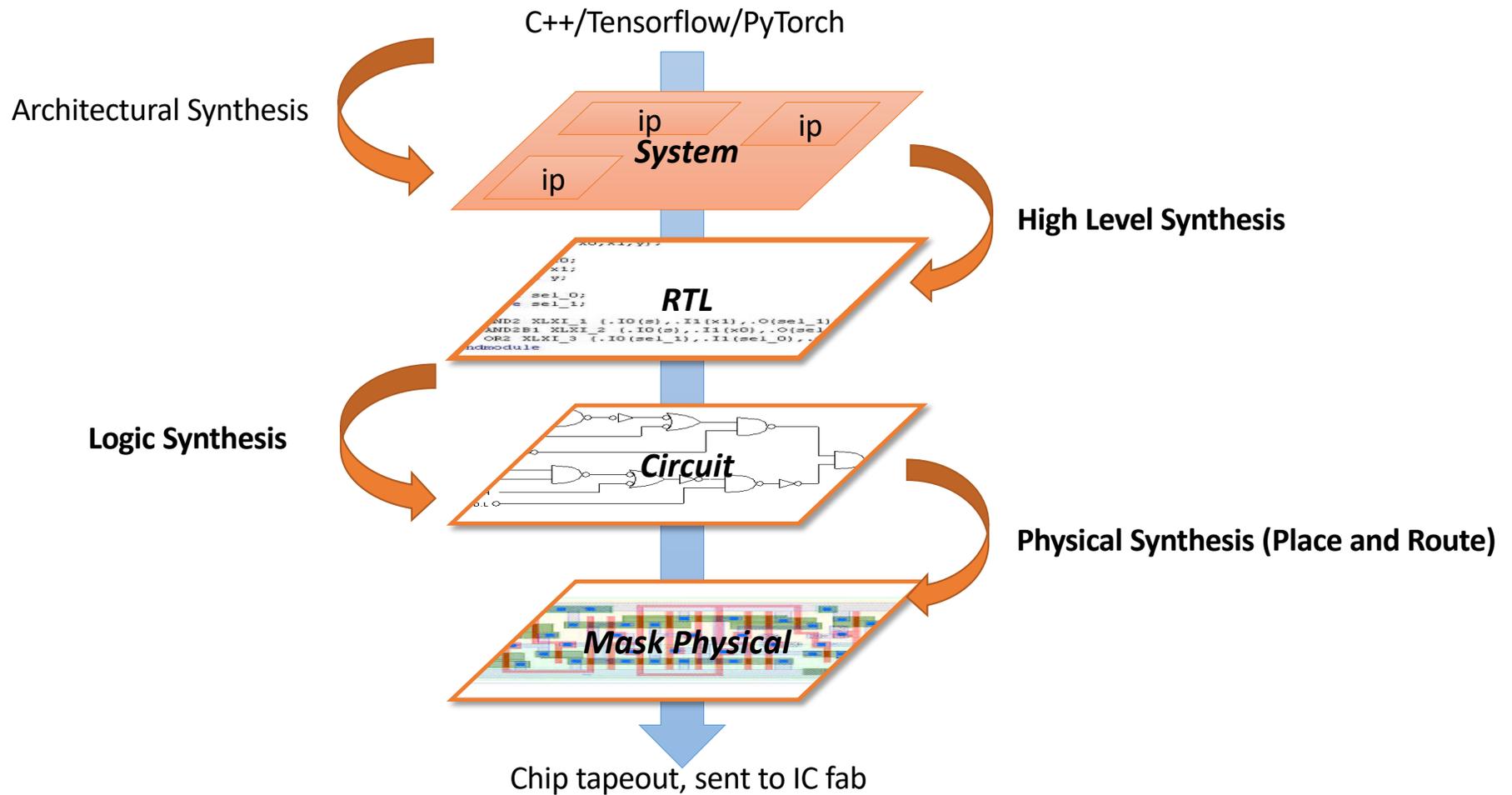
Block Diagram of a RISC-V processor

Source: Florian Zaruba, ETH Zürich
https://riscv.org/wp-content/uploads/2018/05/14.15-14.40-FlorianZaruba_riscv_workshop-1.pdf

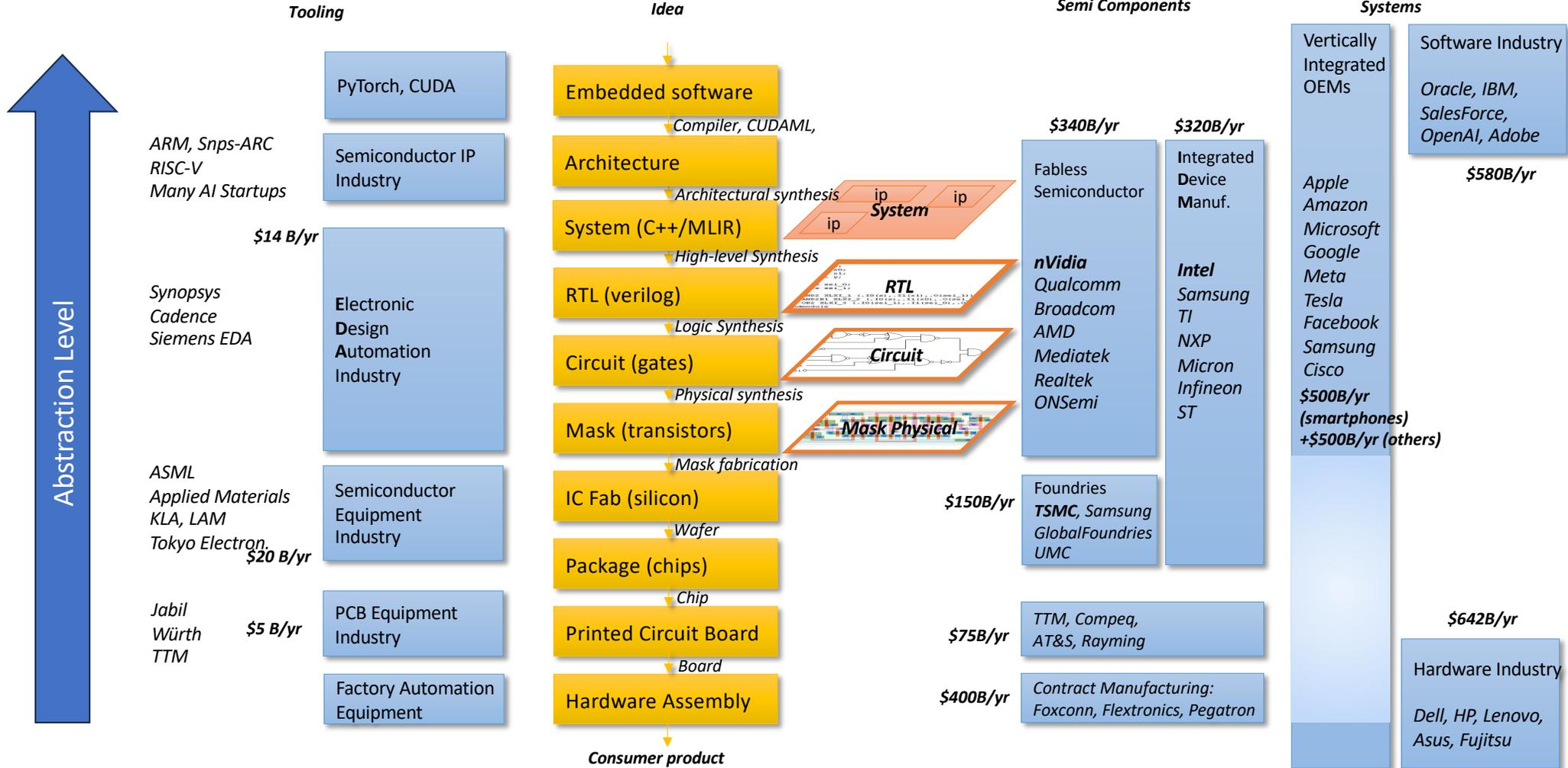


ASIC Layout

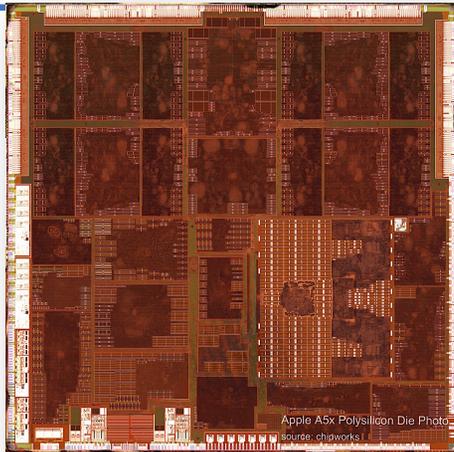
Major Abstraction Levels in Microelectronic Design



The Semiconductor Hardware Ecosystem



What Electronic Design Automation can do (..and Mechanical Design Automation can't)



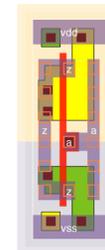
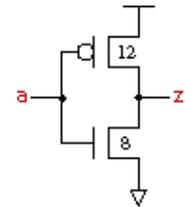
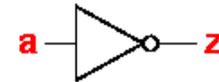
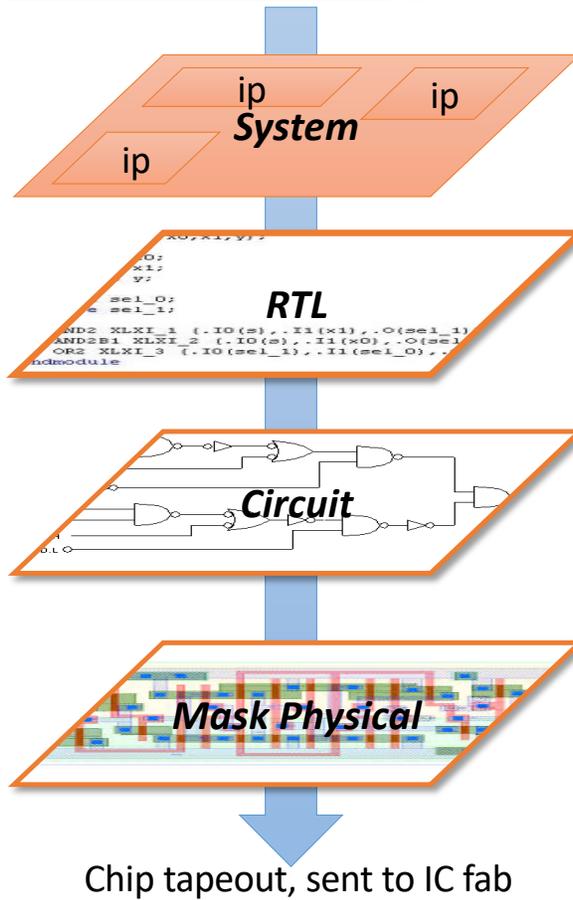
- 10,000,000,000 transistors
- Development cost: \$50M
- Development time: < 1 year
- Development team size: 100
- EDA software: ~\$14B/year



- 4,000,000 parts 0.0005x
- Development cost: \$20B 400x
- Development time: 10 years 10x
- Development team size: 10,000 100x
- MCAD software: ~\$12B/year

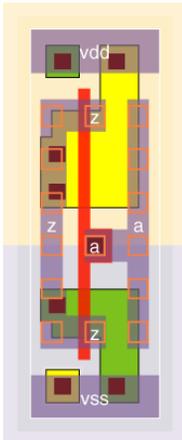
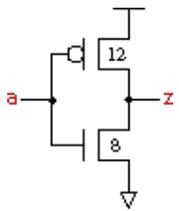
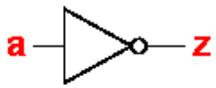
Standard cells enable a reliable flow!

C++/Tensorflow/PyTorch

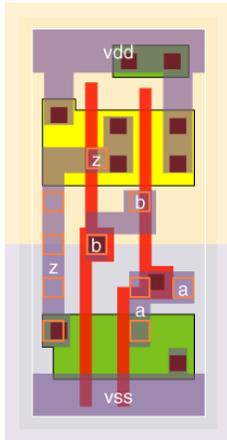
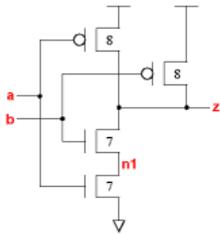
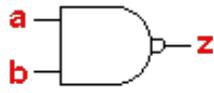


Standard Cell Library: ~100 different types

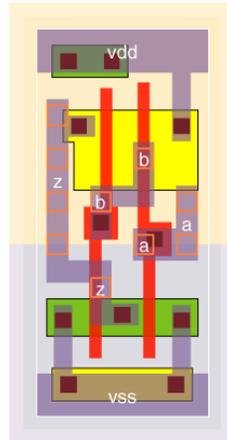
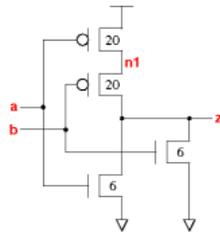
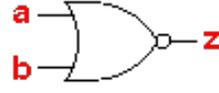
inverter



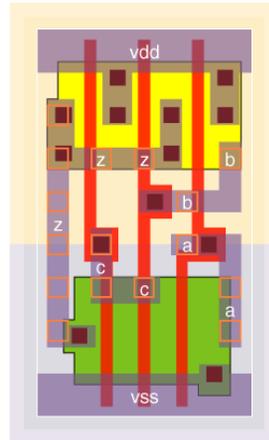
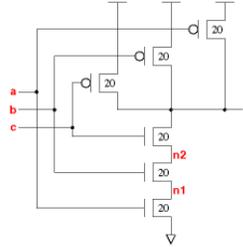
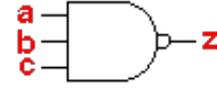
nand2



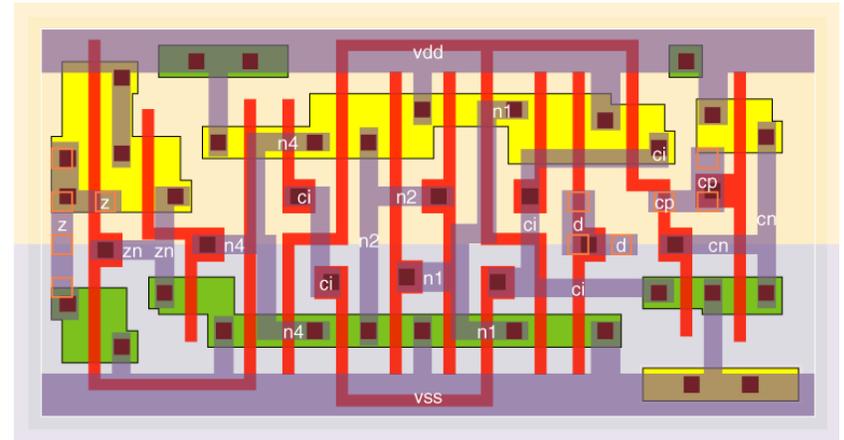
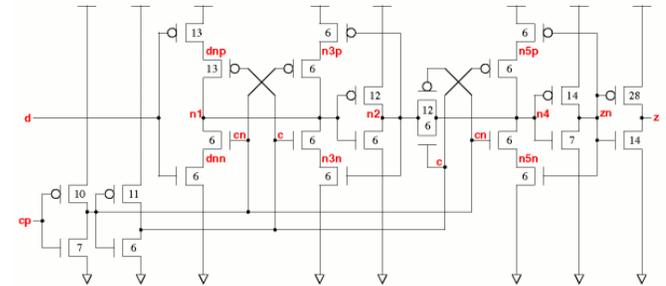
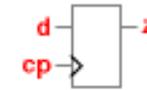
nor2



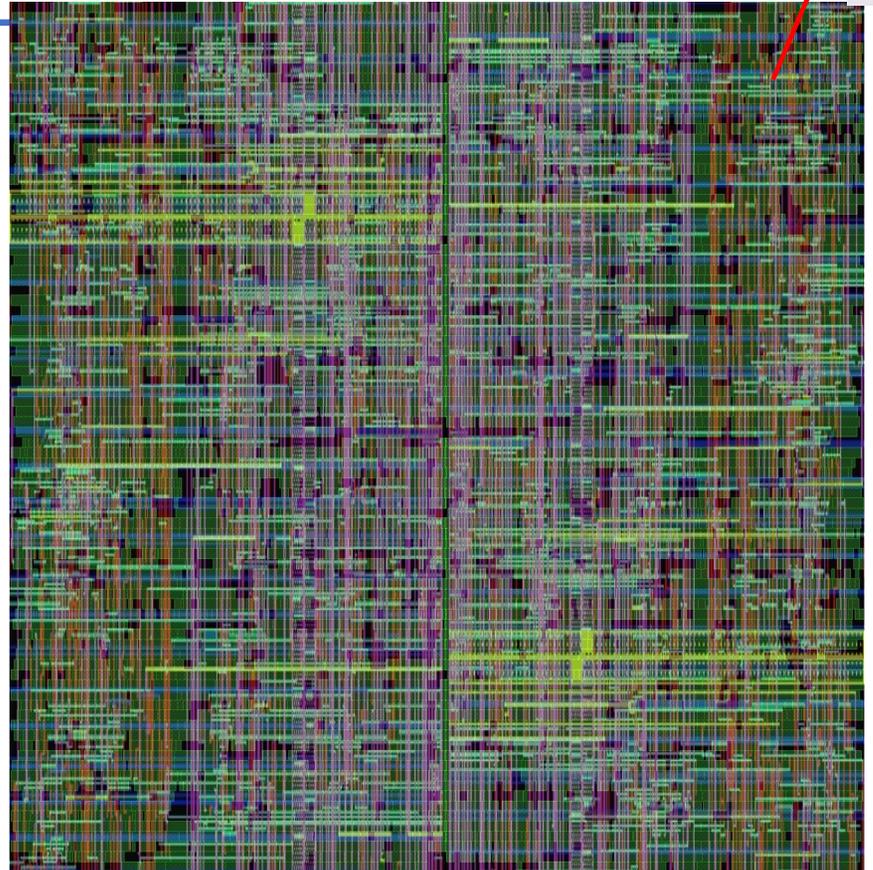
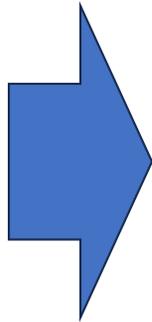
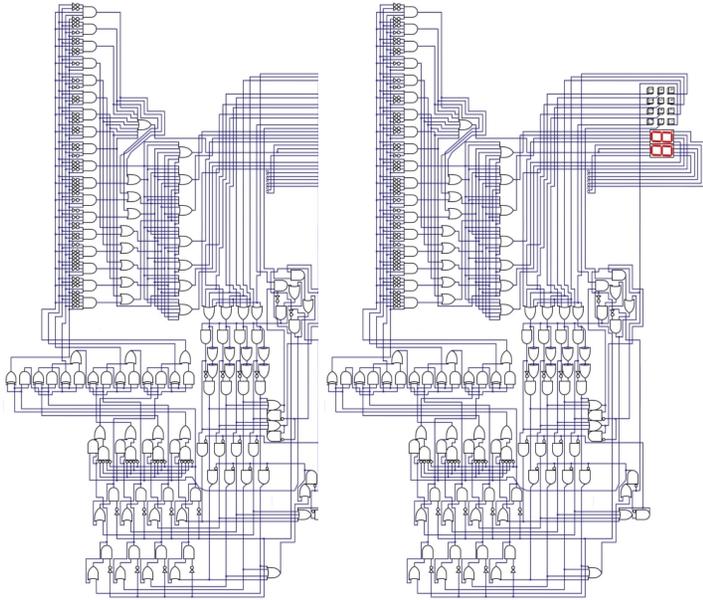
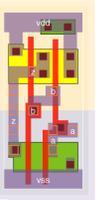
nand3



flipflop



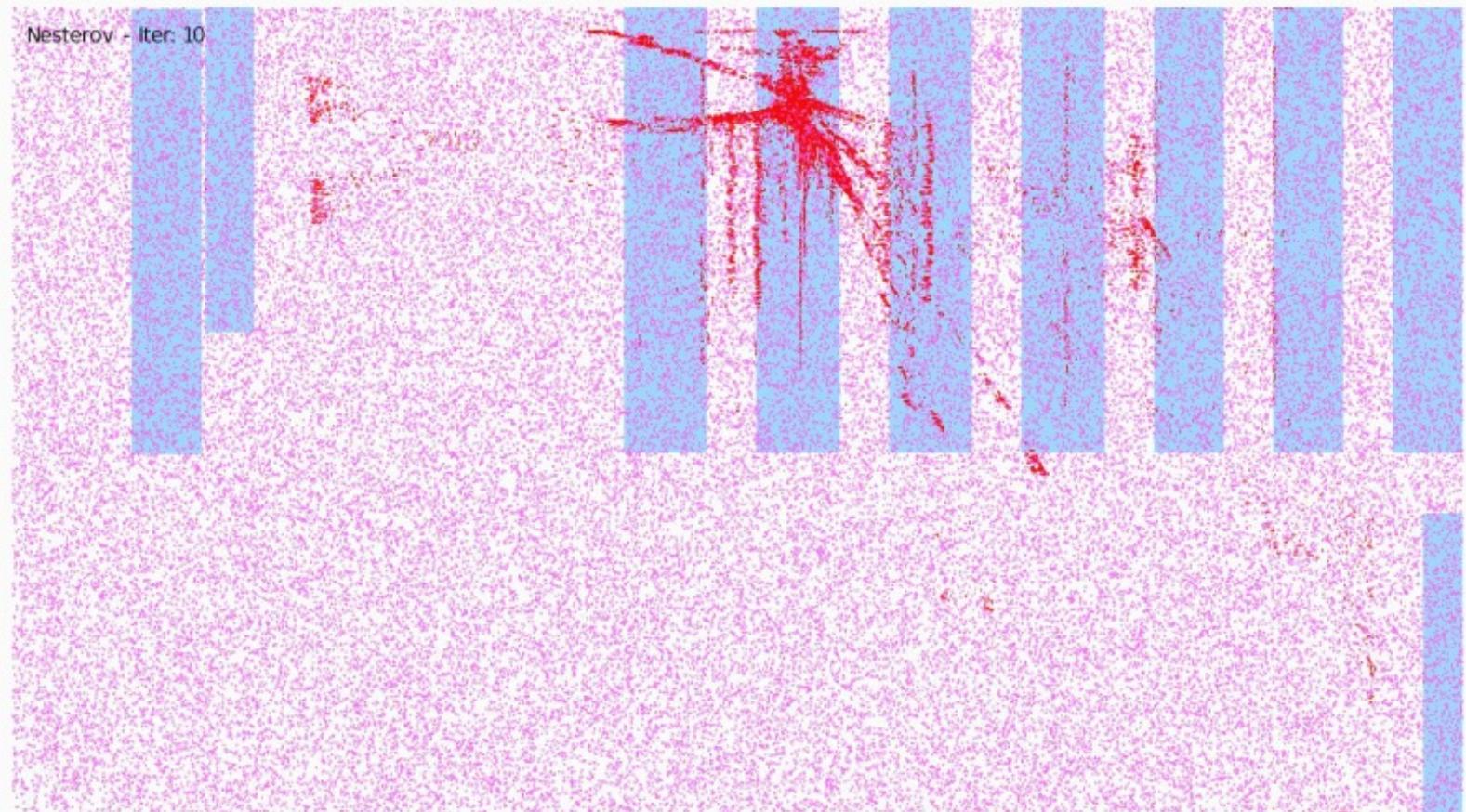
Logic Gates to Placed Standard Cells



Netlist of logic gates

Layout Mask

Placing Standard Cells



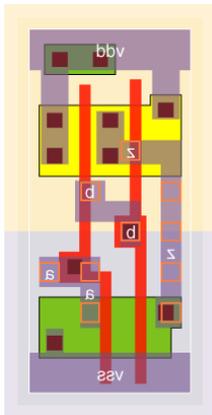
Chung-Kuan Cheng, Andrew B. Kahng, Ilgweon Kang, and Lutong Wang, "RePIAce: Advancing Solution Quality and Routability Validation in Global Placement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018

3 Levels of Physical Hierarchy!

Hides complex Physics and Lithography



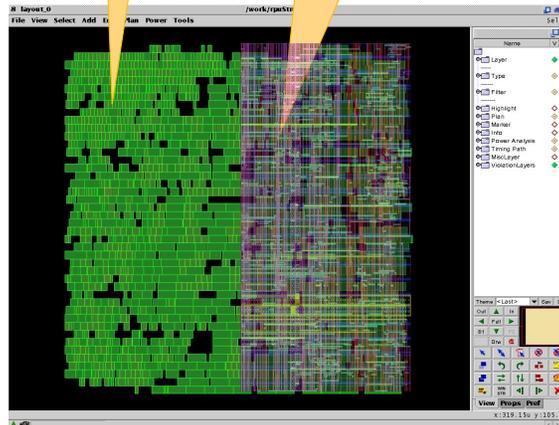
Standard Cell:
4 transistors



Millions of **homogenous** standard cells.

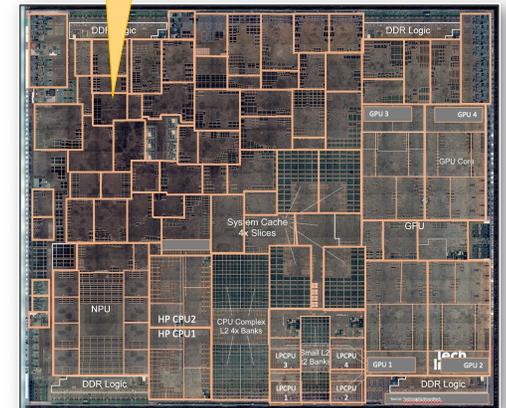
Millions of **homogenous** wires

Block:
10,000,000 transistors

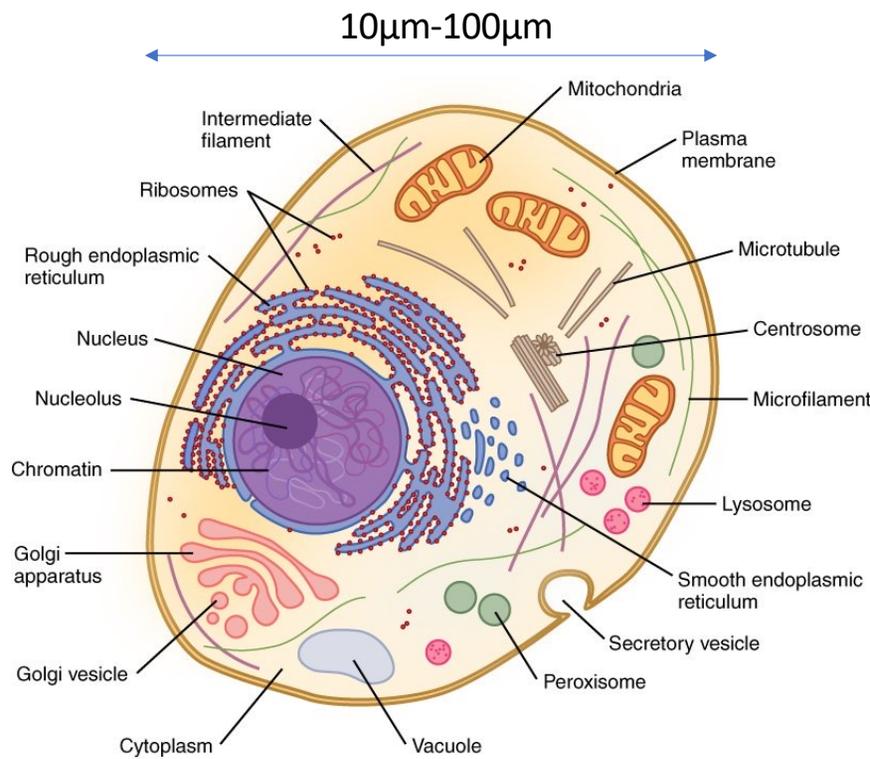


Floorplan with a few dozen **different-sized** blocks at top level

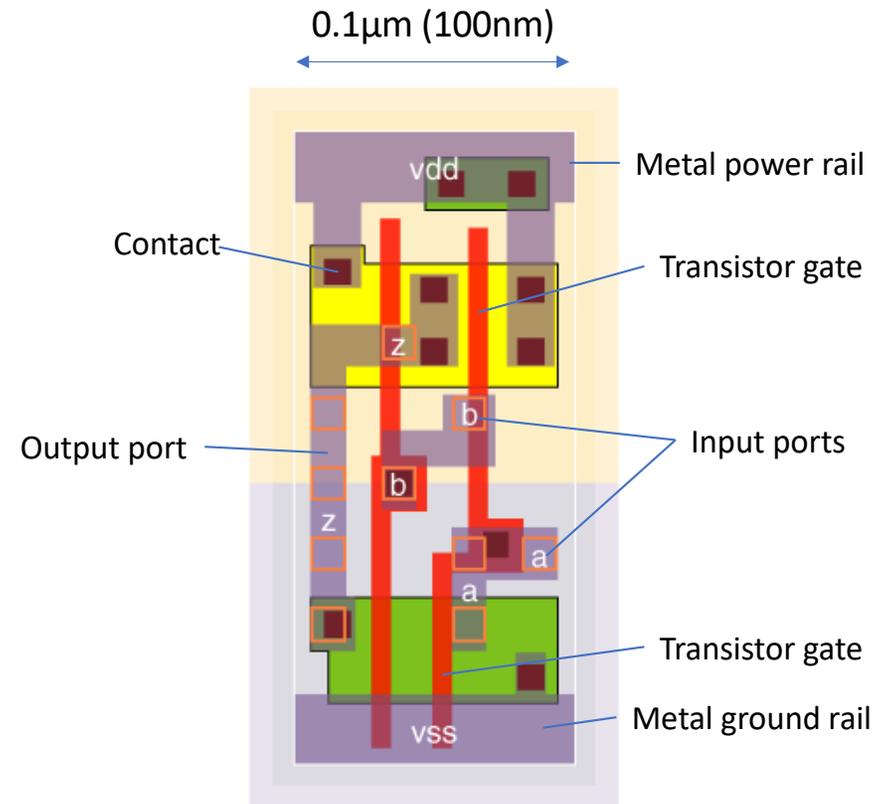
Chip:
10,000,000,000 tr



Biological Cell, Compared to a Standard Cell

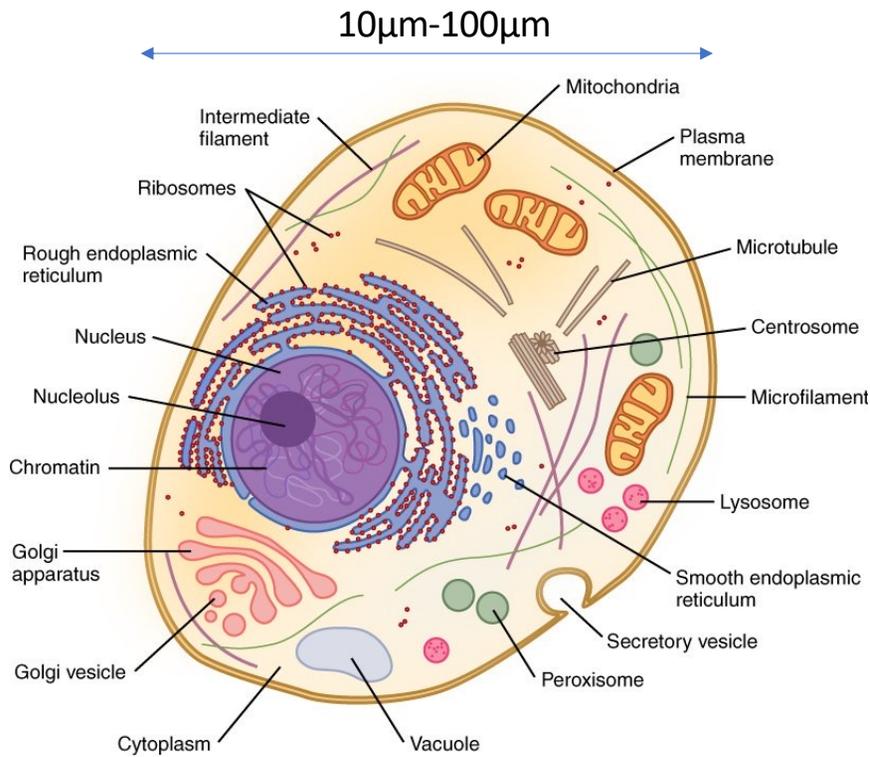
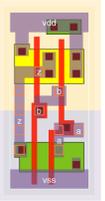


Dominant Elements: C H O P and N
Energy supply: Glucose

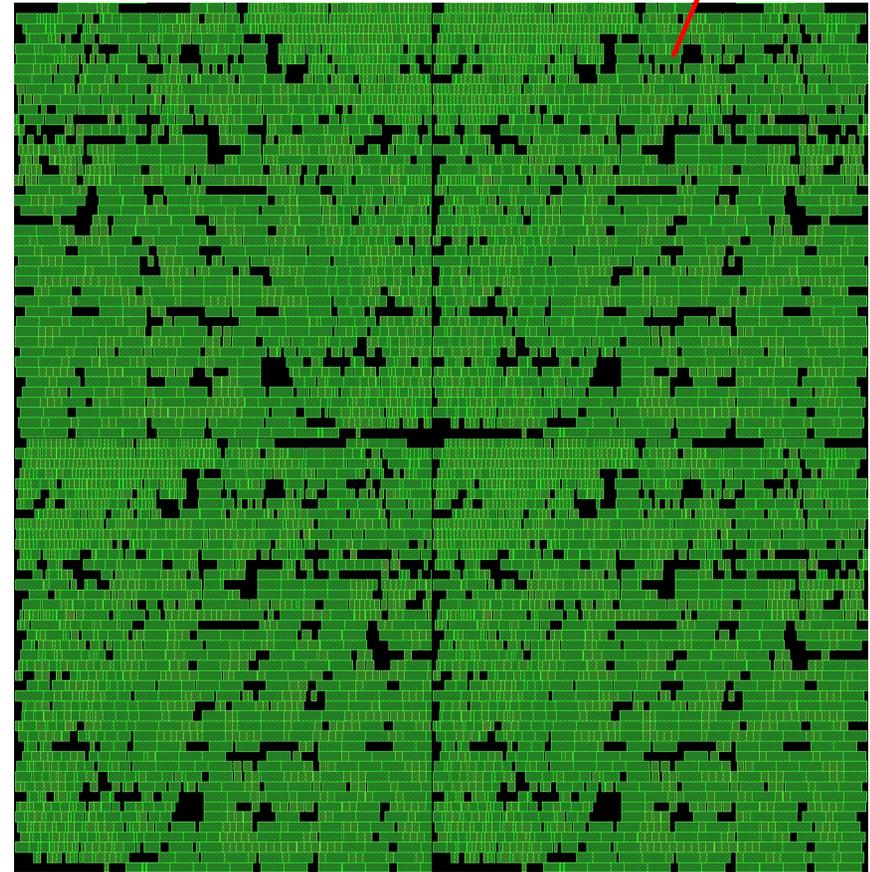


Dominant Elements: Si O Cu Al
Electric energy supply via power rails

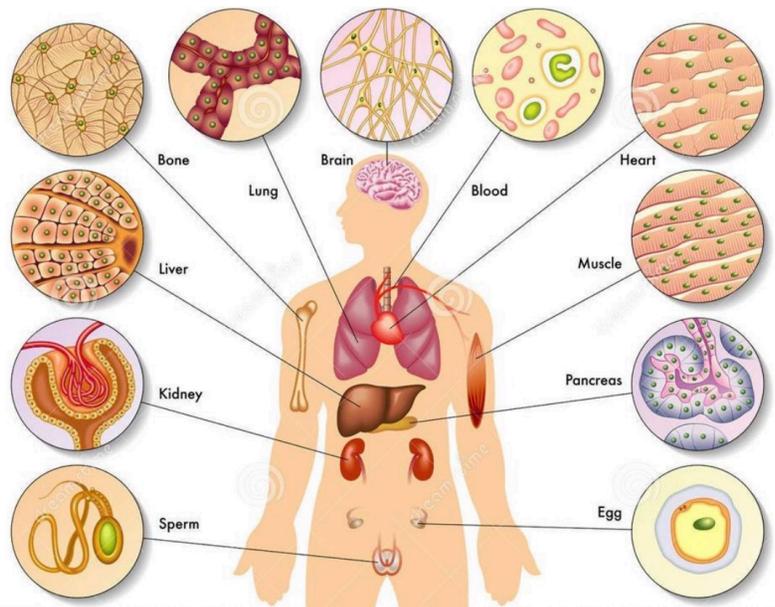
Biological Cell, Compared to a Standard Cell



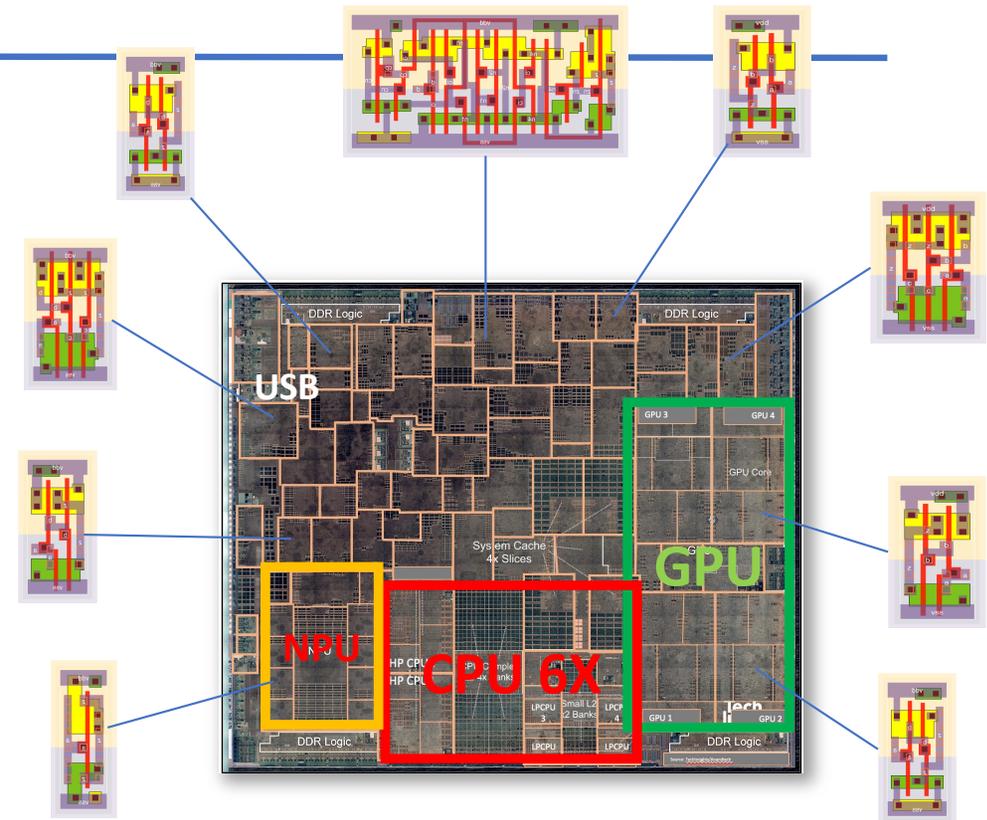
Biological cell is $\sim 300X$ larger
But uses $\sim 10,000X$ less energy



Human vs SoC: Anatomical Similarities



~200 different cell types
78 organs
400 Watt



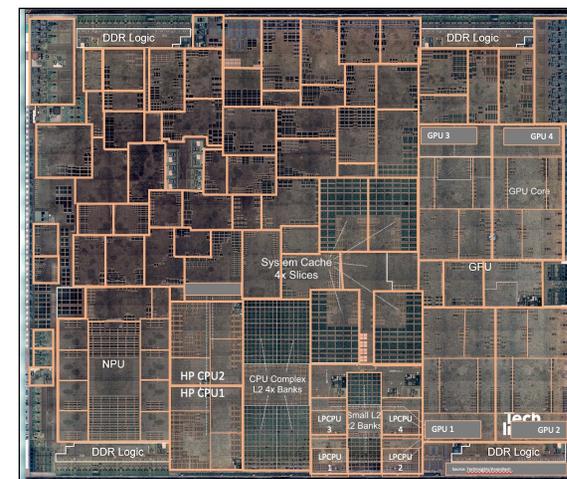
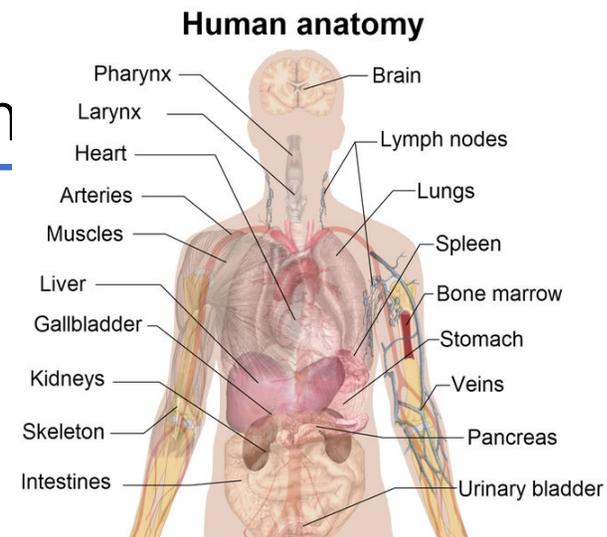
~200 different cell types
~75 blocks
400 Watt (max)

Human Cells vs Standard Cells

	Human Cell/human body	Standard Cell/chip
Cell Library size	~200	~200
Cell components	Nucleus, Ribosomes, membranes, DNA, Golgi, etc.	2-20 transistors, vias, wires
Number of cells	37,000,000,000,000	20,000,000,000
Main elements	C, H, O, N, P	Si, O, Cu, Al
Design	Bottom-up evolution through natural selection, M-years	Top-down creation using EDA tools, months
(re-) production	Division, self-assembly	Lithography
Power	400W	400W
Power per cell	0.001nW	70nW
Infrastructure	Blood vessels, nerves	Power Wires, Clock network
MTBF/lifetime	8 years (cell) /80 years (person)	3 years (econ.)/ 10+ years
Error resilience	Self-healing	None
Failure mechanisms	Cancer, heart disease, infections	Electromigration, heat, ESD
Disposal	100% recycled	84% Landfill, <1% recycled

Key Similarities between Biological Systems and Electrical System

- **Cells are similarly sized**, with minor variation in types
- Cells use **uniform plumbing** for energy supply
- Cells are **composable into organs** (IP blocks) to perform a wild variety of functions
- An organism (or SoC) is built from several such organs blocks
- Somehow, arrangements of billions of cells become 'intelligent'



SoC Anatomy

Numerous as Sand on the Beach...



1000 BCE / Bible, Genesis 22 verse 17:
*I will surely bless you and make your descendants as numerous as **the stars in the sky** and as **the sand on the seashore***

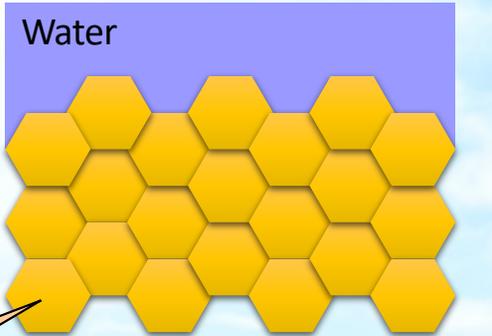
1980 CE / Carl Sagan, Cosmos:
*There are **more stars in the universe** than there are **grains of sand on all the beaches of Earth***

2024 CE / Some dude (Brady Booch) on Twitter:
*There are **more transistors on earth** than **grains of sand on all the beaches of Earth***

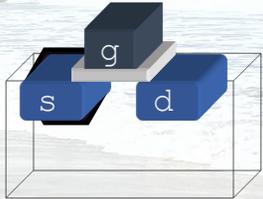
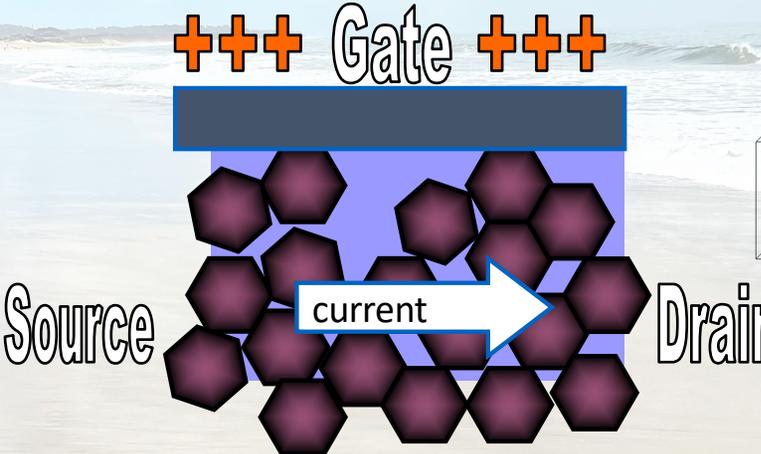
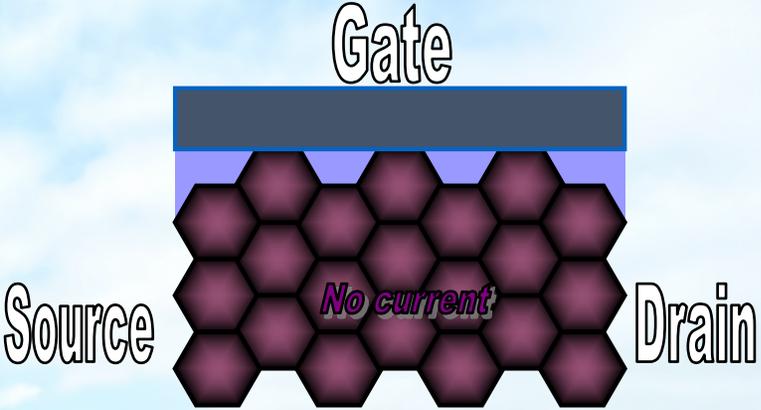
Sand as a Parable for MOS Transistors



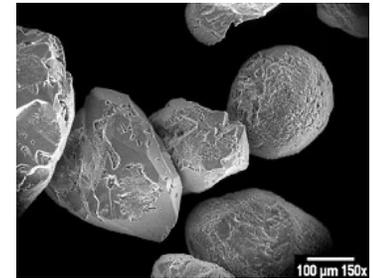
Sand as a Parable for MOS Transistors



Grain of sand

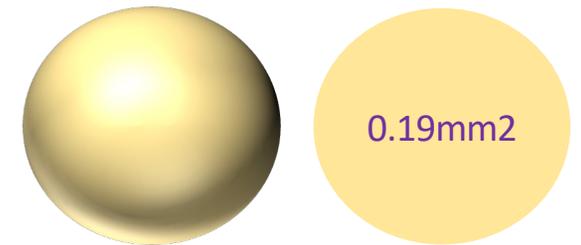


Beach Sand or Stars: Which is Greater?



- There are $\sim 6 * 10^{21}$ (6 sextillion) grains of sand on beaches

- Sand is grains of mainly SiO_2 , typically 0.5mm diameter.
-> a cubic meter of sand contains $\sim 8B$ grains
- Assuming a beach is 200 meter wide and sand layer is 20 meters deep, then one km of beach has $1000 * 200 * 20 * 8B$ grains
= $3.2 * 10^{16}$ grains per km of beach.
- The world has 620,000 km of coastline, of which 31% is sandy
(Source: NASA)

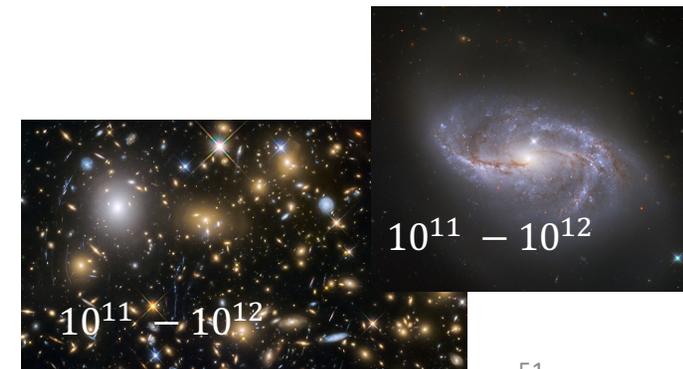


0.5mm

Room for
 $\sim 39,000,000$
Transistors in 5nm

- There are between 10^{22} and 10^{24} stars in the universe

- Between 10^{11} (100B) and 10^{12} (1T) stars per galaxy
- Between 10^{11} and 10^{12} galaxies in the universe (source: ESA)

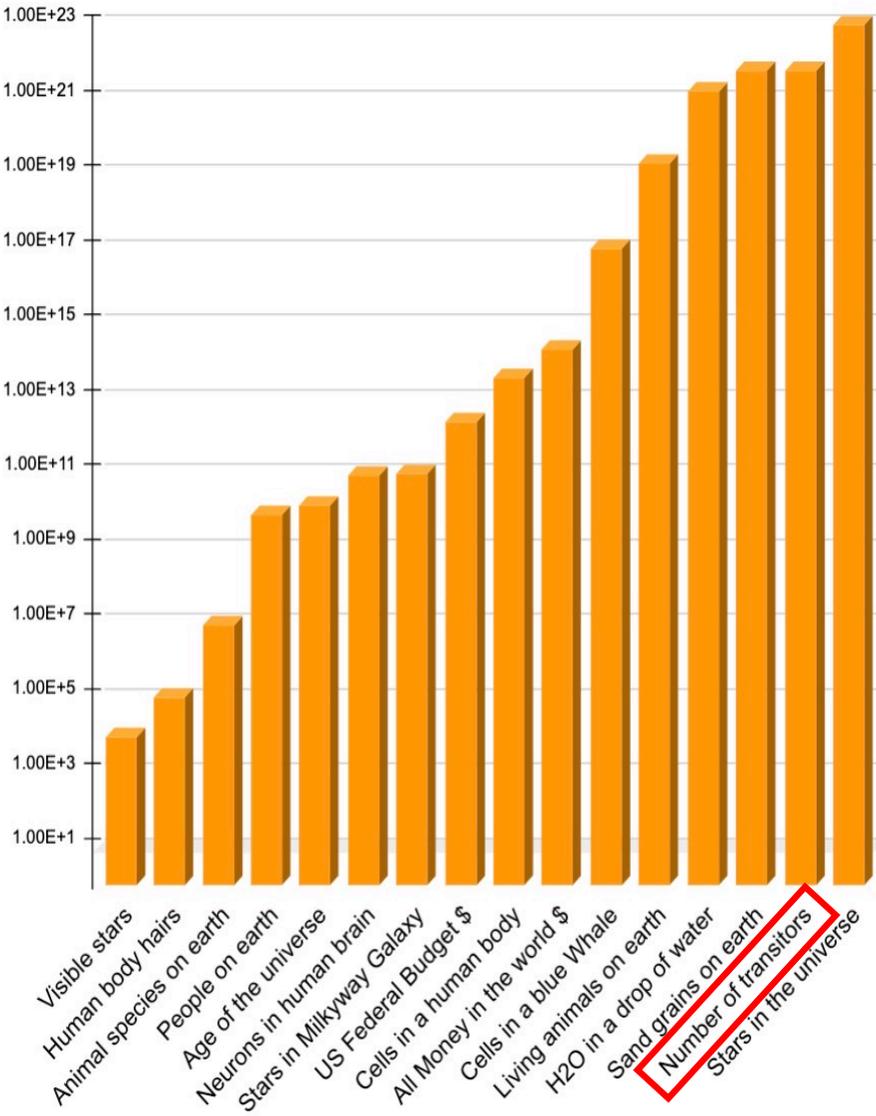
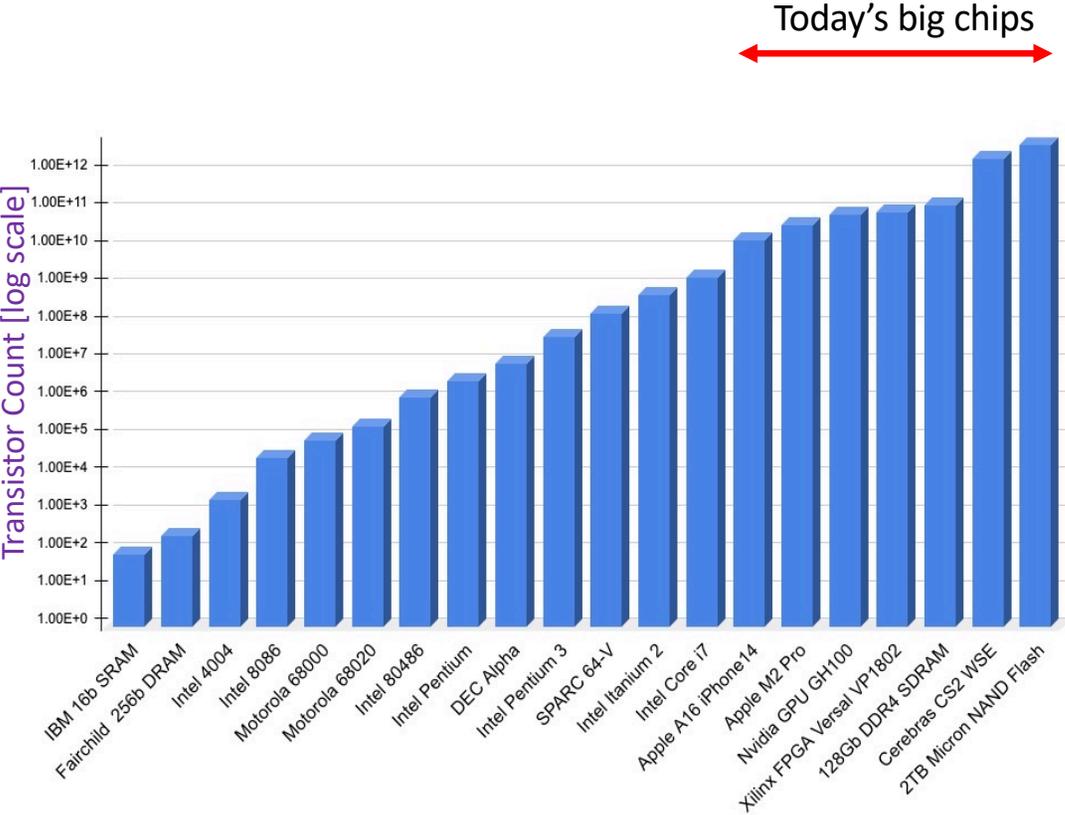


NASA/Hubble

How many Transistors are “Alive” in the World?

- Approx. $8 * 10^{19}$ in 2024 based on number of 12” wafers :
 - TSMC made 13M wafers, most in dense technologies of $\sim 3T$ transistors/wafer = $2.9 * 10^{19}$. They have $\sim 40\%$ of the market.
 - Approx. 72M raw 12-inch wafers were produced in 2023 @ $\sim 1T$ transistors per wafer
- Approx. $1.8 * 10^{21}$ in 2024 alone based on NAND FLASH memory market data:
 - Flash memory market was $\sim \$70B$ in 2024
 - at $\$100/\text{Terabyte}$ means that $\sim 700M$ TB were produced = $1.8 * 10^{21}$ Transistors (assuming $2.6 * 10^{12}$ transistors per TB = 6 bits per cell)
- With average product life of 3 years, we have $6 * 10^{21}$ transistors running, most of them as memory
- Conclusions:
 - There are approximately **as many transistors as grains of sand** on all beaches in the world
 - There are **still more stars than transistors** in the universe

Astronomical Number of Transistors



Electronic Design Automation at Astronomical Scale

- EDA design methodologies pull it off, somehow
- How?
 - Successful algorithms
 - Gradual transition through abstraction level
 - Strict verification
- Next steps:
 - Harness Machine Learning
 - .. And gen-AI

