Interconnect Reliability in Advanced Packaging & Heterogeneous Integration

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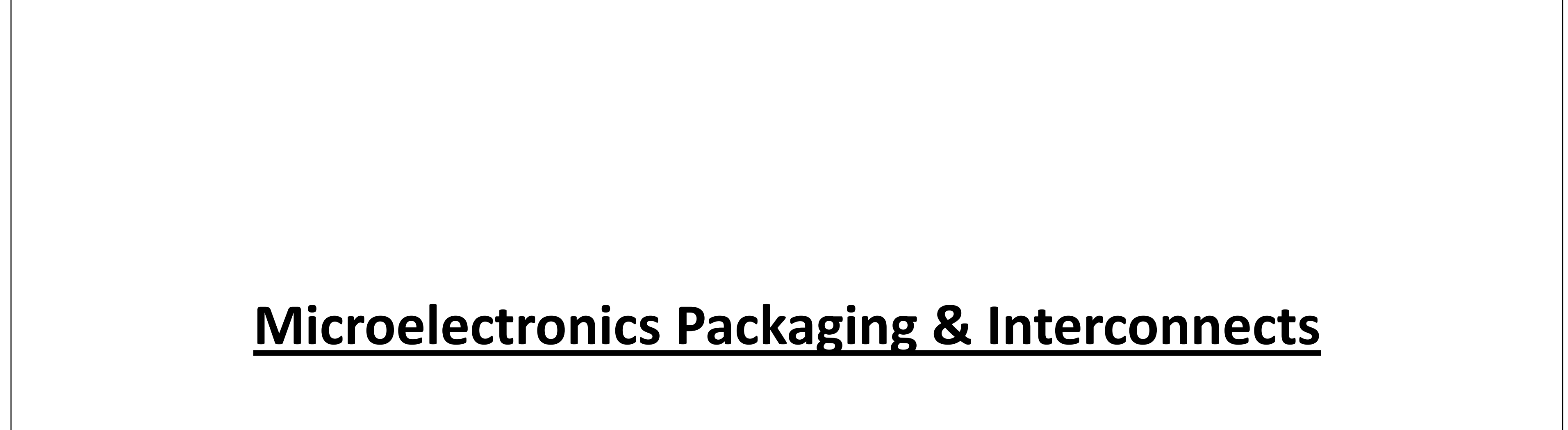
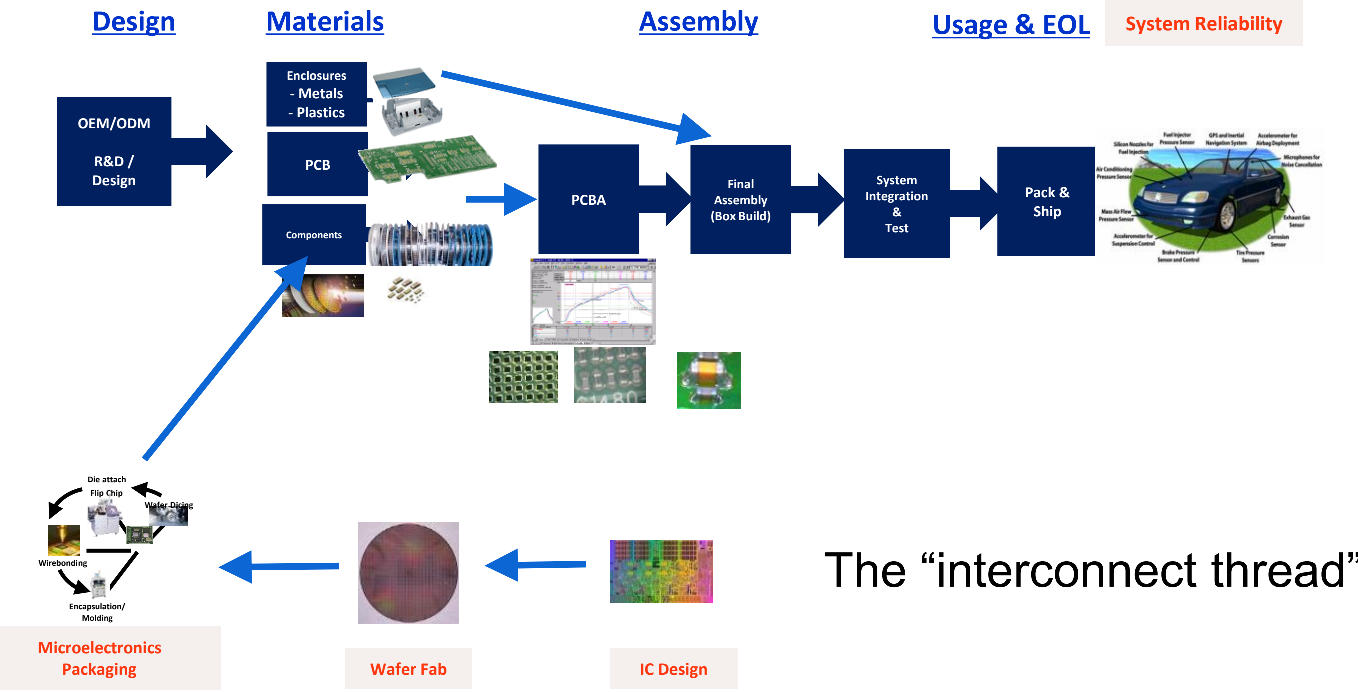
Outline

- Microelectronics Packaging & Interconnects
- Thermomechanical Reliability
    - Chip Package Interactions; Solder Interconnect Reliability; Whiskering
- Electrical & Electrochemical Reliability
    - Electrochemical; Electromigration; High Frequency
- Direct Cu Interconnection
- Thermal Integrity
- Summary



Microelectronics Packaging & Interconnects

Reliability – From the Chip to the System



(Illustration only. Photos from various sources)

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Packaging = Interconnects

(essentially)

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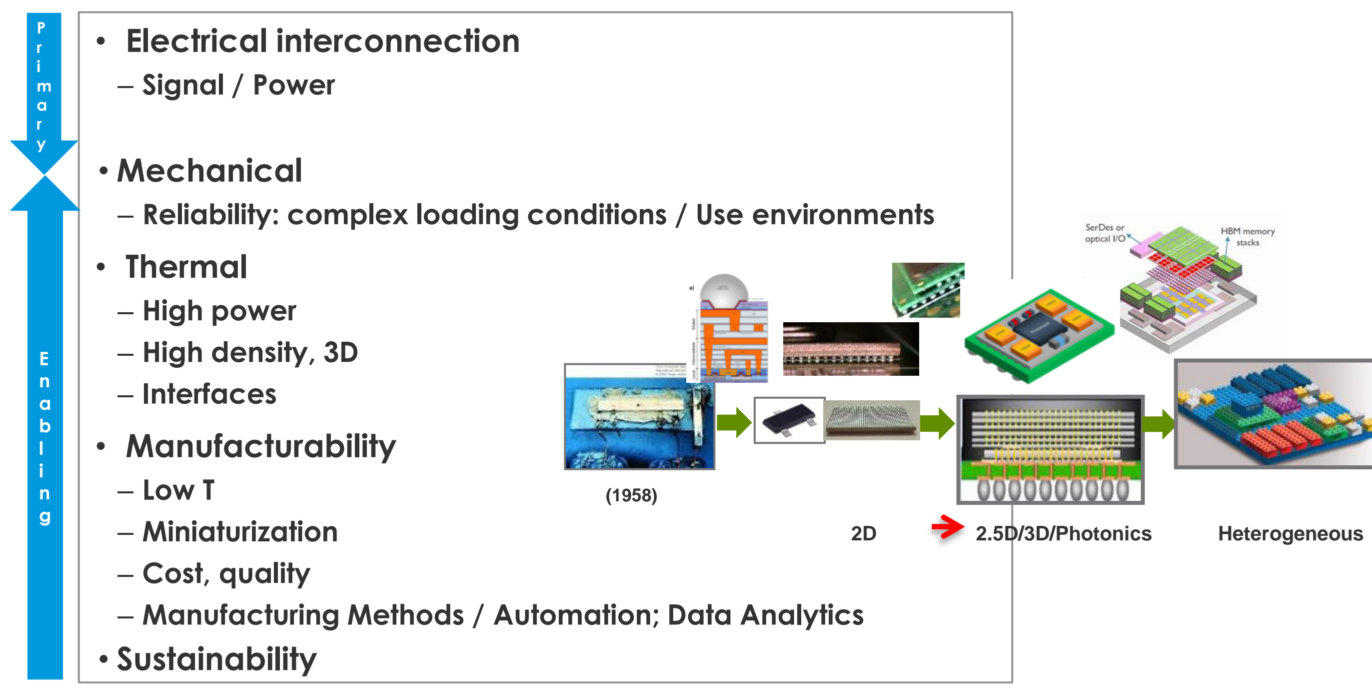
Packaging: Interconnects along the signal chain – from the IC to the system



- **Heterogeneous Integration**
  - A variety of **interconnects** in the same package

(Illustration only. Photos from various sources)

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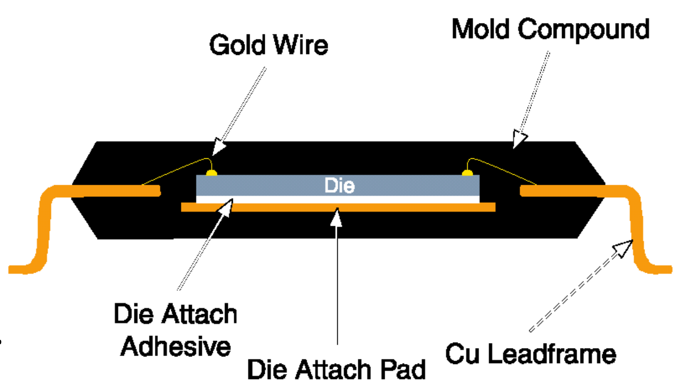
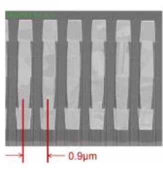
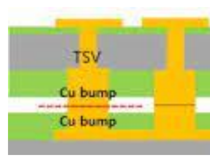
Interconnects: Die – Package – Termination – PCBA - System

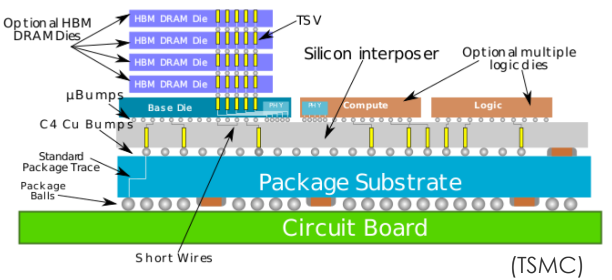
Package PCBA System

- **Chip package interaction (CPI)**
- **eRDL / oRDL**
- **TSV**
- **Wire bonding, flip chip**
- **Solder interconnects, or Direct Cu Interconnection**
  - **Solder in various forms: Solder joint, bump/pillar, BGA ball, …**
- **Termination: leads, balls, pads, …**
- **Photonics**
- **PCB/A**
- **System: Connectors, fibers, cables, …**









(TSMC)

(Illustration only. Diagrams from literature)

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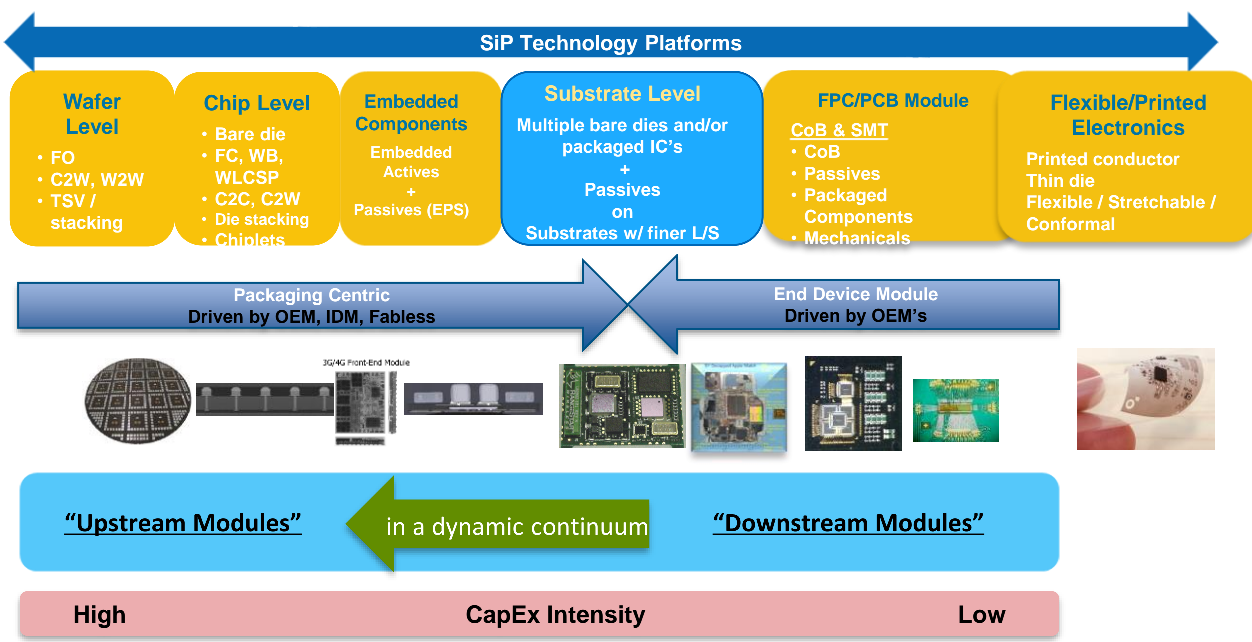
SiP Technology Landscape

Heterogeneous package architecture for heterogeneous integration



SiP Reliability: A variety of interconnects in the same package

(Illustration only. Pictures from various sources)

(D. Shangguan)

Interconnect Reliability

Shorter interconnects

Performance
Power
Area
Cost
Reliability
(PPACR)

- At different levels of interconnection
- With different forms of interconnects
  - WB, Solder joint, bump/pillar, TSV, RDL, Direct Cu Bonding, …
  - Photonics
- Under various environmental / loading conditions
  - Thermo-mechanical, dynamic mechanical
  - Electrical, electrochemical
  - …
- With different failure modes and mechanisms; and
- Different solutions for reliability assurance
  - Design, materials, processes, testing

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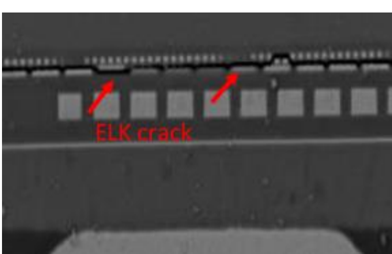
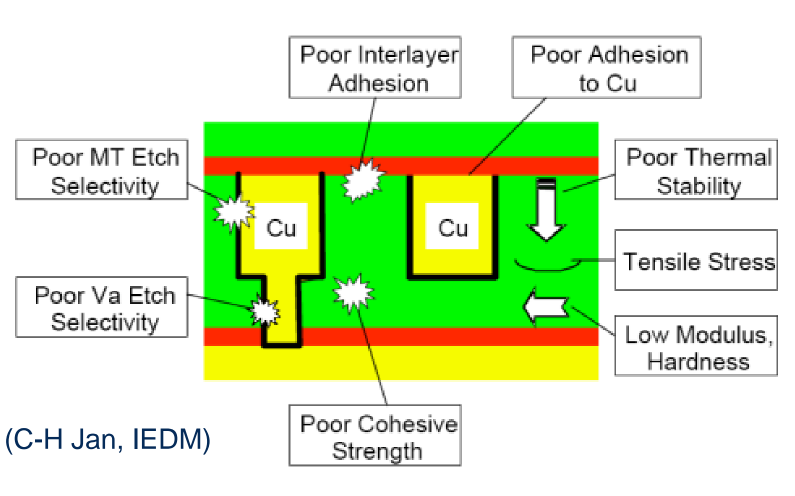
Chip Package Interactions

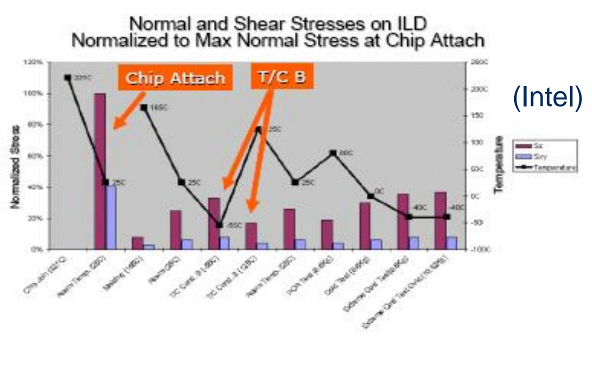


Chip Package Interaction (CPI)

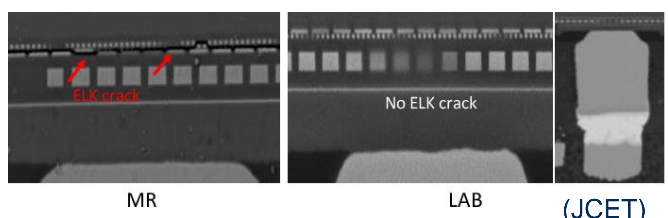
- **Low k dielectrics**
  - Low strength of low k dielectric *vs.* high modulus of SAC solder
    - SiO_2 (k = 3.9); Low k: <3.0
    - Thermo-mechanical strength 10x worse than SiO_2



(C-H Jan, IEDM)



(Intel)



(JCET)

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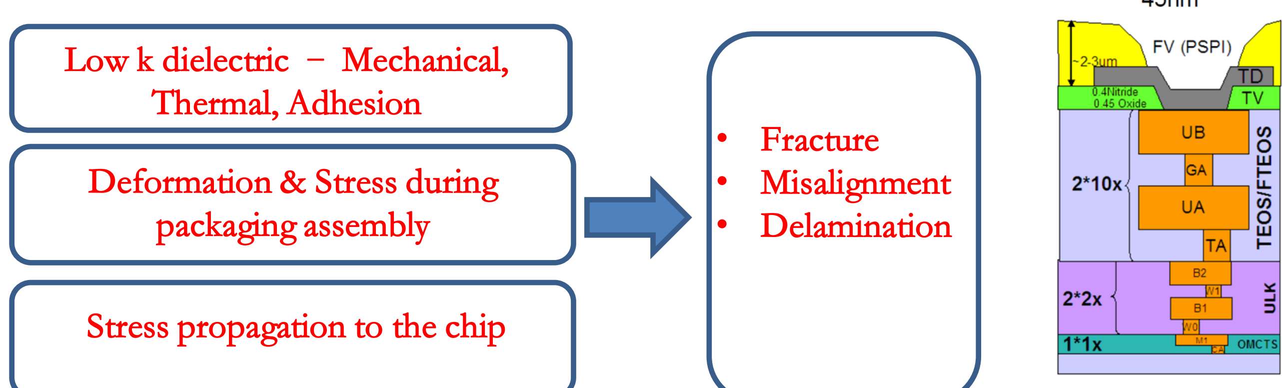
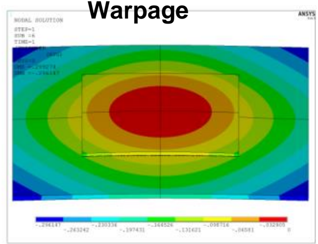
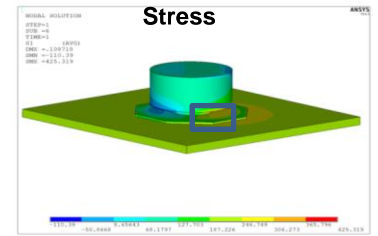
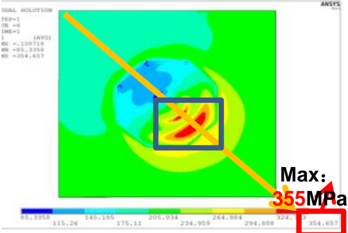
CPI Reliability



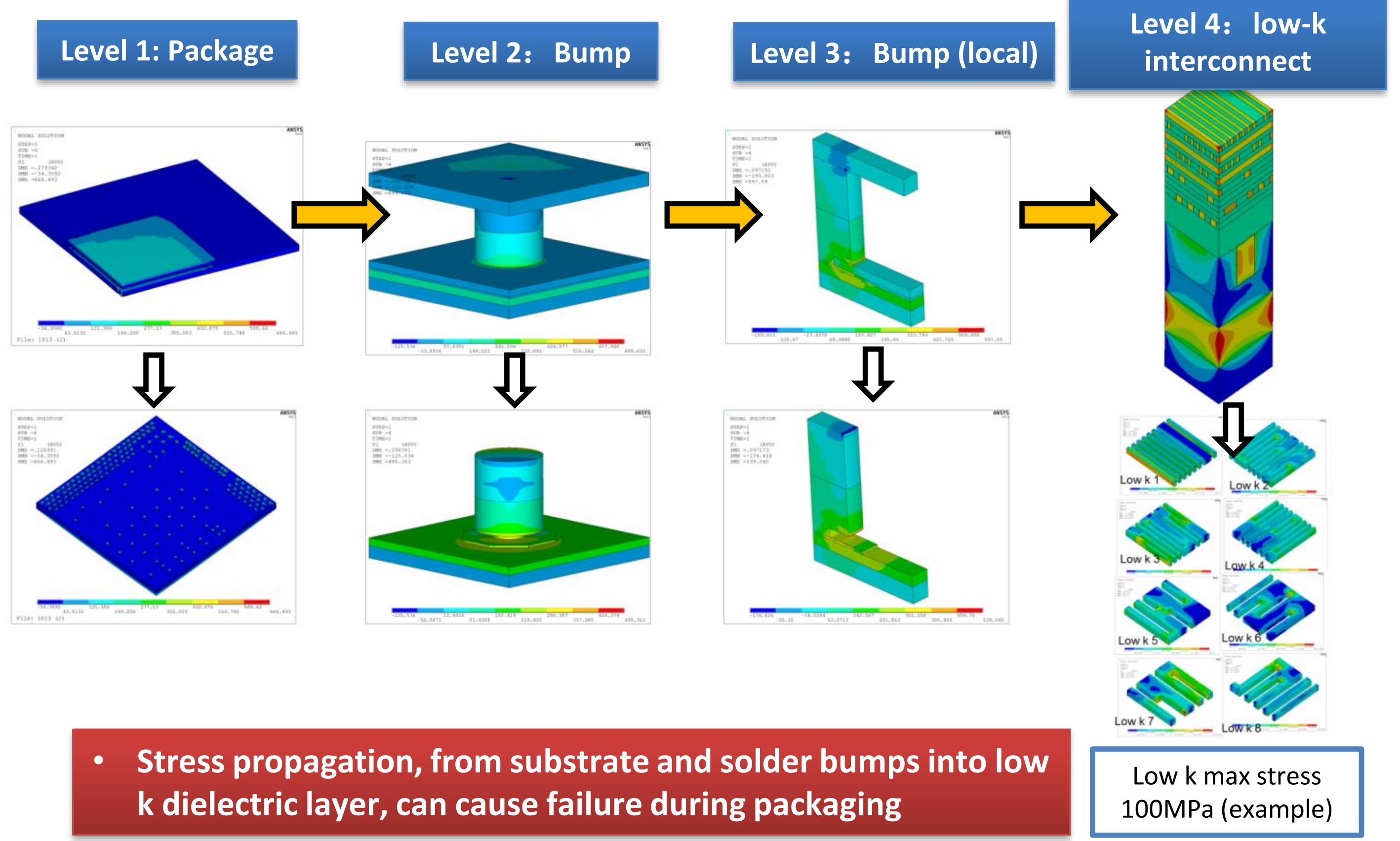






(Rao, Shangguan et al, ECTC)

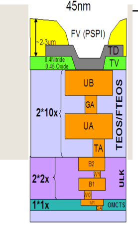
CPI Reliability Modeling: Multi-Level



- Stress propagation, from substrate and solder bumps into low k dielectric layer, can cause failure during packaging

(Rao, Shangguan et al, ECTC)

Design for Reliability for Chip to Package Interaction (CPI)



Simulate Fabrication Process Steps

Read Mask Layout through ICWBEV+

Etching Steps with Temperature

Deposition Steps with Temperature

Final Structure

Chip with bumps

Substrate with bumps

Flip chip bond

Underfill

Stiffener and Heat spreader mount

Ball mount

Lid

Stiffener

Chip

Bump

Solder ball

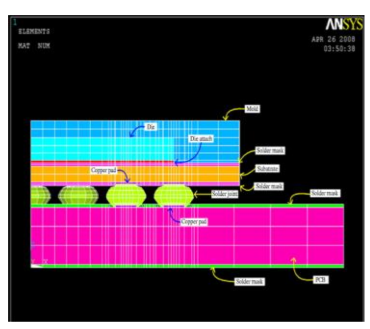
PCB

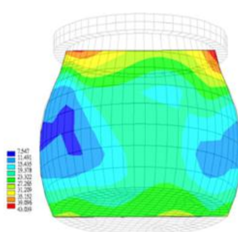
Package substrate

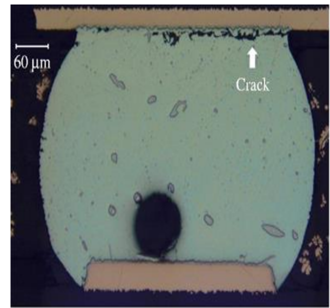
Stress Evolution

(Rao, Shangguan et al, ECTC)

Solder Interconnect Reliability

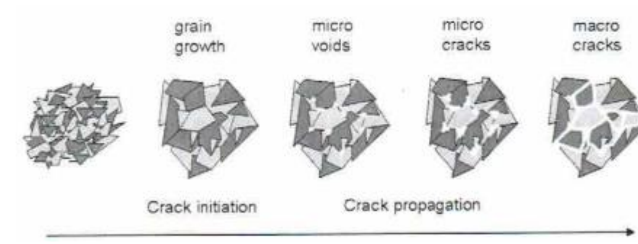




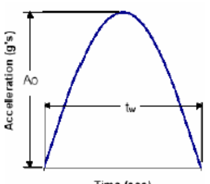


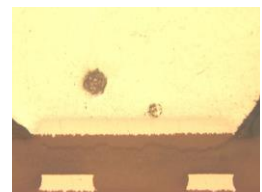
Solder Interconnect Reliability

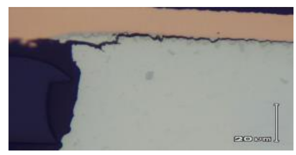
- Under cyclic loading
  - Thermomechanical – Low cycle fatigue (creep/fatigue)
  - Cyclic bending, vibration – High cycle fatigue
  - Crack initiation and propagation



- Under dynamic mechanical loading
  - Drop, Bend, Shear, Pull, Shock – High strain rate
  - High frequency board flexing
  - Strain rate dependency
  - Brittle fracture … sensitive to stress concentration
  - Interfaces







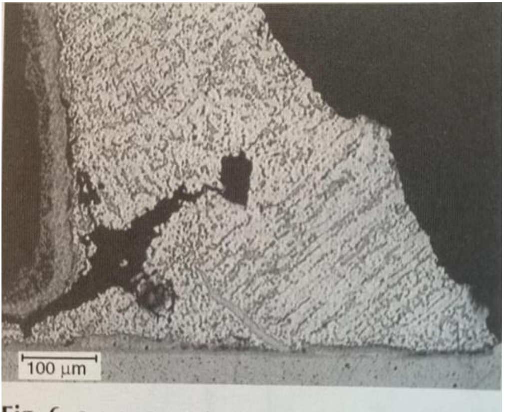


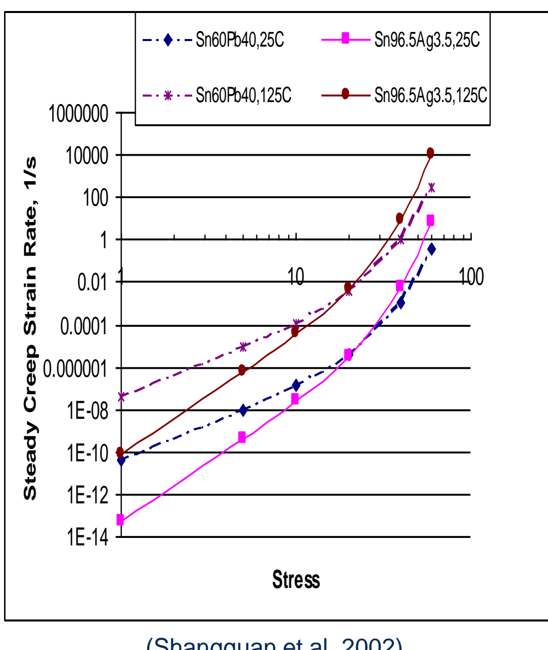
Fig. 6 SnAg3.8Cu0.7 after thermal cycling

© D. Shangguan

Thermomechanical Reliability

- Reliability comparison between SAC and Sn/Pb
- Lower thermal cycling reliability for SAC at high loading levels
  - High CTE mismatch (e.g. Alloy 42 vs. Cu; WLCSP; …)
  - Large thermal cycle range (e.g. automotive)
  - Large size components (e.g. 2512 ceramic chip resistor) or low stand-off (e.g. LGA)

$$\Delta\gamma = C\frac{L_D}{h_s}\Delta\alpha\Delta T$$



(Shangguan et al, 2002)

High Reliability Solders

Sometimes, failures are not due to the absence of

an intended connection, but the presence of

an unintended one…

(D. Shangguan)

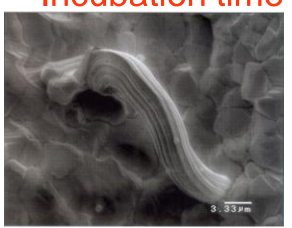
Sn Whiskers

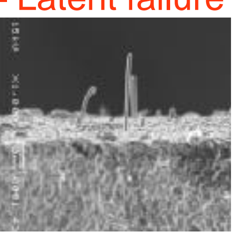
A spontaneous columnar or cylindrical filament, usually of mono-crystalline Sn emanating from the surface of a plating finish

Mechanism

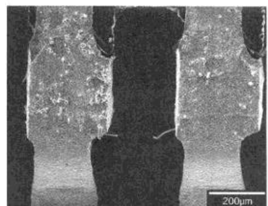
- **Compressive stresses (>7MPa) due to:**
  - > **Residual stress within the plating**
  - > ***Irregular* IMC (Cu_6Sn_5) at the interface… *continuously regenerating the driving force***
  - > **Forming/application stress**
  - > **Surface defects (scratches, dents)**
  - > **Thermomechanical (CTE mismatch)**
  - > **Oxidation**
- **Certain crystalline microstructure favorable to a *localized* surface eruption**
- **Stress relief through recrystallization and grain growth**

Incubation time – Latent failure





(@ 0.1-10 °A/s, or 0.3-30 mm/yr)



Typical: 1-5 µm diameter / 1-500 µm long

Interconnect Reliability: Electrical & Electrochemical

- **Electromigration**
- **Electrochemical**
- **High Frequency**

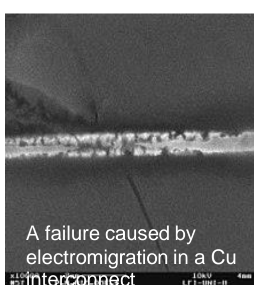
Electromigration

Movement of atoms based on the flow of electrical current through a material

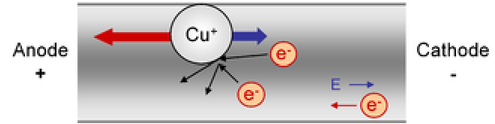
- ‘vacancies’ and ‘deposits’

Black’s Equation: MTTF= $CJ^{-n}e(Ea/kT)$ where

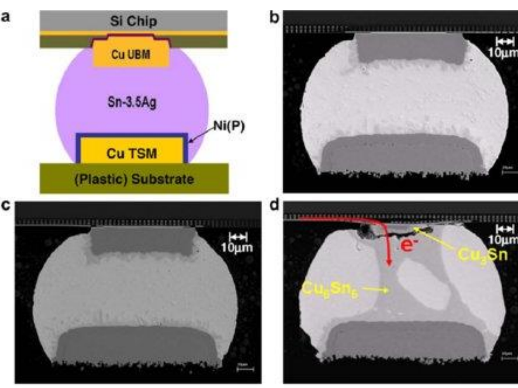
- *C= a constant based on metal line properties;*
- *J = the current density;*
- *n = integer constant from 1 to 2*
- *T = temperature in deg K;*
- *k = the Boltzmann constant; and*
- *Ea = Activation Energy*


A failure caused by electromigration in a Cu interconnect

- Cu or Al interconnects: 10^6 to 10^7 A/cm^2
- Solder joints (SnPb or SAC): 10^4 A/cm^2
- Bi has high propensity for electromigration & segregation -- potentially brittle solder joints

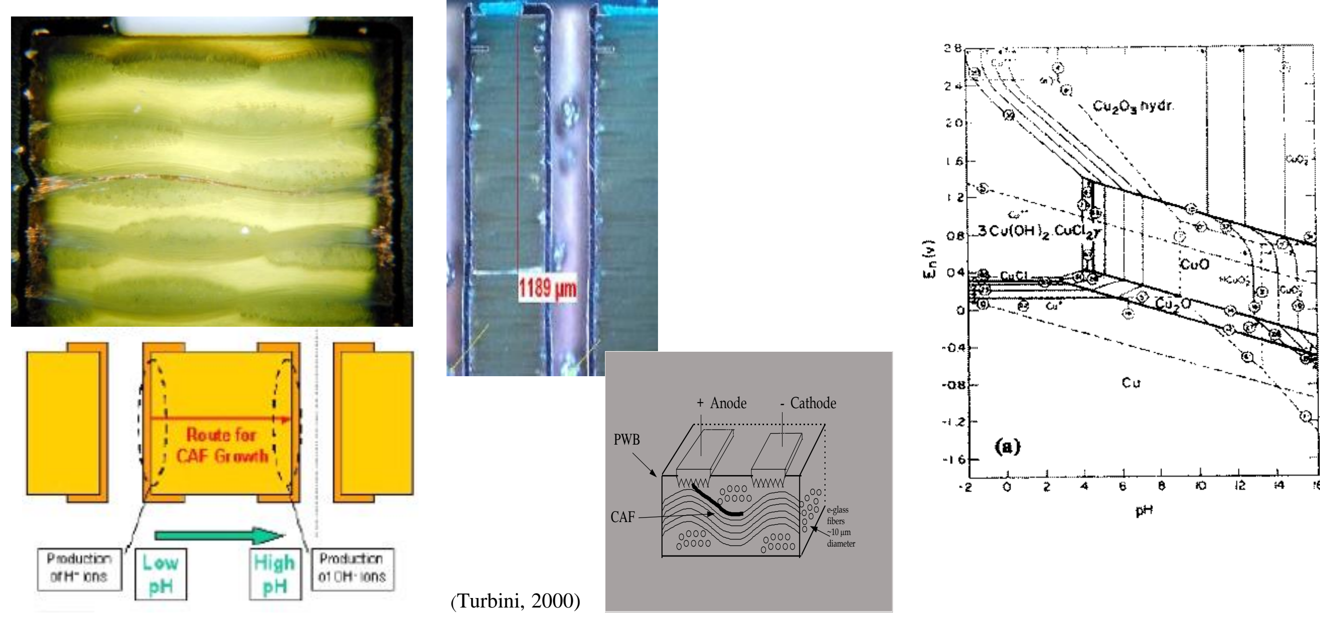


Electromigration (red arrow) is due to the momentum transfer from the electrons moving in a wire



(a) Schematic of a solder bump prior to current stressing, (b) intact solder structure, (c) control sample subject to aging but not current stressing for 300 h, and (d) solder bump subject to current stressing of 5.16 Â 10 4 A/cm 2. (S-H Chae)

Conductive Anodic Filament (CAF)

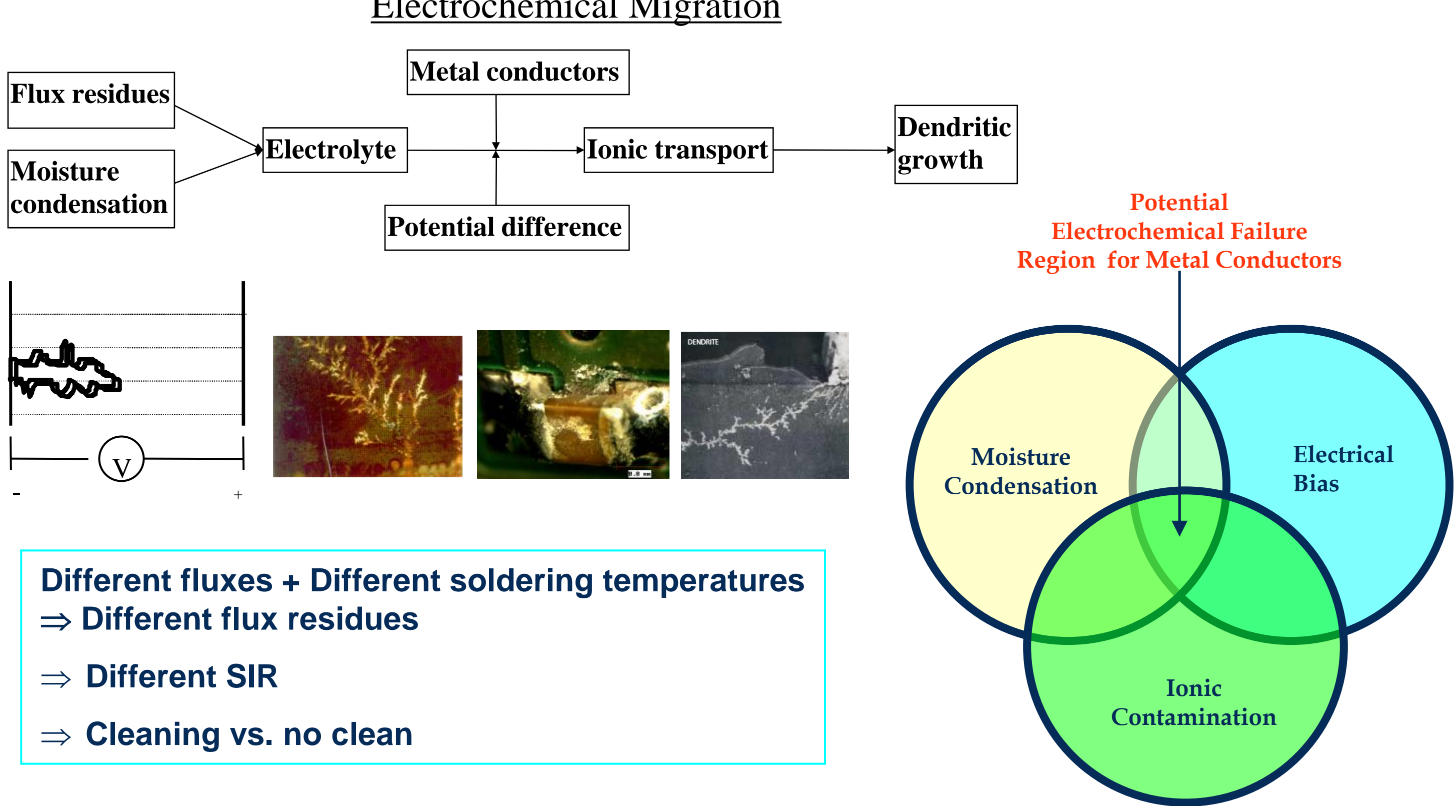


… a conductive filament forms in the substrate along the epoxy resin / fiberglass interface

$Cu_2(OH)_3Cl$ - semiconductor

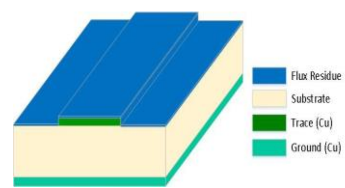
(D. Shangguan)

Electrochemical Reliability



High Frequency:
Signal Integrity vs. No-Clean Residue

No-clean flux residue can provide an alternative path to signals at high frequency



Microstrip with solder flux residue

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+\frac{10}{u}\right)^{-a.b}$$

$u = W/H$ is the trace width to substrate height ratio

$$a = 1 + \frac{1}{49} ln\left[\frac{u^4+(u/52)^2}{u^4+0.432}\right] + \frac{1}{18.7} ln\left[1+\left(\frac{u}{18.1}\right)^3\right]$$

$$b = 0.564\left[\frac{\varepsilon_r-0.9}{\varepsilon_r+3}\right]^{0.053}$$

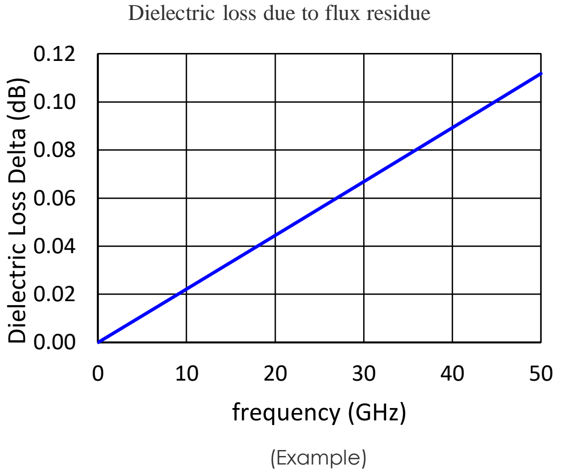
Length (L)	254.000	(mm)
Width (W)	0.406	(mm)
Thickness (T)	0.046	(mm)
Height (H)	0.178	(mm)
ε_r	3.000	
tan (δ)	0.0017	

(Example)

$$\varepsilon_{eff}(T) = \varepsilon_{eff} - \frac{(\varepsilon_r-1)(T/H)}{4.6\sqrt{W/H}}$$

$$d(f) = 27.3L\frac{\varepsilon_r\left(\varepsilon_{eff}(f)-1\right)\tan\delta}{\sqrt{\varepsilon_{eff}(f)}(\varepsilon_r-1)\,C/f}$$

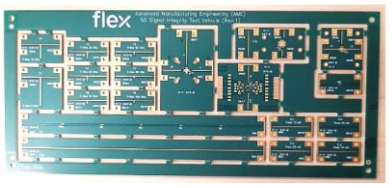
Dielectric loss due to flux residue



(Example)

(Shangguan et al, IEEE Trans. 2020)

Signal Integrity vs. No-Clean Residue

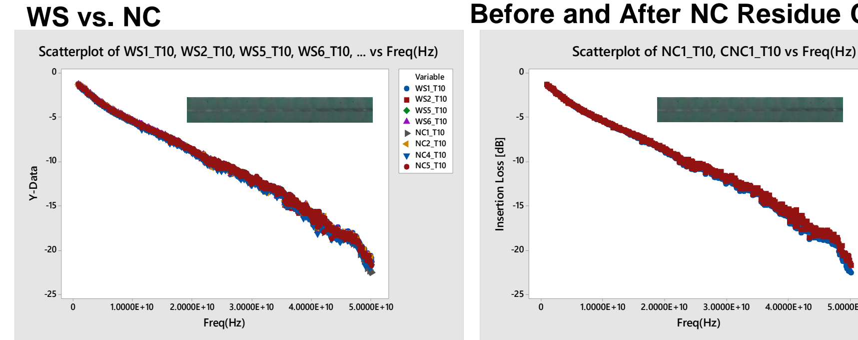


Vector Network Analyzer (VNA)
Up to 50GHz

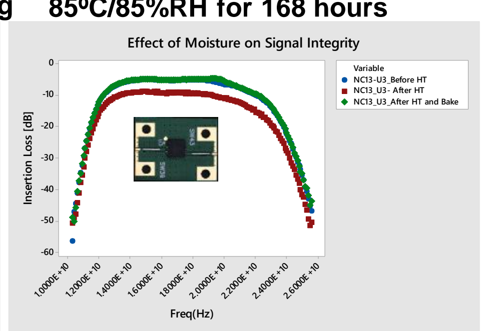
Example of a Device Under Test (DUI)

WS vs. NC

Before and After NC Residue Cleaning



85ºC/85%RH for 168 hours



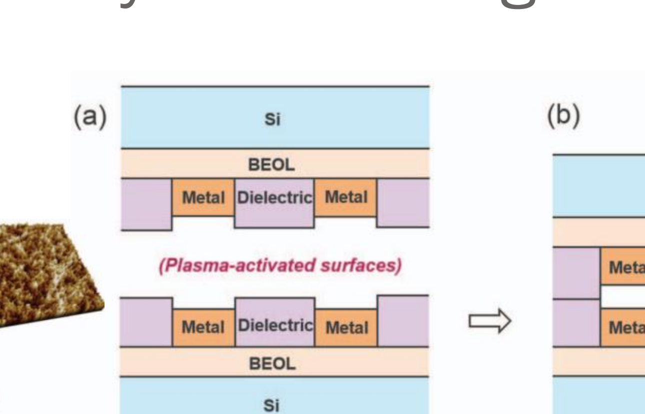
- The effect of no-clean residue on signal performance was relatively small as compared to other variables such as frequency, design and moisture
- Higher frequency can result in higher loss, depending on the component design. Wider trace would help to lessen the signal loss when the product operates at high frequency
- Moisture can be a critical factor resulting in high signal insertion loss and affecting the signal integrity performance

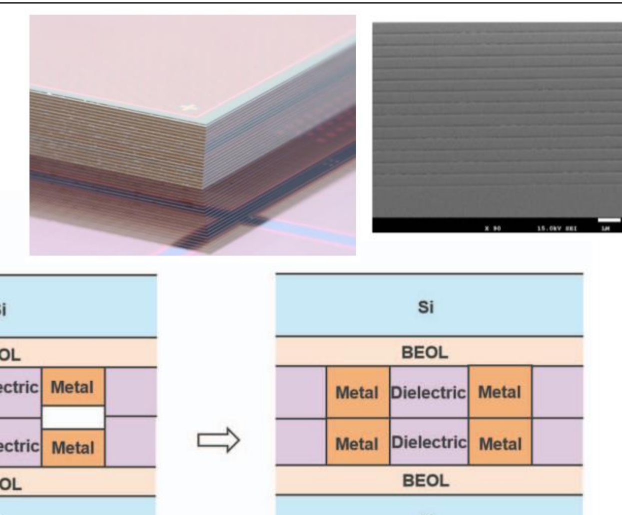
Signal integrity more sensitive to flux residues at higher frequencies

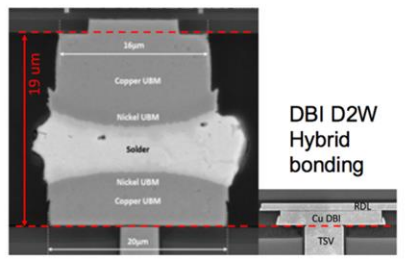
(Shangguan et al, SMTAI 2003; SMTAI 2019; IEEE CPMT Trans. 2020)

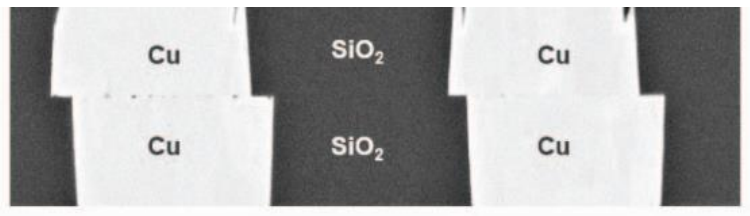
Direct Cu Interconnects: Hybrid Bonding

Hybrid Bonding







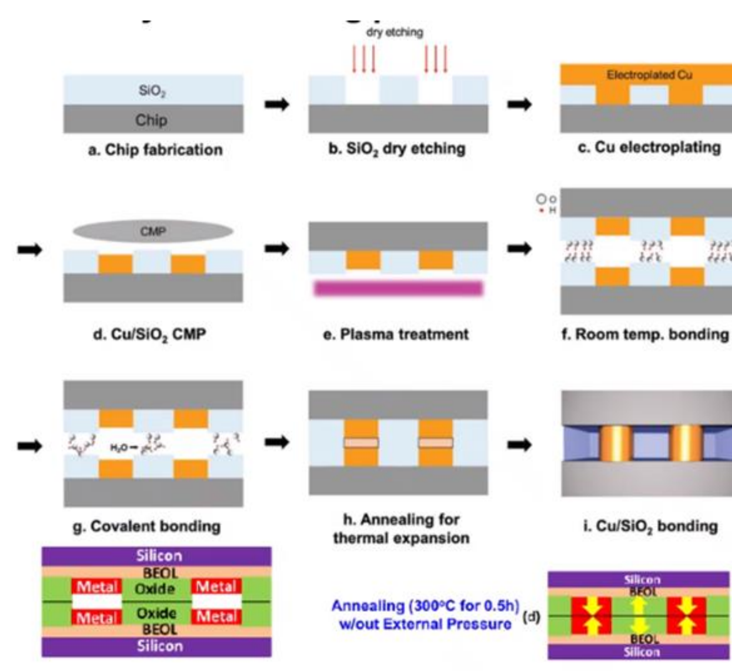


(Xperi)

Hybrid Bonding

<u>Critical factors for yield & throughput</u>

- CMP: flat, clean, dishing control
- Dielectric materials
- Cu microstructure
- Dicing
- Warpage
- Alignment
- Thin wafer handling
- Cleanliness
- Metrology



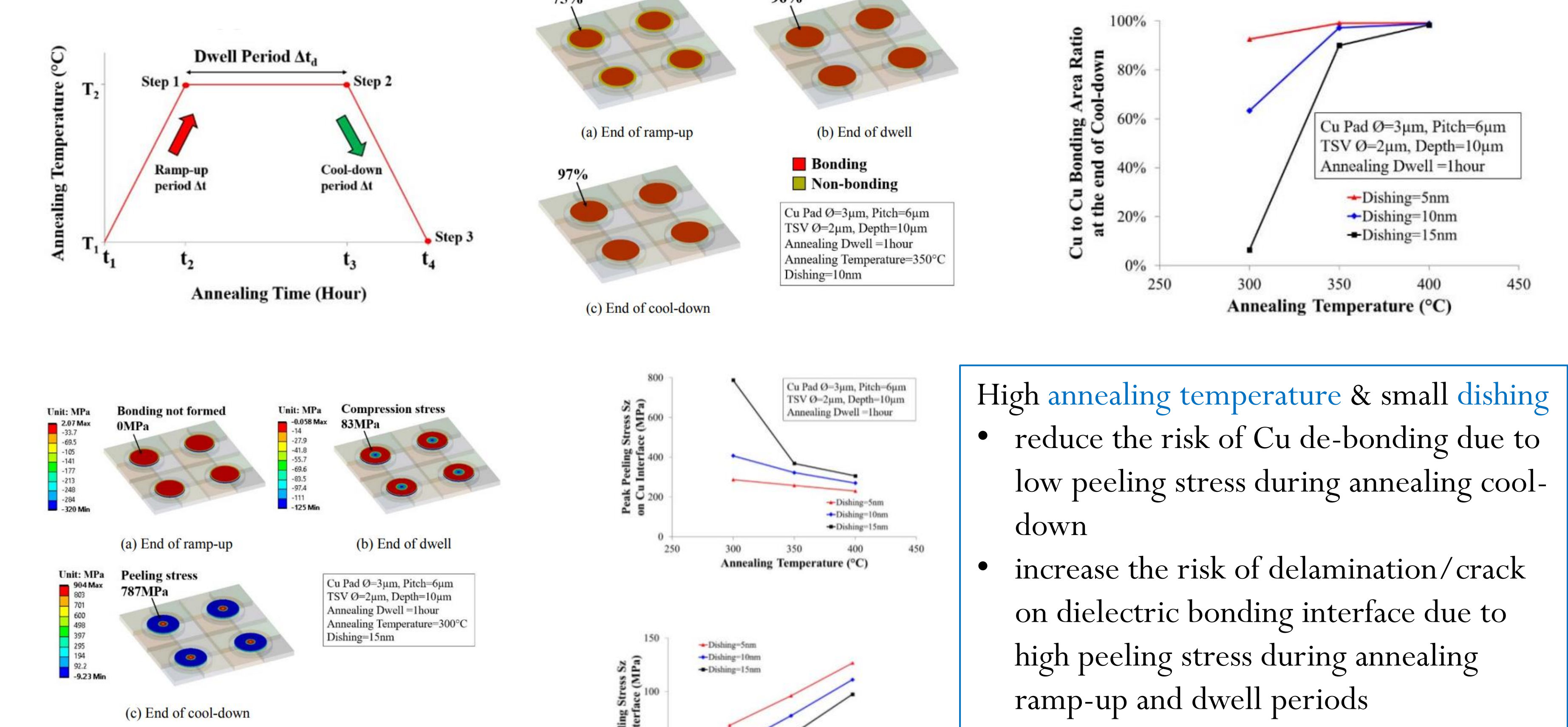
Picture Source: Park, J., Kang, S., Kim, M.E., Kim, N.J., Kim, J., Kim, S. and Kim, K.M. (2023), Advanced Cu/Polymer Hybrid Bonding System for Fine-Pitch 3D Stacking Devices. Adv. Mater. Technol. 2202134.

Hybrid Bonding: Reliability

Potential Reliability Threat	Degradation
Moisture ingress	Cu corrosion → high-resistance interconnect → open circuit Large leakage current → lower TDDB performance → dielectric breakdown
Thermomechanical stress	Delamination (Cu/Cu, Cu/dielectric) Leakage current High-resistance interconnect → open
Electromigration	High-resistance interconnect Open
Copper diffusion	Large leakage current → lower TDDB performance → dielectric breakdown
Dielectric breakdown	Large leakage current TDDB

Robustness and reliability (at pitches>1μm):
- Similar to BEoL interconnect

(Moreau et al, ECS Journal of Solid State Science & Technology, 2022)



High annealing temperature & small dishing

- reduce the risk of Cu de-bonding due to low peeling stress during annealing cool-down
- increase the risk of delamination/crack on dielectric bonding interface due to high peeling stress during annealing ramp-up and dwell periods

(A*STAR)

Process optimization is critical

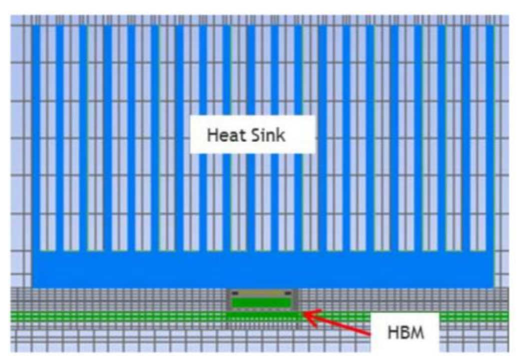
Hybrid Bonding - Reliability

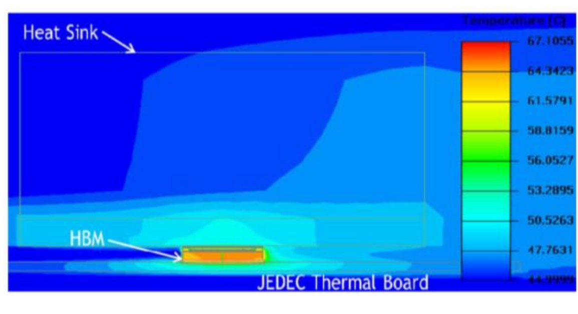
Test	Standard	Test Condition	Sample Size	Test Duration	Results	Resistance Change
Temp. Cycling	JESD22-A104D Condition M	-40°C to 150°C, 1000 cycles.	45	2000 cycles	45/45 pass	1.5% to 3.4% drop
High Temp. Storage	JESD22-103D	225°C, 1000 Hours	22	2000 hrs	22/22 pass	1.2% to 2.0% drop

(Xperi)

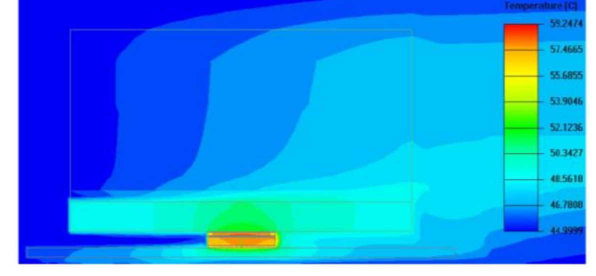
- Both the high temperature storage and the temperature cycling showed superior reliability
- No voiding induced by intermetallic growth during high temperature storage
- No Cu oxidation at high T - Cu interconnect completely shielded from the environment by the surrounding oxide, so is not a problem
- High T improved joint quality by further Cu diffusion across the bond interface

Hybrid Bonding – Thermal





Micro-bump stack (w/ underfill)



Cu-Cu direct bonding

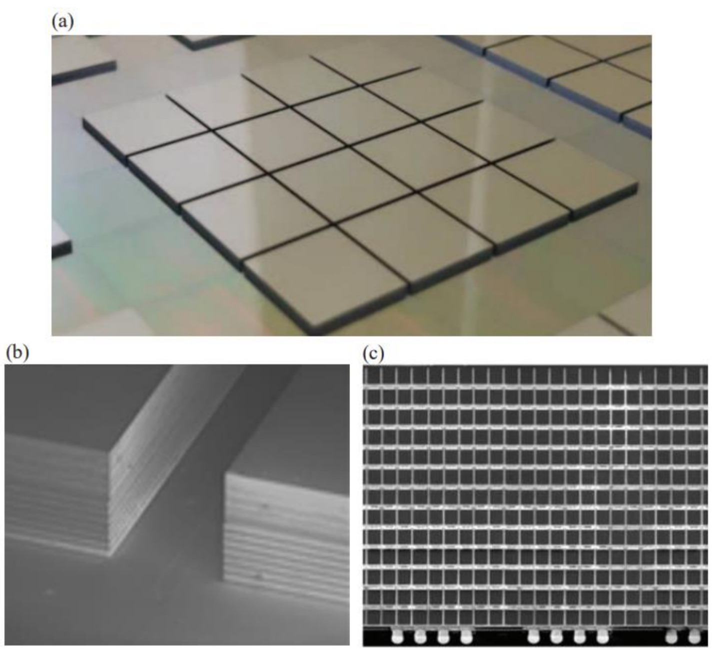
4 die stack HBM, w/ forced convection (3m/s air velocity)
Ambient temperature 45^0C, Operating power 2W on each die

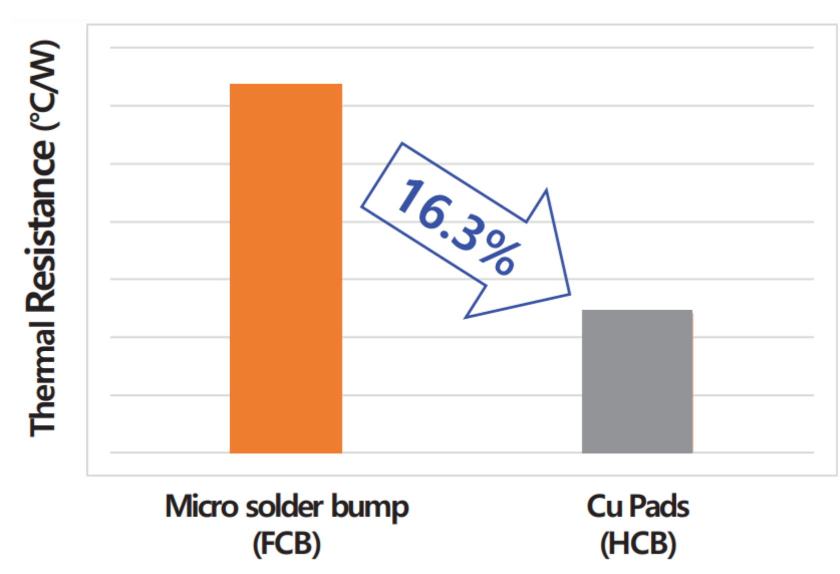
Hybrid bonding

- Lower Tj
- Reduced ΔTj (hottest/coolest)

(Xperi)

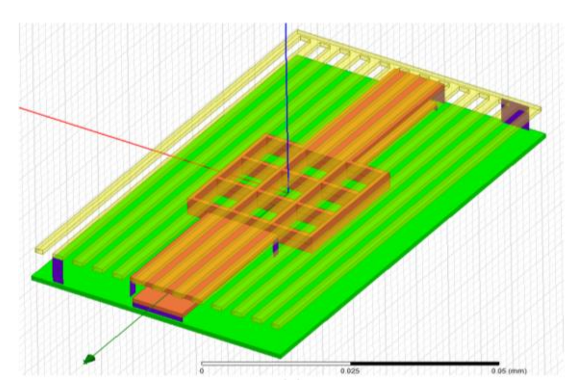
Hybrid Bonding – Thermal

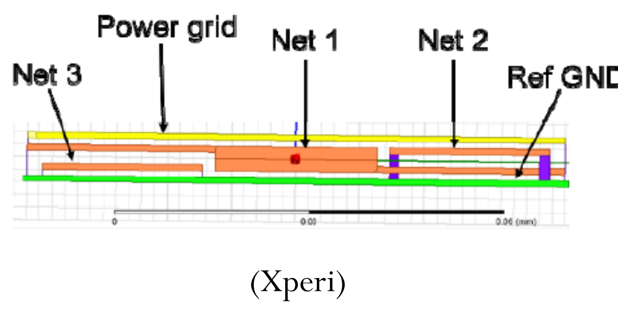




(Samsung)

Hybrid Bonding – Electrical

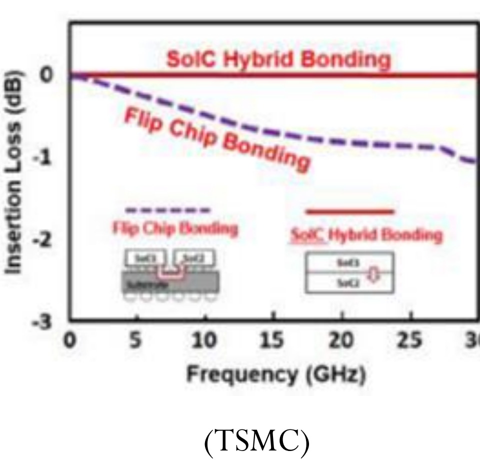




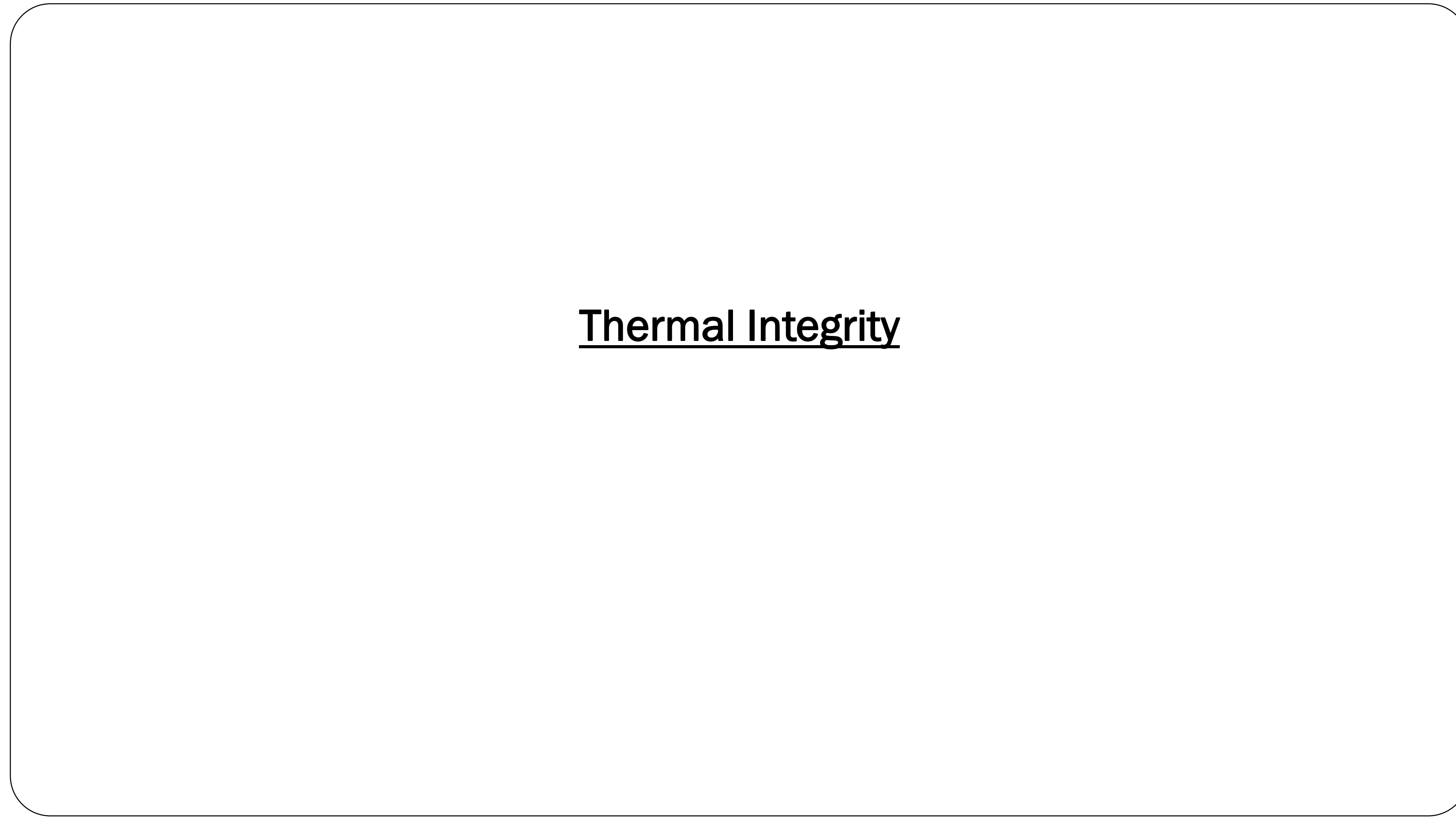
(Xperi)

As compared with TCB:

- Reduced parasitic capacitance
- Smaller insertion loss

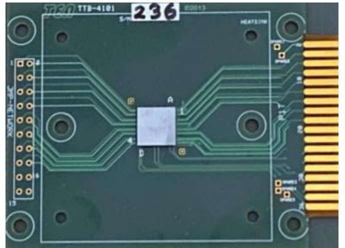
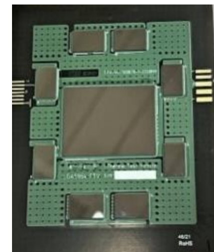


(TSMC)


Thermal Integrity

Thermal Test Chips: Thermal Twin for Thermal Integrity

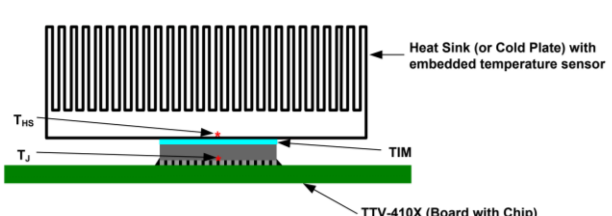
- Any chip size - Embedded metal resistor heaters and temperature sensors in directly addressable Unit Cells
  - Configurable “hot spots” & integrated temperature sensors – at Unit Cell level (1x1mm, 2.54x2.54mm)
  - Uniformity, consistency, stability, precision, scalability; Conforms to JEDEC JESD51-4
- Thermal Test Chips, Thermal Test Vehicles, Thermal Load Boards
  - Various packaging formats (FC or WB; COB, BGA, LGA, multi-chips, FO, stacked/3D, …)
  - Integrated with thermal management solutions
- Instrumentation and thermal measurement system
  - Power cycling

Thermal Test Chip
Underfill
Flip Chip Bumps
Package Substrate
Ball Contacts

TEA Thermal Engineering Associates

Made in America



Summary

Packaging

Miniaturize the interconnect

+

Ensure its reliability

= PPACRS

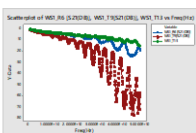
- **P**erformance
- **P**ower
- **A**rea
- **C**ost
- **Reliability**
- **Sustainability**

(D. Shangguan)

Reliability vs. Miniaturization

- **Smaller solder interconnects – more susceptible to thermomechanical failures**
- **Higher current density – electromigration**
- **Tighter spacing**
  - **Solder extrusion; Whiskering; α particle emission (^{210}Pb, ^{214}Bi, …)**

- **Importance of the interface**
  - **As the solder volume decreases - Interfacial IMC's**
  - **Interfacial thermal resistance**
- **Heterogeneous integration and diversity of packaging methods (devices, materials, interfaces) in the same module**
  - **More complex (often interactive) reliability failure modes and mechanisms**
- **Process yield**
  - **Voids, …**



- **Electrical: Signal integrity – cross talk, EMI……in the 5G era**
- **Thermal integrity**

(D. Shangguan)

Reliability of Electronics Systems

Electronics Reliability = Chip (Transistor + Interconnect)

\+

Interconnect (chip level + package level + system level)

- **A variety of environmental/loading conditions and associated failure modes and mechanisms**
  - **Thermomechanical, mechanical, chemical, electrochemical, electromigration, materials degradation, radiation, ESD, UV, …**
- **Advanced packaging and heterogeneous integration present new complexities for reliability**
- **Reliability assurance demands holistic solutions**
  - **Design, processes, testing**
  - **Materials: High reliability solder, low temperature solder, ultra low residue flux, thermal interface materials, …**

(D. Shangguan)

Thank You !

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