Design-for-Test in 2D is hard! What can you expect for 3D?

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Motivation

Design-for-Test is always challenged by latest design complexities

- Today: AI Chips
- Example
  - ~1 GB of on-chip memory across >60k memory instances
  - 4000 Memory BIST controllers
  - 1200 Logic BIST controllers
  - 1500 Embedded compression logic test controllers
  - 2500 OCCs
  - 2000 Test mode control bits
  - 50 embedded 1149.1 TAP controllers
  - Loads of on-chip monitors and sensors
  - …

A single test setup might take 7-10M cycles at JTAG speed

Not counting actual test patterns

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Unfortunately, one driver for 3D are those high-demand designs

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Agenda

Requirements of multi-die (2.5D / 3D) DFT

State-of-the-art 2D DFT

Expanding into multi-die

Role of test standards, actual and industry published

Summary

Requirements of multi-die DFT

Ensure the assembled product is defect free

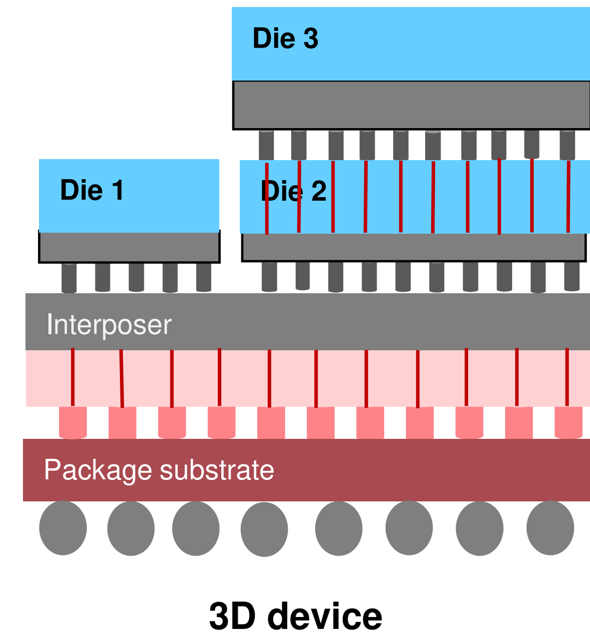
- Each 2D die (chiplet, tile, …) is defect free
- The 3D stack, 2.5D assembly is defect free

Cost considerations and trade-offs

- Known Good Die (KGD)
- Wafer-level die interconnect test
- Partial stack test
- Stack-level interconnect test & repair

- Reuse die-level DFT as much as possible for stack-level
  - Hardware and test patterns

- Allow heterogenous 3D integration also for DFT



3D device

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State-of-the-art 2D DFT What is important for 3D ?

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State-of-the-art 2D DFT – What is important for 3D ?

1. Test time
   - Test delivery to die
   - Test response off die
   - Diagnosis volume data collection, logic and memory
2. Test access
   - Wafer-level die IO access is very narrow

Narrow, high bandwidth interface at die IO

High bandwidth test distribution method on chip

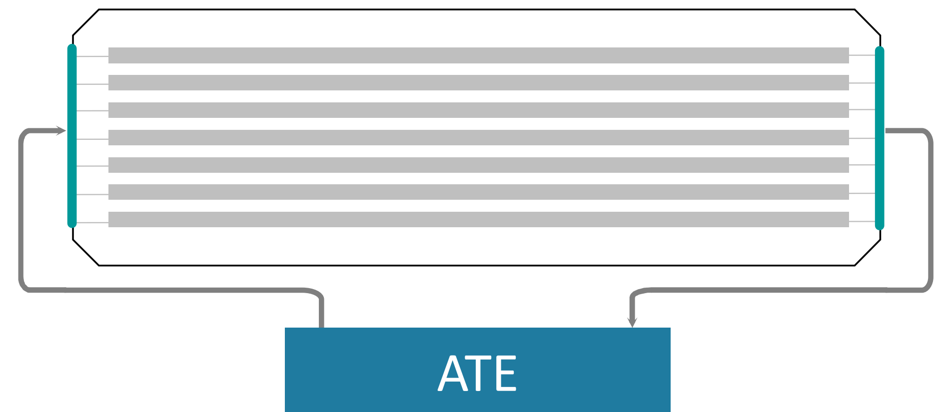
Configurable for wafer / package

3. Tool compute resources
   - Inability to represent the entire die in memory
   - Compute pattern once, map to die test access architecture

Hierarchical test methodology

Scan

- Developed to fully automate test pattern generation
- Necessary for debugging and diagnosis



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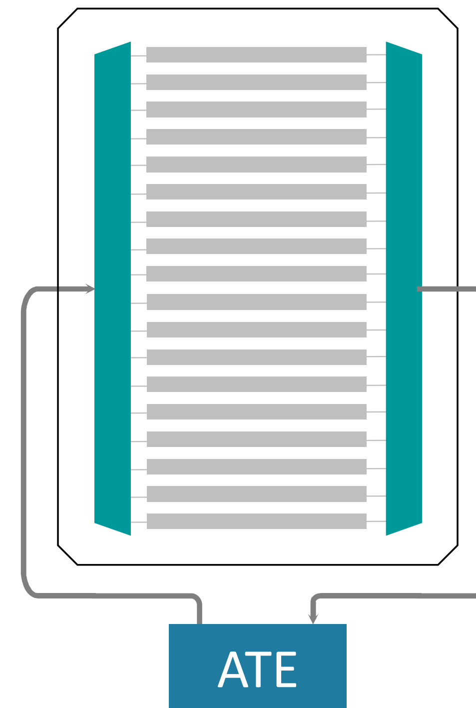
Test compression

- Developed to reduce the cost of test
- Two orders of magnitude reduction of test data volume and time
- Based on scan DFT



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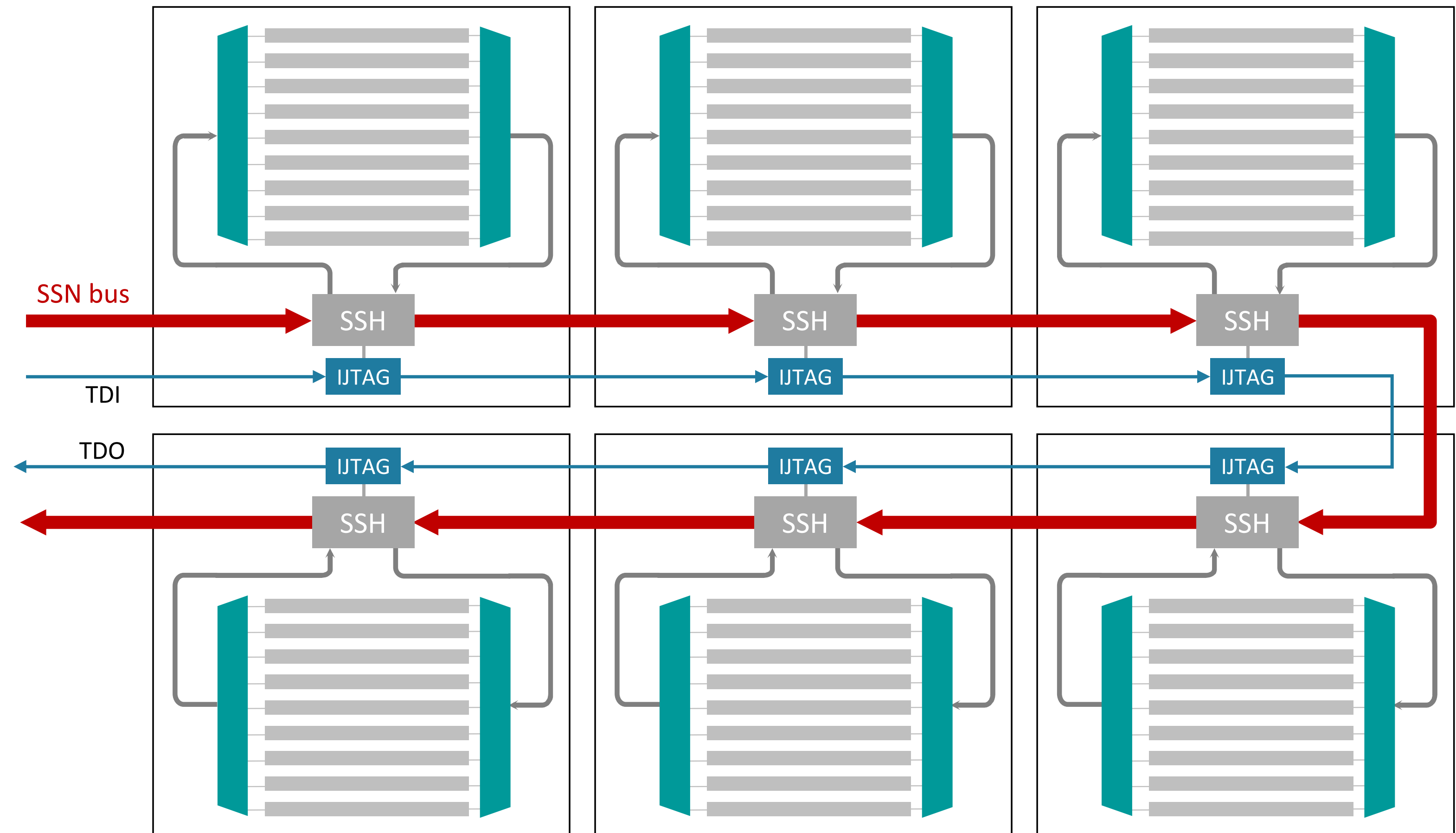
Streaming Scan Network (SSN)

SoC-level DFT

- Additional compression
- Identical cores
- Input-only streaming
- Reduced test time
  - 400 MHz
- Simplified DFT implementation
- More balanced power
- Universal streamer



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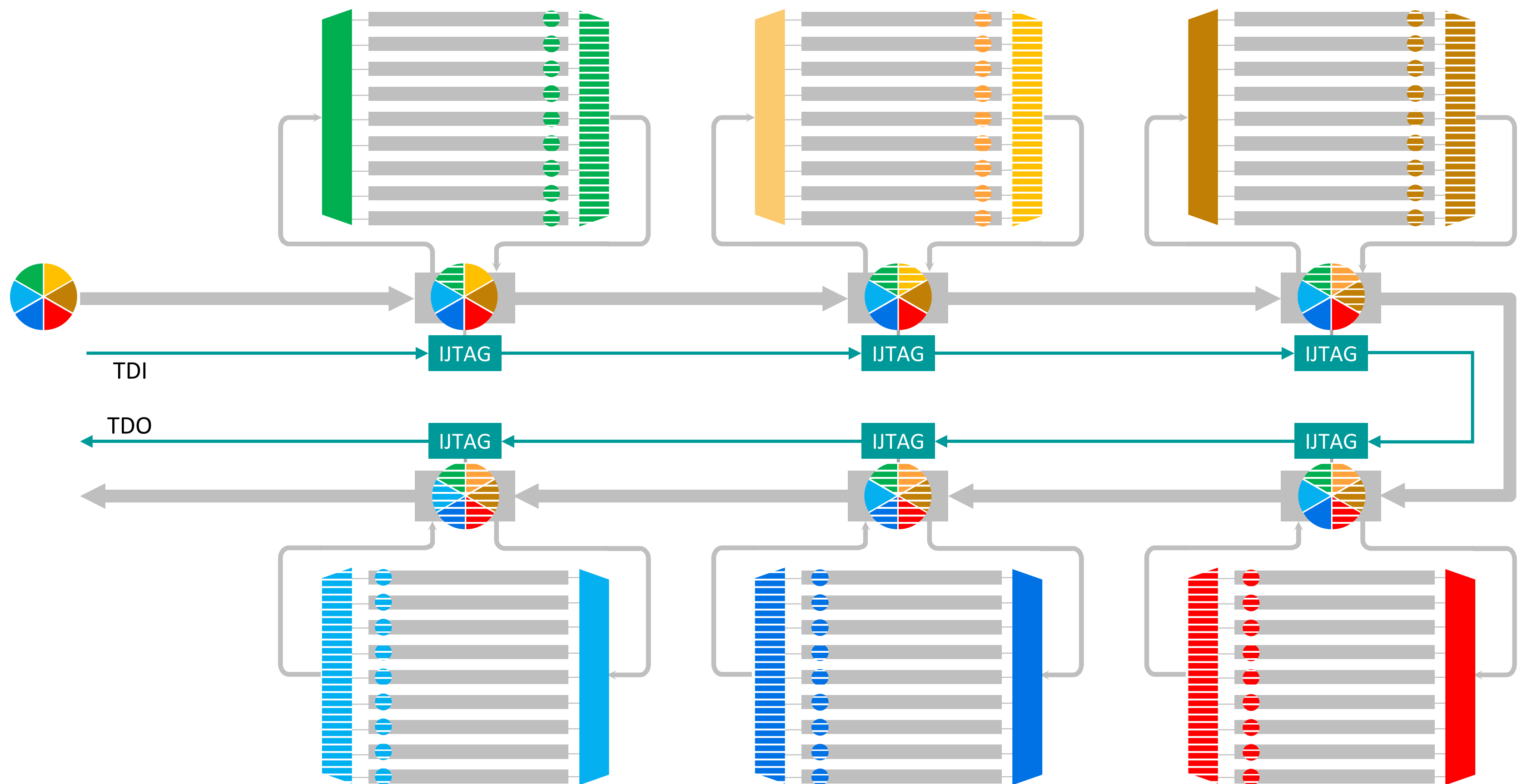
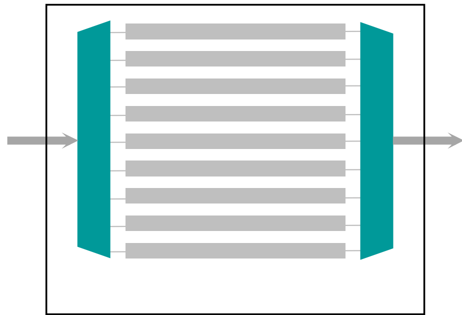
Packetized scan data distribution



Hierarchical DFT



- Patterns for cores
- Retargeted to SoC level
- Formed into packets
- Allows change of SSN bus width after the fact
- Adjusts to available wafer / package resources

SSN bus

SSN bus

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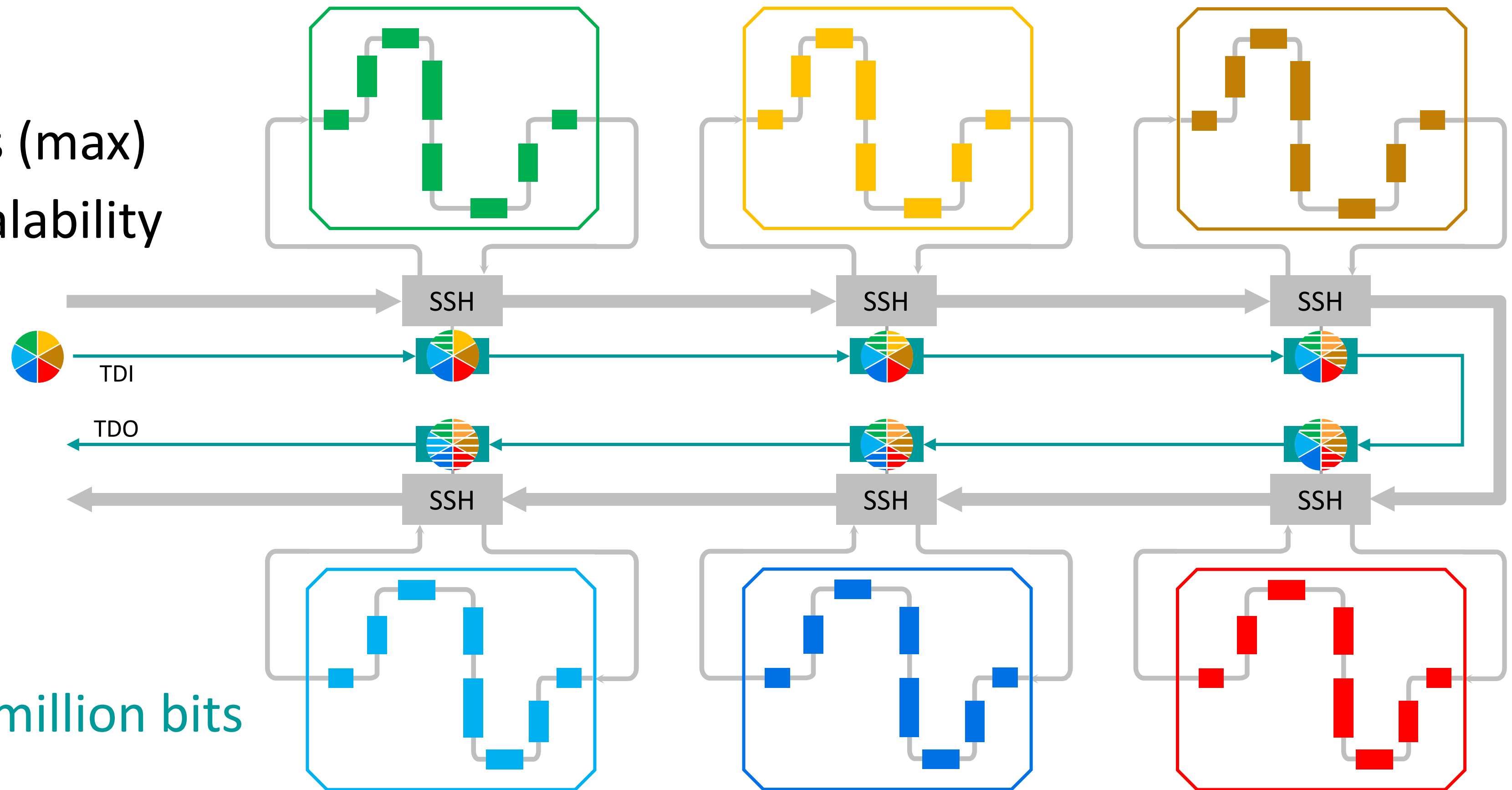
Standard IJTAG

- 1-bit bus
- 100 Mbit/s (max)
- Limited scalability
- Large SoC:
  - SSN
  - EDT
  - OCC
  - LBIST
  - MBIST
  - IJTAG
- Total: >10 million bits



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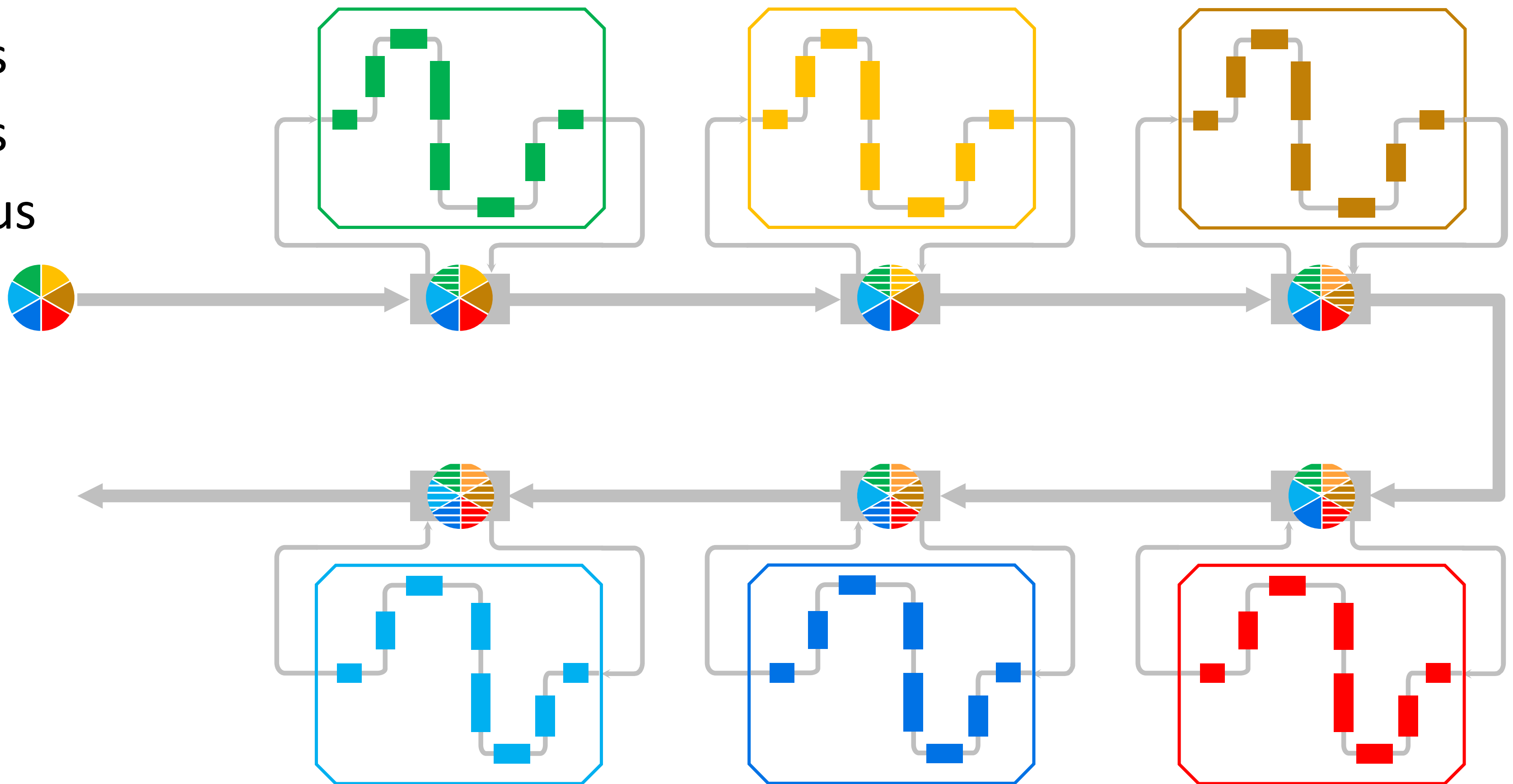
High-bandwidth IJTAG

- 32-bit bus
- 64-bit bus
- 128-bit bus
- …
- 400 MHz
- 12 Gbit/s



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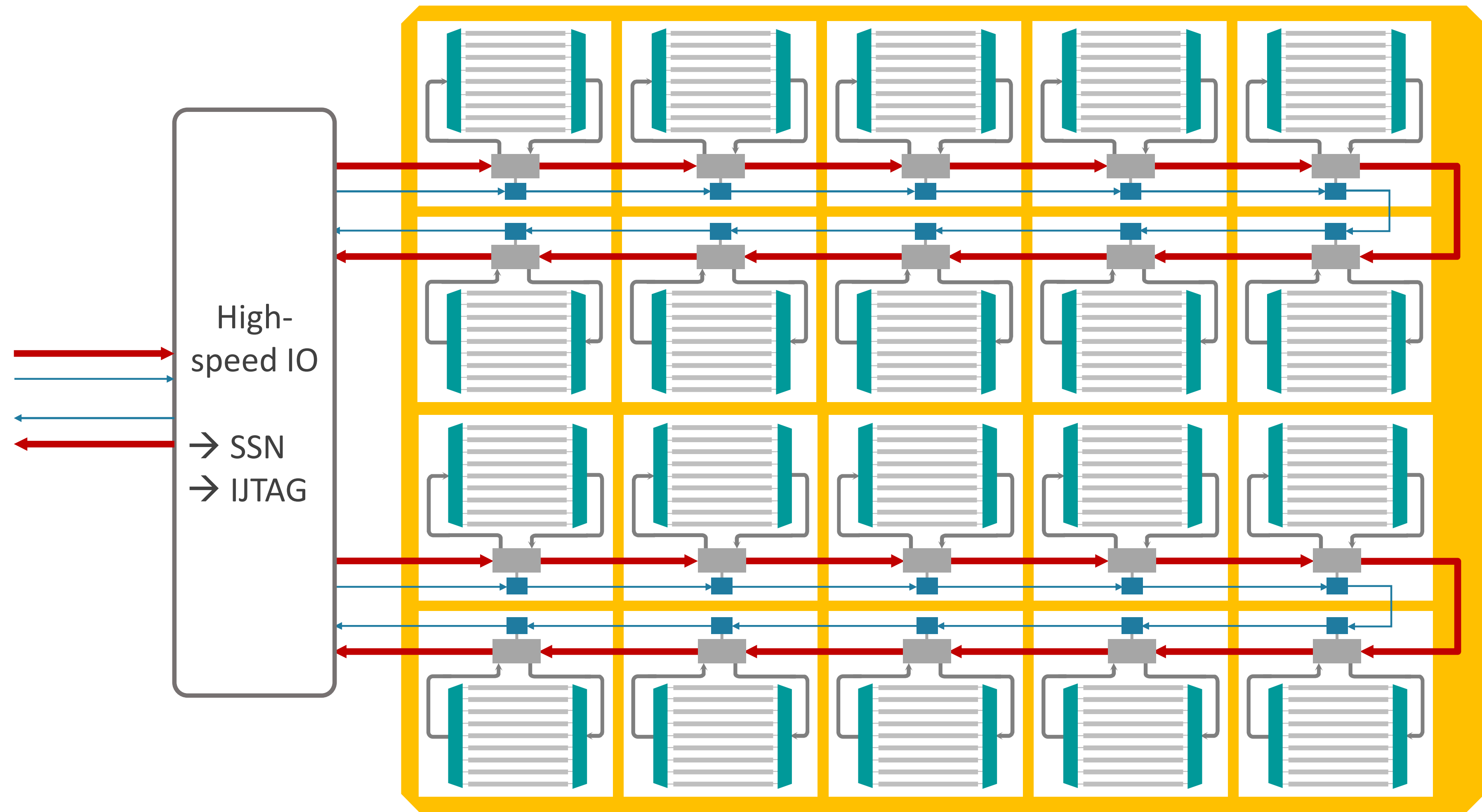
High-speed IOs



State-of-the-Art 2D DFT – What is important for 3D ?

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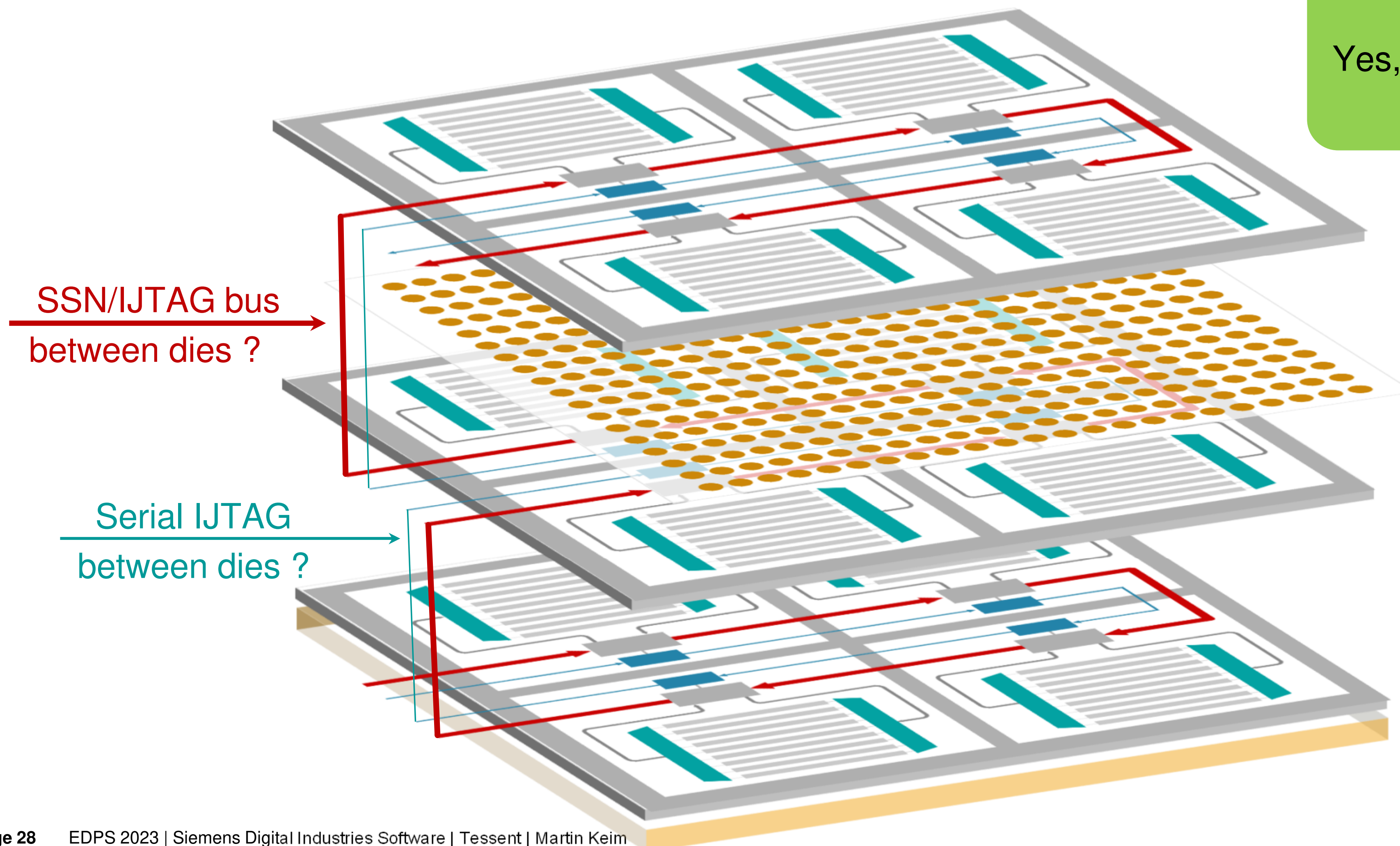
Full hierarchical test methodology

Expanding 2D DFT into 3D

So far …

Yes, but …



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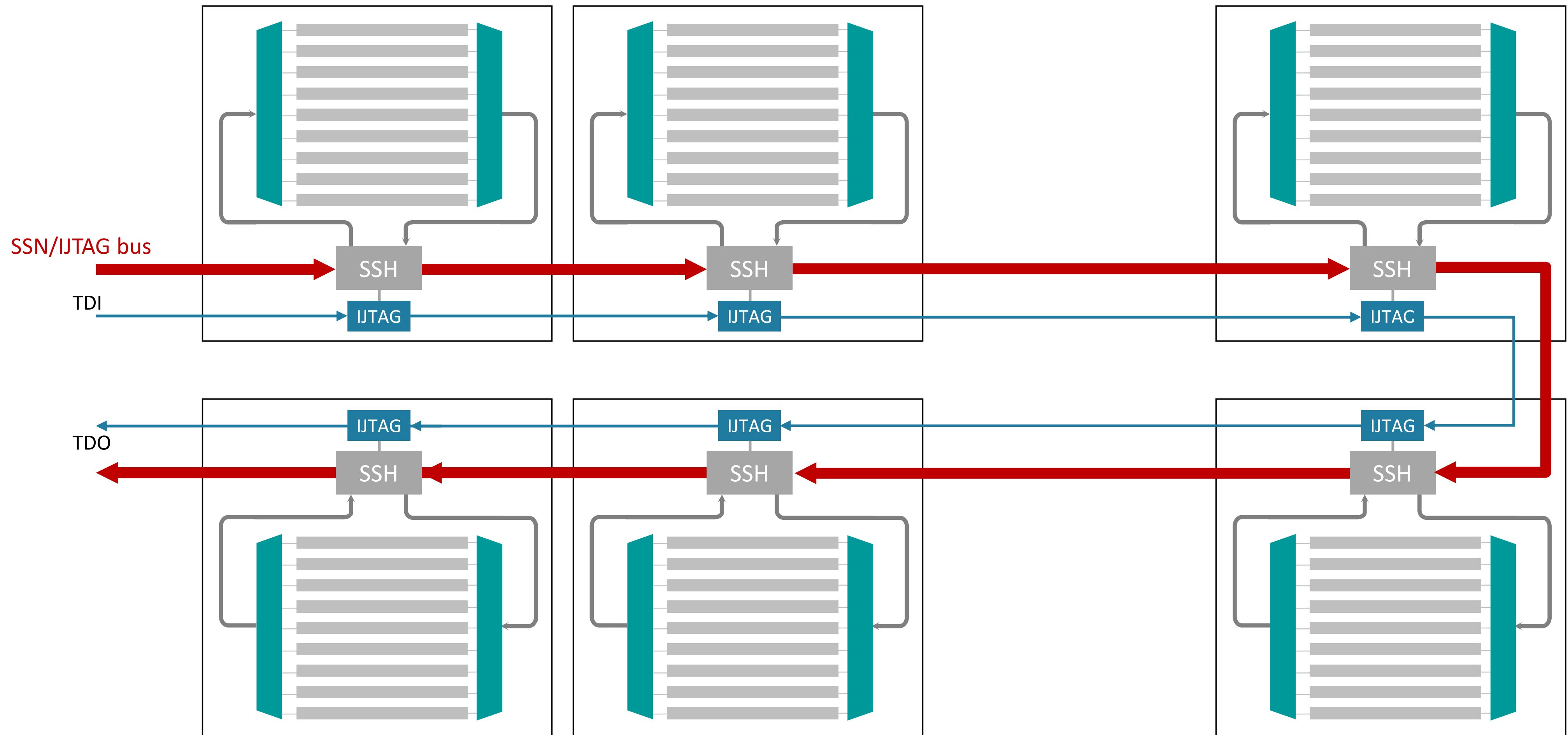
Streaming Scan Network easily expands to 3D



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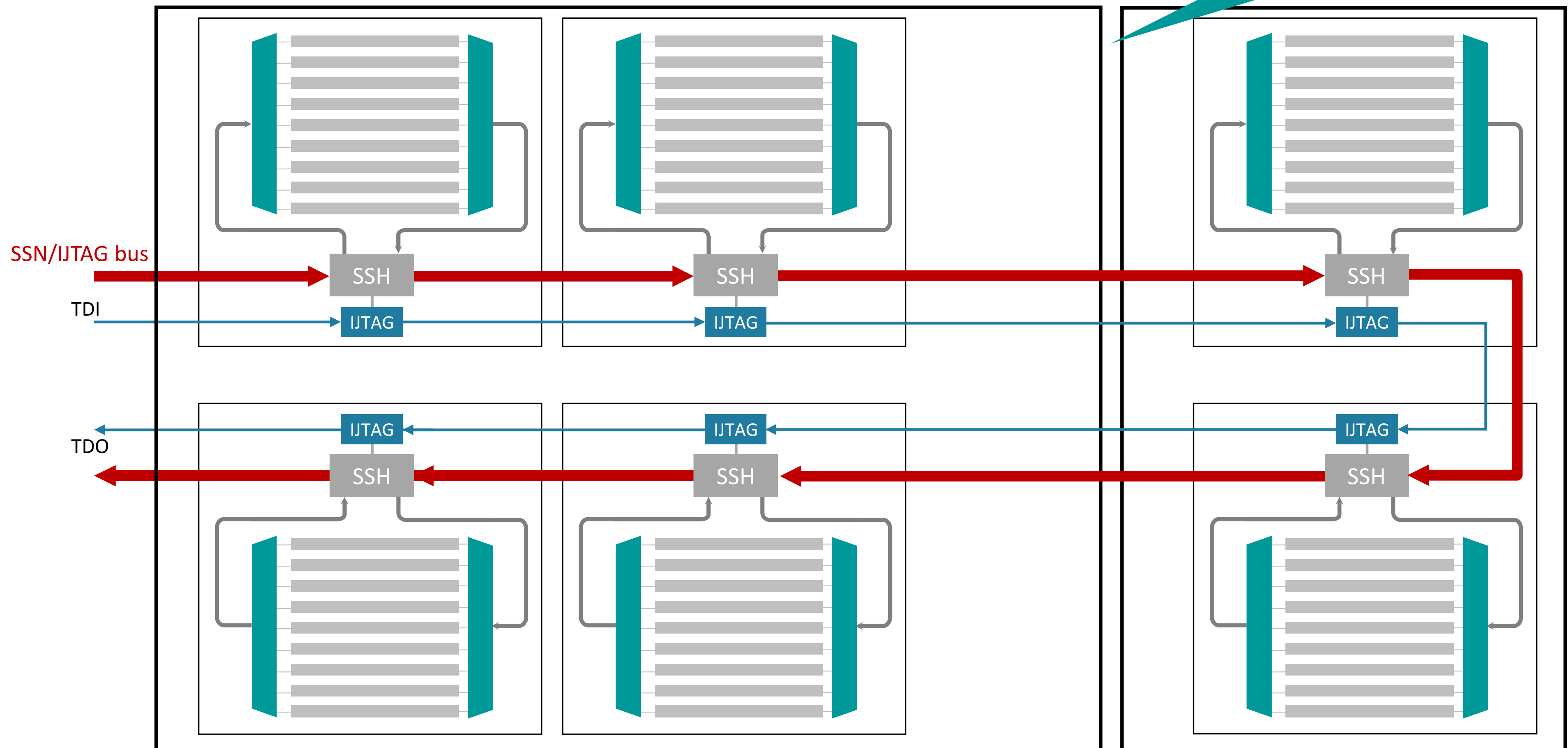

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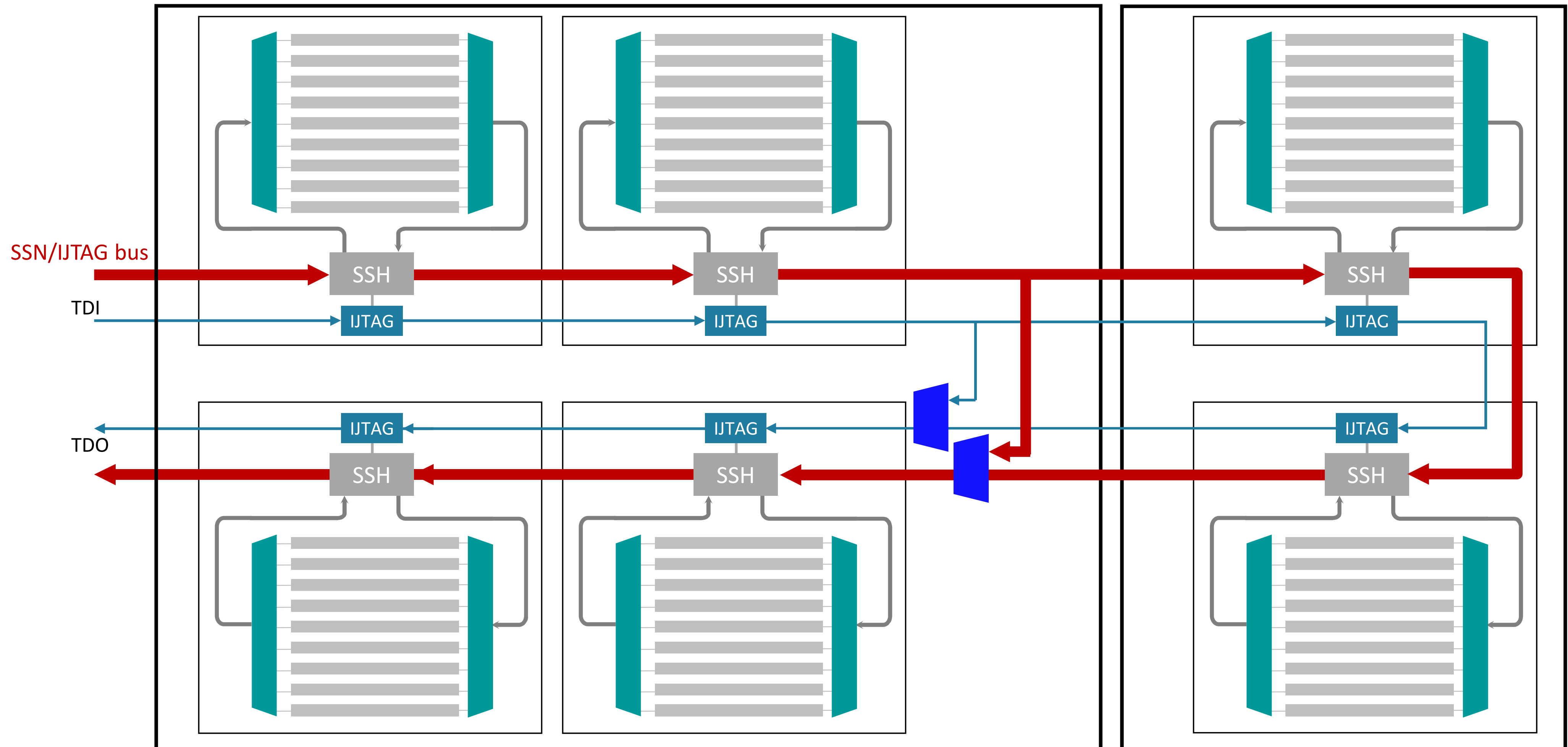
Streaming Scan Network easily expands to 3D



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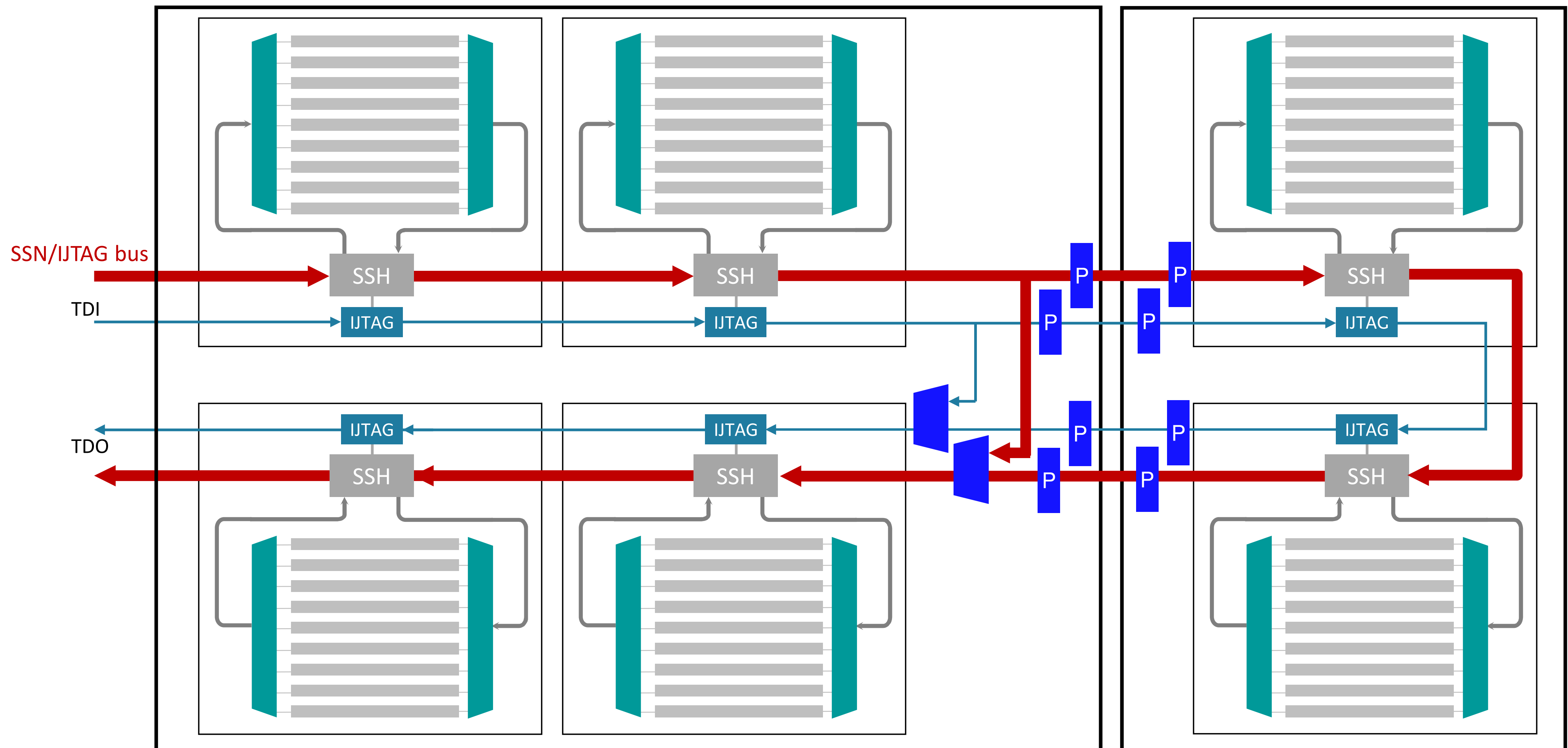
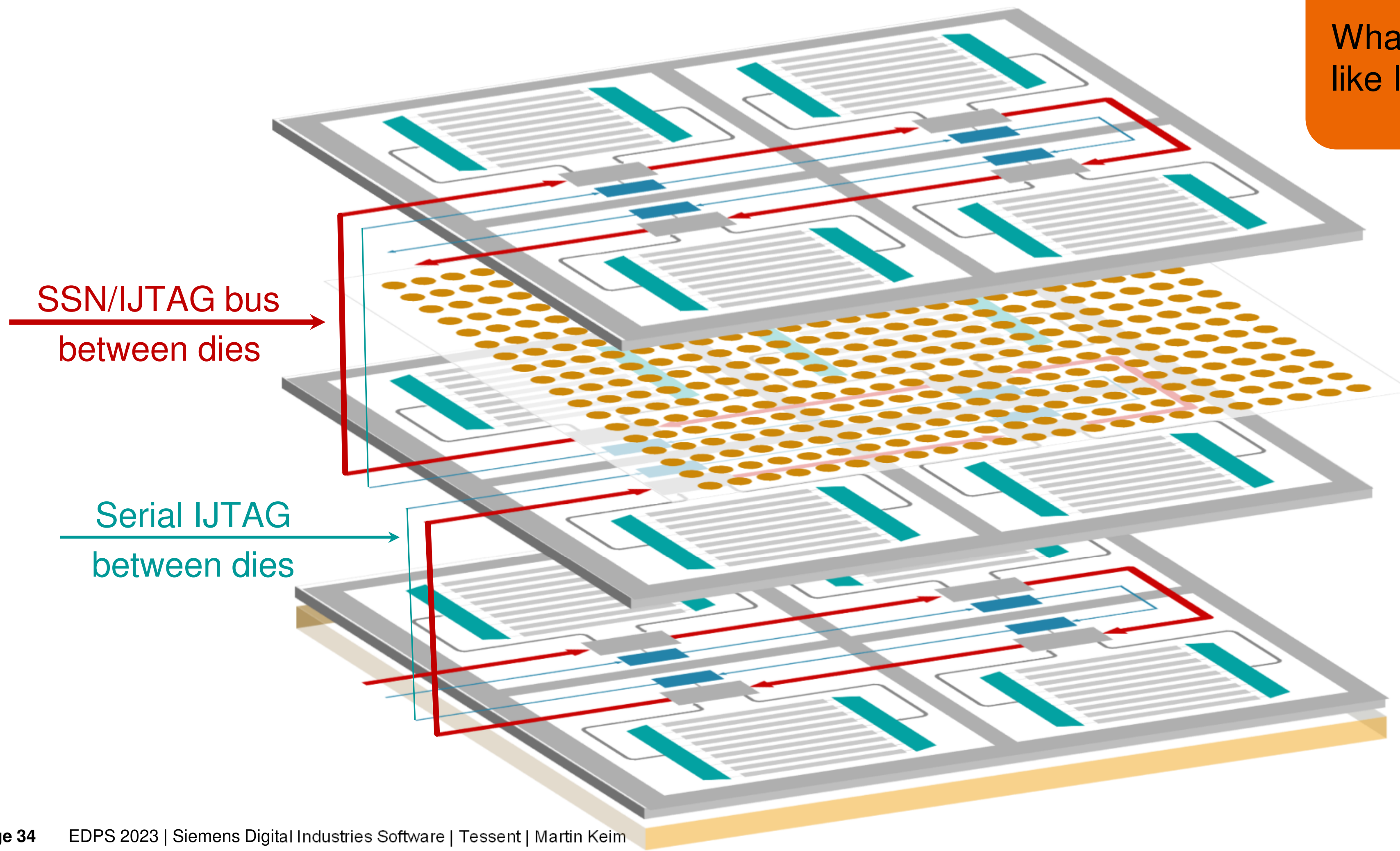
Streaming Scan Network easily expands to 3D



So far …



What about standards like IEEE 1838 ?

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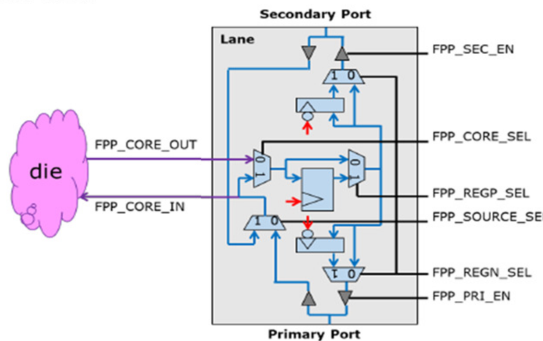
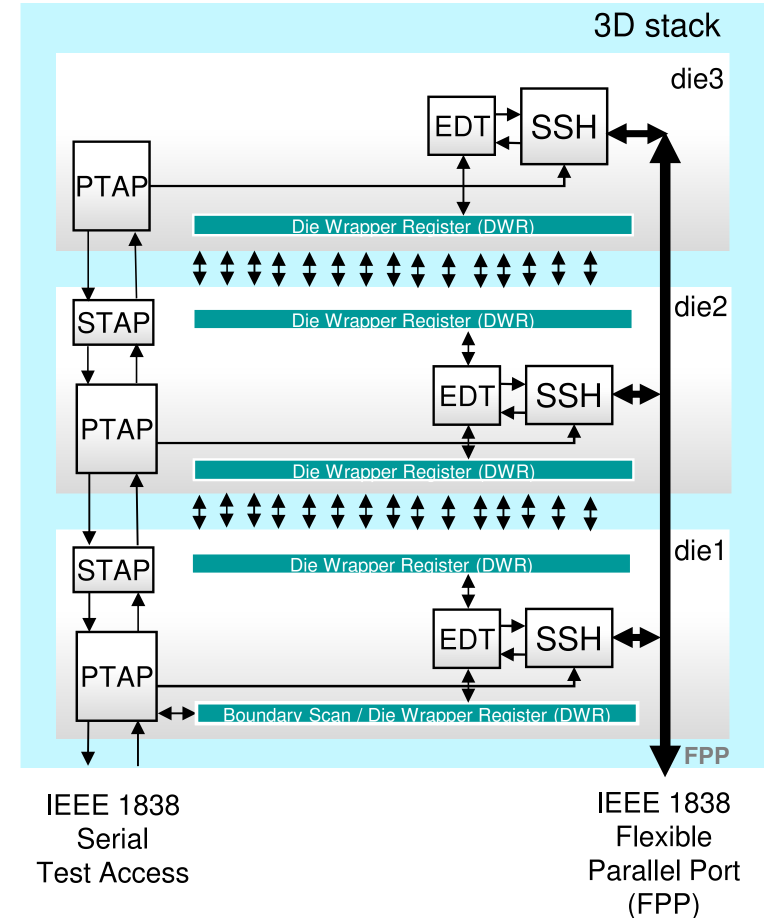
IEEE 1838 Standard

Test access architecture for three-dimensional stacked integrated circuits

- Hardware and protocol for control and data signal transportation
- **Required** serial test access via PTAP / STAP
  - Primary Test Access Port (PTAP) = 1149.1 TAP with 3D registers
  - Secondary Test Access Port (STAP) = to connect to the next die
  - One PTAP per die, one STAP per next die
- **Optional** Flexible Parallel Port (FPP)
- Die Wrapper Register (DWR)
  - Suggested usage die-to-die test



Flexible parallel port (FPP)



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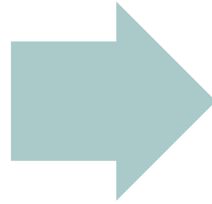
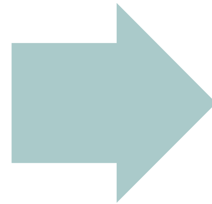
Implementing IEEE 1838

PTAP / STAP



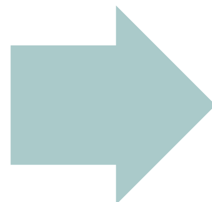
Compliant implementation through IEEE 1687 (slow, serial IJTAG usage)

FPP



Compliant implementation through Tessent SSN (scan patterns and high bandwidth IJTAG usage)

DWR



Core wrapper cells and chip wrapper cells build up the DWR

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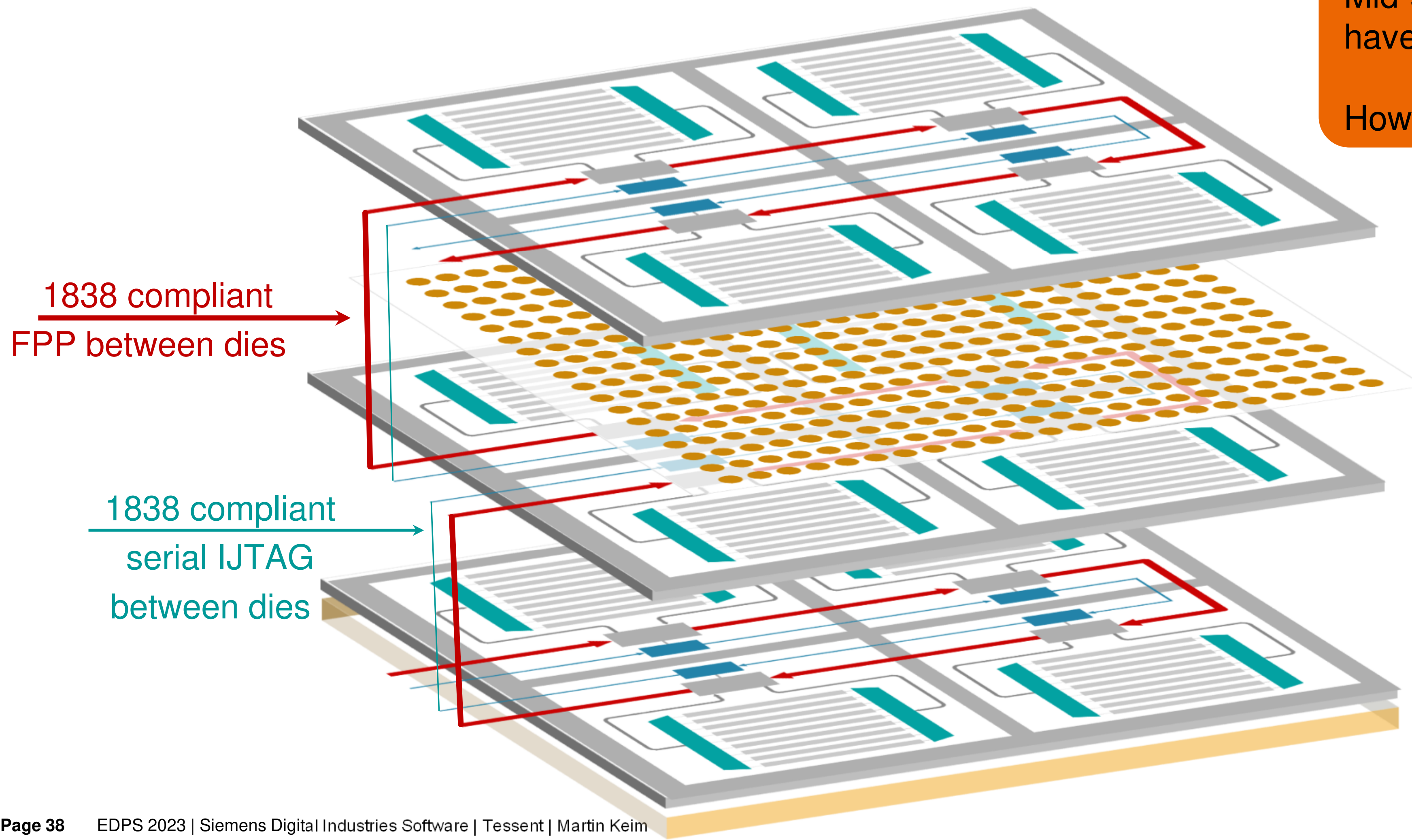
So far …

Mid-stack dies don’t have pads.

How to wafer-probe?



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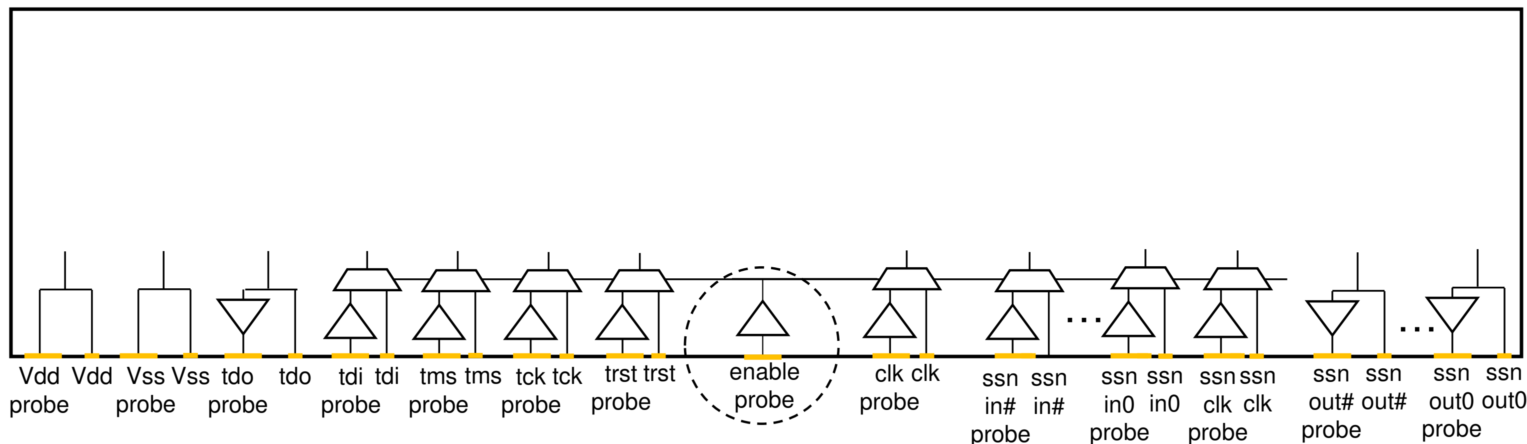
Wafer probe: Muxed probe pads

Microbump probe is difficult due to fine microbump spacing

Additional "sacrificial" probe pads with standard bump pitch

- Test IO’s, functional clocks, resets and sampling of power/ground for each supply
- Critical to have flexibility in number of test IOs (wafer vs. package)
- Without redo of the entire scan ATPG pattern generation

Probe Enable & multiplexer can automatically be added during DFT insertion



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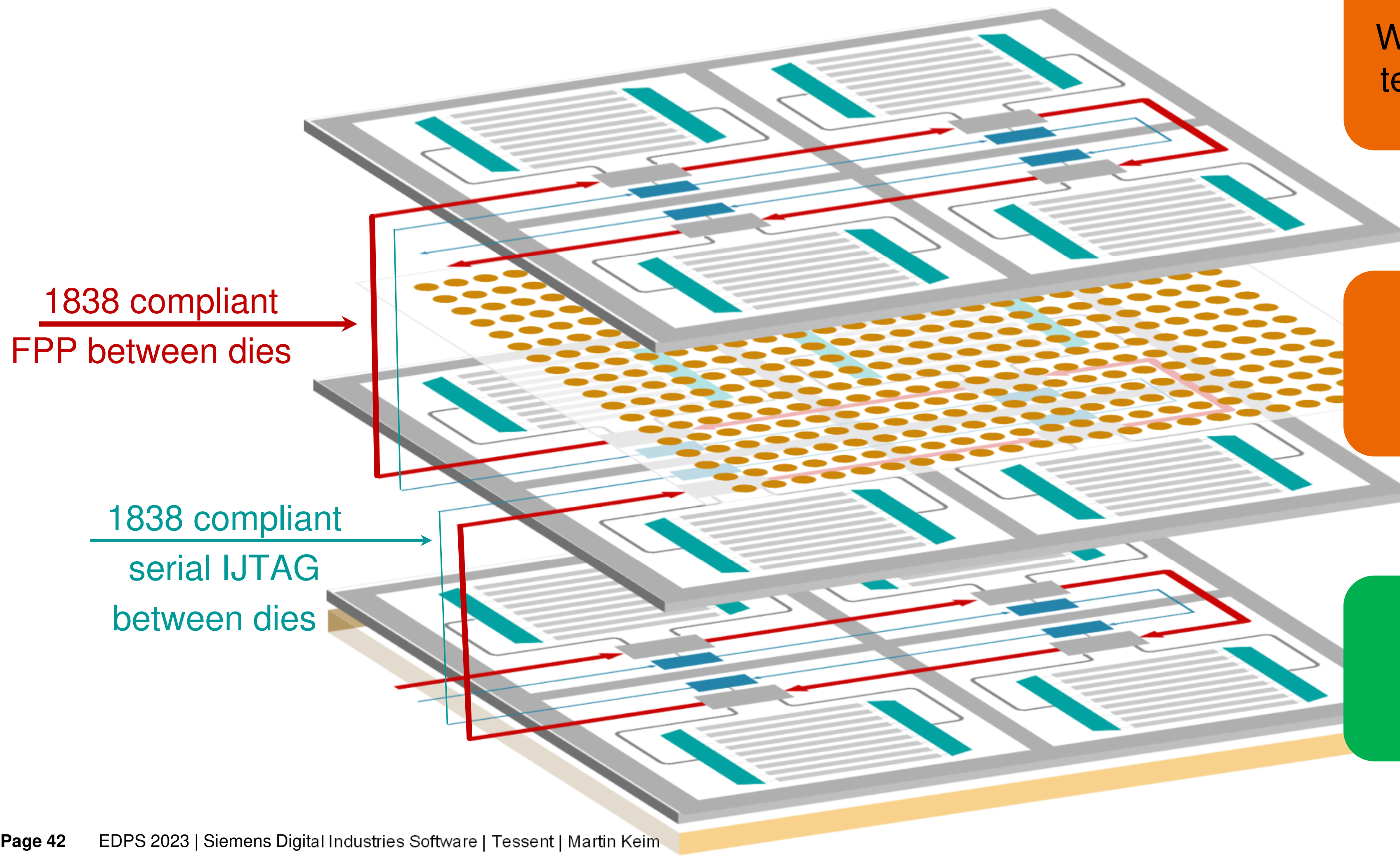
So far …



What about interconnect test at wafer and stack?

DFT has no standard solution (yet)

Only proprietary solutions exist

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Looking at test standards
Actual and industry published

IEEE Test Standards

1149.1-2001 / 2013 / 202x (JTAG) *

- Base for serial access
- 2013 expands to embedded IP

1500-2005 / 2022

- Embedded cores

1687-2014 / 2024 (?) (IJTAG) *

- Embedded IP
- Defines pattern (PDL) and hardware (ICL) description languages
- Retargeting through design hierarchy

1838-2019

- 3D assembly
- No test
- No information transfer language

P3405

- Die-to-die test & repair

P1838a

- Boundary Scan for Multi-Die devices

Industry making standards

Industry is filling in the gaps

- Design methodology
- Data exchange
- Die-to-die test, repair

Example: TSMC published their “3DBlox”

* : IEEE Standard currently under revision

Many, many interface standards

2.5D standards are emerging like UCIe

Most use a PHY with tests like:

- IP-specific tests, PLL/DLL tests
- DFT, scan, memory BIST, boundary scan

Many support 1000's of IO's between dies

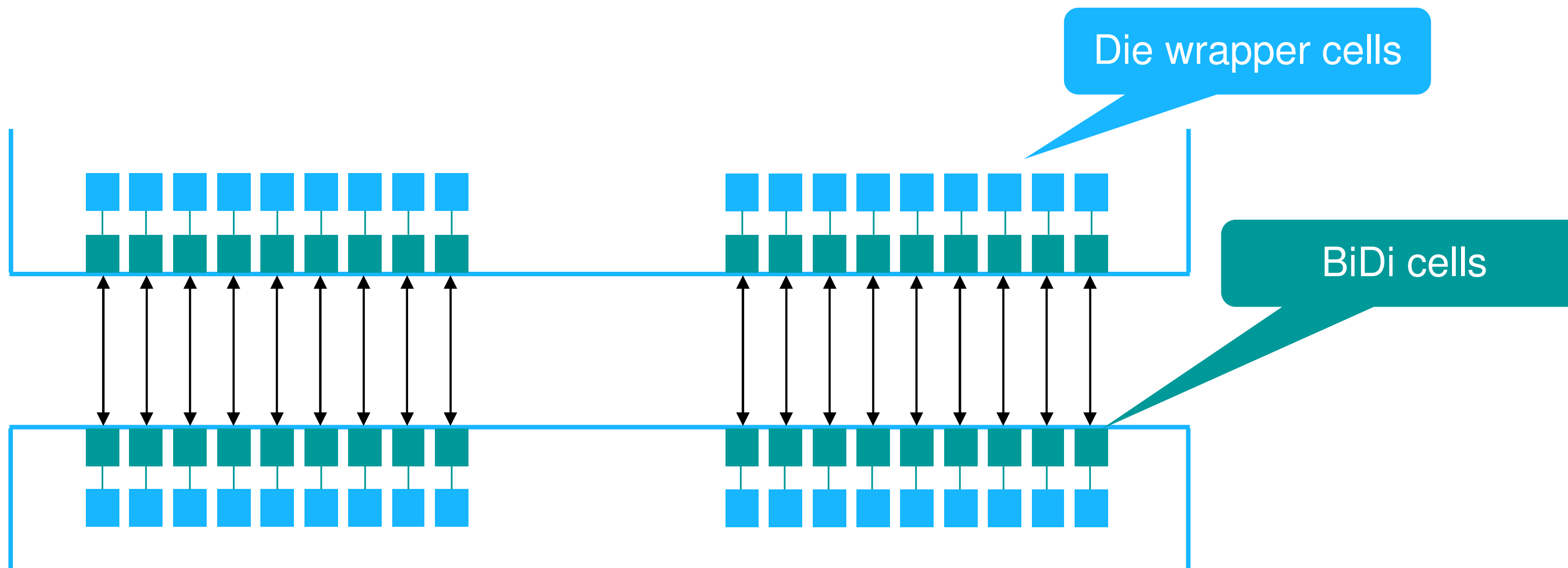
- IO BIST with hard/soft lane redundancy
- Use of "spare" lanes

UCIe – Universal Chiplet Interconnect Express
OpenHBI – Open High Bandwidth Interconnect
BoW – Bunch-of-Wires
HBM – High-Bandwidth Memory
USR/XSR Serdes – Ultra Short Reach / Extra Short Reach Serdes

3D direct die-to-die interconnect & test

Bidirectional connection for (most) interconnects

- Allows wafer-level (short) loop-back test
- Allows stack-level short & long loop-back test
- Stuck-at, delay (shorts, opens)



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3D direct die-to-die interconnect & test

Bidirectional connection for (most) interconnects

- Allows wafer-level (short) loop-back test
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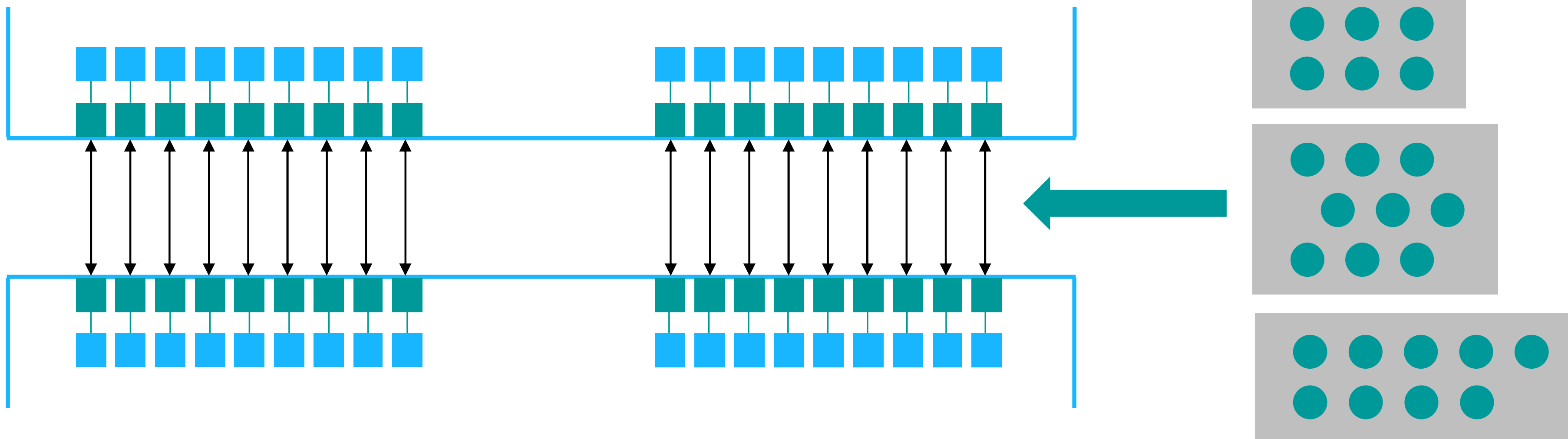
Test needs to know the topology (BIST, ATPG)

- Higher quality test
- Information for diagnosis
- Information for repair



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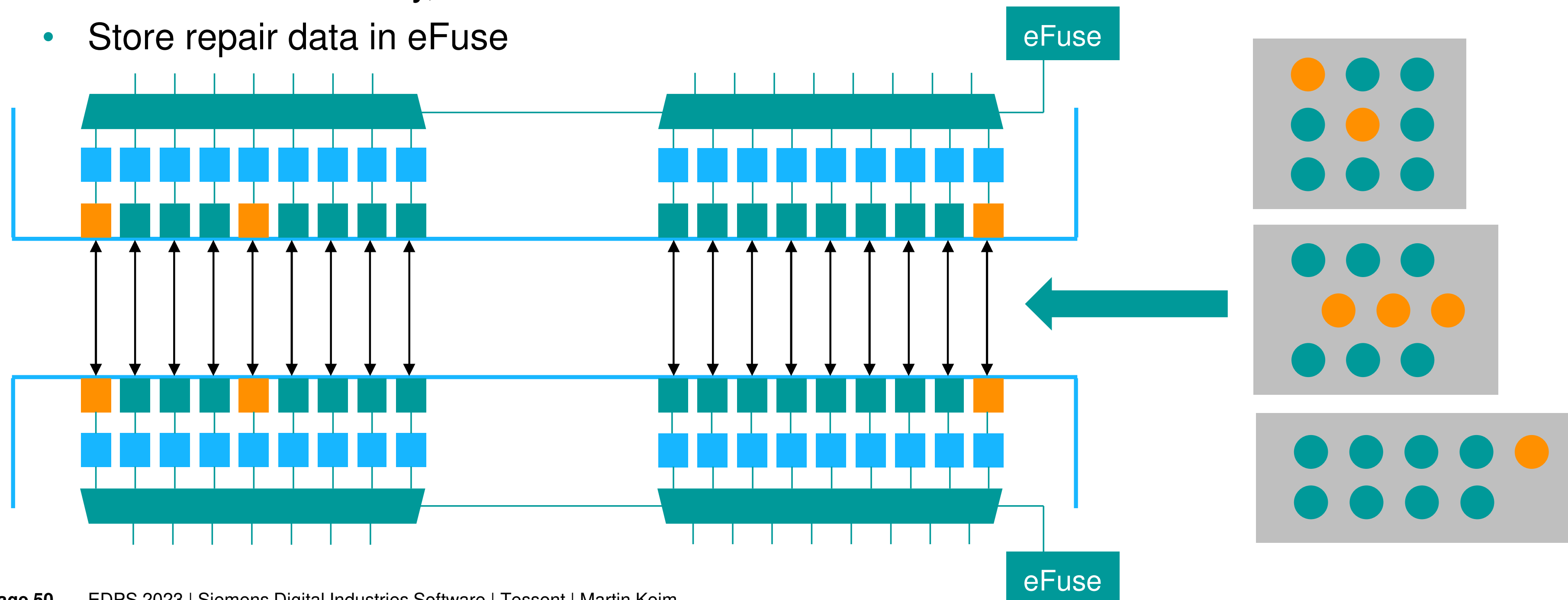
3D direct die-to-die interconnect & repair (IEEE P3405)

Repair of (TSV) interconnect

- Assume some (TSV) interconnects are broken
- Deploy “some” spare interconnects
- Implementation similar to Memory IO repair
  - For 2D TSV array, same solution on both sides
- Store repair data in eFuse

IEEE P3405: Information exchange files

- How many spares per TSV group?
- Assignment of spare to TSV within a group?
- Ensure compatible repair for both dies



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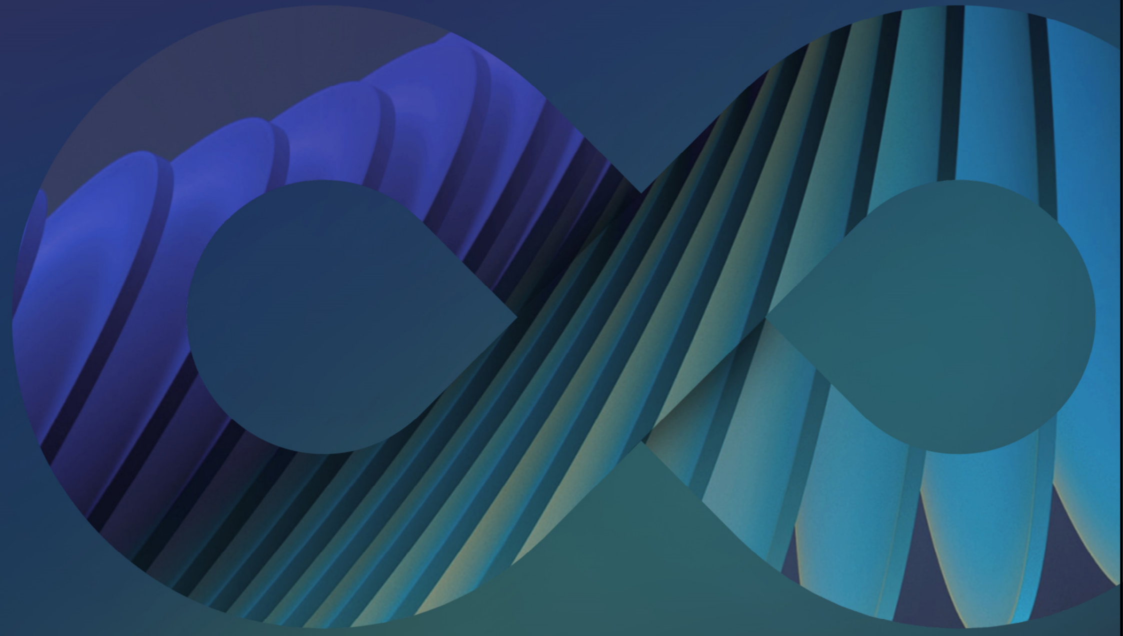
Summary



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Summary of Design-for-Test for 3D

Ensure the assembled product is defect free

- Each 2D die (chiplet, tile, …) is defect free
- The 3D stack, 2.5D assembly is defect free

Cost considerations and trade-offs

- Known Good Die (KGD)
- Wafer-level die interconnect test
- Partial stack test
- Stack-level interconnect test
- Stack-level interconnect repair
- Reuse die-level DFT as much as possible for stack-level
  - Hardware and test patterns

BiDi solution might be too expensive

No standard solution

No standard solution

- Allow heterogenous 3D integration also for DFT

No support from standards

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Thank you