Universal Chiplet Interconnect Express (UCIe)™ : An open industry standard for Chiplets

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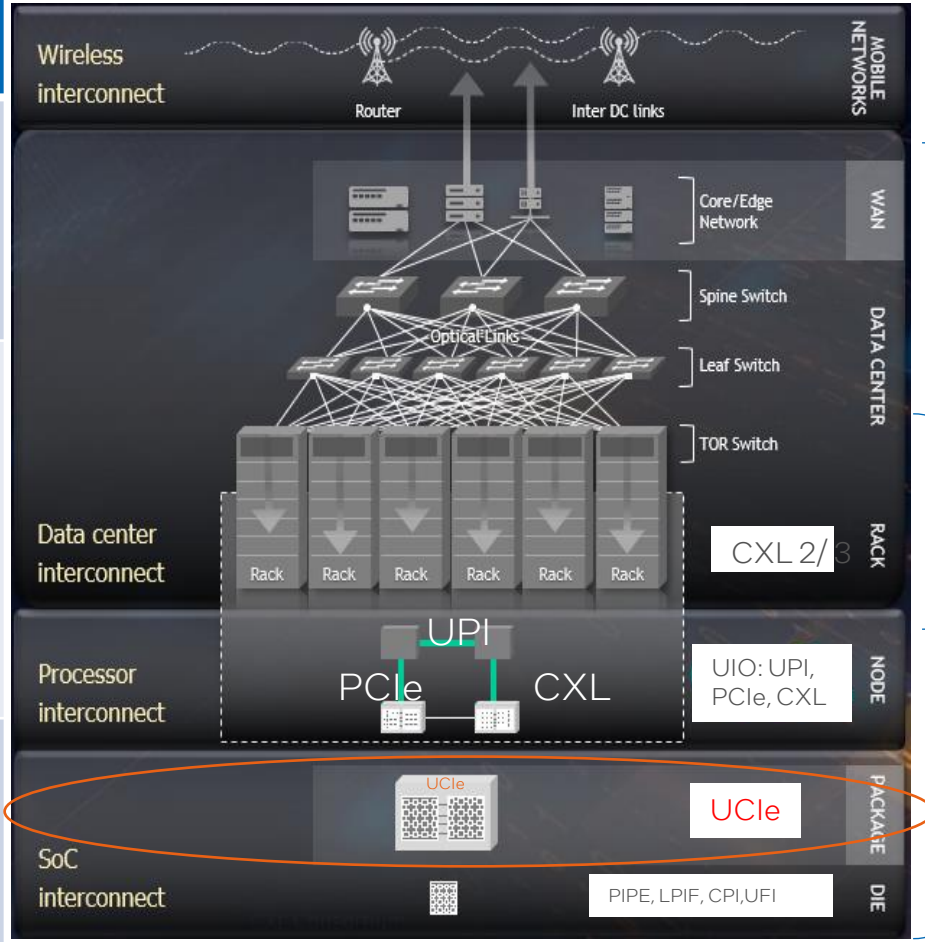
Agenda

- Interconnects in Compute Landscape
- On-Package Interconnects: Opportunities and Challenges
- Universal Chiplet Interconnect Express (UCIe): An Open Standard for Chiplets
- Future Directions and Conclusions

Taxonomy, characteristics, and trends of interconnects

	Category	Type and Scale	Data Rate/ Characteristics	PHY Latency (Tx + Rx)
Off-Package	Latency Tolerant (Narrow, very high speed)	Networking / Fabric for Data Center Scale	56/ 112 GT/s-> 224 GT/s (PAM4) 4-8 Lanes, cables/ backplane	20+ ns (+ >100 FEC)
Off-Package	Latency Sensitive (Wide, high speed)	Load-Store I/O Arch. Ordering (PCIe/ CXL / SMP cache coherency – PCIe PHY) Node (-> Rack)	32 GT/s (NRZ) -> PCIe Gen6 64 GT/s (PAM4) Hundreds of Lanes Power, Cost, Si-Area, Backwards Compatible, Latency, On-board -> cables/ backplanes	<10ns (Tx+ Rx: PHY-PIPE) 0-1ns FEC overhead
On-Package	Latency Sensitive (super-wide, high speed)	Load-Store and proprietary	4 G – 32G (single-ended, NRZ) 2D, 2.5D (-> 3D) Thousands of Lanes Ultra low power, ultra low latency High b/w density	<2ns (PHY – Transaction Layer)



Load-Store I/O: From Package/ Node to Rack / Pod

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Moore Predicted “Day of Reckoning”

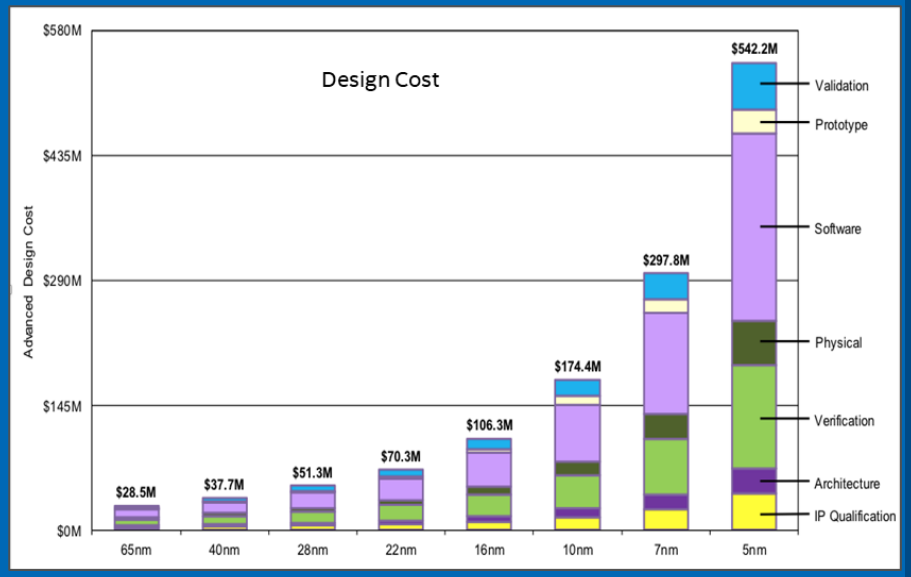
“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1].”

-Gordon E. Moore

[1]: “Cramming more components onto integrated circuits”, Electronics, Volume 38, Number 8, April 19, 1965

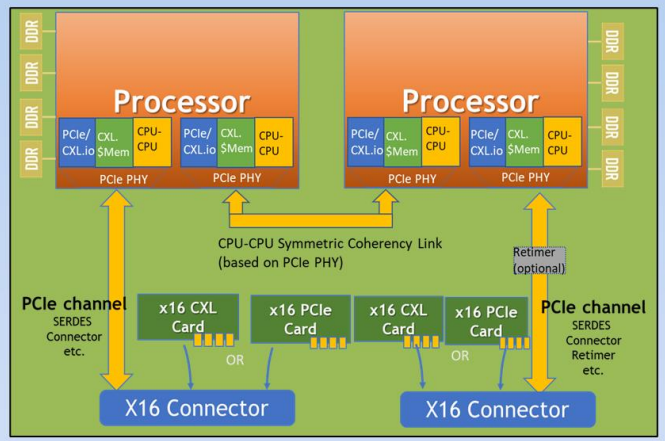
Drivers for On-Package Chiplets

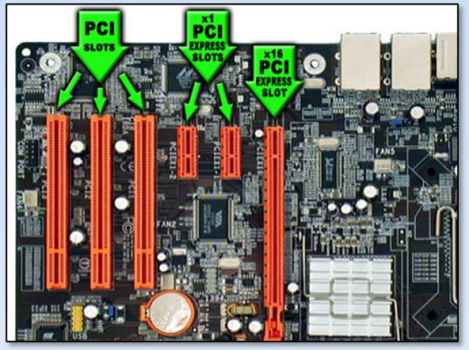
- Reticle Limit, yield optimization
- Increasing IP porting costs
- Time to Market (Late binding)
- Besoke solutions
- Optimized process / functions
  - E.g., Memory, logic, analog, optics



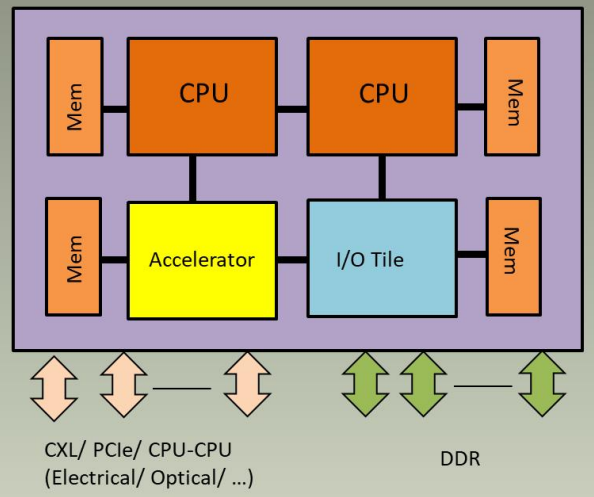
Source: IBS (as cited in IEEE Heterogeneous Integration Roadmap)

Design Choice: Seamless Integration from Node → Package → On-die enables Reuse, Better User Experience

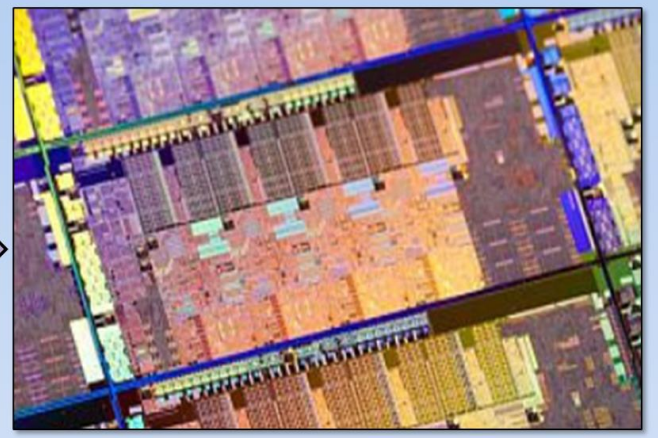




Node / Board Level Integration



Package Level Integration
(with on-package interconnects)



On-die Integration

Same Software, IP, and Subsystem to build scalable solutions offers economies of scale , time to market advantage, and seamless user experience. Innovations at the open slot in board level needs to migrate to package level for multiple usages!

Agenda

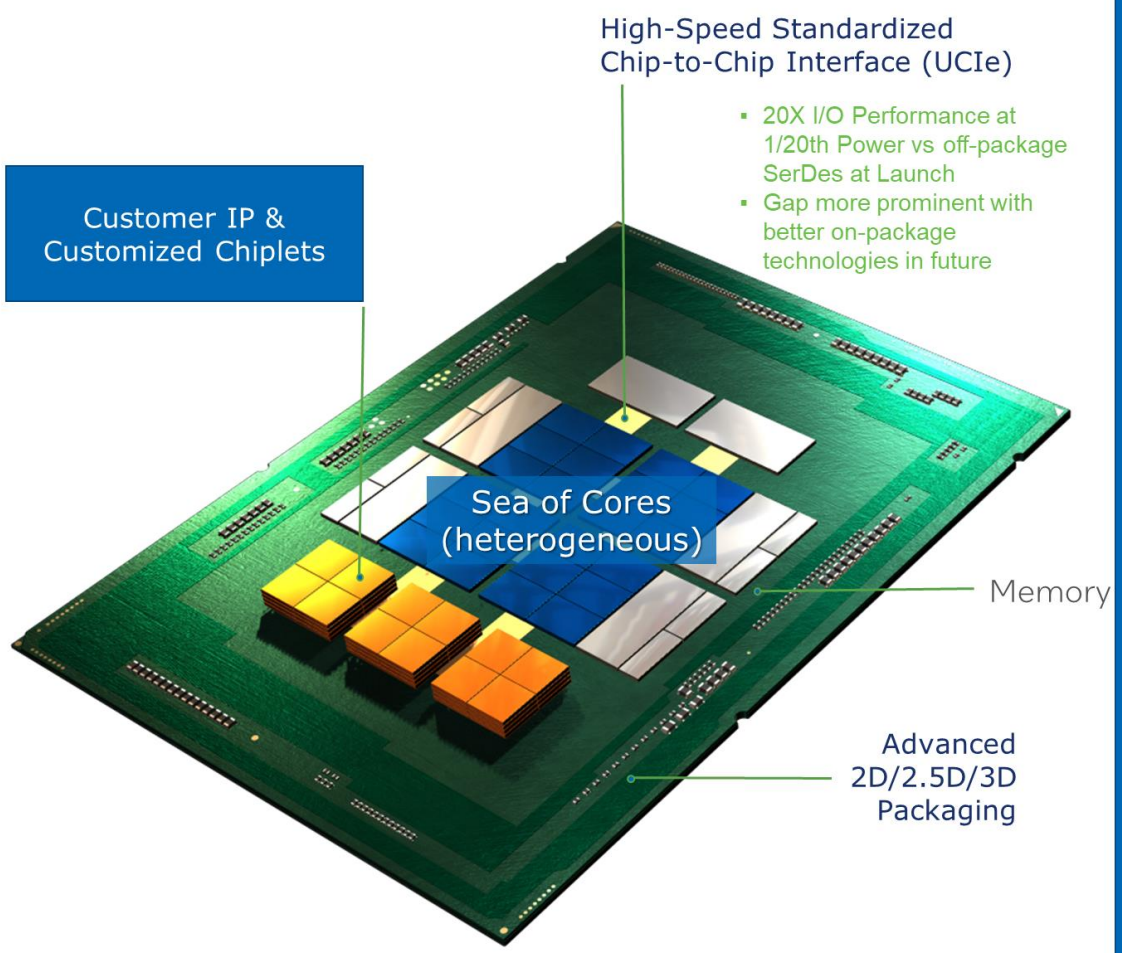
- Universal Chiplet Interconnect Express (UCIe): An Open Standard for Chiplets

Guiding principles of UCIe

1. Open Ecosystem with Plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)

Motivation for UCIe



Align Industry around an open platform to enable chiplet based solutions

- Enables SoC construction that exceeds maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing/ process locked IPs)

UCIe: Key Metrics and Adoption Criteria

Key Performance Indicators

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
  - Technology, frequency, & BER
- Reliability & Availability
- Cost: Standard vs advanced packaging

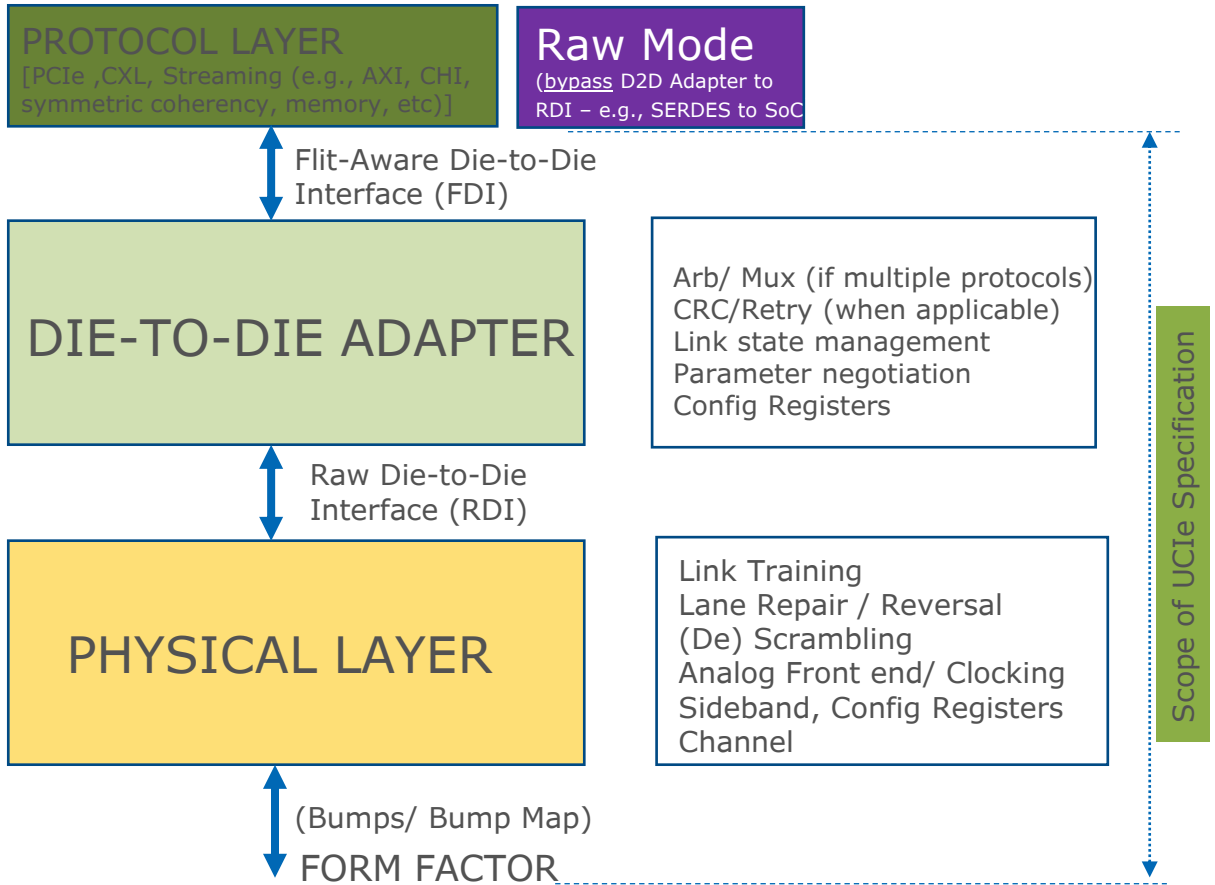
Factors Affecting Wide Adoption

- Interoperability
  - Full-stack, plug-and-play with existing s/w
  - Different usages/segments - ubiquity
- Technology
  - Across process nodes & packaging options
  - Power delivery & cooling
  - Repair strategy (failure/yield improvement)
  - Debug – controllability & observability
- Broad industry support / Open ecosystem
  - Learnings from other standards efforts

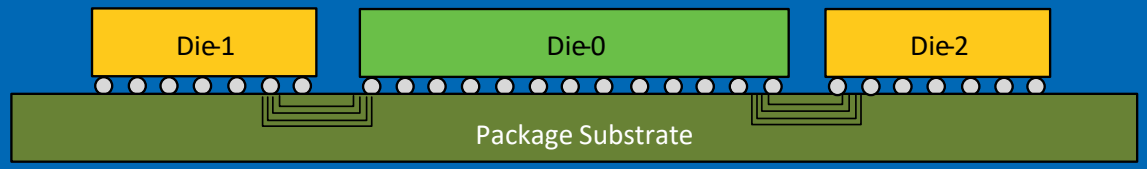
UCIe is architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria

UCIe 1.0 Specification

- **Layered Approach with industry-leading KPIs**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:** Reliable delivery
  - Support for multiple protocols: bypassed in raw mode
- **Protocol:** CXL/PCIe and Streaming
  - **CXL™/PCIe® for volume attach and plug-and-play**
    - SoC construction issues are addressed w/ CXL/PCIe
    - CXL/PCIe addresses common use cases
      - I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
    - Protocol can be anything (e.g., AXI/CHI/SFI/CPI/ etc)
- **Well defined specification**: interoperability and future evolution
  - Configuration register for discovery and run-time
    - control and status reporting in each layer
    - transparent to existing drivers
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface



UCIe 1.0: Supports Standard and Advanced Packages

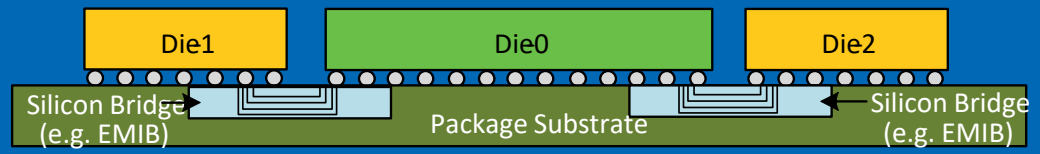


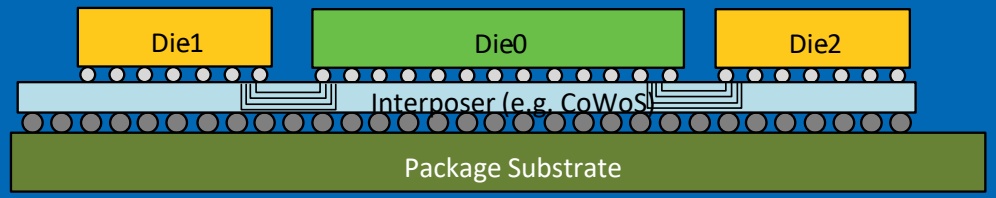
(Standard Package)

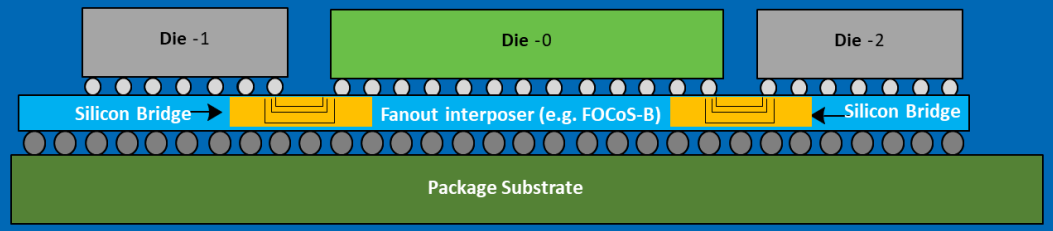
Standard Package: 2D – cost effective, longer distance

Advanced Package: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer







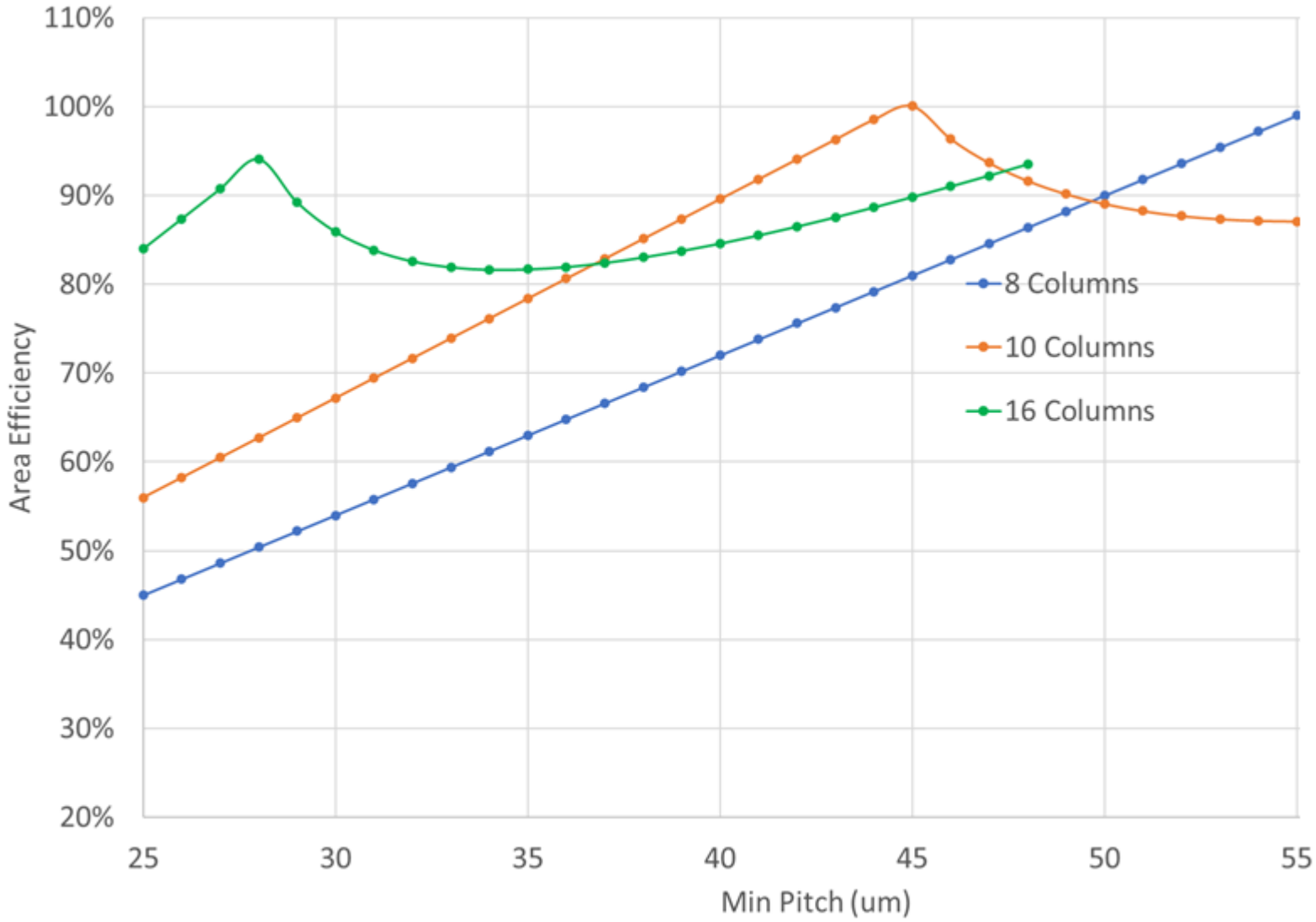
(Multiple Advanced Package Options)

One UCIe 1.0 Spec covers both type of packaging options

UCIe 1.1 Specification

- Released in Aug 2023 – fully backward compatible w/ UCIe 1.0
- Enhancements for Automotive Usages
  - Preventive Monitoring (registers to capture eye margin)
  - Run-time testability (per-Lane error log)
- Streaming Protocols with Full Stack
  - D2D reliability & Multi-protocol (e.g., CHI w/ CXL)
- Cost optimization for Advanced Package
- Compliance enhancements

UCIe-A area/column type efficiency plots

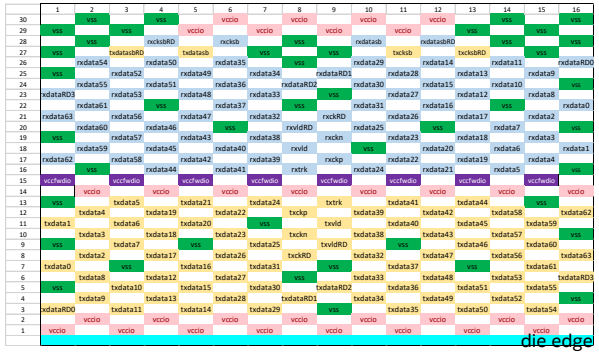


- Points of overlap are the optimal cross-over points between recommended 8/10/16-column bump maps
- At the lower bump pitch range, >80% area efficiency is acceptable given overall magnitude of PHY depth is lower
- As bump pitch increases, >90% area efficiency is desired due to the much bigger PHY depth (um)
  - Example: 10% of 1000um is greater than 20% of 400um

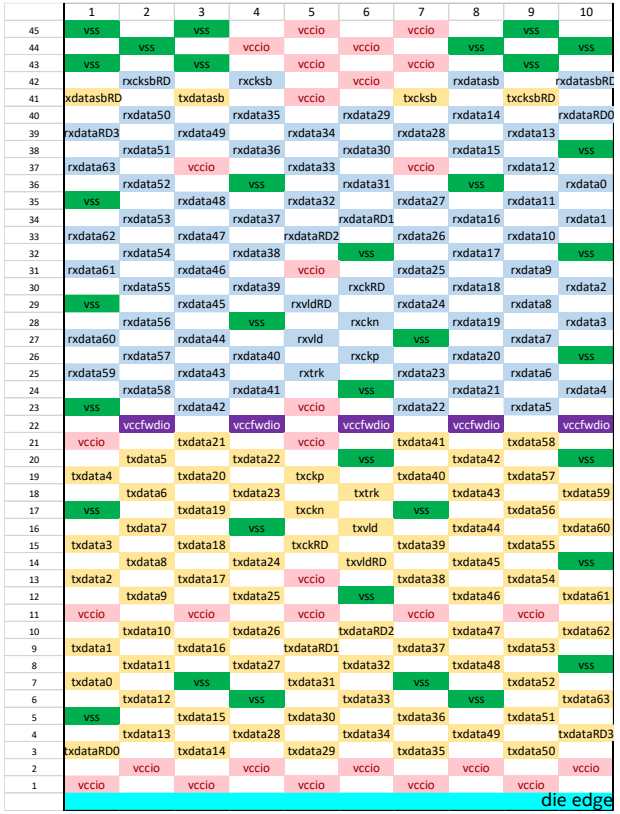
UCIe-A bump map optimization

- Two newly introduced bumpout configurations for maintaining optimized BW/mm^2 across allowable bump pitch range
  - Existing bumpout : 10-column
  - New: 8-column, 16-column
  - Suggested usage guideline:

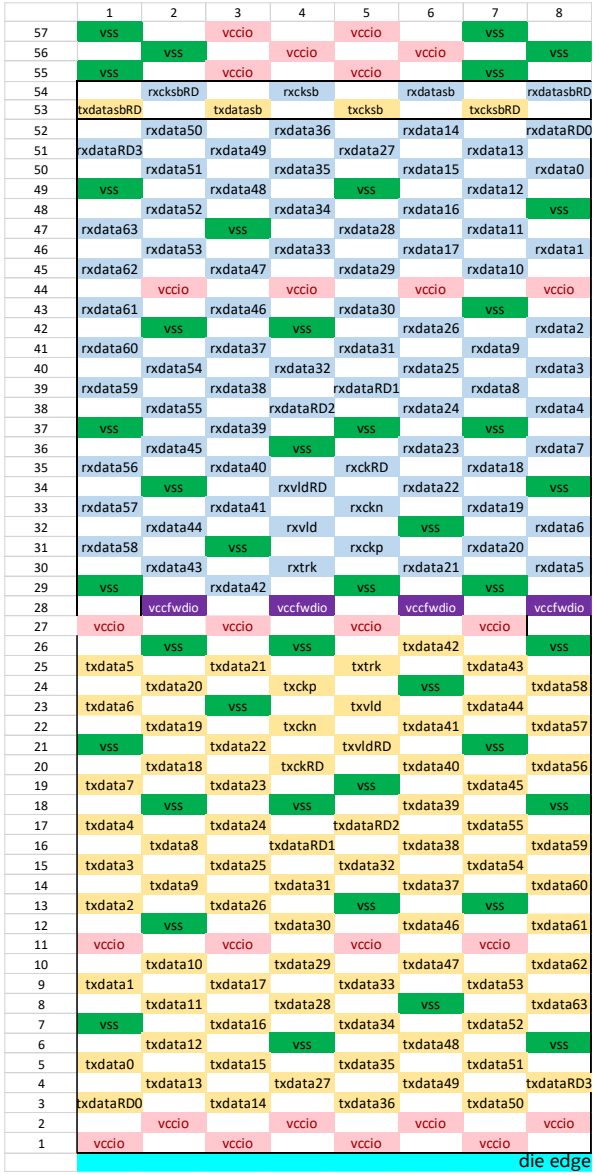
BP	Max Data Rate by Spec	Columns within 388.8 shoreline
25-30	12	16
31-37	16	
38-44	24	10
45-50	32	
51-55	32	8



16Col
Recommended for
25-37um bump pitch



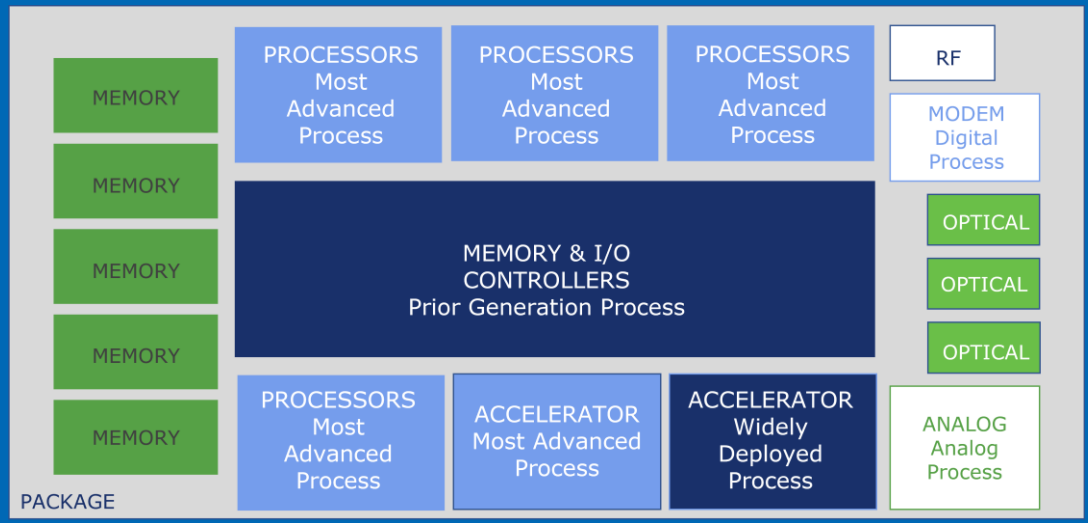
10Col (in spec 1.0)
Recommended for
38-50um bump pitch

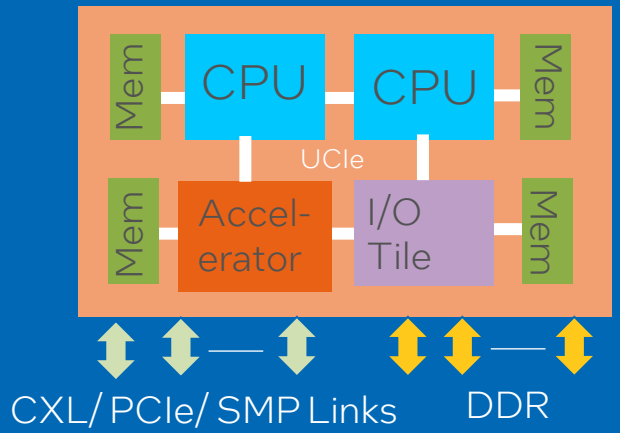


8Col
Recommended for
51-55um bump pitch

UCIe Usage Model: SoC at Package Level

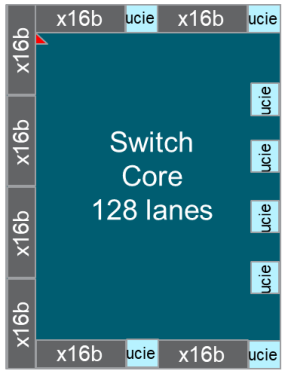
- SoC as a Package level construct
  - Standard and/ or Advanced package
  - Homogeneous and/or heterogeneous chiplets
  - Mix and match chiplets from multiple suppliers
- Across segments: Hand-held, Client, Server, Workstation, Comms, HPC, etc
  - Similar to PCIe/ CXL at board level



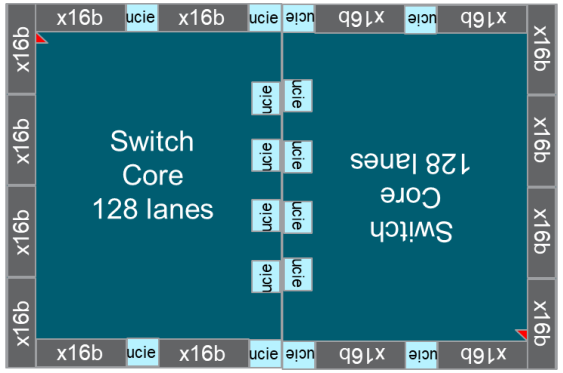


Example Scale-up SoC from homogeneous dies: Large Switch with on-die protocol as streaming over UCIe

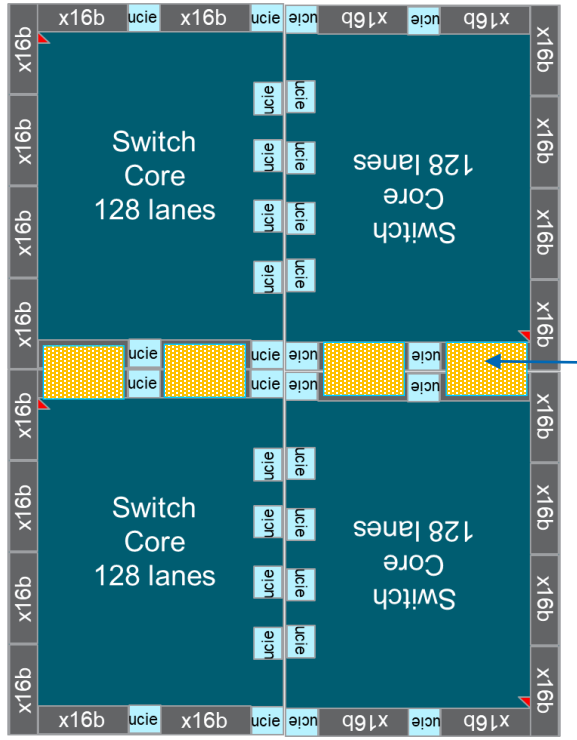
- Need large radix CXL switches – challenges: reticle limit, cost, etc.
- UCIe based Chiplets should help with scalable products
- 64G Gen6 x16b CXL links
- UCIe as d2d interconnect – while this is a scale-up CXL switch , a switch vendor may prefer to have their on-die interconnect protocol be transported over UCIe rather than create a hierarchy of switches which will not work for CXL 2.0 tree-based topology



Small CXL Switch (128 lanes)



Medium-sized CXL Switch (256 lanes)

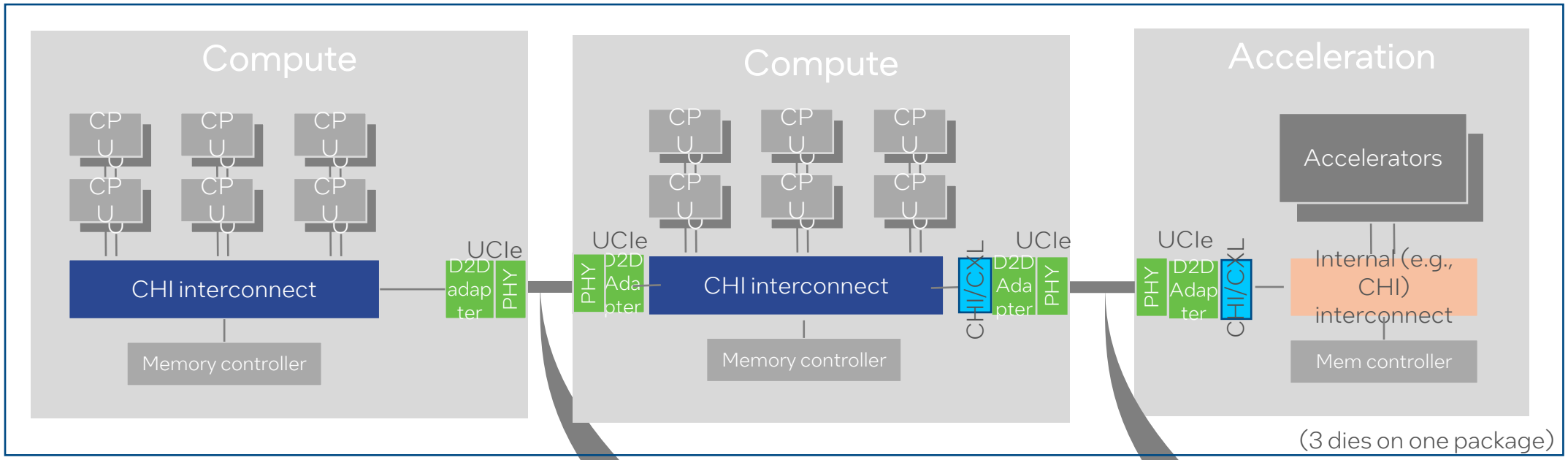


Large CXL switch (512 lanes)

One can construct CPUs (low, medium, large core-count CPUs) from smaller dies connected through UCIe using the same principle
Here the UCIe PHY and D2D adapter will carry the packetized version of internal CPU interconnect fabric

Ack: Nathan Kalyanasundaram

Example Scale-up Package using Streaming and open-plug-in using PCIe/ CXL



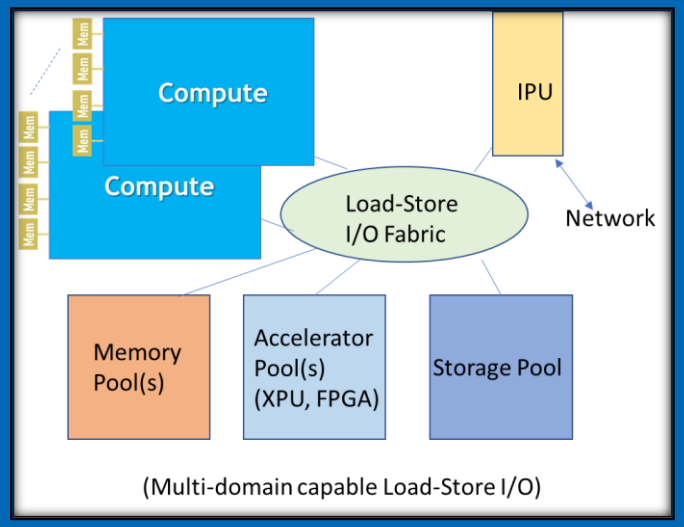
Not drawn to scale

- Transporting the same on-chip protocol allows seamless use of architecture specific features without protocol conversion
- Streaming interface with additional flit formats provide link robustness using UCIe defined data-link CRC and retry

- Any device type in this open plug-in slot with CXL (or CHI if both support it)

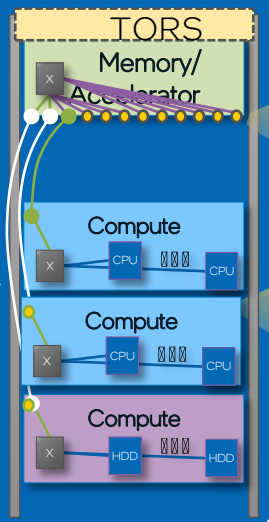
Ack: Marvin Denman, Bruce Mathewson, Francisco Socal, Durgesh Srivastava, Dong Wei

UCIe Usage: Off-Package Connectivity with UCIe Retimers

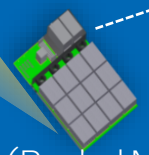


(Vision: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/ sharing as well as message passing)

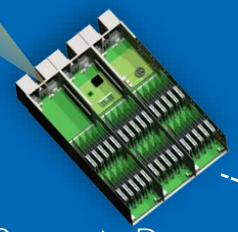
(Pod of Racks)



CXL Rack / Pod level connected using long-reach media (Electrical/ Optical/ ..) through UCIe Retimers (e.g., co-packaged optics)

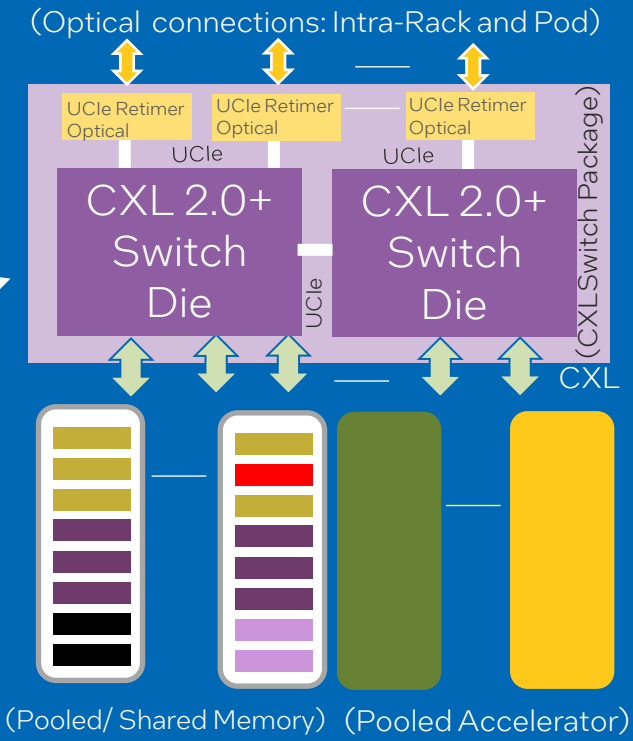


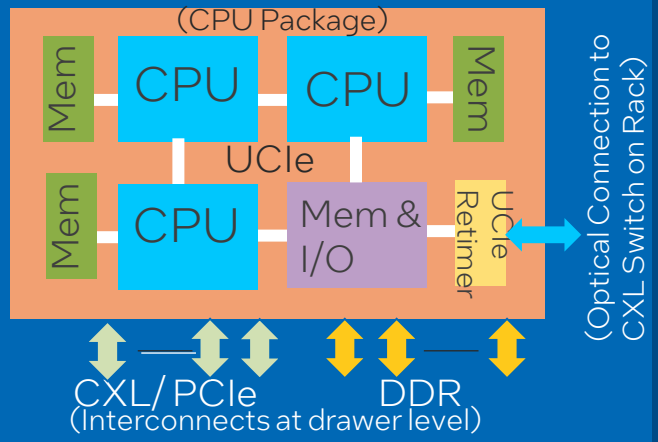
(Pooled Memory / Accelerator Drawer)



(Compute Drawer)

(Physical Connectivity using UCIe-Retimer based co-packaged optics)





Rack/ Pod Level resource pooling/ sharing with UCIe

UCIe 1.0: Characteristics and Key Metrics

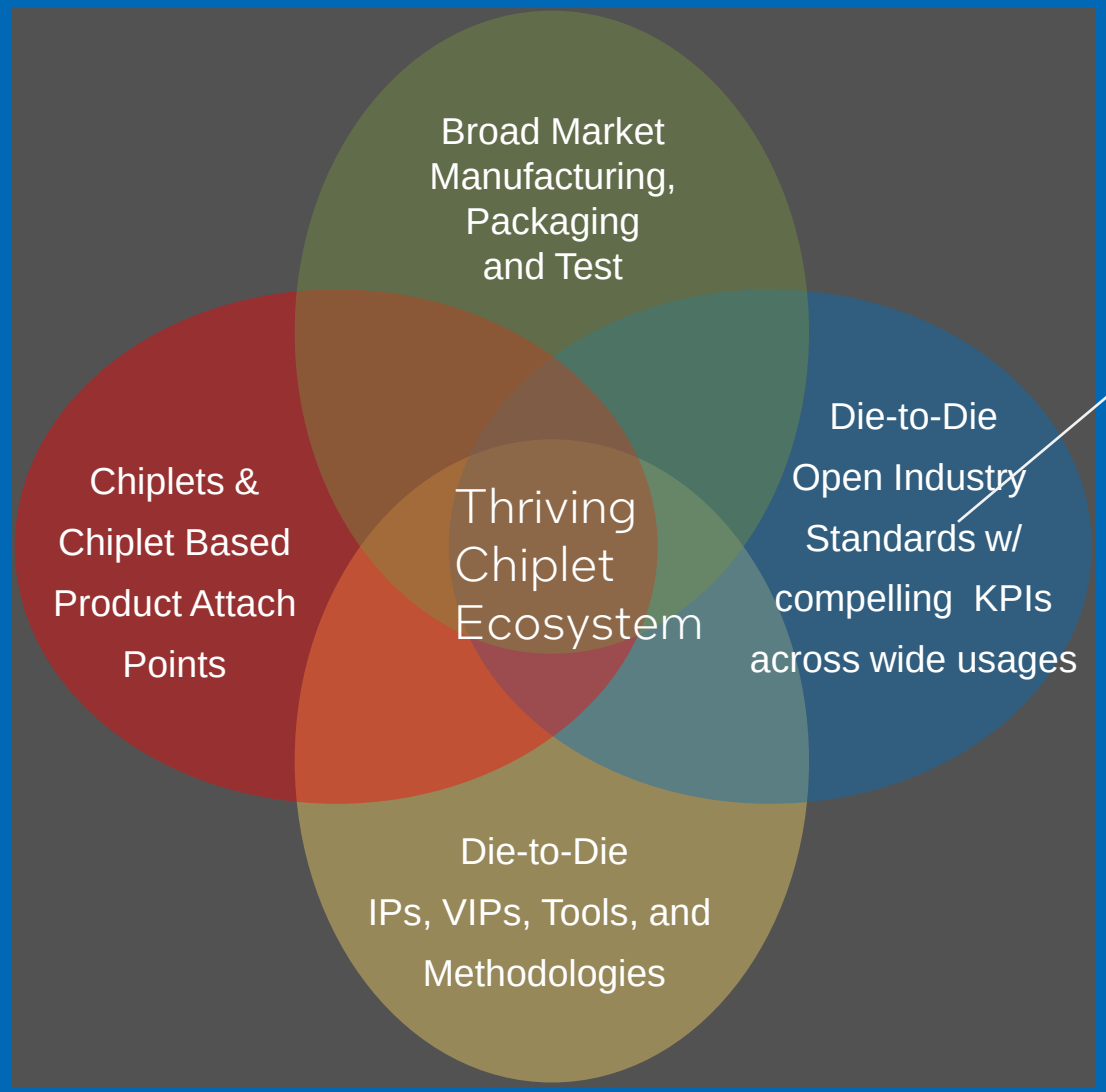
CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm^2)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

UCIe 1.0: Characteristics and Key Metrics

UCIe 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years.
Wide industry leader adoption spanning semiconductor, manufacturing, assembly, & cloud segments.

Ingredients of broad inter-operable chiplet ecosystem



D2D Specs

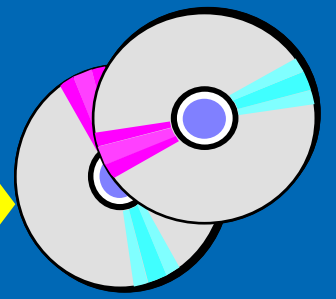
Well-defined Specs

(Electrical,
Logical,
Protocol (e.g., PCIe/ CXL)
Software,
Form-Factor,
Management)

C&I Test Spec

Test criteria based on Specs

(Test Definitions,
Pass/Fail Criteria:
Electrical, Logical,
Protocol, Software)



Test Tools And Procedures

Test H/W & S/W *Validates*
Test criteria
- Compliance
- Interoperability

PASS

FAIL

(Clear Test Output)

Predictable path to design compliance with UCIe

120+ Member Companies and growing!

UCIe™ Universal Chiplet Interconnect Express

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive
The open chiplet ecosystem.

JOIN US!

Alibaba Group · AMD · arm · ASE GROUP · Google Cloud · intel · Meta · Microsoft · NVIDIA · Qualcomm · SAMSUNG · tsmc

The First UCIe Silicon Interoperability: Intel with Synopsys IP on TSMC - Precursor to Innovations

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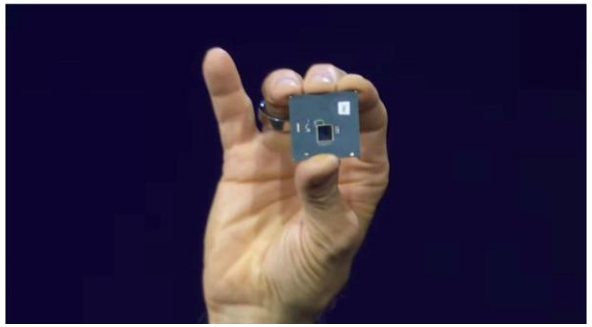
At today's Intel Innovation keynote, Pat Gelsinger showcased the first UCIe interoperable demo featuring technology from UCIe Consortium member companies Intel Corporation, Synopsys Inc and TSMC.

The Pike Creek test silicon contains an Intel UCIe IP chiplet fabricates on IFS Intel 3 and a Synopsys UCIe IP chiplet fabricated on a TSMC N3E process node and packaged using EMIB advanced packaging technology. This demo highlights the UCIe open standard-based chiplet ecosystem, and the future of chiplet interoperability.

Learn more from Tom's Hardware: https://bit.ly/3Lpzn5i
#UCIe #UCIeConsortium #chiplets



Future Directions and Conclusions

Chiplets and D2D interface are essential to the compute continuum

- Power-efficient performance, yield optimization, different functions, custom solutions, cost-effective

UCIe standardization will propel the development an open ecosystem

- Open plug-and-play "slot" at package level will unleash innovations
- Evolution needs to track the underlying packaging technology to deliver compelling metrics
- 3D, Form-factor, New Protocols, and manageability are some other areas for innovation

The open chiplet journey with UCIe just started! Join us in what will be an exciting journey for decades!