Challenges and Opportunities on Thermal Modeling and Simulation for Advanced 3DIC System

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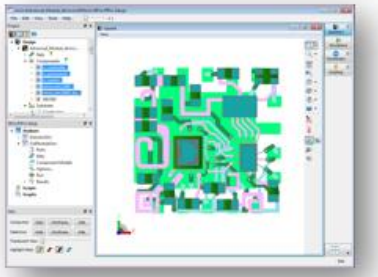
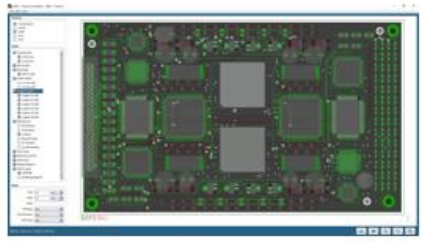
EDPS

Oct., 2023

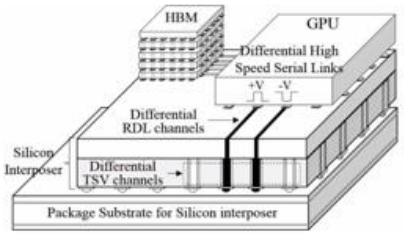
Electronics, Semi and Optics – Thermal/Reliability as Common Challenge



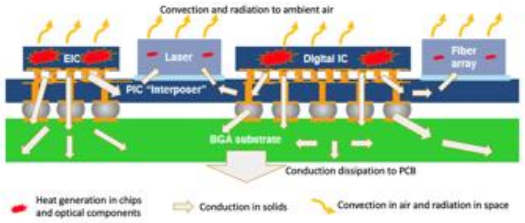
RF, PMIC, AMS



Chip-Package-Board



FinFET and 3D-IC

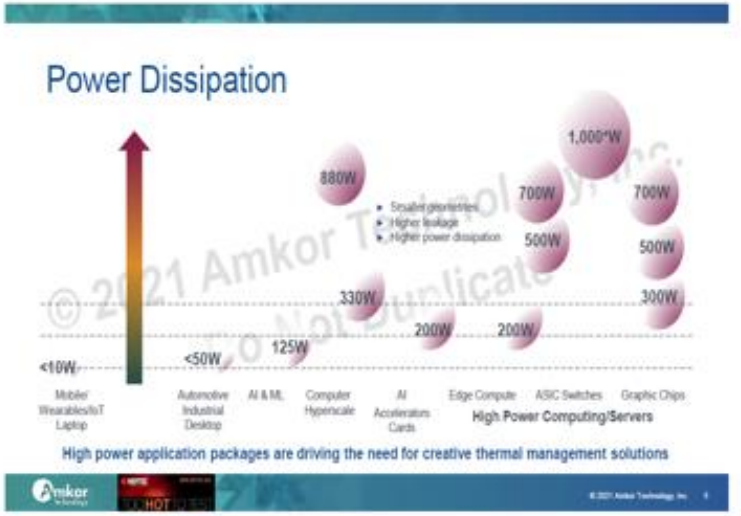


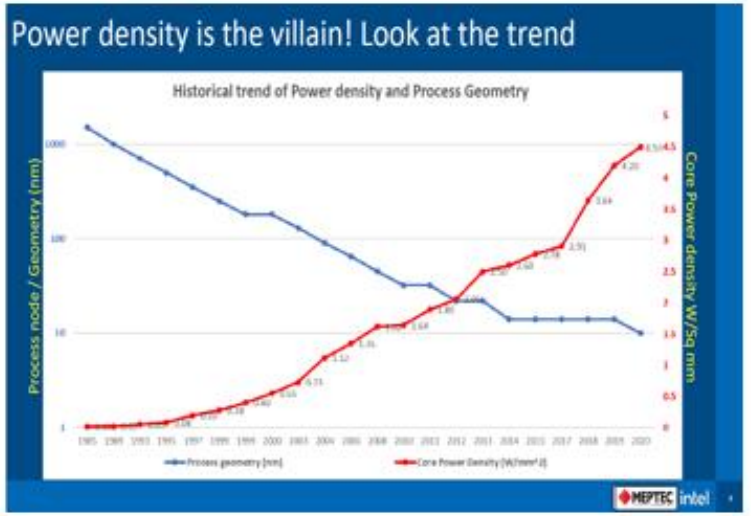
Co-packaged electro-optical

5G/6G and Edge IoT

HPC and Cloud

Automotive, Aerospace and Industrial





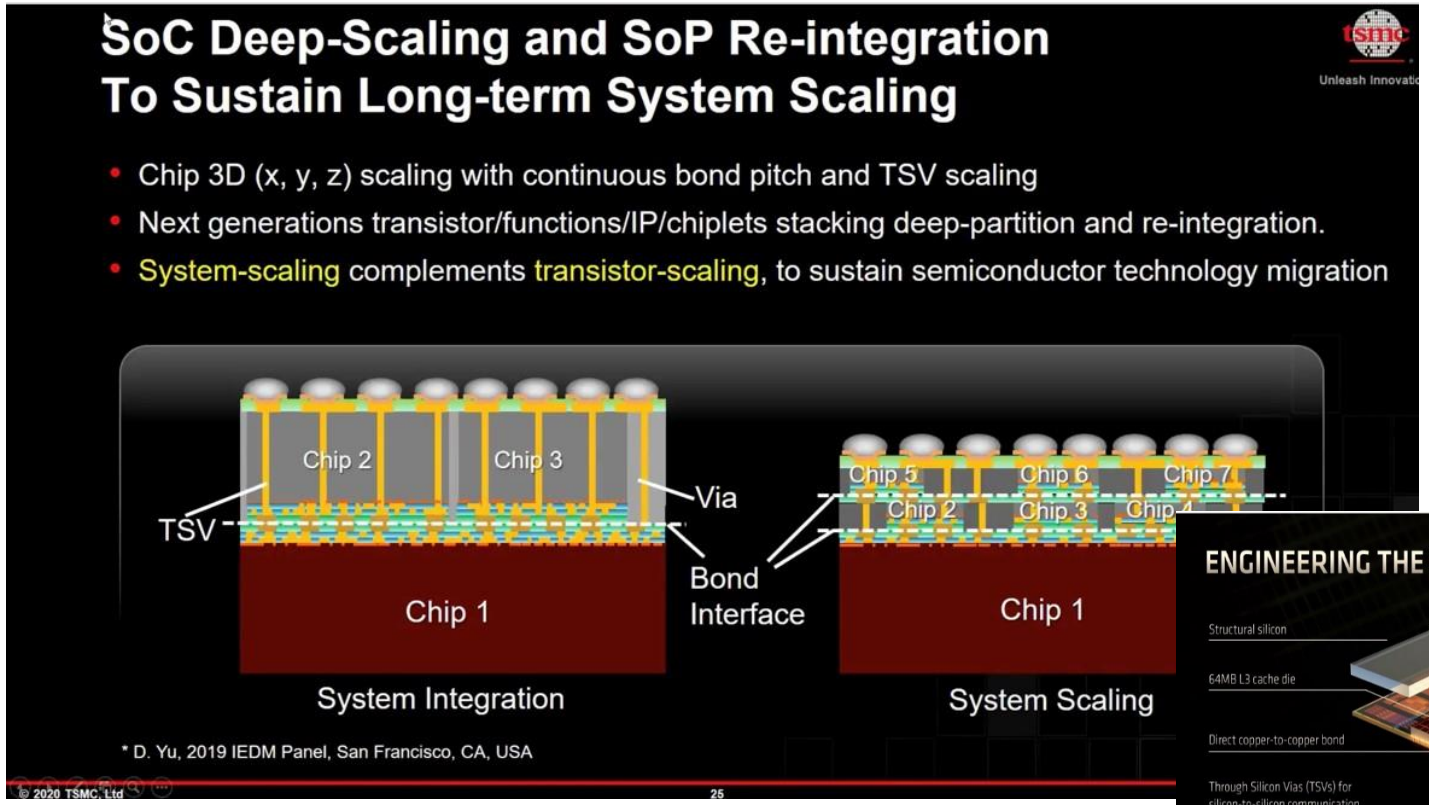
Ref : Too Hot to Test, 2021

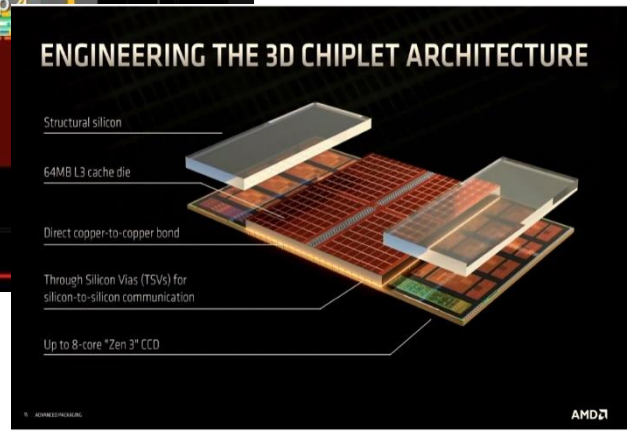
Multiphysics Solutions for SI/PI/TI/Reliability
(**Electromagnetics, Optics, Thermal**) x (Die, 3D-IC, Package, Board)

Thermal/Reliability challenges for Heterogeneous Integration 3DIC

- Early and layout on-chip and package/system thermal/stress analysis
- ESD/EMI/EMC/Rad hard of chip-package-system and on-chip wearout
- High-freq power and signal integrity including TSVs/Interposer
- Co-optimization of package/chip thermal/stress migitation with ML

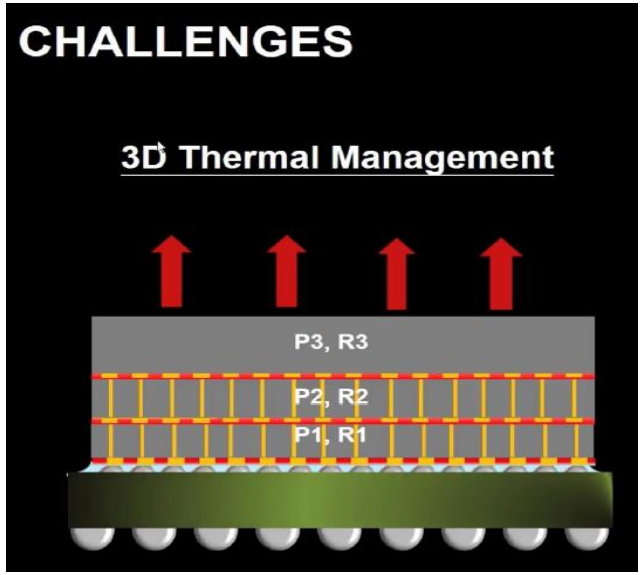
Aggressive System Scaling with 3DIC Requires Thermal/Stress Analysis Solution

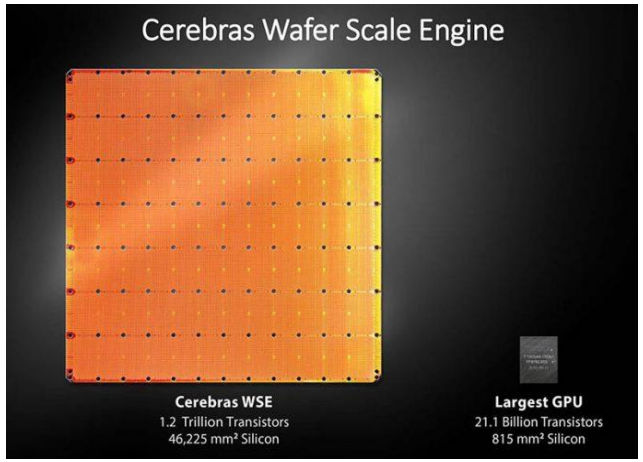




SoIC innovative bump-less bonding

AMD, Hot Chips 2021

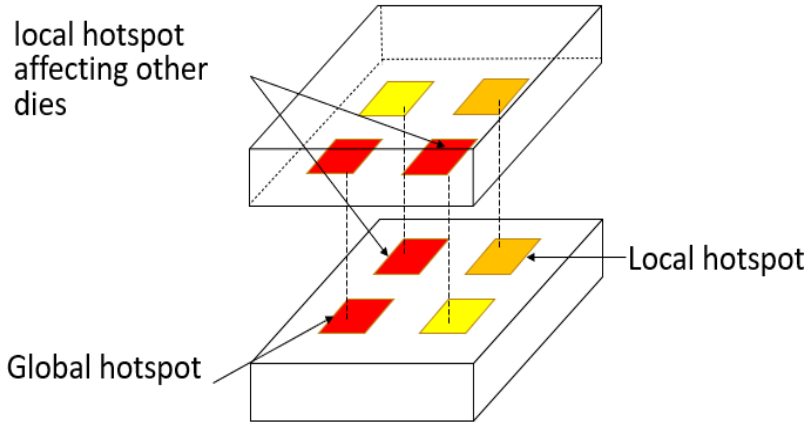


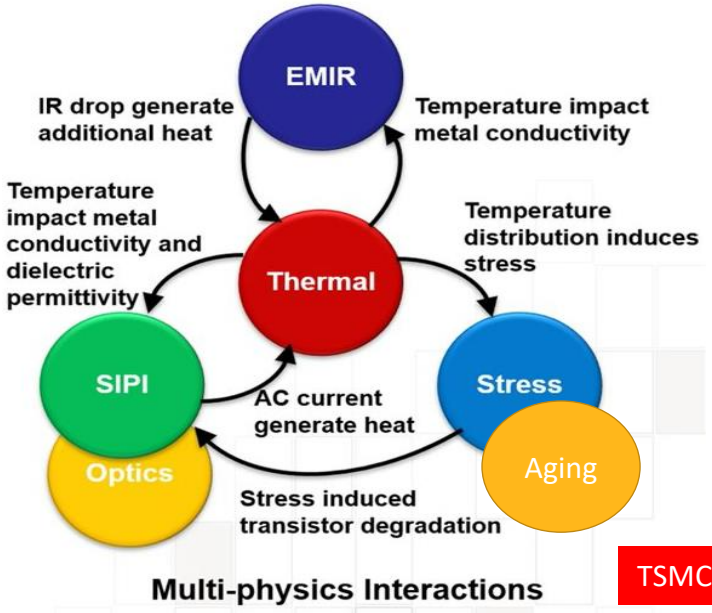


Cerebras, Hot Chips 2021

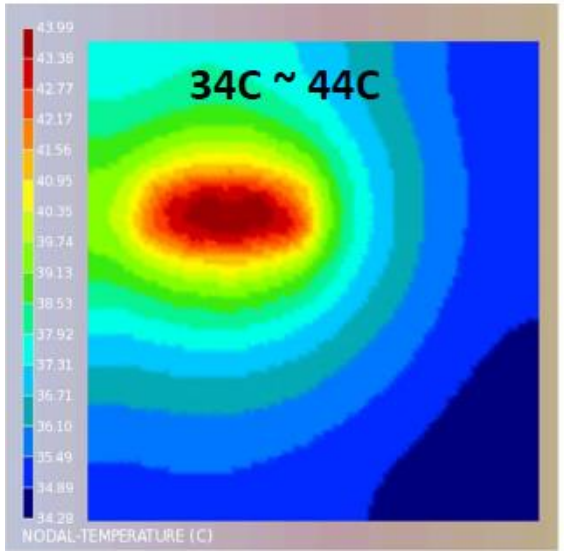
Doug Yu, TSMC, ECTC keynote speaker, 2020
Focusing on PPAT (Power/Performance/Area/Temperature)

Challenge for Accurate Multi-Die Thermal Analysis

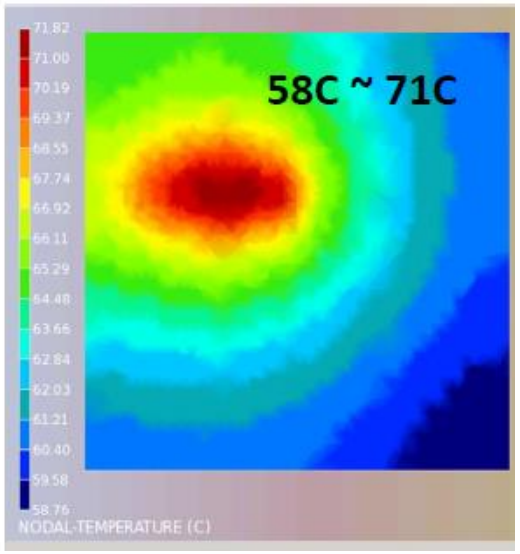




TSMC courtesy



Local Hotspot



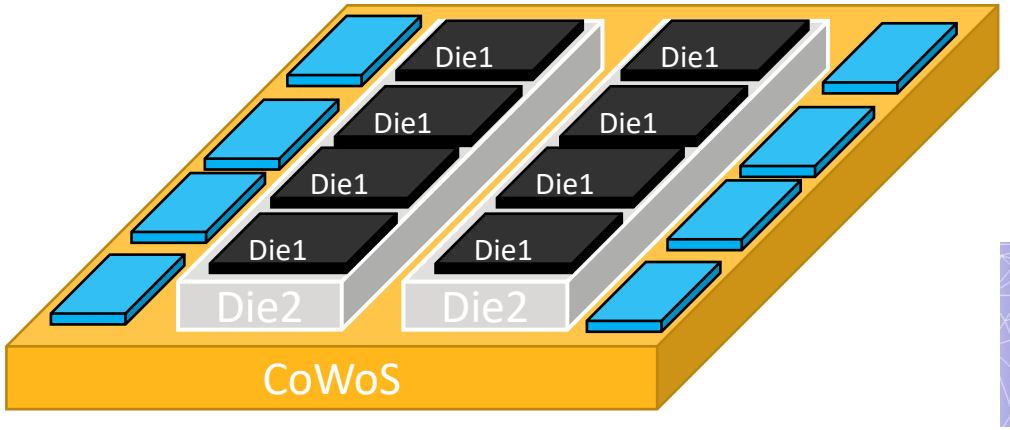
Global Hotspot

- **Vertical die-to-die thermal crosstalk can cause additional ~20C to ~30C hotspot temperature difference**

High-Capacity Static Thermal Flow Much Needed for Large 3DIC

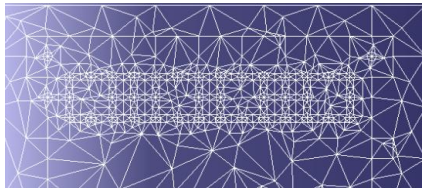
Driving applications: HPC / AI / 5G

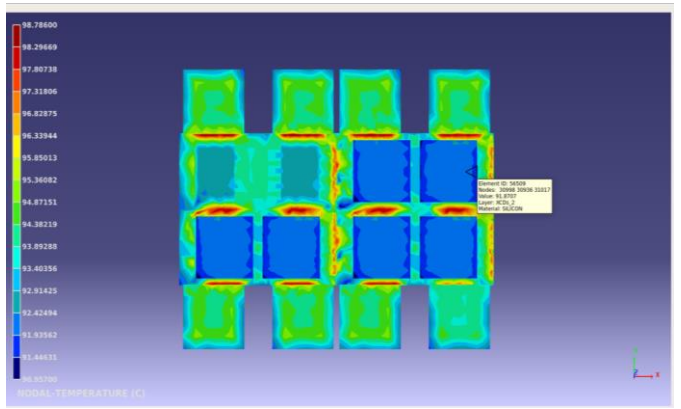
- ✓ Hierarchical CTM stitching technique to assemble the thermal model to handle heterogenous 3D-IC system
- ✓ **Intelligent Adaptive Meshing** can be applied to finish the hierarchical thermal simulation in hours and continue to innovate on fast and accurate hierarchical thermal simulation
- ✓ 3D-IC junction Tmax optimization with HTC applied on the package surface and heat spreader components included.



3D-IC system with CoWoS package

Region-based adaptative meshing





Thermal result for large 3DIC

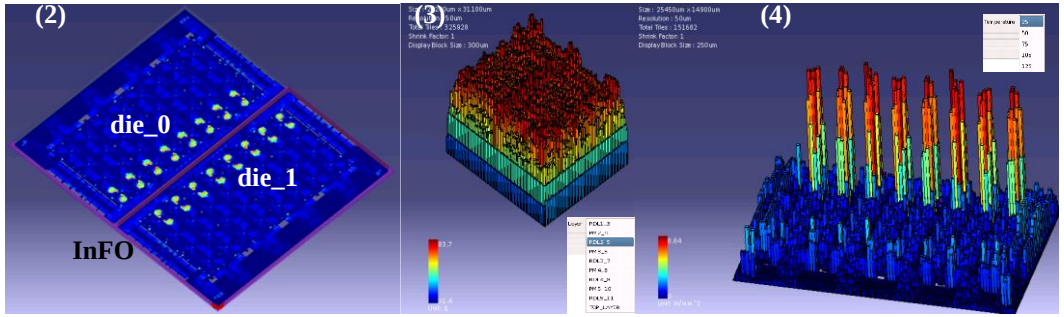
"Invited Paper: Solving Fine-Grained Static 3DIC Thermal with ML Thermal Solver Enhanced with Decay Curve Characterization", H. He, N. Chang, et al., ICCAD, 2023

System-Aware Thermal Solution of 3D-IC

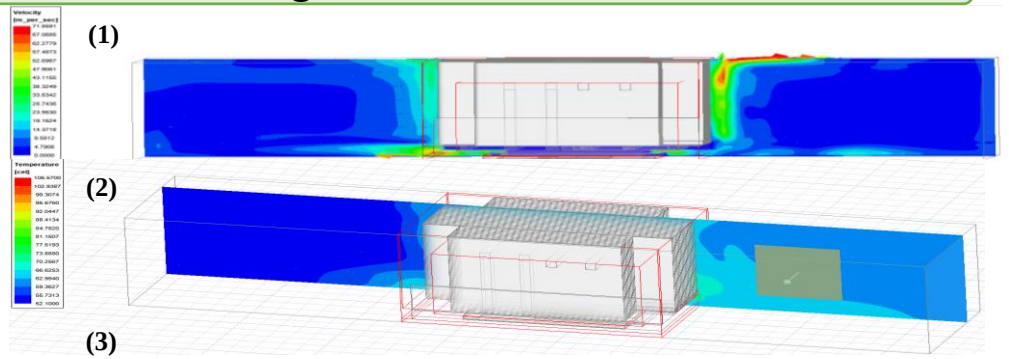
SANECHIPS

Driving applications: mobile / networking

	Item	Size	RedHawk-SC Electrothermal（ET）
Backend	die_0	~25.4 mm*14.4 mm	Detail CTM
	die_1	~25.4 mm*14.4 mm	Detail CTM
	InFO	~26.4mm*31.3 mm	Detail CTM
	C4 bump	~0.4M	
Pkg/System	PKG	icepeak-Model	Boundary condition
	PCB	icepeak-Model	Boundary condition
	Heat Sink	icepeak-Model	Boundary condition

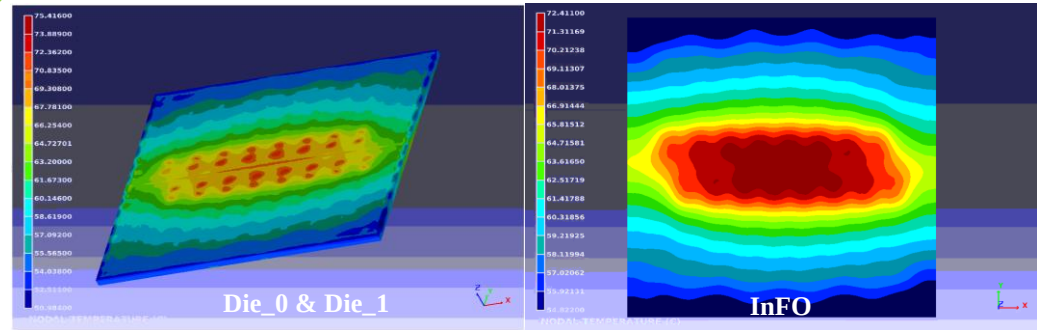


1) and 2) structure diagram of 3DIC stack-up components
3) Tile-based metal density distribution in InFO CTM
4) Tile-based temperature-dependent power distribution in logic die CTM




```
Scalar data "SurfaceValue(Surface(MoldingCompond), Heat_Tr_Coeff)"
NumElems 19956
4.7820000000000001e-01 3.2451000000000001e-02 8.3275000000000002e-02  2.8908716991644593e+02
4.7820000000000001e-01 3.2951000000000001e-02 8.3275000000000002e-02  2.8908716991644593e+02
4.7886000000000001e-01 3.2951000000000001e-02 8.3275000000000002e-02  2.8908716991644593e+02
4.7820000000000001e-01 3.2451000000000001e-02 8.3275000000000002e-02  2.8908716991644593e+02
4.7886000000000001e-01 3.2951000000000001e-02 8.3275000000000002e-02  2.8908716991644593e+02
4.7886000000000001e-01 3.2451000000000001e-02 8.3275000000000002e-02  2.8908716991644593e+02
4.7820000000000001e-01 3.2951000000000001e-02 8.3275000000000002e-02  8.1086046631143881e+02
4.7820000000000001e-01 3.3390999999999997e-02 8.3275000000000002e-02  8.1086046631143881e+02
4.7886000000000001e-01 3.3390999999999997e-02 8.3275000000000002e-02  8.1086046631143881e+02
4.7820000000000001e-01 3.2951000000000001e-02 8.3275000000000002e-02  8.1086046631143881e+02
4.7886000000000001e-01 3.3390999999999997e-02 8.3275000000000002e-02  8.1086046631143881e+02
```

System thermal boundary condition analysis in Icepak

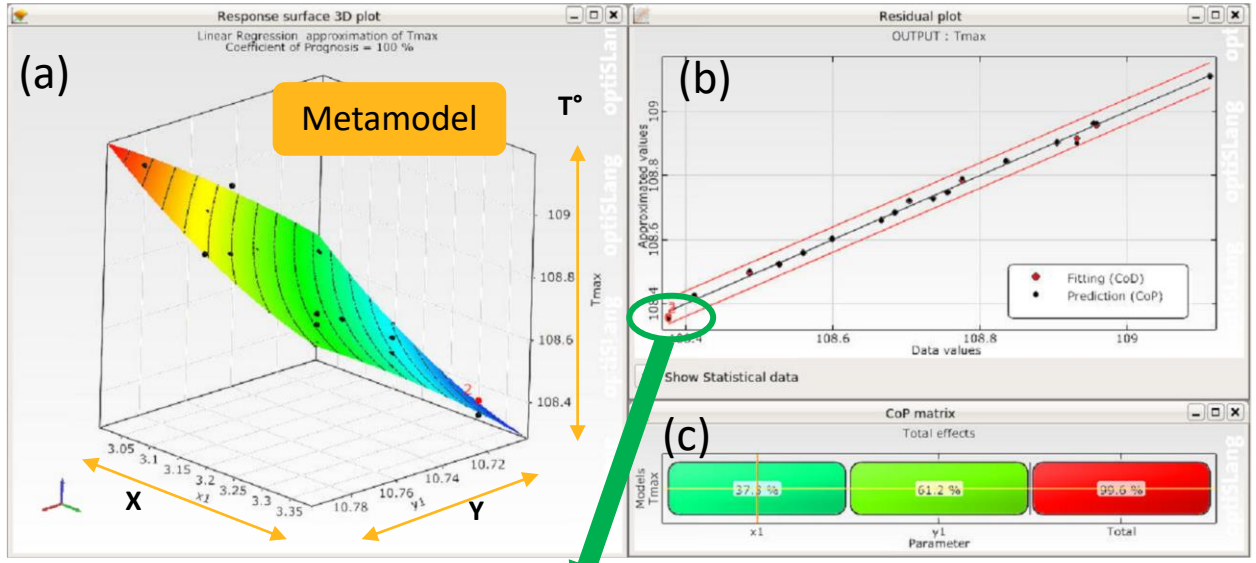


RHSC-ET Thermal Results with Icepak Boundary Condition

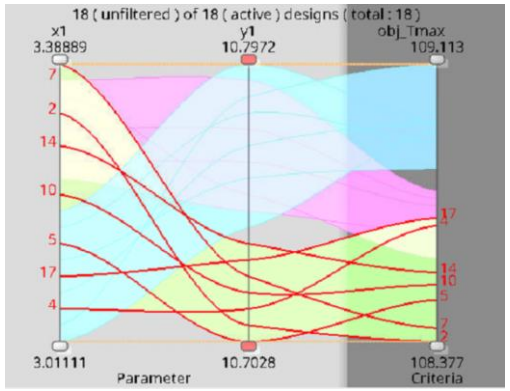
Early design exploration: Thermal Sensitivity Analysis

OptiSLang Sensitivity results

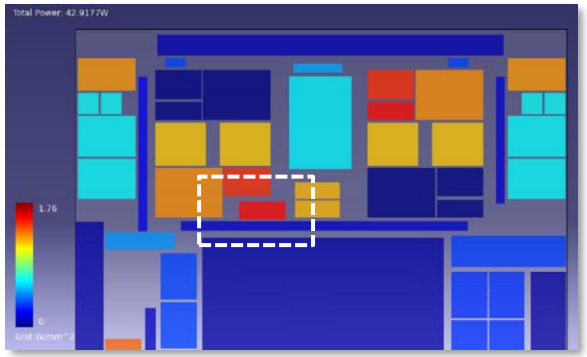
Sensitivity Analysis /OptiSLang GUI



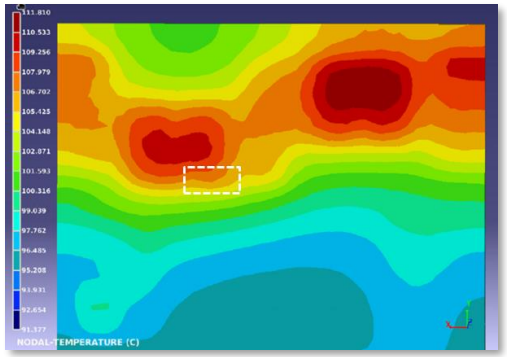
(d) *Parallel coordinate plot with clustering*



Optimum power distribution



Thermal Map



Sensitivity analysis plots interpretation

- *CoP matrix*
  - y_1 has more effect on T_{max} than x_1
- *Response surface 3d plot*
  - Shows the approximation surface plot of objective function in terms of selected design variables
- *Residual plot*
  - Displays T_{max} bounds for the given limits for x_1 and y_1
  - Comparison between predicted and actual T_{max} to assess the quality of prediction
- *Parallel coordinates plot with clustering*
  - Plots all design variables and objective function, clustered by k – means
  - Significance of y1 on Tmax shown by CoP matrix can also be observed here

Findings

- ✓ Base design: T_{local} = *108.96°C*
- ✓ Alternate design: T_{local} = *108.38°C*
- ✓ Reduction in T_{local}: ΔT_{local} = 0.58°C for ΔX= 0.315 mm & ΔY= 0.039 mm
- ✓ T° is mostly sensitive to Y axis

Design variables

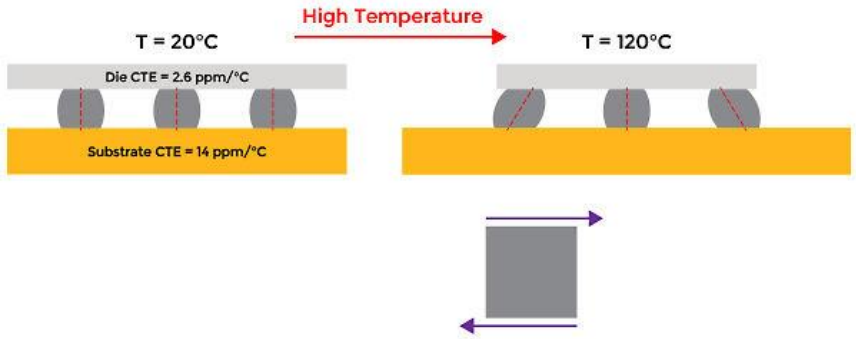
x and y position of power tile

Workflow details

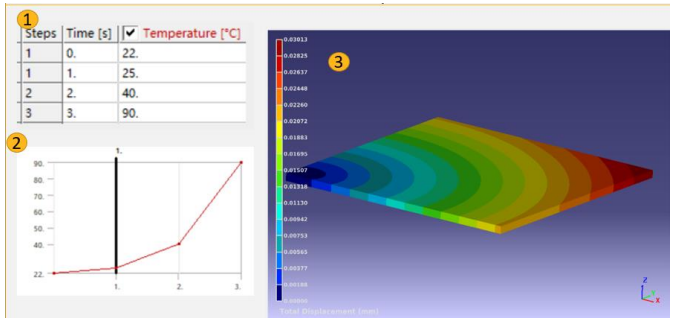
#scenario = 18
Total runtime = 51 minutes

Thermal-Induced Stress Simulation Methodology

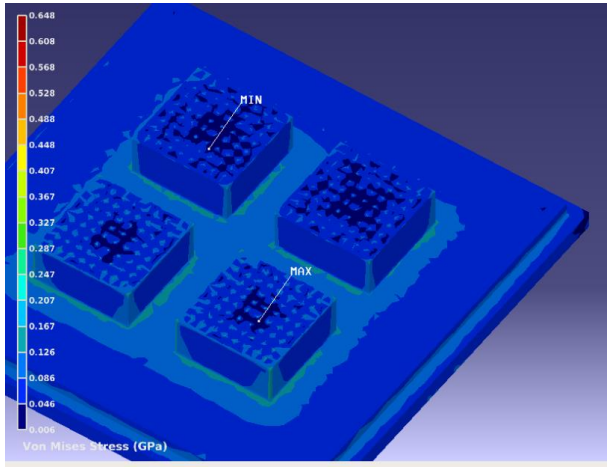
- Mechanical stress caused by change of temperature of a material
  - Thermal expansion during assembly or in operation
  - Temperature cycling in operation
  - Thermal impacts on strain/stress



Coefficient of thermal expansion (CTE) mismatch between two materials causes warpage and displacement

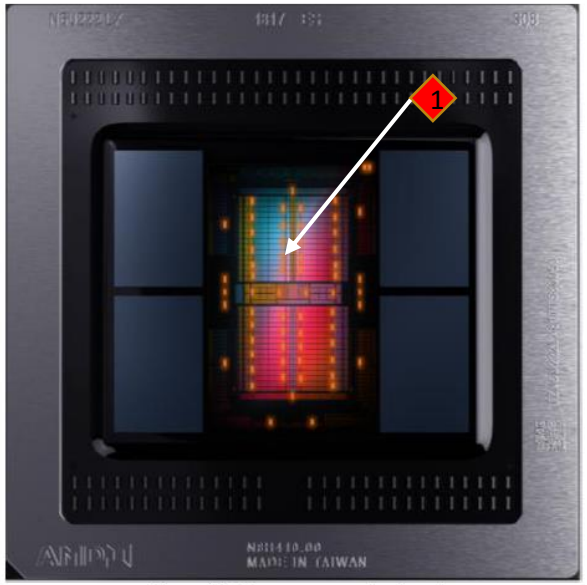


Step-temperature impact on displacement



Von Mises Stress

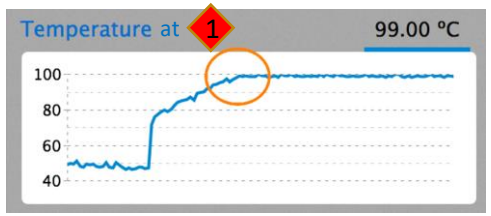
Detailed On-Chip Sensor Based Thermal Throttling Simulation



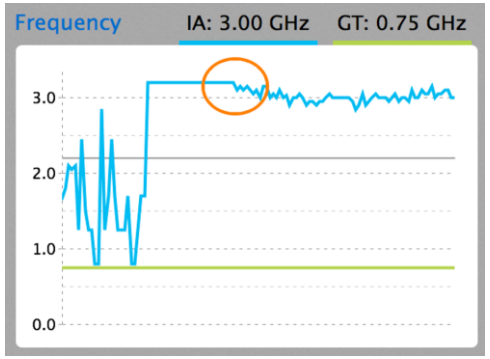
Note: HBM sensors not depicted

64 Sensor locations highlighted on VEGA 20 of Radeon VII card (picture from AMD)

Dynamic Power Mode Selection due to DVFS



If temperature at location 1 reaches the threshold of 100C



The DVFS control logic lowers the voltage and frequency of the GPU

[Vega 20: Under The Hood - The AMD Radeon VII Review: An Unexpected Shot At The High-End (anandtech.com)]

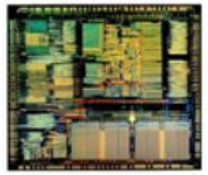
- The trend is that there will be more and more on-chip thermal sensors for DVFS control
- Optimization of on-chip thermal sensor locations are much needed and can be achieved through architecture-level and detailed layout-level thermal simulation

Chip, Package, System Aware Thermal Throttling Simulation

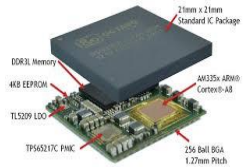
simulating thermal throttling in system

Driving applications: Datacenter / Mobile

IC

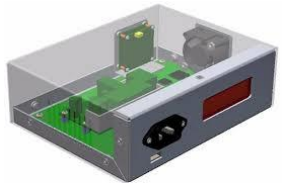


Package

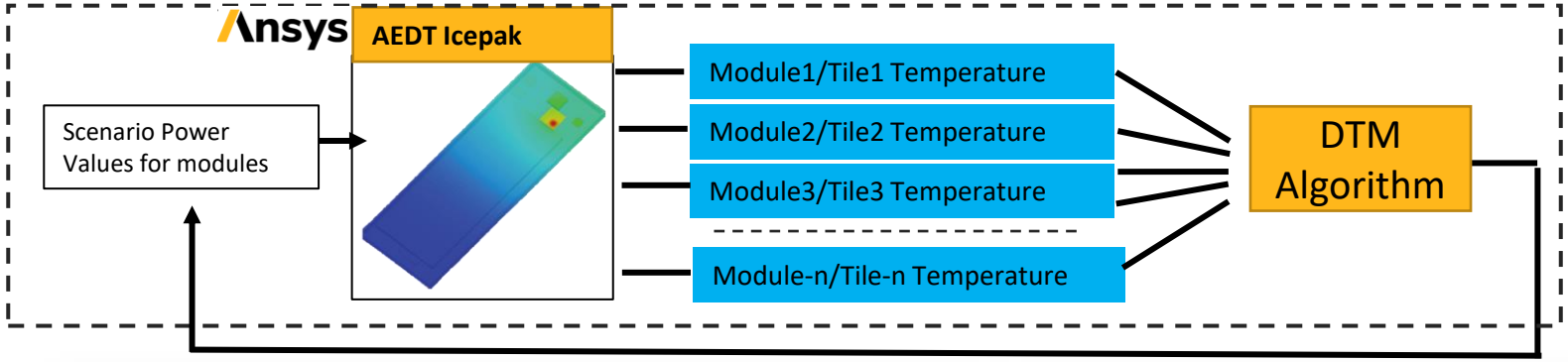


PCB

SYSTEM



Emulator activity profiling for
RTL power
+
Augmented Thermal Simulator
+
RH-SC Electrothermal



Fast and Accurate Thermal Analysis of Smartphone with Dynamic Power Management using Reduced Order Modelling

Sivasubramani Krishnaswamy, Palkesh Jain, Aniket Kulkarni, Ankit Adhiya
ANSYS Inc., Canonsburg, PA 15317
sivasubramani.krishnaswamy@ansys.com, palkesh@qti.qualcomm.com, aniket.kulkarni@ansys.com, ankit.adhiya@ansys.com

Thermal Sensor Placement based on Meta-Model Enhancing Observability and Controllability

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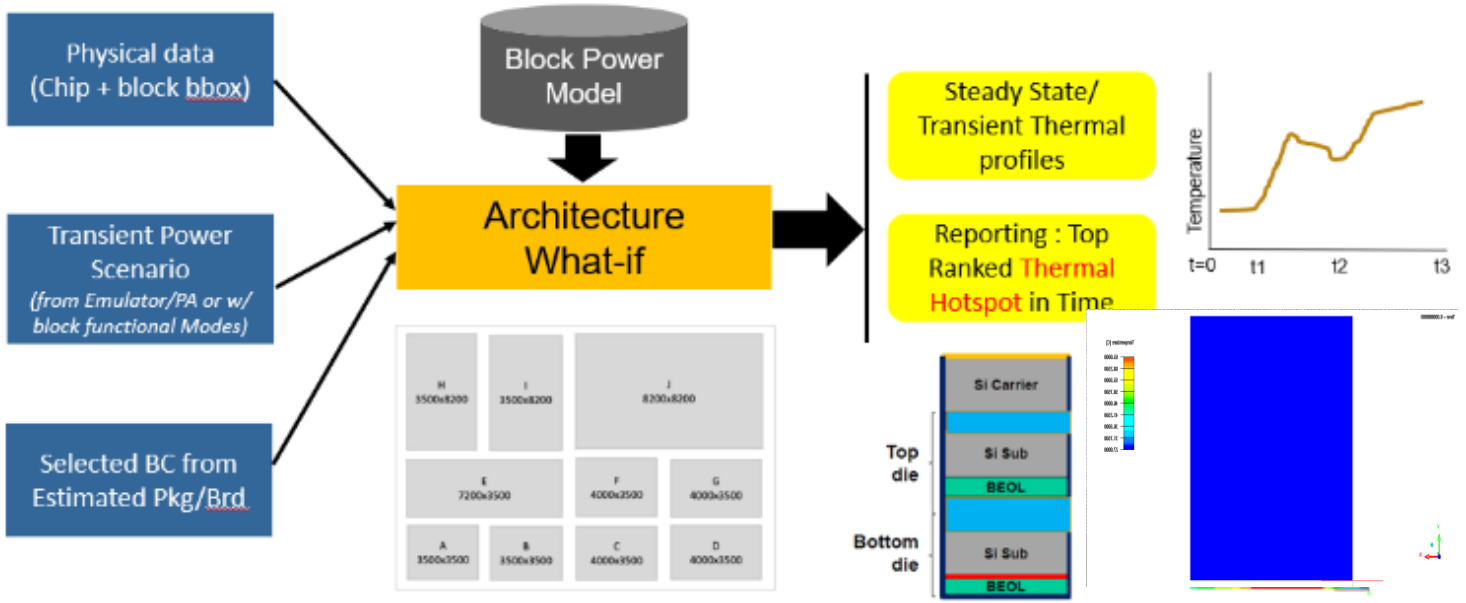
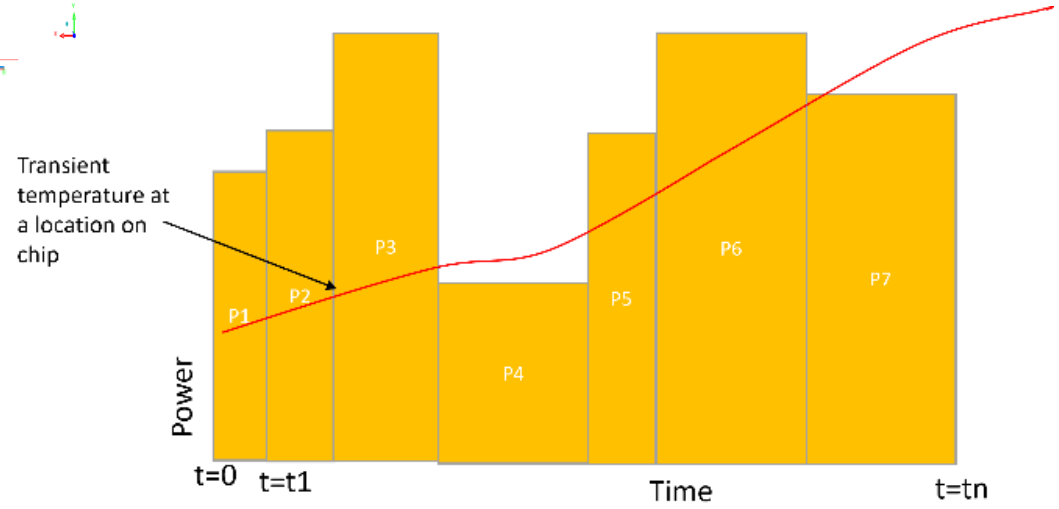
Fast Static/Transient Thermal Analysis Needed for 3DIC Multiphysics



- Performance and reliability degradation
  - Aging, EM, IR drops, stress, switching speed, etc.
- Fine grained thermal analysis on large 3DIC designs not possible using purely traditional FEA/CFD based approaches
- Long sequences of transient power need to be simulated to accurately predict how thermal hotspots change with time

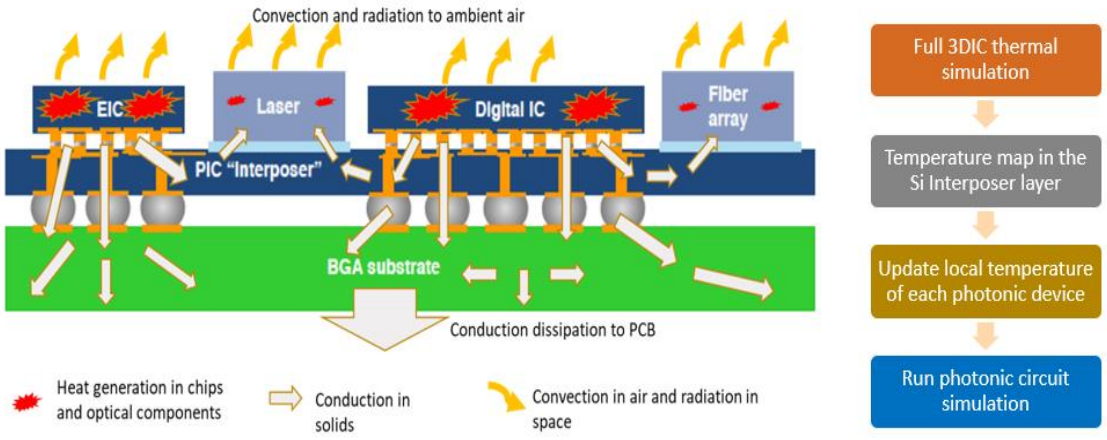
Architecture level fast static/transient thermal analysis for various optimizations are required. (i.e. power/DvD/thermal/stress/test/sensor place)

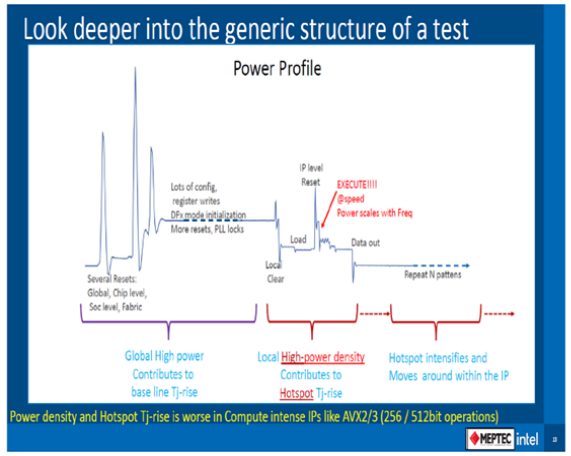


"Emerging Challenges on Thermal Modeling and Simulation for Advanced 3DIC Systems", N. Chang, Keynote, REPP, 2022

Emerging Challenges and Opportunities on Thermal Modeling and Simulation for Advanced 3DIC System

Solving for Digital IC and EIC on heat generation
Solving for PIC Package: heat generation, dissipation, and thermal couplings of chips and optical components





- Scan test
  - ✓ Shift in : many chains w/ 100s of MHz, high Cdyn (about 3-10X of real-world application) w/ high total power
  - ✓ Capture @speed : running at GHz of speed for several cycles, high power density / power, severe Vdroop and high Tj-rise at different locations;
    Tj-rise ↓, Fmax ↑, Vmin ↓, Vdroop ↓, Power ↓
- Functional test
  - ✓ Cache load / Structured Based Functional Test, system ported test
  - ✓ Shmoo plot of Fmax, Vmin, Tj-rise, Vdroop, Power
  - ✓ Thousands of test patterns each of 0.5-1msec generating high power density, Tj-rise, and Vdroop
  - ✓ Tj-rise and Vdroop are correlated too due to leakage power exponential dependence of Tj-rise

Ref : Too Hot to Test workshop, Intel, 2021, https://youtu.be/0gPSbZqbXUg

Challenges and opportunities on thermal modeling and simulation for advanced 3DIC systems:

- Performing fine-grained static and transient thermal analysis on large 3DIC designs is required and demand adaptive meshing or machine-learning technology to overcome the limitation using traditional CFD/FEA based solvers.
- Architecture-level thermal and thermal-induced stress analysis are required due to the thermal coupling from cross-die horizontally and vertically with transient-based power profile among chiplets in 3DIC.
- Heterogeneous Integration 3DICs may consist of analog/mixed-signal and digital designs which have very different thermal and stress requirements that need to be co-optimized among chiplets and package in 3DIC.
- For Silicon Photonics 3DICs, accurate thermal gradient analysis is required for the co-optimization of 3DIC package and required thermal heater for PIC design.
- Testing of large 3DIC consisting of CPU/GPUs, etc. presents a major challenge due to multiple localized thermal hotspots and dynamic voltage drop affecting yield. Co-optimization of test techniques and localized thermal hotspots and Vdroop on 3DIC should be considered.

Grand Challenges in Thermal/Reliability Simulation for 3DIC

Anticipate Physical Integrity Challenges

New ASIC

Architecture Design (Spec)

Functional & Logic Design (RTL)

Schematic / Circuit Design (Netlist)

Physical Design (P&R)

Physical Verification (SignOff)

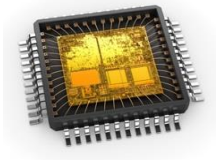
/Ansys

Fab / Foundry / Packaging

Testing & Certification

/Ansys

Production



« Shift **UP** »

Designers wish to have earlier visibility on the effectiveness of thermal/stress integrity

« *Shift Left* »

Floorplanning | PG Grid | Placement | CTS | Routing & Timing → SignOff

Step 1 • Architecture Level Thermal/Stress What-if Flow

Step 2 • RTL/Gate/CPS Thermal/Stress What-if Flow

Step 3 • Handling large 3DIC static/transient thermal Flow

Step 4 • Solving exacerbated CPS/Chip-level reliability issues

Simulation

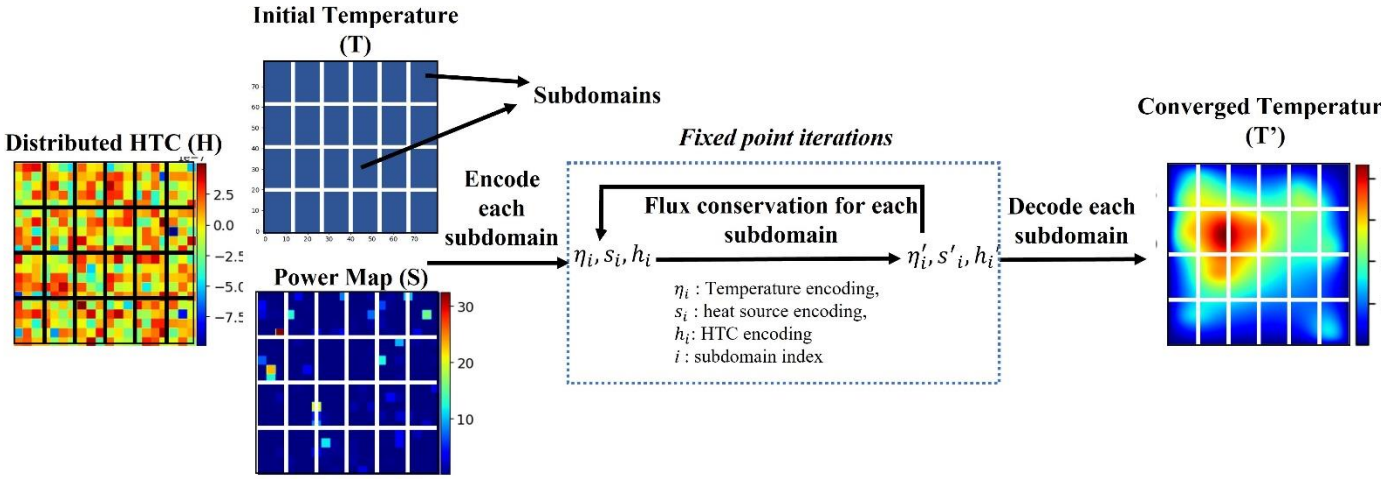
Explorations
Define limits with Physics

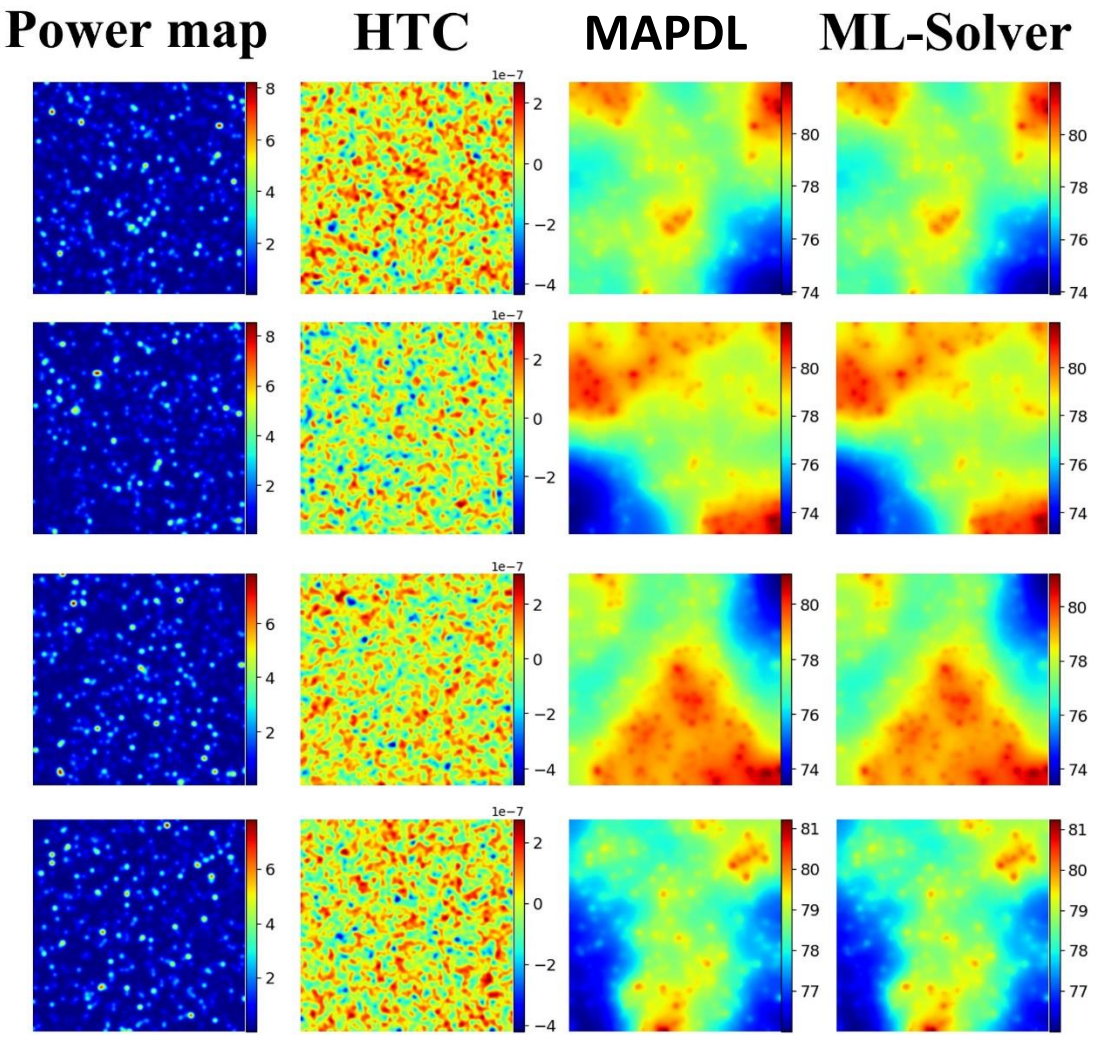
Validation
Confirm Layout with Physics

Qualification
Calibrate the Models

Possible Machine-learning based Static Thermal Solver with Distributed HTC

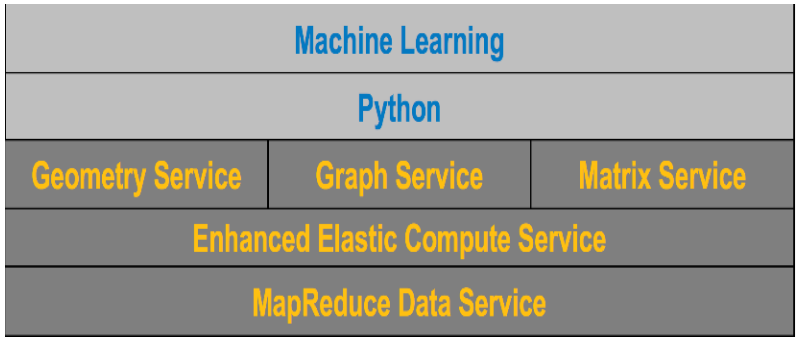
- Developed a novel Machine-Learning based Thermal solver to accurately predict chip temperatures for arbitrary power maps and distributed HTC patterns.
- The ML-Solver is inspired from keys ideas of traditional Ansys solvers. It iteratively solves for temperature on discrete subdomains given the power map, HTC and initial temperature. Flux conservation in each iteration is established using pre-trained ML models
- The ML-Solver is about 100x faster than current solvers and accurately predicts high-fidelity temperature maps on the chip.



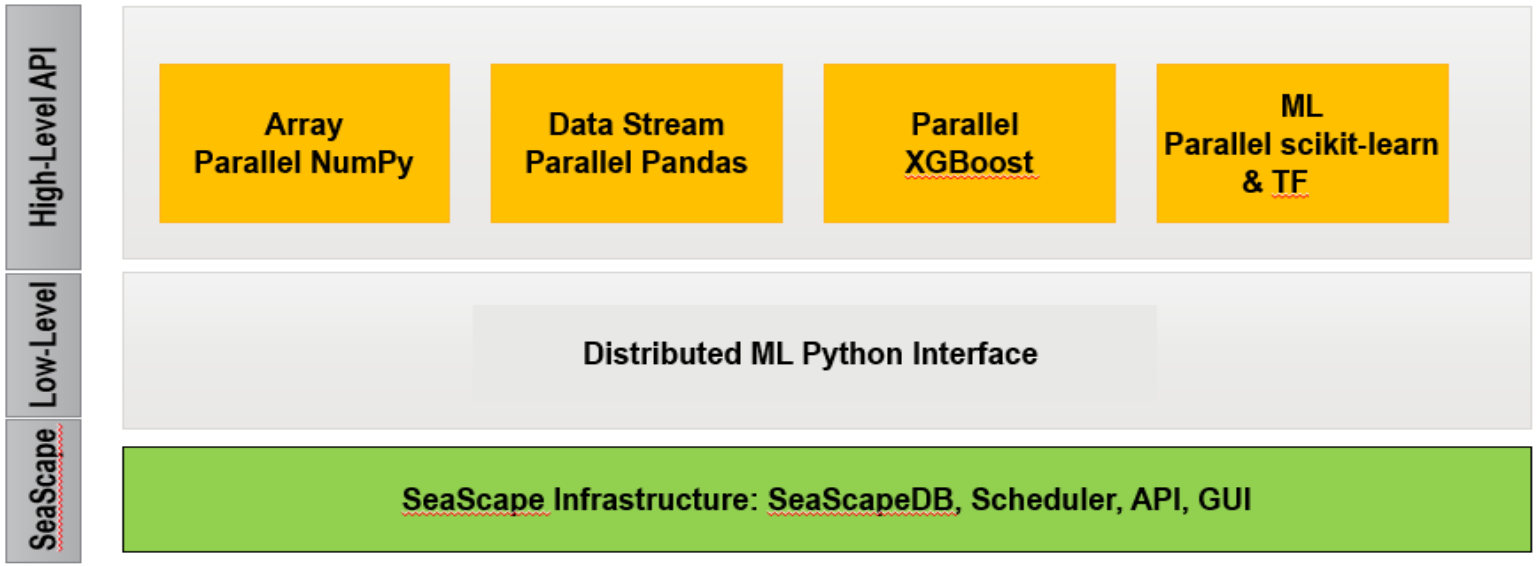


Ranade, R., Haiyang, H., Pathak, J., Kumar, A., Wen, J. & Chang, N. (2022). A Thermal Machine Learning Solver for Chip Simulations. *4th ACM/IEEE Workshop on Machine Learning for CAD*

Thermal Multi-physics Solving Augmented by Distributed ML Framework



SeaScape Distributed Computational Platform



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2. "High-Speed, Low-Storage Power and Thermal Predictions for ATPG Test Patterns", Z. Liang, N. Chang, et al., ITC, 2023
3. "A Composable Machine-Learning Approach for Steady-State Simulations on High-resolution Grids", R. Ranade, et al., Neurips, 2022
4. "A Thermal Machine Learning Solver for Chip Simulation", R. Ranade, H. He, J. Pathak, N. Chang, A. Kumar, J. Wen, IEEE MLCAD, 2022
5. "ML-based Fast On-chip Transient Thermal Simulation for Heterogeneous 2.5D/3D IC Designs", N. Chang, A. Kumar, J. Wen, H. He, S. Pan, D. Geb, W. Xia, S. Asgari, M. Abarham, Q. Li, Y. Li, Z. Feng, IEEE VLSI-DAT, 2022
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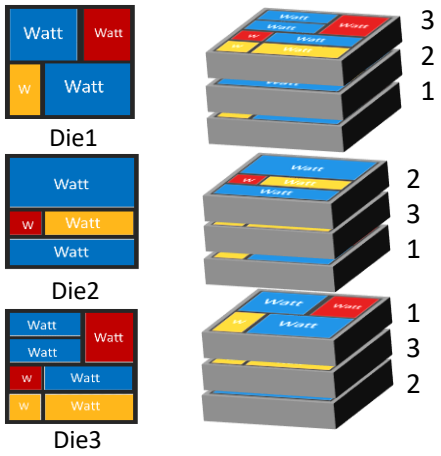
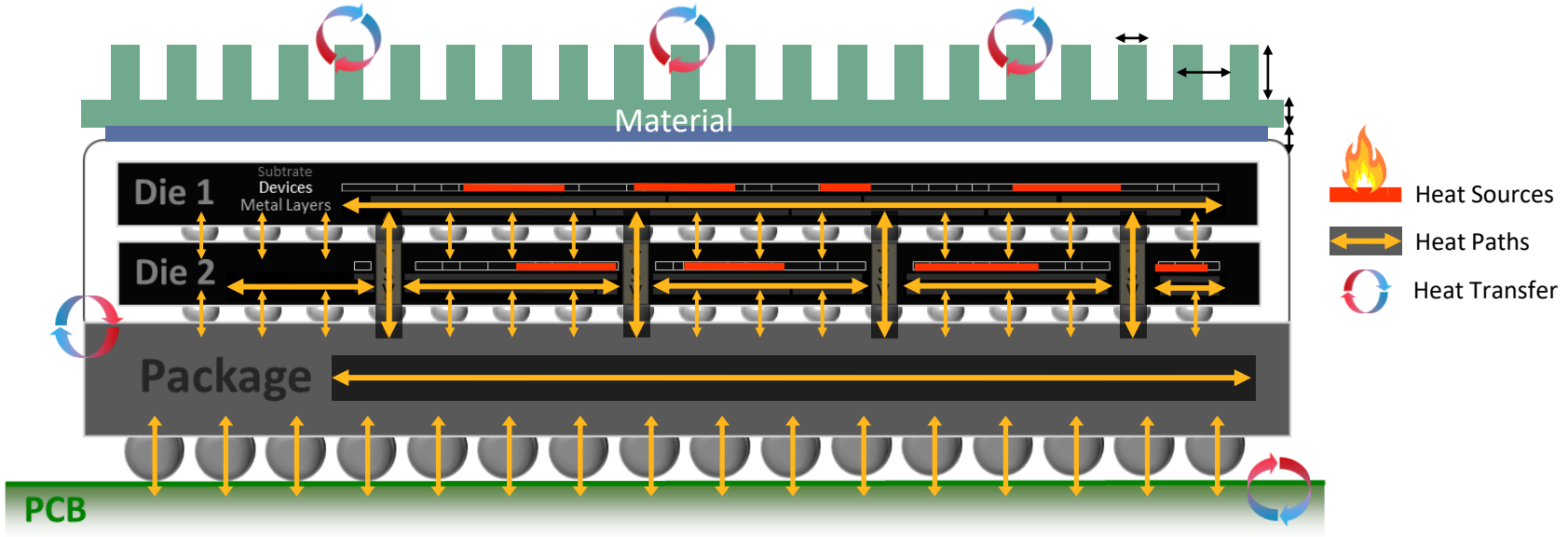
12. "DNN-based Fast Static On-chip Thermal Solver", J. Wen, S. Pan, N. Chang, W. Chuang, W. Xia, Deqi Zhu, A. Kumar, E. Yang, K. Srinivasan, Y. Li, IEEE SEMI-THERM, 2020.

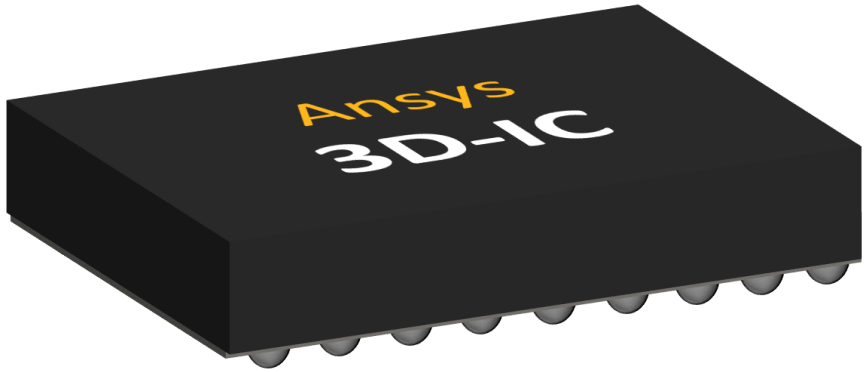
3D-IC Thermal Integrity



Power Distribution in 3D



Heat Dissipation

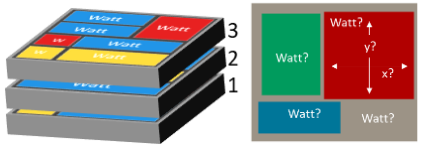


Simulation is driving Implementation

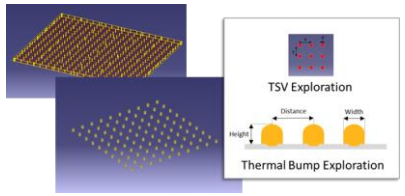
Machine Learning is enabling Simulation-based optimization

ML-based Power & Thermal Design Space Exploration in System Technology Co-optimization (STCO)

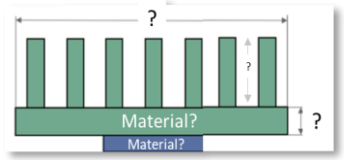
CTM, other power source



Die/pkg/pcb/tsv/bump model



Heatsink, Boundaries model



✓ **Bill of Material**
✓ **Architecture**

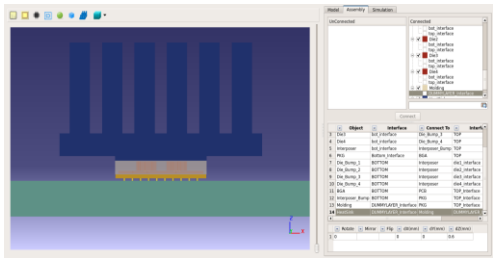
✓ **Performances**
✓ **Cost**

Exploration module
Power, Heatsink, BC

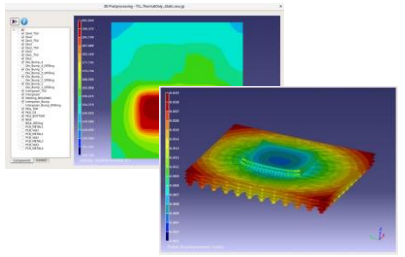
Goals setting
Max T°, Gradient, Warpage…

/ML Optimizer

Model Assembly → Static, Transient → Temp contour, Thermal Stress, …



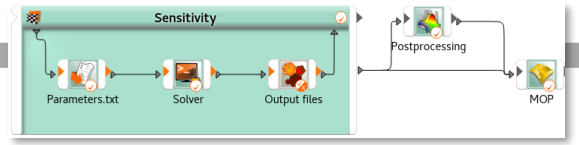
Thermal/ Stress Solvers



Results Postprocessing
✓ **Warpage**
✓ **T°$_{Max}$** (EM)
✓ **ΔT°** (Timing)

/ML Optimizer

Variable Sweeping

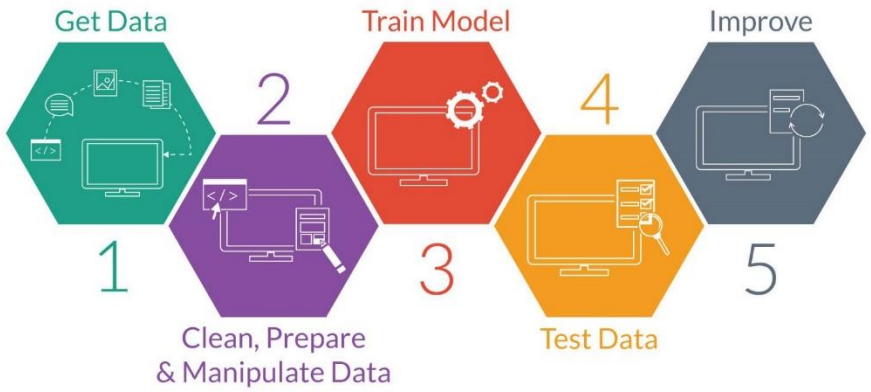


Sensitivity Analysis

ML-based MetaModel Training

Need for “Thermal aware” Architecture Validation with the Help of Machine Learning

ML-based Adaptive Metamodel of Prognosis Framework



AMOP for scalar values:

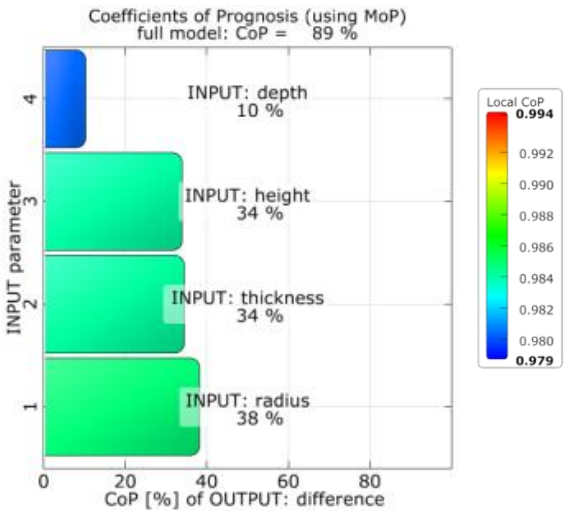
- Objective measure of prognosis quality = **CoP**
- Determination of relevant parameter subspace
- Determination of optimal approximation model
- Approximation of solver output by fast surrogate model without over-fitting
- Evaluation of variable sensitivities

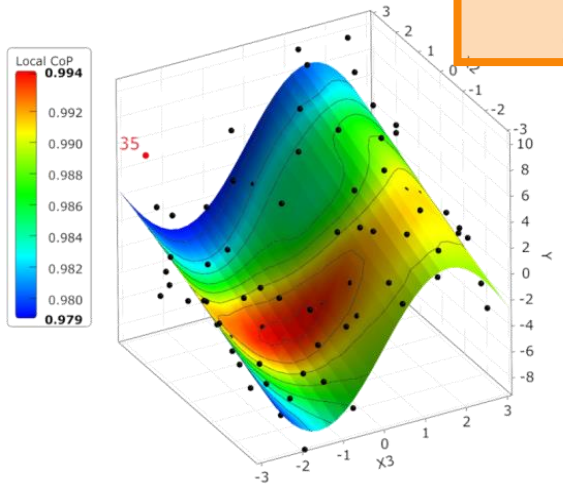
calculate forecast quality using **CoP** (**C**oefficient **o**f **P**rognosis)

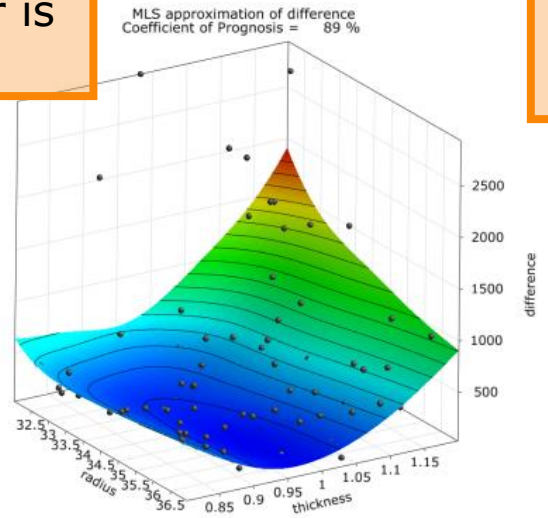
The winner is … **MOP**

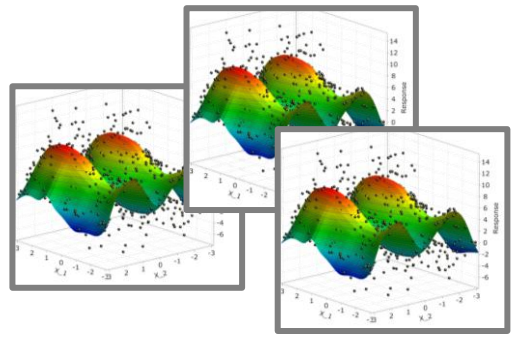
investigate response by response based on DOE sampling

generate competing meta-models









Optimization of Mobile Pkg Material Calibration for Thermal/Stress Integrity

As-is process/Challenges

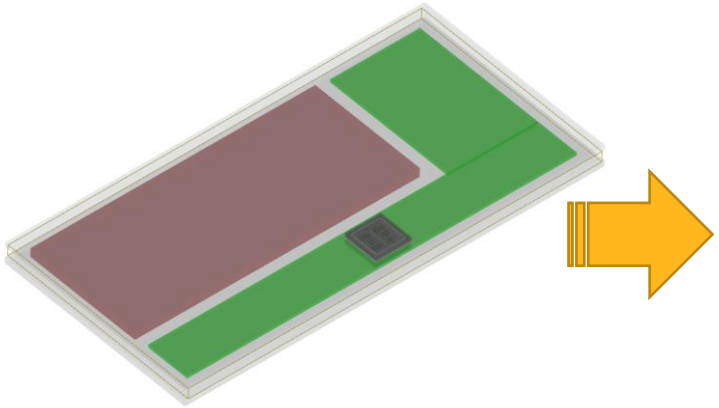
- Sensitivity analysis of thermal material properties of mobile AP
- Fast and Accurate equivalent virtual thermal testing model → Simple Model
- Trial & Error approach for fine tuning material → Expensive!
- Too many trials (1000+) need to be performed for 10+ parameters
- Challenges:
  - Significant manual effort for 1000+ trials
  - Accurate simple model for transient thermal analysis
  - Reduced Dependency on package type

Ansys Value Stream

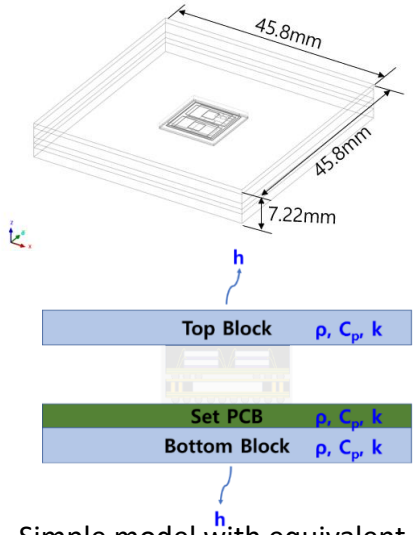
- Robust workflow integration and optimization with optiSLang-AEDT Icepak
- Reduced input BC conditions and material properties (h,K,CP and Den)
- Sensitivity analysis with thermal material parameter of components.

Outcome

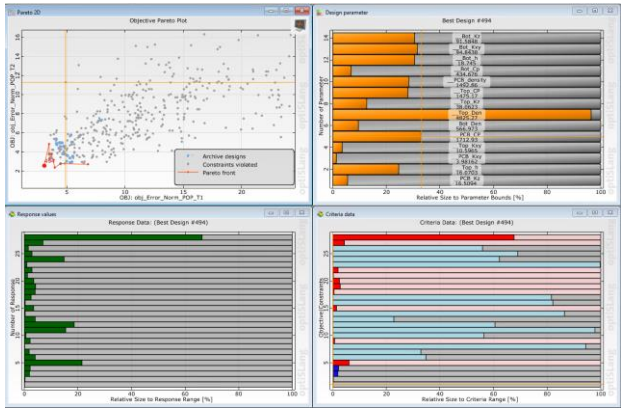
- Extract optimized equivalent properties of Simple model that is well matched with reference data
- Automatic DOE reduction to reduce the overall time for optimization.
- Reduced time for optimization and increased accuracy
  - 2~4 Weeks → 4~5 Days

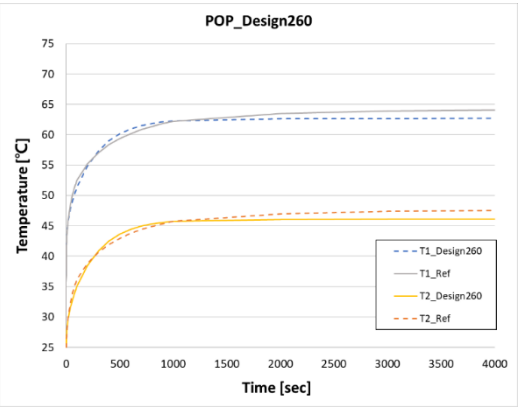


Full set model of smartphone



Simple model with equivalent thermal material property





"Thermal Model Simplification of Mobile Device with Adaptive Metalmodel of Optimal Prognosis (AMOP)", V. Krishna, et al., iTherm, 2022

Summary

- Thermal plays a key role in 3DIC Multiphysics interaction and demand for fast early architecture trade-off and layout-level sign-off solutions
- Customized ML technology enable innovative applications in the speed-up of Multiphysics simulation and fast in-process co-optimization
- optiSLang can work with Ansys Multiphysics tools and other companies' tools for co-optimization of design workflow including thermal-centric co-optimization scenario

Acknowledgement

- Thanks to Akhilesh, David, Mehdi, Saeed, Haiyang, Rishi, Wenbo, Prakash, Chris, Lang, Jerome, Preeti, Hua, Zakir, Chunta, Jibin, Mallik, Jay, Tianhao, Prith, and Ying for many discussions of fast thermal simulations and GPT applications

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Ansys