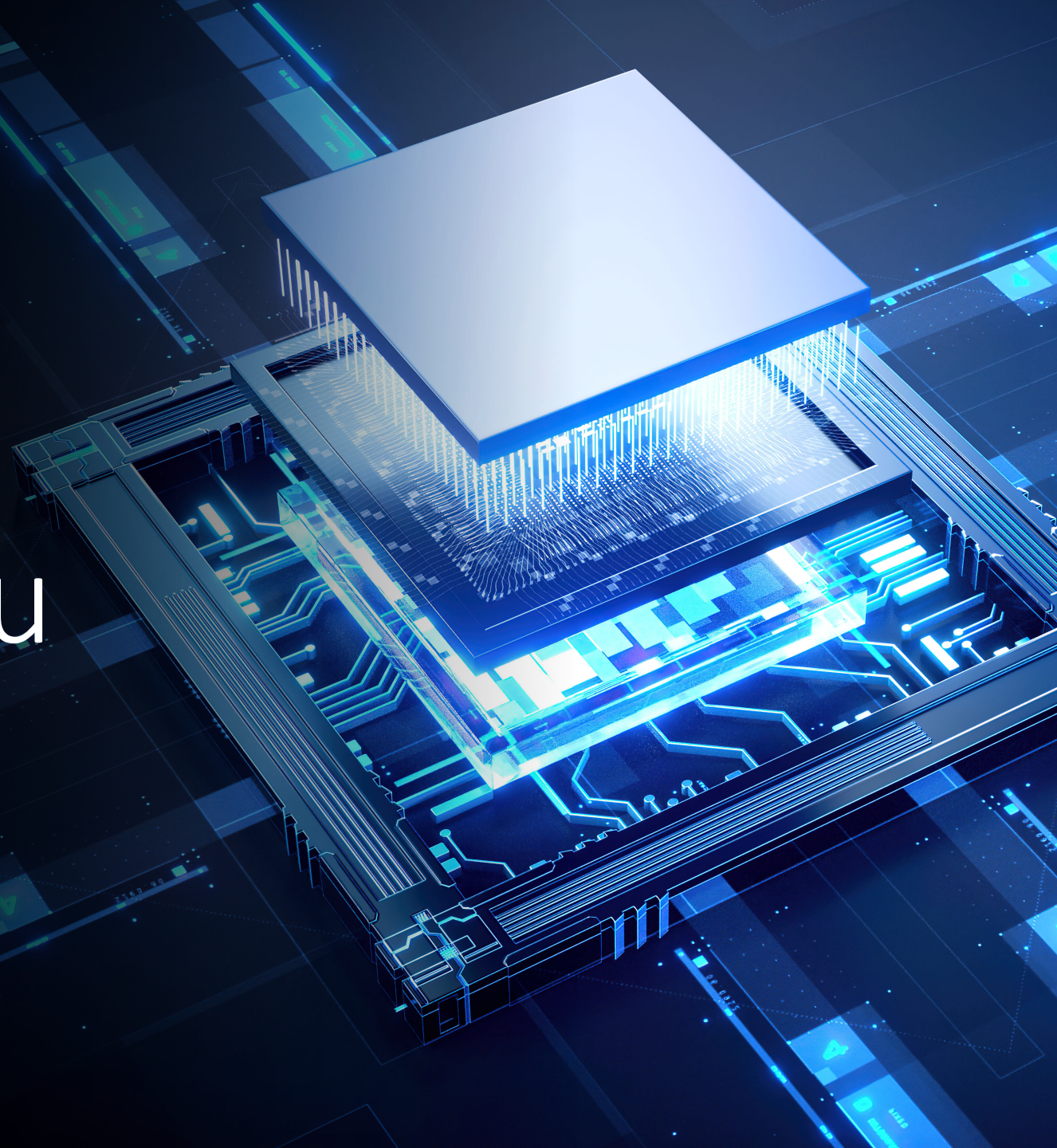
Si2: Value and Velocity with You



Robert Aslett

CEO Silicon Integration Initiative (Si2)

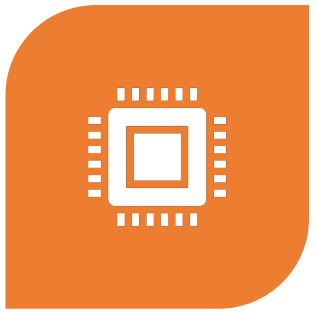
https://si2.org

Electronic Design Process Symposium

Oct. 5 Sunnyvale CA.

or.. Planes, Trains and Automobiles

Outline



SILICON INTEGRATION INITIATIVE (SI2)

VISION AND IDEAL STATE

SOLVING THE VELOCITY PROBLEM

STRATEGY 1.1

Prologue

“ I am he as you are he as you are me
And we are all together”

- I am the Walrus by John Lennon / Paul McCartney

Prologue … in other words

Si2 is us

When industry-wide collaboration is needed, the Si2 community provides the means to deliver more value to its members than they can achieve alone.

Key Messages

- Si2's vision is to apply its purpose to the entire scope of semiconductor design.
- Our ideal state is when we deliver the greatest value, when it is needed, and then increase it through virtuous cycles of value creation $(VC)^2$.
- The relative success of OpenAccess and Compact Model Coalitions have not been replicated. The reason for this is our velocity lags that of the industry.
- We must rethink our approach, so critical programs covering UPM, 3D multi-die, processed data, AI/ML, data mgmt. and other opportunities deliver value sooner.
- Our strategy is evolving but there are three things we should do now: 1) deepen member engagement; 2) shorten learning cycles, and 3) harmonize our roadmaps.

Si2 Purpose

Provide collaborative technology and services which enable advanced semiconductor design integration, leading to industry-accepted standards.

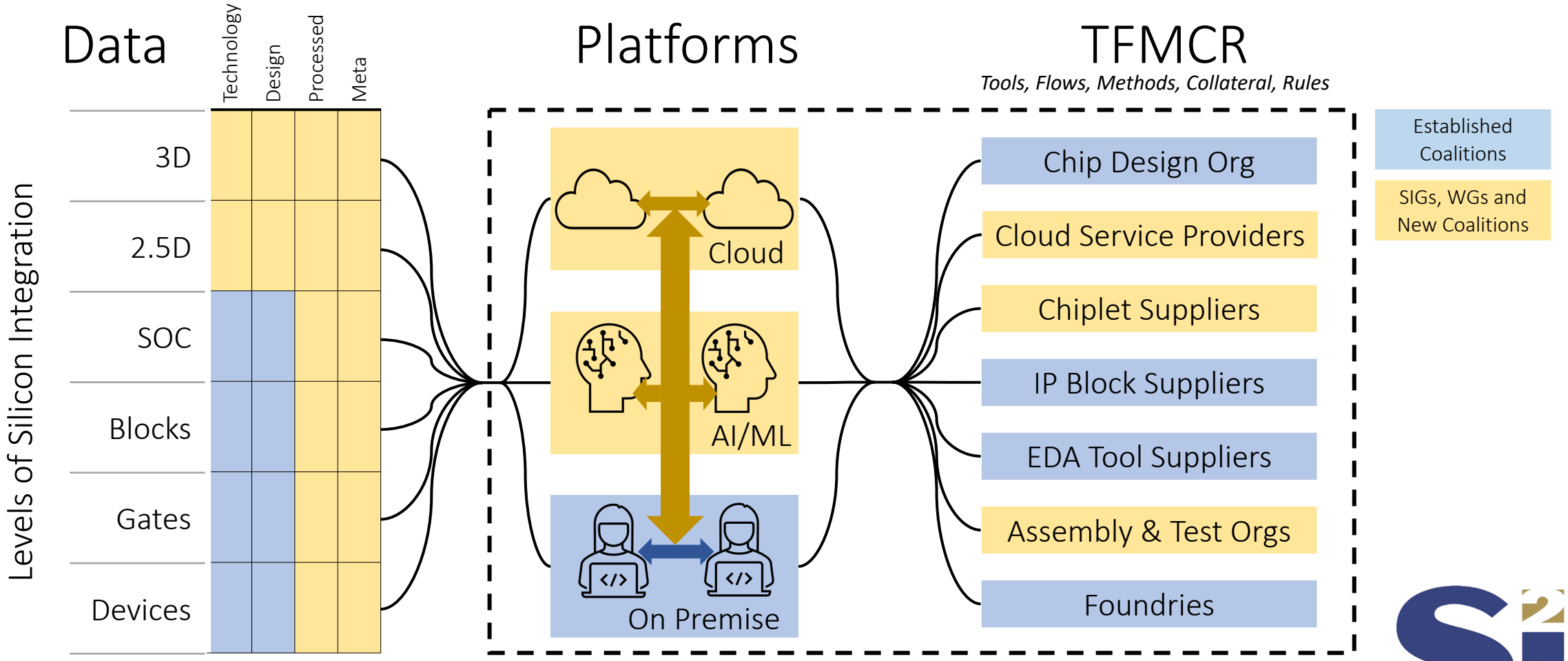
Offer these standards, technology, and services to all interested organizations and individuals at a fair and reasonable cost.

Si2 is driven by its members

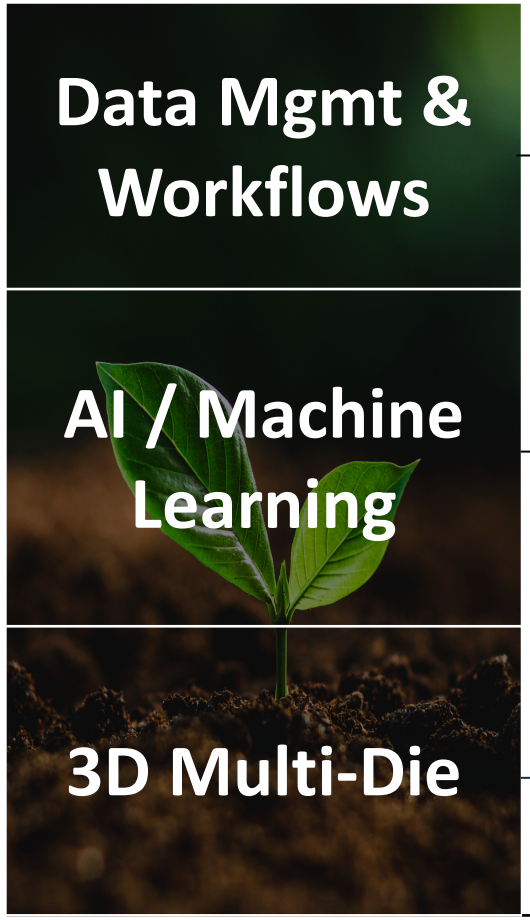
Not shown: the Si2 Board of Directors and the Technology Steering Group

Vision: Address the growing scope of semiconductor design

many to many: interoperability is critical



Current SIGs and OpenStandards Working Groups



Focus: Time-consuming data management tasks of 1) locating and accessing the data needed, 2) reducing, sorting, organizing data for processing and 3) Correlating design and test data.

Focus: Best practices and current gaps in AI and ML strategies for EDA digital design that affect interoperability.

Focus: Workflows that integrate 3D multi-die components while ensuring interoperability and a secure supply chain with traceability across suppliers.

Focus: A standard format for, and means of, securely sharing high volumes of processed data resulting from AI and cloud-based pre/post-Si design and test flows.

SIGs

OpenStandards WGs

Current Coalitions

A collaborative environment based on an extensible reference API that defines classes and member functions to create, access & manage design databases throughout the design process.

A collaborative environment focused on selecting, standardizing and then developing Verilog-A descriptions of standard SPICE device models and useful APIs.

Forming: A collaborative environment focused on helping member companies benefit from the UPM/IEEE-2416 power standard by integrating the standard into their workflows via development of IP-to-system power models, tools & methods.

Si2 Ideal State

Deliver the greatest value, when it is needed, and then increase it through virtuous cycles of value creation

Value

Results have value if they contribute to Si2's purpose in a way that members will pay

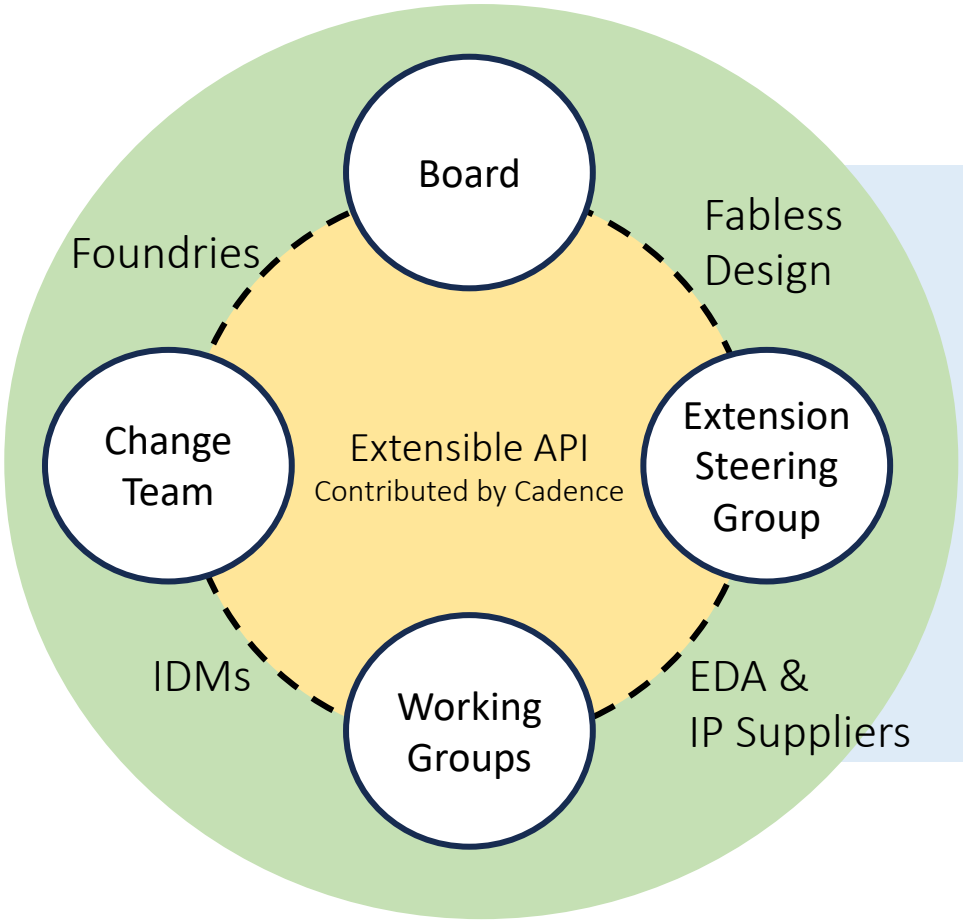
Note: Members pay with their time, technology contributions and dues

Virtuous Cycles of Value Creation (VC)^2

Collaboration cycles that build on previous results and deliver increasing value.

OAC: An example of Virtuous Cycles of Value Creation

A collaborative environment based on an extensible API; supported by Si2 staff



47 corporate members; 20+ years of innovation

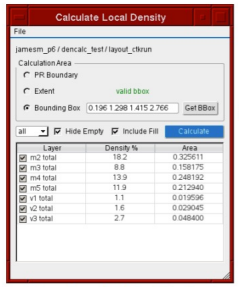
- Continuous development of extensions in a way that assures compatibility with related applications.
- Rapid prototyping and innovation on top of the trusted industry standard
- Set development priorities for the reference implementation
- Redistribution rights for executables developed using SW developed by Si2 staff and contributed by members.

OAC: A sampling of extensions

Source: James Masters & Benjamin Hoefer (Intel) - Si2 OA Workshop (9/28/2023)

Density Calculator

oaScript + oaxPop : Density Calculator



Density calculated using oaShapeQuery and oaxPop

Density Calculator: Quick in-editor solution for real-time density feedback

- All mask layers with full hierarchy depth supported
- Derived layer calculations available (not shown here)

Performance on medium-size block

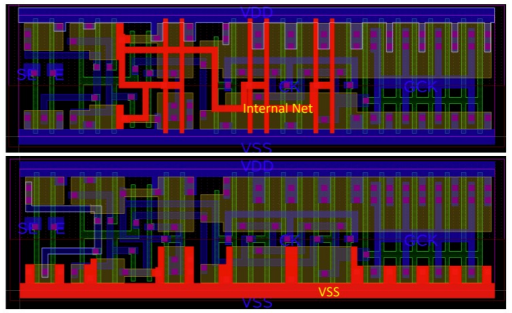
- Hierarchy depth: 4
- Number of queried layers: 19
- Shape count: ~277k
- Runtime: ~1 second* (with C++ helper class)

Bounding box query received from layout editor

Node Highlighting

oaxPop : Node Highlighting

- Extracted connectivity on all cells within NanGate* StdCell contribution to Si2
- Verified functionality by spot-checking dozens of cells
  - Found and fixed some bugs
  - Included text labels (nets)
- Shown example (right):
  - CLKGATETST_X8
  - Internal Net (top)
  - VSS Net (bottom)

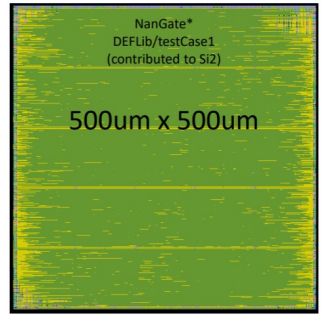


Block Signal Extraction

oaxPop : Block Signal Extraction

- M1-M5, 3.7M shapes, 50k instances
- Extracted ~144k nodes
- Total runtime ~1m 40s (~1m insert + ~37s extract)

Layer	# Shapes	Insert Time
metal1	620461	11.84
via1	268895	4.94
metal2	1146388	19.38
via2	423655	8.09
metal3	847523	14.18
via3	137119	2.39
metal4	227053	3.64
via4	34974	0.57
Metal5	52772	0.66
Total Insert	**3758840**	**65.69**
Total Extract		**37.61**
Total Runtime		**103.30**

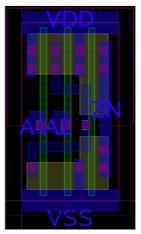


Layout Netlist Creation

oaxPop: Layout netlist creation

- **Objective:** extract connectivity and create a SPICE* layout netlist
- **Application:** Layout-versus-schematic (LVS)
- Code Profile:
  - Python code, 335 lines total (w/comments)
  - YAML config – derived layers, connectivity, device formation and terminals
  - Demonstrated on several NanGate* standard cells, contributed to Si2
  - Example will be included in oaxPop v2.0 release

OA Design



YAML Config

```
connect:
  poly:     [contact, ngate, pgate]
  ndiff_sd: [contact]
  pdiff_sd: [contact]
  metal1:   [contact]

devices:
  nmos:
    layer: ngate
    terminals:
      d: [ndiff_sd, left]
      g: ngate
      s: [ndiff_sd, right]
    parameters:
      w: width
      l: height
  pmos:
    layer: pgate
    terminals:
      d: [pdiff_sd, left]
      g: pgate
      s: [pdiff_sd, right]
    parameters:
      w: width
      l: height
```

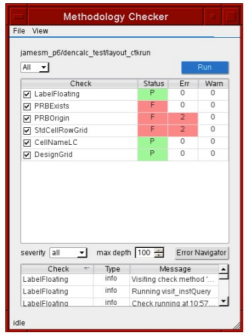
Note: for brevity, the derived layers definitions in this YAML config are not shown here.

Output

```
.subckt AND2_X1 A1 A2 ZN
Mm0 VDD A1 _n0 pmos w=0.05 l=0.315
Mm1 _n0 A1 _n1 nmos w=0.05 l=0.21
Mm2 VSS _n0 ZN nmos w=0.05 l=0.415
Mm3 VDD _n0 ZN pmos w=0.05 l=0.63
Mm4 _n1 A2 VSS nmos w=0.05 l=0.21
Mm5 _n0 A2 VDD pmos w=0.05 l=0.315
.ends
```

Methodology Checker

oaScript + oaxPop : Methodology Checker



Error Navigator started in layout editor

Methodology Checker: Quick check of design methodology compliance

- All mask layers with full hierarchy depth supported
- Many other Intel-specific checks exist (not shown here)

Use of oaxPop essential

- DesignGrid: `err = wires - grid`
- StdCellRowGrid: synthesize row grid; `err = stdcell_prb - row_grid`
- LabelFloating: 2x2 DBU label squares; `err = lbls - lbls.touching(shps)`

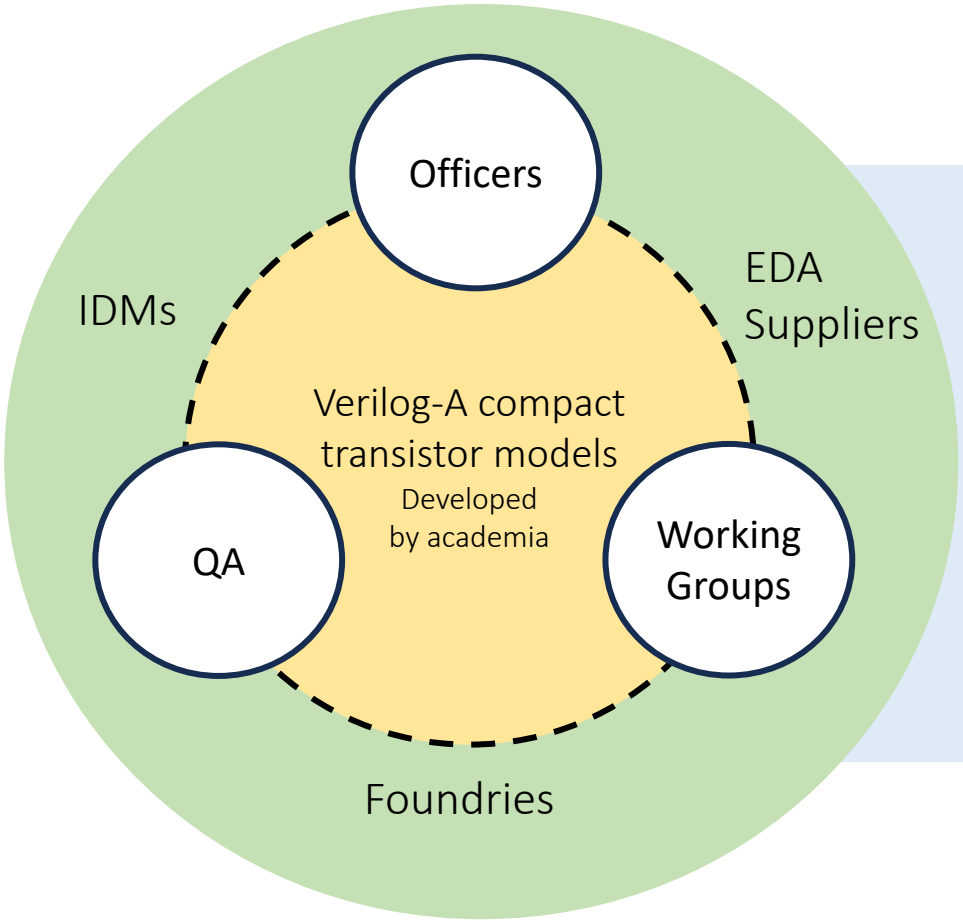
Color Shifting

oaxColor Overview

- In 2012 Cadence authored a *Data Model Specification for "Multi-Pattern Technology Support"* document
- oaxColor WG has released an OpenAccess extension implementing an API to read/write coloring information according to the Cadence specification
  - C++ reference implementation
  - Scripting support with oaScript (python, ruby)
  - Developed on top of the extension framework (oaxPop, oaxConn, etc)
- **Goal**: Standardize how OpenAccess users interact with MPT Coloring information in an accessible and extensible API.

CMC: An example of Virtuous Cycles of Value Creation

A collaborative environment based on compact model R&D; supported by Si2 staff



32 corporate members; 28 years of innovation

- Selection of standard models, APIs and related utilities.
- Alignment of R&D worklists with member priorities.
- Continuous refinement in a way that assures compatibility and accuracy with target applications (e.g., circuit simulators).
- Redistribution rights for executables developed using released Verilog-A descriptions.

CMC: The growth of standard compact models

CMC Working Groups
Chaired by CMC Members

CMC Members

Model Developers

BSIM: UC Berkely

HSIM: Hiroshima Univ.

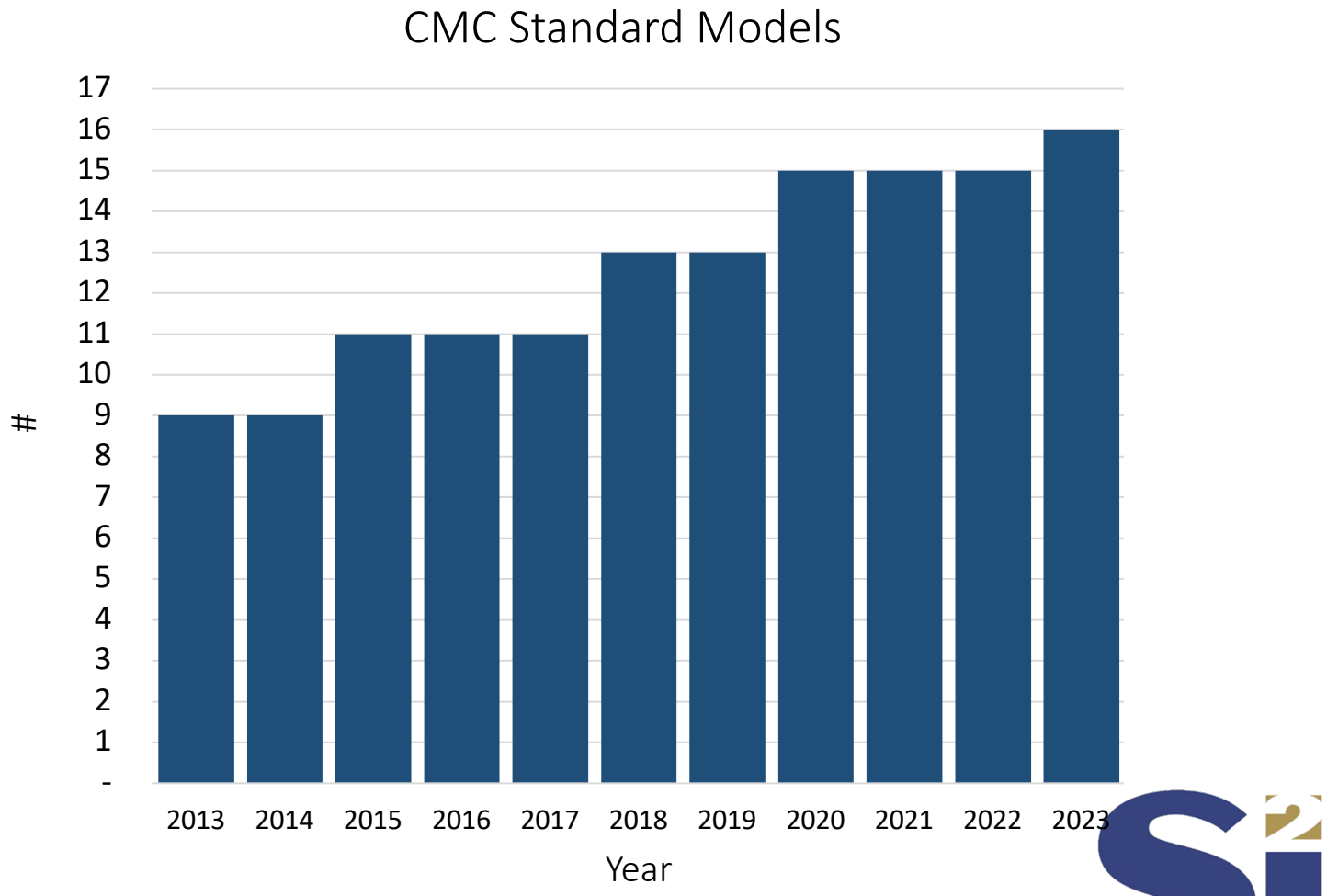
HICUM: UC San Diego/AD

PSP, L-UTSOI: CEA-LETI

HEMT, ESD: Macquarie Univ.

MEXTRAM: Auburn Univ.

MVSG: Waterloo University



However, we have not replicated this in other areas

The primary issue is velocity, where:

$$\text{Velocity} = \Delta\text{Value}/\Delta\text{time}$$

measured from SIG or WG start to production usage by an engineer.

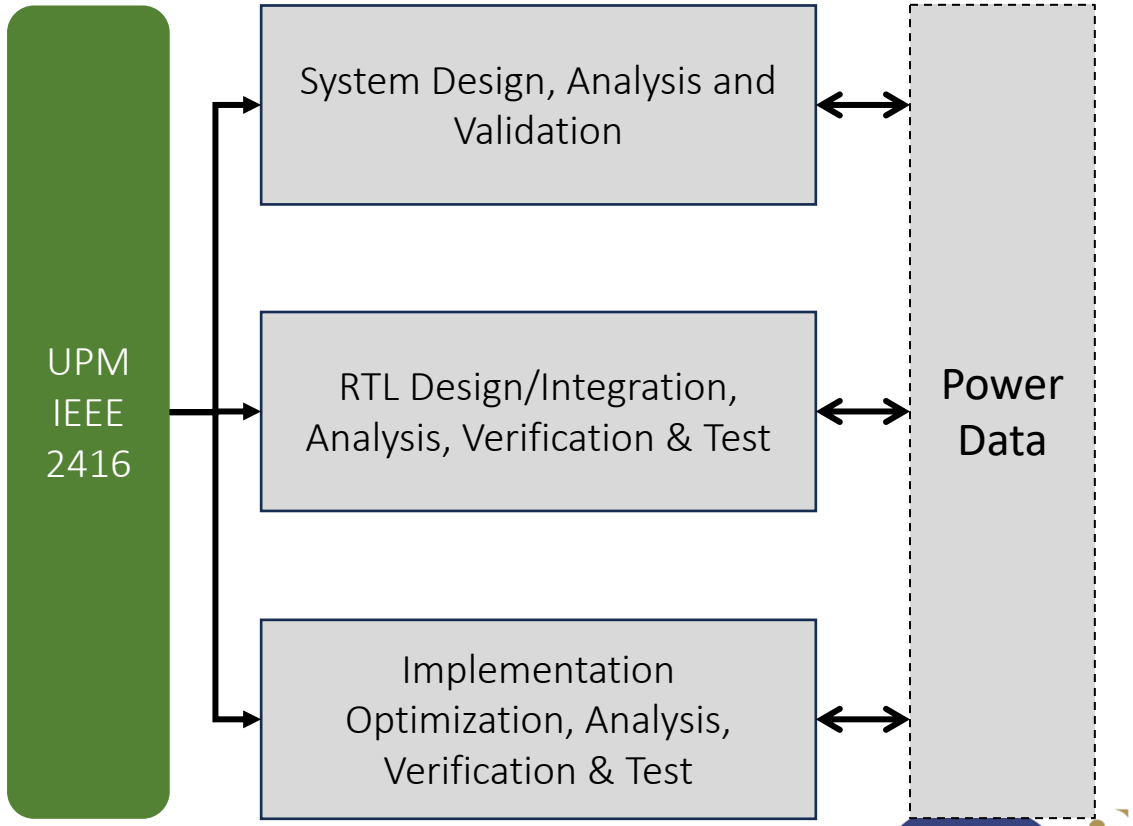
Example: The Unified Power Model (UPM)

IEEE 2416-2019

“ This standard describes a parameterized and abstracted power model enabling system, software, and hardware intellectual property (IP)-centric power analysis and optimization.

It defines concepts for the development of parameterized, accurate, efficient, and complete power models for systems and hardware IP blocks usable for system power analysis and optimization.

These concepts include, but are not limited to, process, voltage, and temperature (PVT) independence; power and thermal management interface; and workload and architecture parameterization. “



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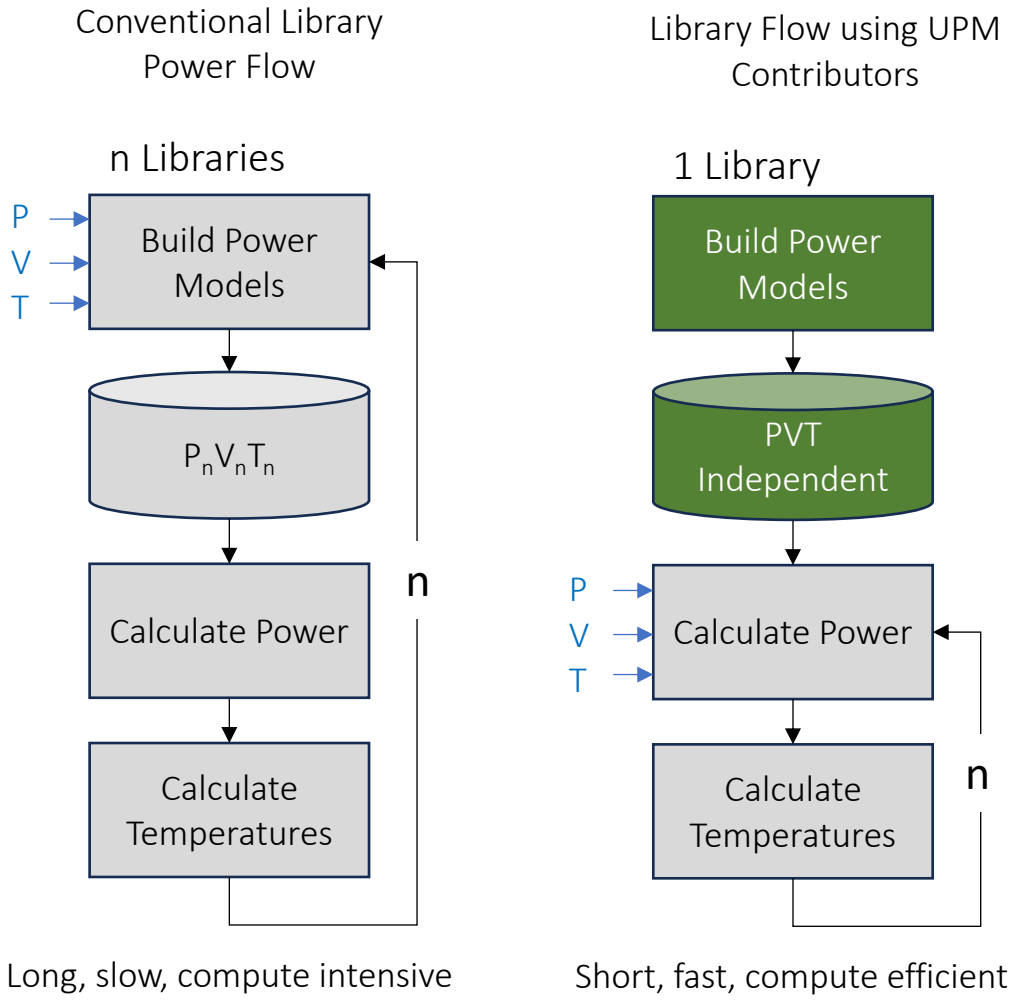
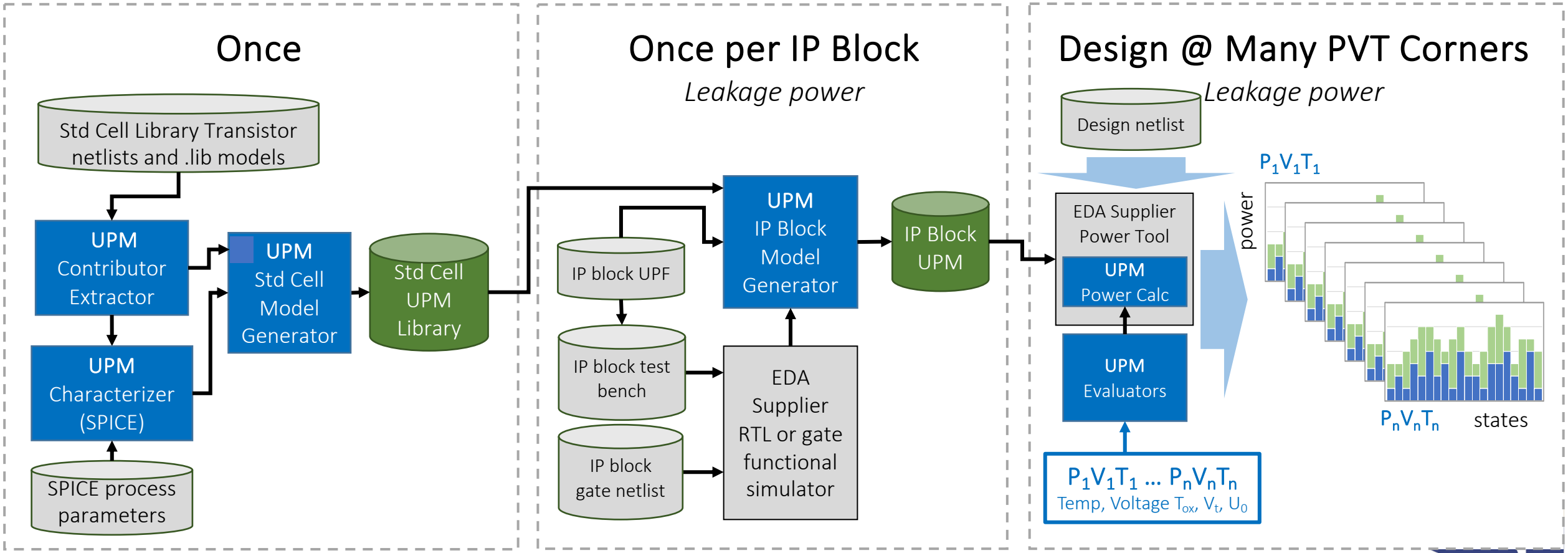


Example: UPM for an IP Block

new capabilities developed to enable the UPM standard

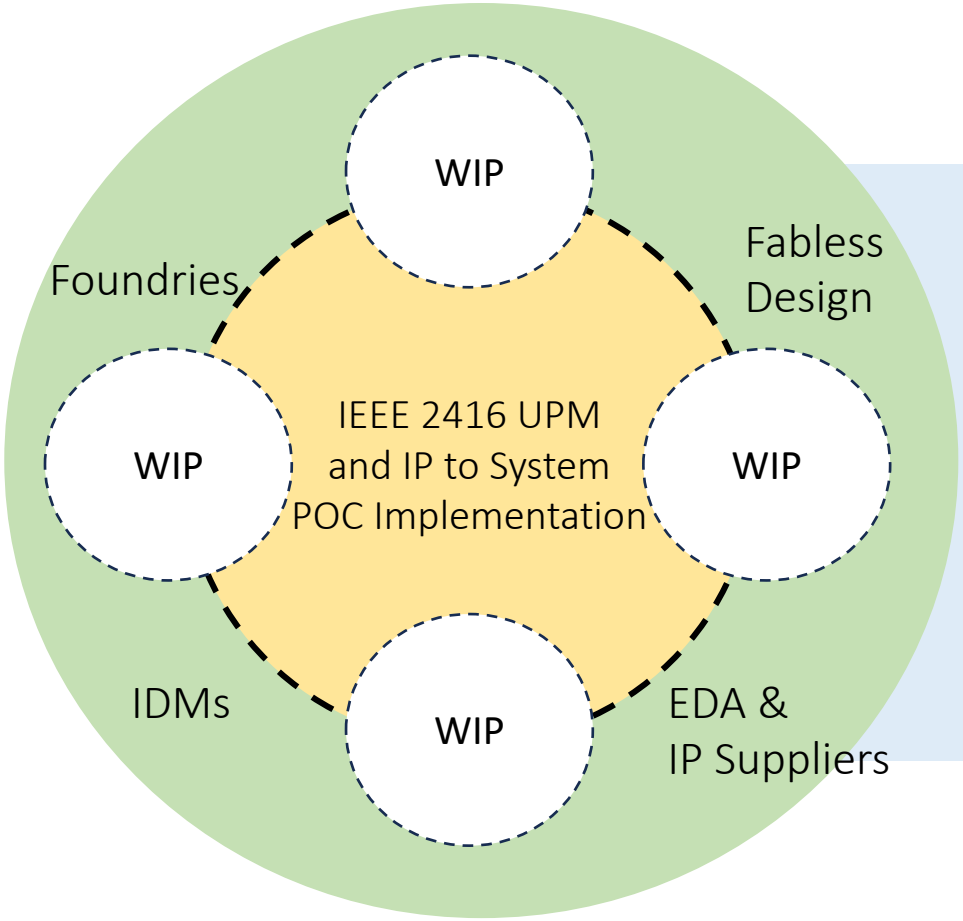
The UPM Model

Existing Capabilities



The New Unified Power and Thermal Coalition

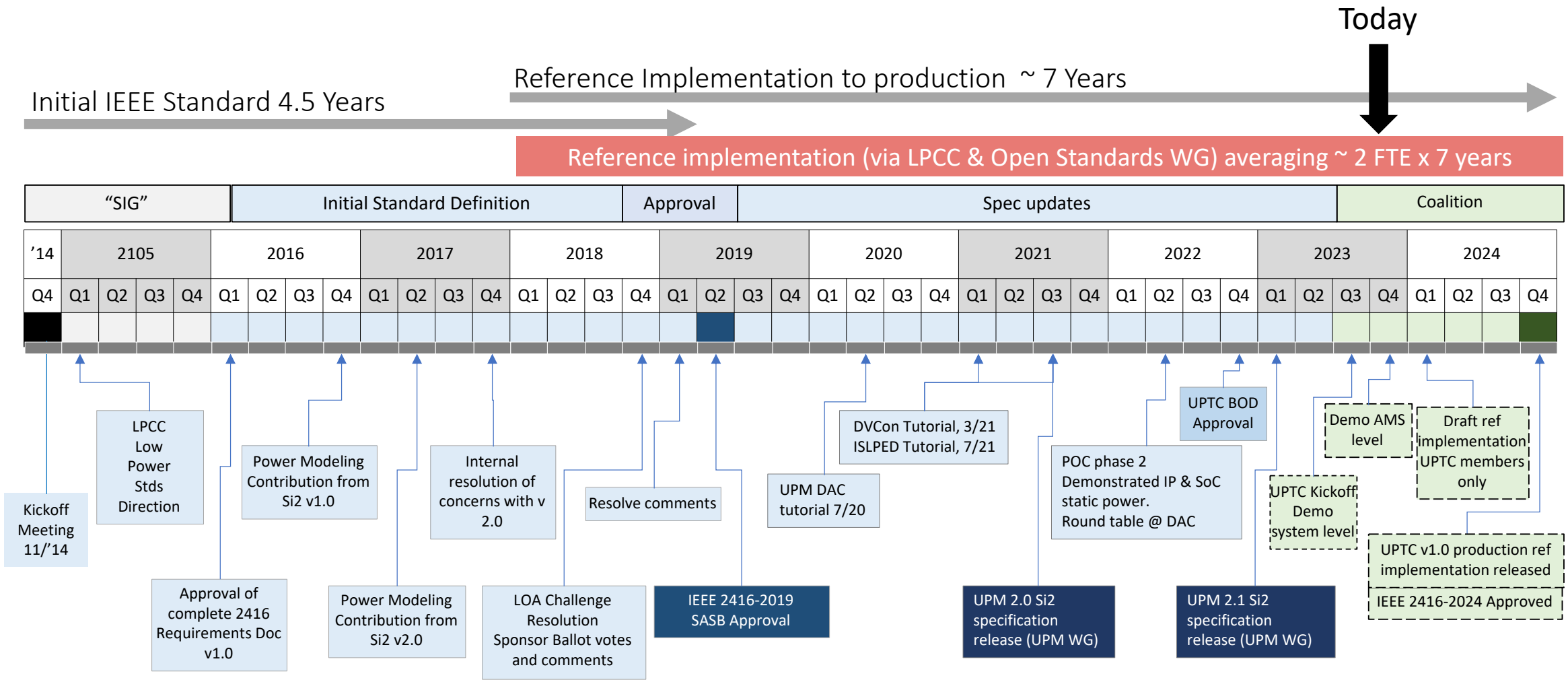
A collaborative environment based on IEEE 2416 UPM; facilitated by Si2 staff



5 → 9 corporate members; just starting

- Prototyping and innovation on top of a trusted industry standard
- Continuous development of related technology in a way that assures compatibility
- Collective influence on development priorities of the reference POC implementation and related EDA tools
- Redistribution rights for executables & products developed using the software developed by Si2 and contributed by others

Sounds good, but it took 9 years to get to this point.

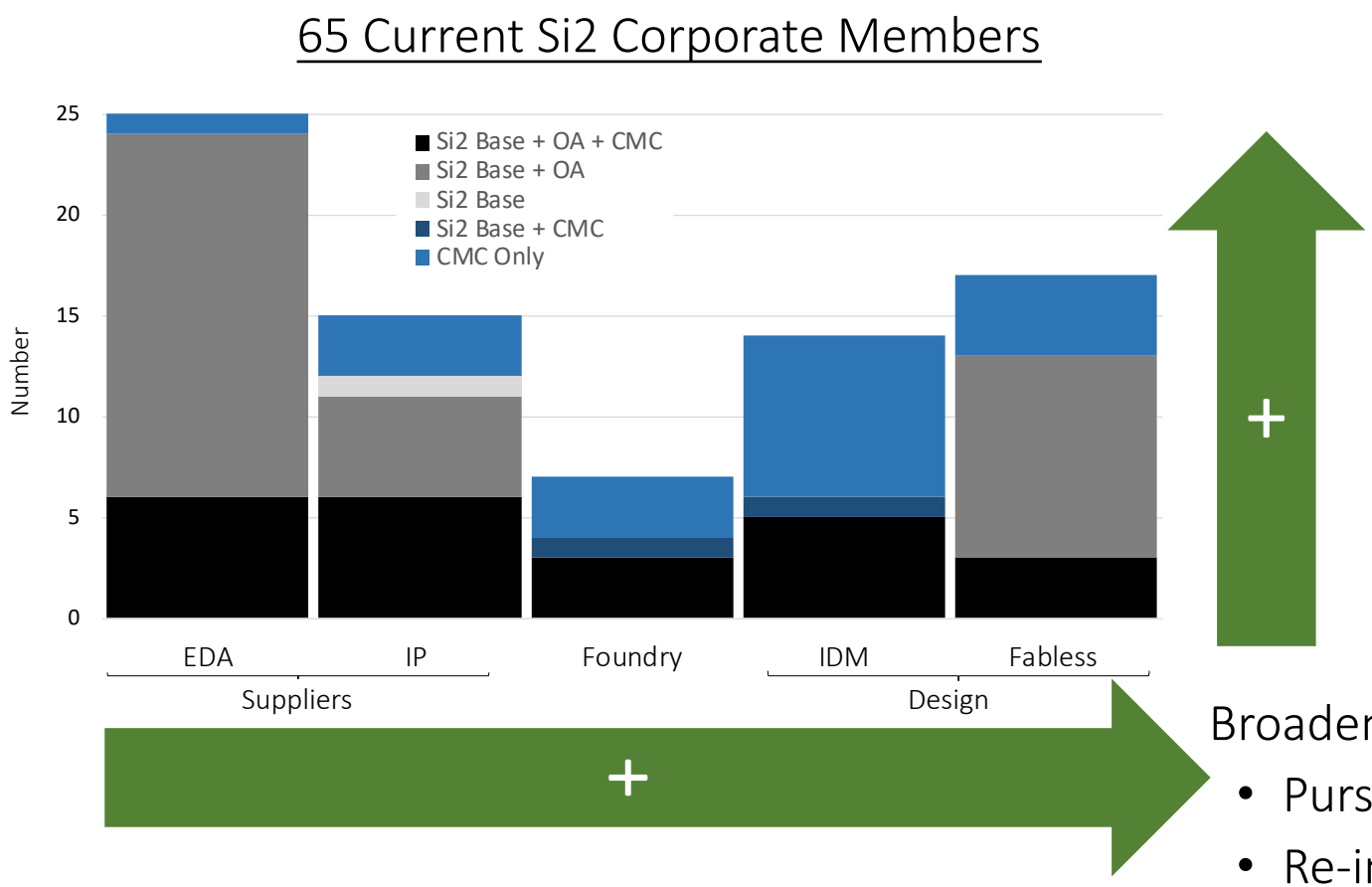


How do we increase our velocity?

We must rethink how we identify and co-develop new Si2 standards, related collateral and POCs.

While we have those conversations there are three things we should do now that will help….

1. Broaden, deepen member engagement to obtain strong agreement on value – increase the numerator



Add missing members per segment and deepen participation from those already here by:

- Increasing collaboration return (value)
- Decreasing collaboration cost
- Factoring in opportunity cost

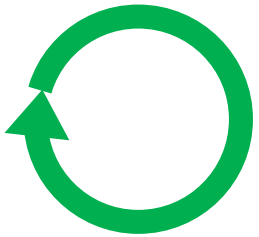
$C_{premium} = C_{return} - C_{cost} - C_{opportunity}$

$C_{premium}$ must be >>0

Broaden expertise represented in Si2 by:

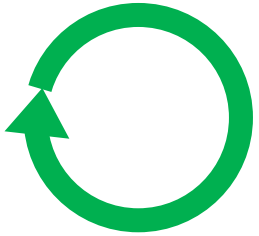
- Pursuing new adjacencies (e.g., Assembly & Test, CSPs..)
- Re-invigorating academic memberships
- Engaging with relevant gov't programs

2. Shorten learning cycles to get to the best implementation sooner – reduce the denominator



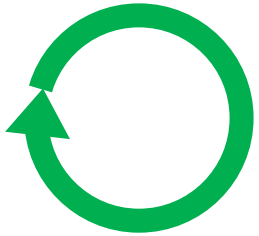
Special Interest Groups

- Socialize, hypothesize, publish
- Report out to TITAN on a regular cadence for re-commitment



OpenStandards Working Groups

- Apply “Look, Ask, Model, Discuss, Act (LAMDA)” for rapid POCs
- Release min. viable features/POCs on a set cadence for early, frequent feedback
- Hire and apply Si2 funded engineers or contractors at critical points

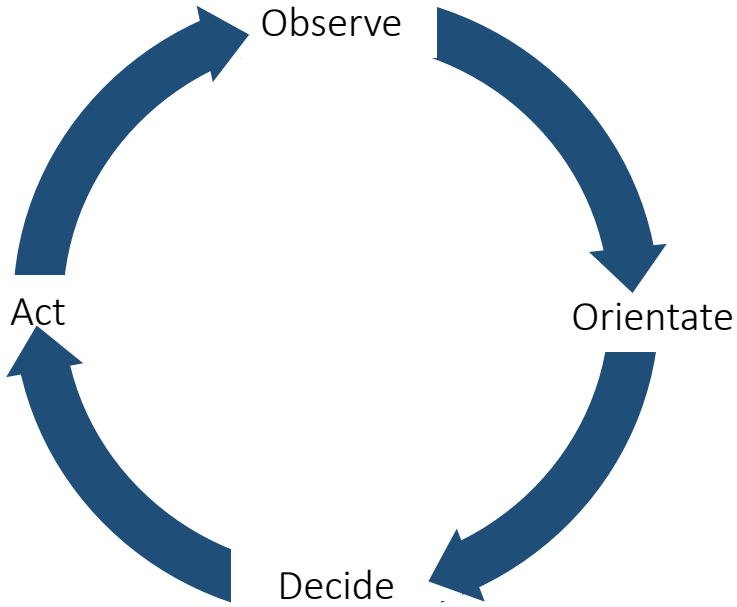


Coalitions

- Invest in systems to enable continuous integration of member contributed code
- Employ systems/processes to collect usage information for continuous improvement

3. Harmonize our roadmaps to avoid strategic dissonance on the question of value

TITAN: Discover relevant induced or autonomous changes to the current state of public member roadmaps and priorities via conversations with Si2 members



Si2 Staff: Publish and communicate revised Si2 roadmap and priorities.

TITAN: Analyze the information obtained through observation and synthesize into a recommendation.

Si2 BOD: Provide feedback on relative value/priority of recommendations. Make decision.

Si2 Strategy 1.1 (2.0 will be in Q1 2024)

- Intercept new levels of integration (3D), pre-post Si data management (DMW), processed data (SPEED), and new design platforms (AI/ML).
- Increase velocity by investing in the means to broaden/deepen member engagement, shorten learning cycles, and a harmonize roadmaps.
- Make UPTC the next $(VC)^2$. Follow the lead of our members and invest in the engineering resources needed to succeed.
- Continuously extend and innovate on top of OAC and CMC standards and technology. Use them to help solve interoperability issues in adjacent areas.

Remember

“ I am he as you are he as you are me
And we are all together”

- I am the Walrus by John Lennon / Paul McCartney

Hop on the bus.

If you are not a member of Si2, you should be.

Source: Adobe Stock

Q&A