Signal Integrity and Electromagnetic Analyses Techniques for High-speed Interconnects in 3DICs

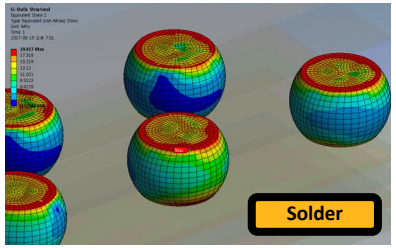
Dr. Yorgos Koutsoyannopoulos

EDPS 2022

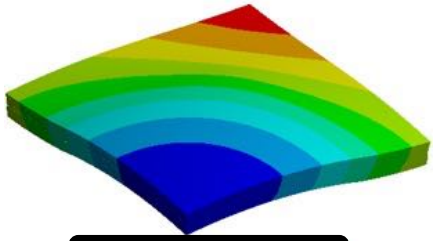
Ansys

Ansys Multi-physics Pervasive Simulation

Structural

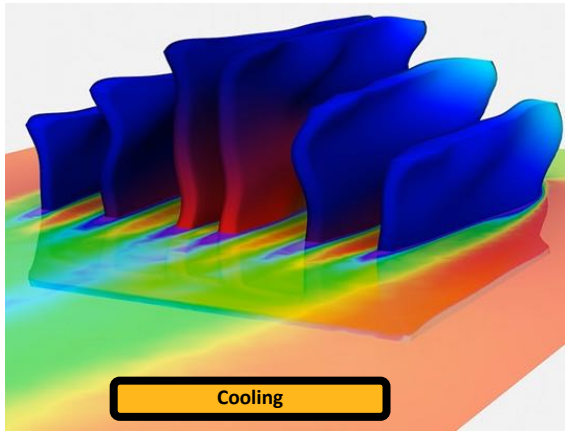


Solder



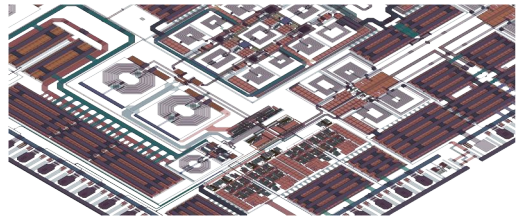
250C Warpage

Fluids

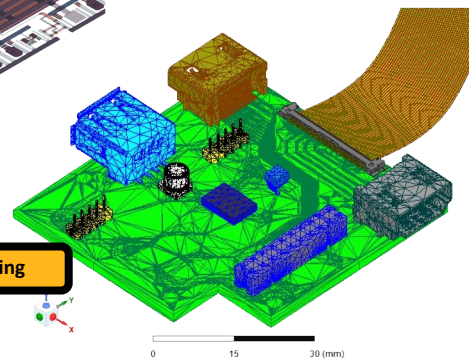


Cooling

Electronics

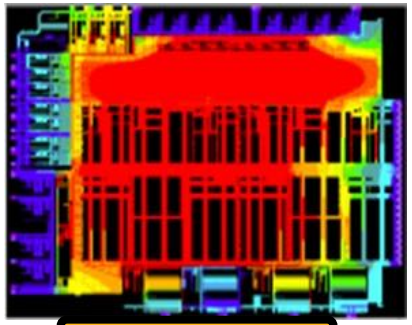


Full-Wave Extraction

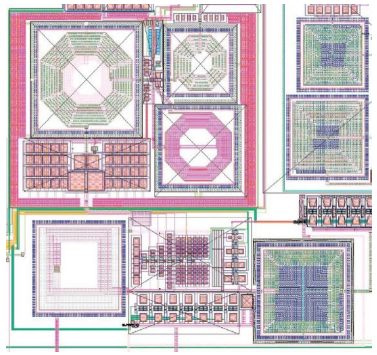


Full-Wave System Modeling

Semiconductors



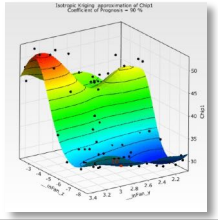
On-die Voltage Drop



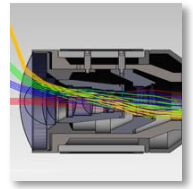
On-die EM-Extraction

Cloud

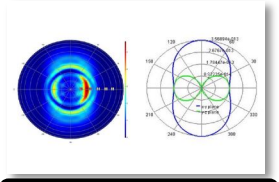
Many Others



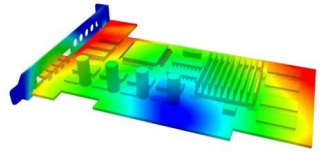
AI Optimization



Lighting/HUD Display



Photonics



Reliability/Materials

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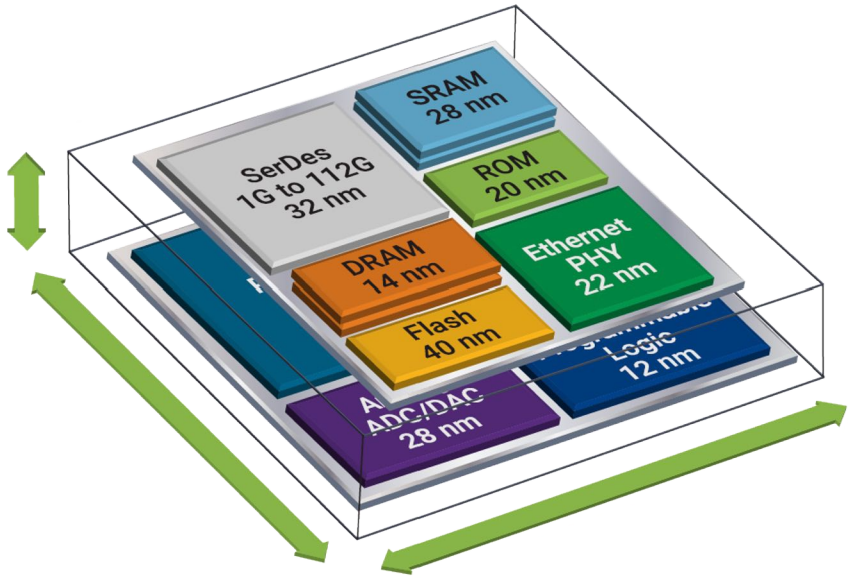
3D IC Engineering Challenges

Engineering Goal



Manage effectively **2.5D/3D Heterogeneous Integration** aiming at **maximizing Power-Performance-Area volumic density**

Engineering Requirements

- **Explore** design trade-offs in early stage with physics insights for optimal architecture selection
- **Implement** optimal design with sophisticated helpers (routers, design-rules checkers, …) and progressive design refinement capabilities
- **Analyze** thoroughly the performance against relevant operating conditions throughout the design process
- **Assess** chip-package to system-level electrical, thermal and structural integrities for reliable, safe and secure, semiconductors solutions
- **Ensure** optimal materials selection for reliability, cost and sustainability targets

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Delivering Quantified Business Impact

Performance

10%

Higher performance per Watt[1]

Speed

30%

Development time reduction[2]

Cost

50%

Cost reduction[3]

1) https://www.ansys.com/advantage-magazine/volume-xiii-issue-2-2019/early-simulation-avoids-chip-burn
2) https://www.ansys.com/en-gb/news-center/press-releases/10-23-19-ase-group-significantly-advances-semiconductor-packaging-development
3) https://fluidcodes.com/wp-content/uploads/2020/04/crossed-signals-aa-v11-i3.pdf

MULTIDISCIPLINARY COLLABORATION

CO-DESIGN & CO-ANALYSIS | MATERIALS INTELLIGENCE | RELIABILITY & QUALITY | SAFETY & CYBERSECURITY

SILICON TO SYSTEM WORKFLOWS

CHIPLETS READINESS | HETEROGENEOUS INTEGRATION: DESIGN EXPLORATION | MULTI-DIE IMPLEMENTATION | MULTIPHYSICS ANALYSIS | SYSTEM VERIFICATION

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Deep Dive on Solving On-Die Electromagnetic Solutions

Solving the Signal Integrity Problem

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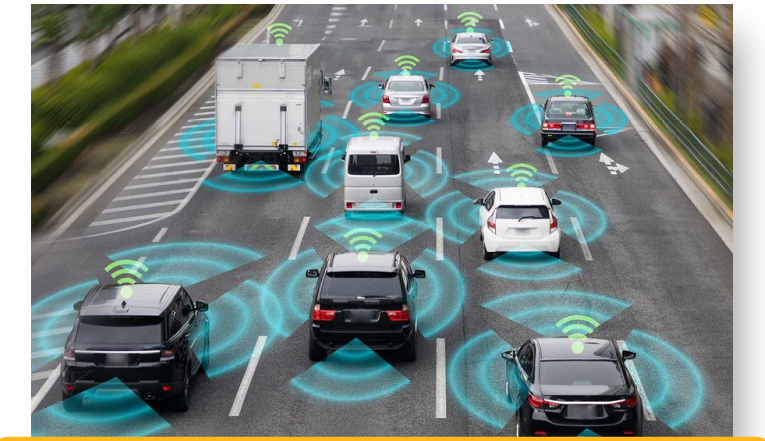
Target Applications of Electromagnetic Analysis in Auto/5G/6G/QC

AI Processors



Autonomous Vehicles

SoCs at VERY High Frequencies!

HBM-GPU core multi-Gbps I/O

rs

Superconductive silicon for QC

Cloud Infrastructure
Multi-Gbps networking

5G/6G Mobile Comms

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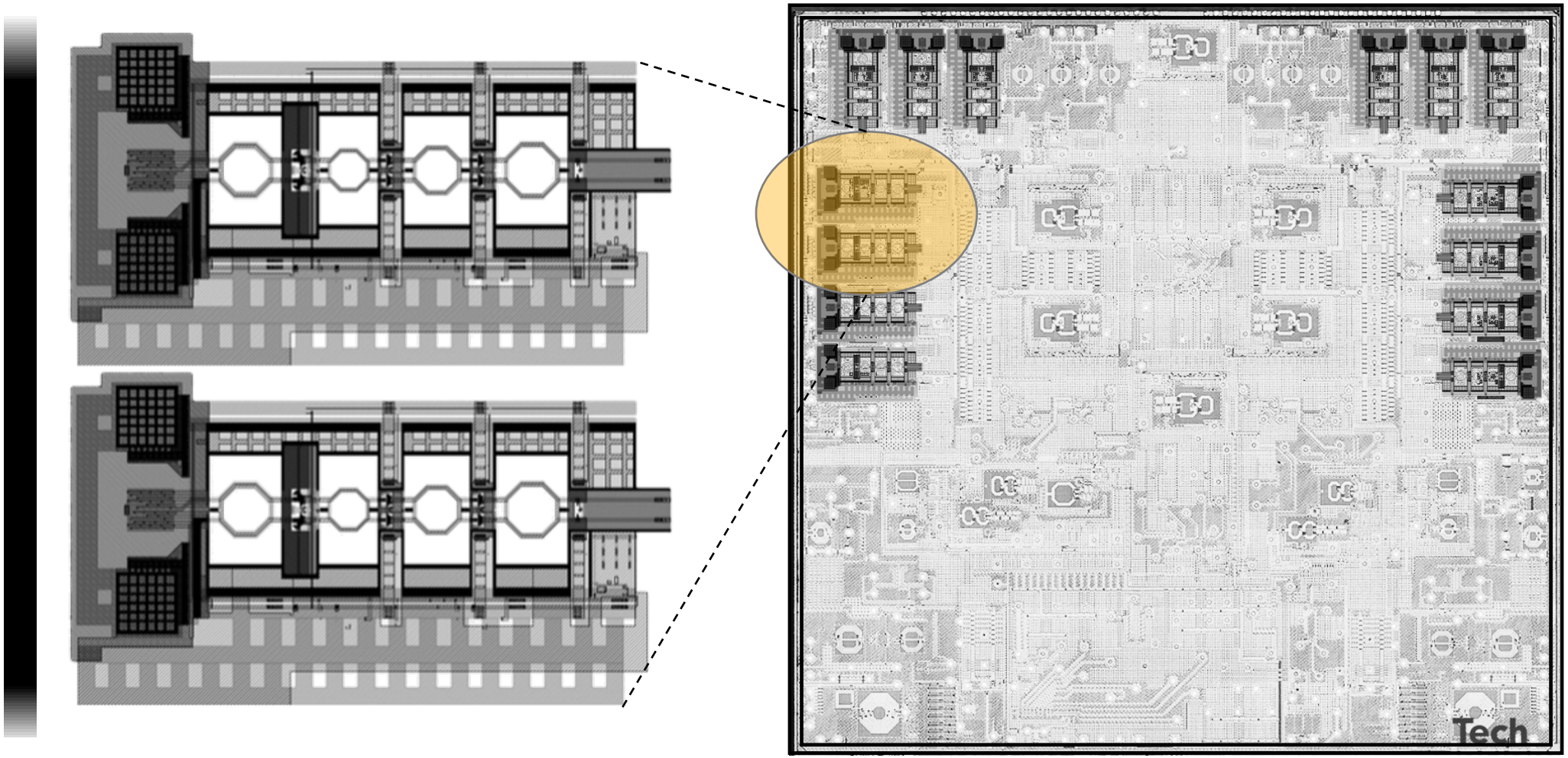
Why EM-aware Matters?



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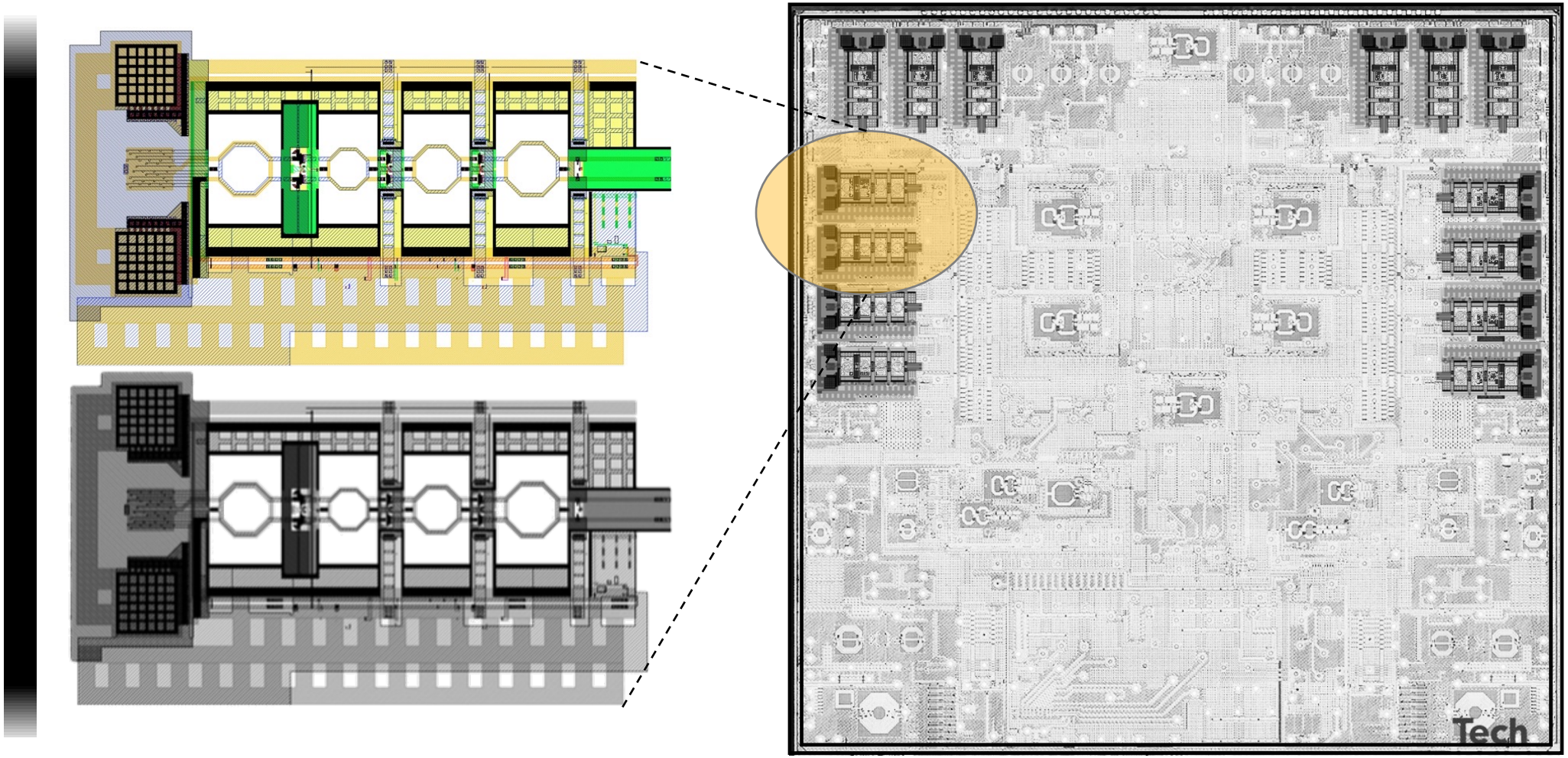
Why EM-aware Matters?



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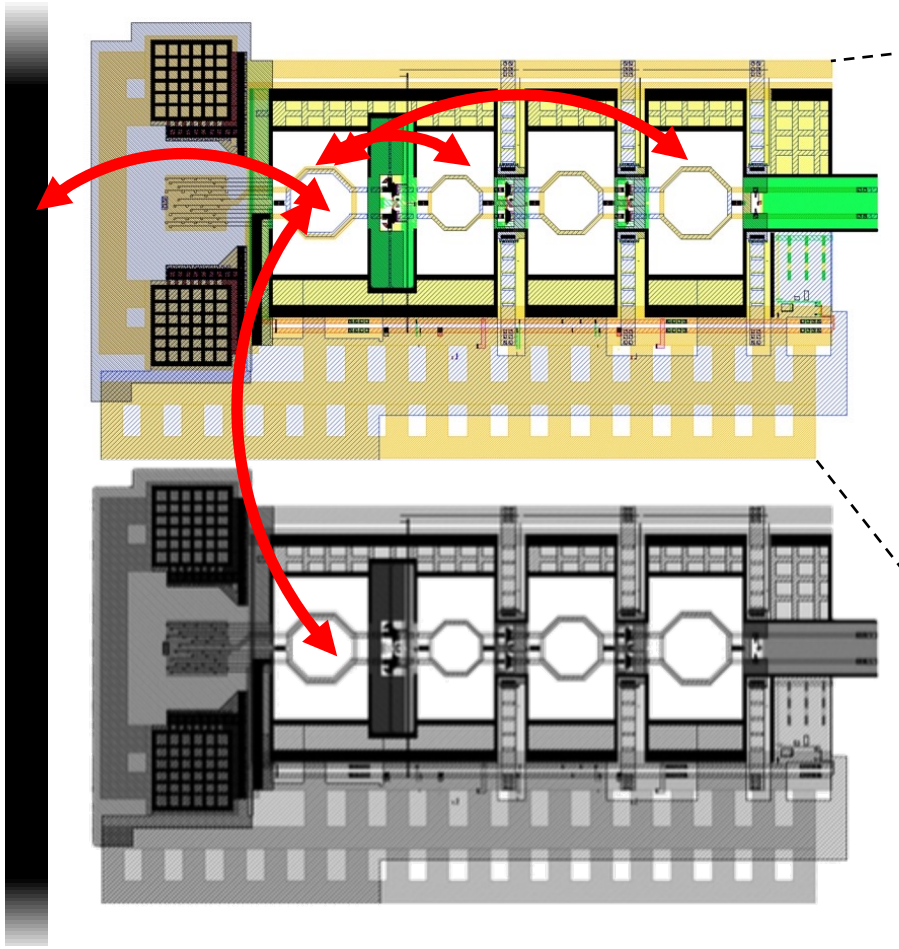

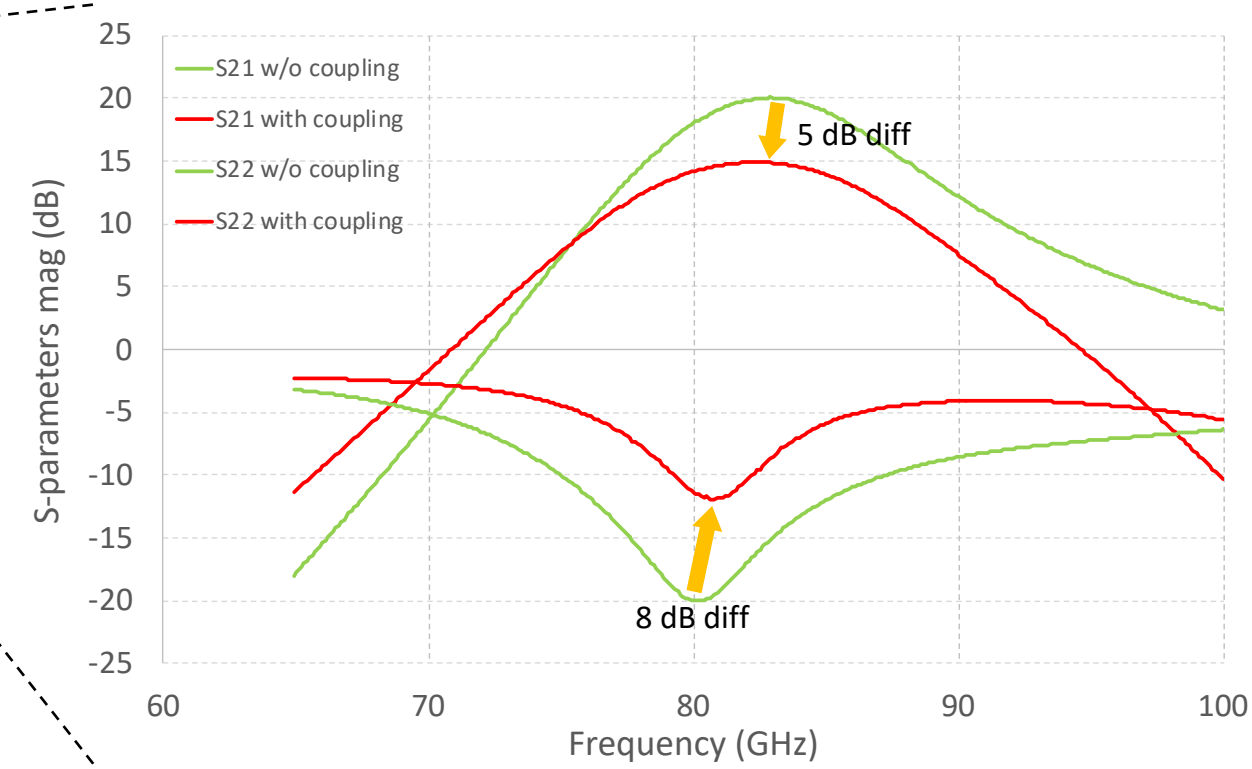

- Significant deterioration of frequency response due to intra-block EM coupling

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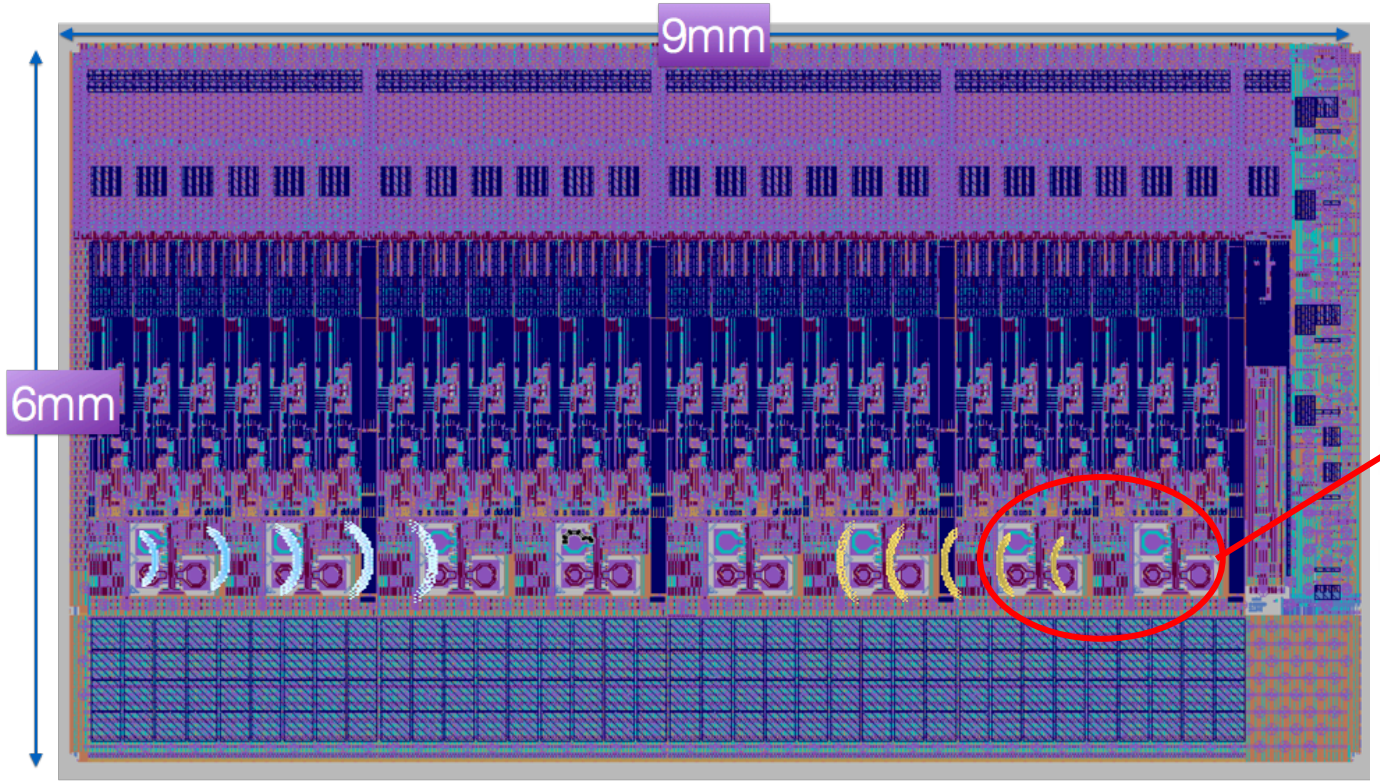
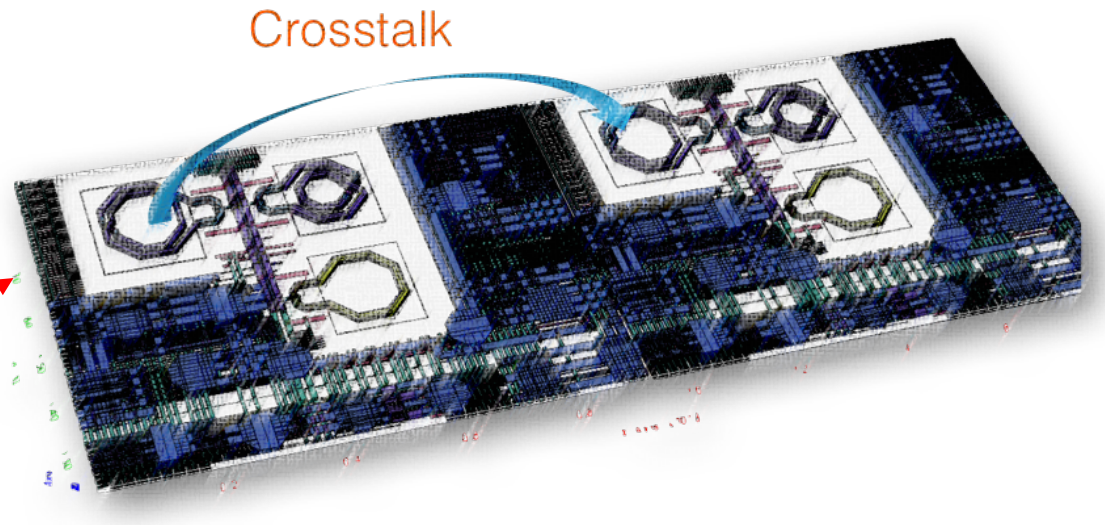
Mitigating Risks of Electromagnetic Crosstalk at SoC Level

- Ansys provides EM analysis with enough capacity and speed to address large SoC and 3DIC designs up to 3nm CMOS nodes
- Portfolio of products offers complete EM-aware design flow from concept to tape-out sign-off!





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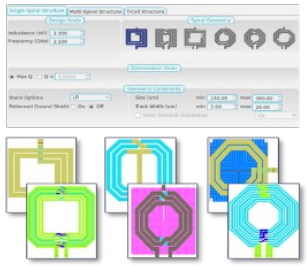
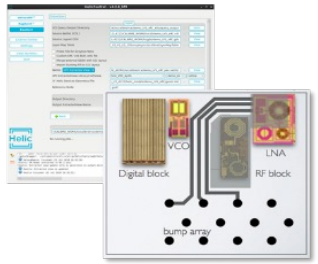
A comprehensive EM-aware Workflow for 3DICs and SoCs

VeloceRF
EMag-Aware **Synthesis**

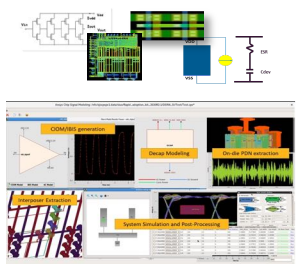


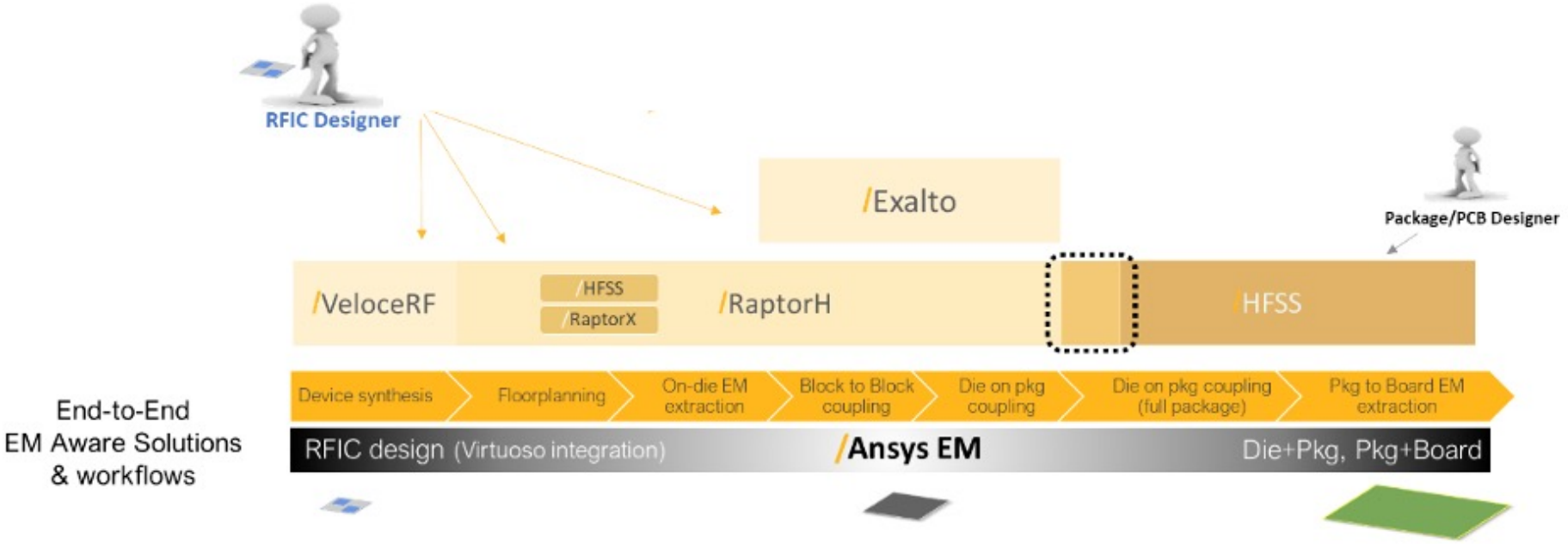
RaptorX/H/Qu
EMag-**Extraction**

Exalto
Post-LVS EMag **Workflow**



CSM powered by RaptorX
EMag-Aware **SI Analysis**





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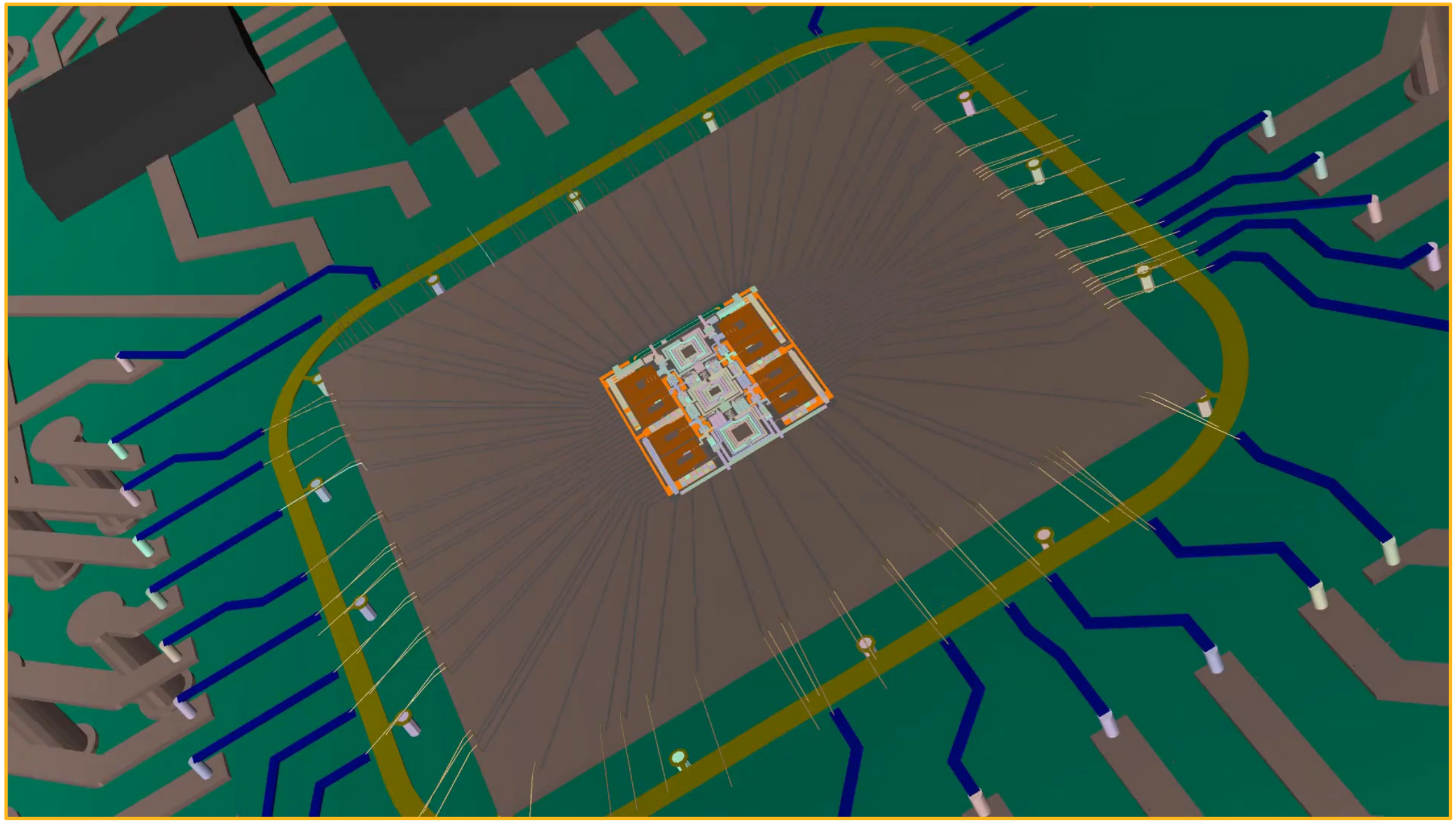
Simulating Multiscale Problems With HFSS Mesh Fusion



Industry Trends in Electromagnetic Extraction

Advanced Problems in On-Die Electromagnetic Extraction

Ansys

Who Should Worry About Electromagnetic Extraction?

- Almost all positions:
  - Design managers tasked with system performance
  - Package designers tasked with SI
  - CAD managers tasked with flow development
  - EM experts who advise on advanced EM topics
- Heterogenous design means each party loses some control of your part
  - All parts interact
  - Cannot afford to design in a silo anymore
  - This flow will recapture control of design
- Sign-off on circuit design with SPICE analysis is a given, but must be expanded to full EM sign-off
- Old method of SPICE only sign-off of design, and then performing EM analysis to understand failure once parts are fabricated and tested will no longer work
  - Don’t simulate past failure, simulate early for future success
- Two types of 3DIC designers now:
  - Those who care about the problem now
  - Those who will care about the problem for future designs
  - Not if you will care about this, but when

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SoCs Trends and EM extraction challenges

Trends

- Frequency escalation – upper 5G frequency bands and sub-THz-range 6G bands
- Rapidly increasing data rates
- Even higher integration and layout density
- Small form factor packaging
  - Extensive use of redistribution layers (RDL)
- 3DIC schemes become mainstream
  - InFO, WoW, CoWoS, iCAP, etc.
- Near-threshold (low-power) design
- Increased need for automatic layout simplification

EM modeling challenges

- Increased frequencies entailing higher meshing complexity
- Layout complexity increase
  - Materials
    - Multiple transitions of dielectric layers
    - Density-based definition of electrical and geometrical values
  - Biasing (LDE) effects
  - Millions of via transitions and dummy fill
- Higher integration necessitating co-extraction of
  - Analog and digital
  - Chip and part of package
- EM modeling of structures with hundreds of nets and ports!

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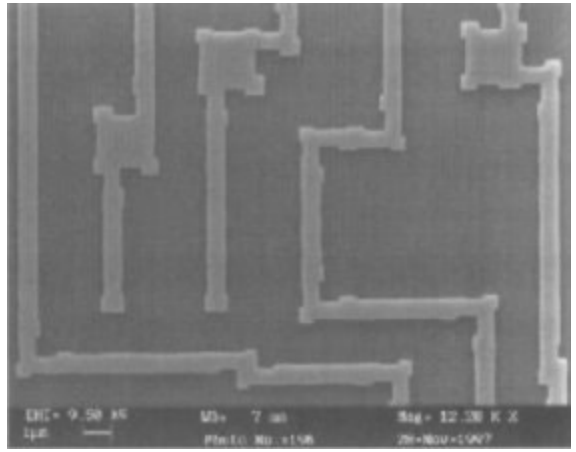
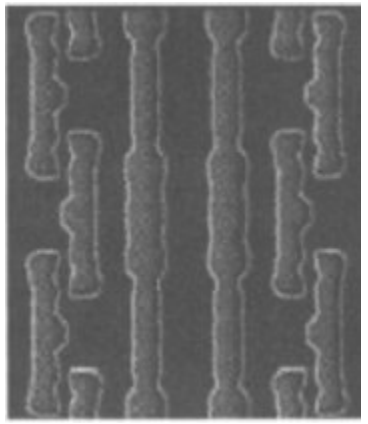
Advanced Fabrication Effects

- Also known as “Layout Dependent Effects” (LDE)
- Emerged at 40nm semiconductor processes; effect much more prominent at 28nm and below
- Drawn metal shapes and material parameters become dependent on the actual IC layout density
- What is going to be fabricated is NOT what is drawn in the layout
  - Width, spacing, and resistivity depend on the layout
- Affects conductor dimensions in x, y, z axes as well as material parameters (ε_r, R_{sh})
- Effects further exacerbated by multi-patterning
- Relative information provided by means of complex tables integrated in technology files from foundries



Images: Nanofabrication: Principles, Capabilities and Limits, Zheng Cui, Springer 2010.



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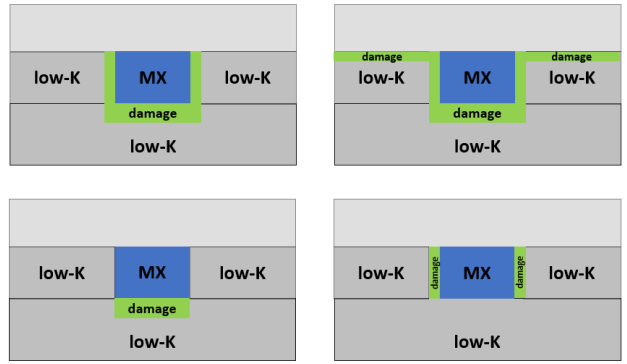
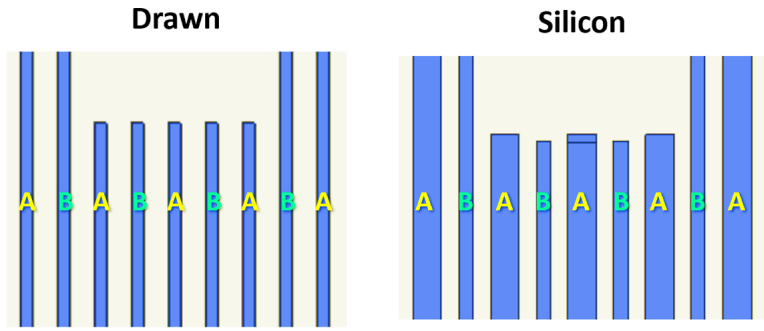
Fabrication Effects Considered in Advanced nm Nodes

5, 3 and 2 nm

Category	Description	RaptorX
Conductor	Multi-patterning / Coloring	✓
Conductor	ETCHING (single or multiple tables)	✓
Conductor	Width dependent changes in resistivity over temperature	✓
Conductor	Metal thickness variation (Resistance)	✓
Conductor	Metal thickness and density bounds (Resistance)	✓
Conductor	Metal thickness variation (Capacitance)	✓
Conductor	Metal thickness and density bounds (Capacitance)	✓
Conductor	Sidewall damage thickness variation	✓
Dielectric	Constant damage thickness	✓
Dielectric	Bottom dielectric thickness variation	✓
Dielectric	Side dielectric thickness variation	✓
Via	Via contact resistance varies with via area	✓
Via	Via resistance change over temperature varies with area	✓





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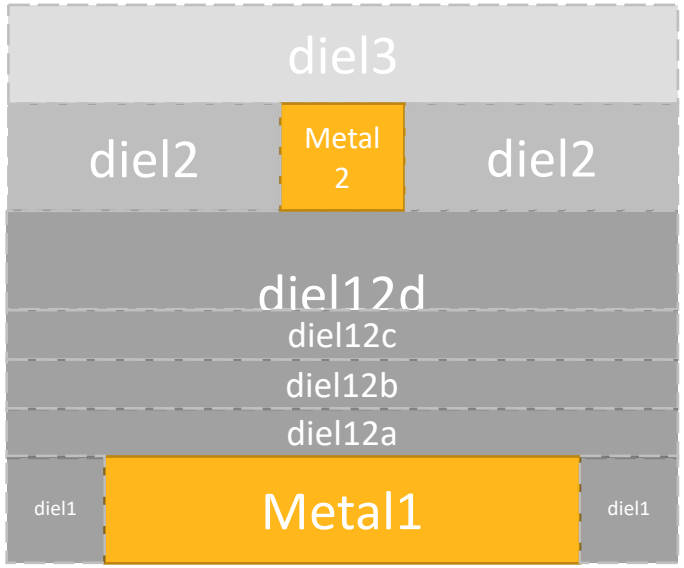
Advanced Fabrication Effects Overview

- What is drawn:



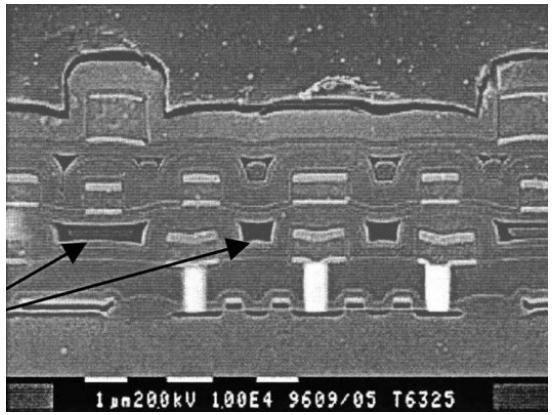


Image source doi:10.1016/j.mser.2004.06.002

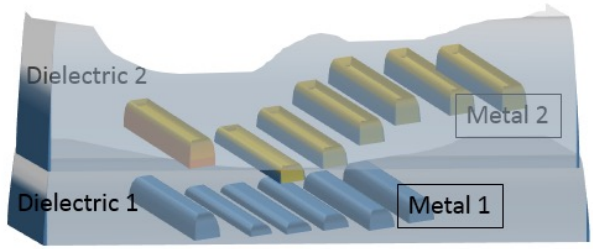
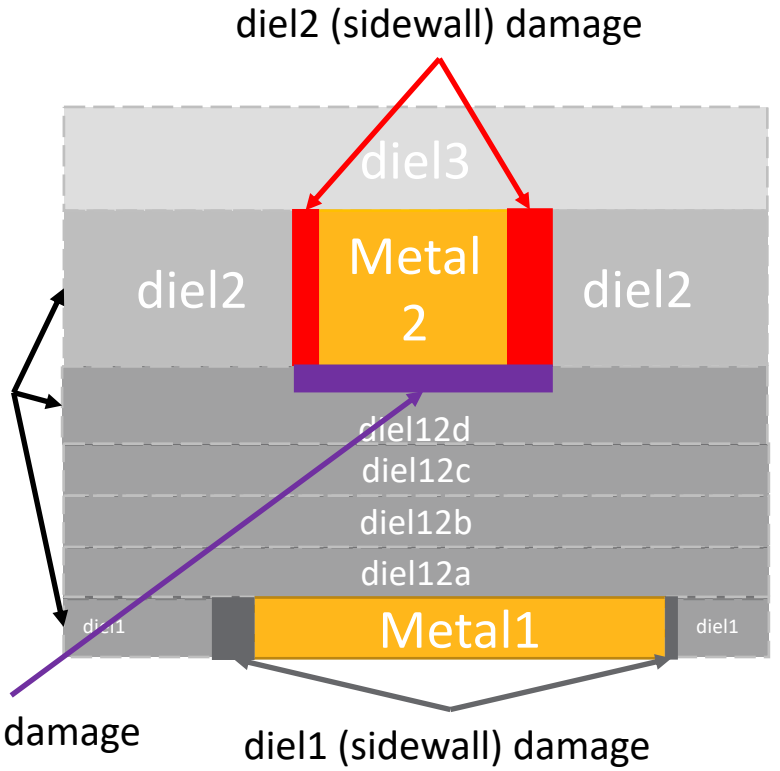


Image source http://www.vlsi-expert.com/2015/07/importance-of-cmp-process.html

Nothing is planar, nothing is standard.
Every layout is a different stackup!

- What is fabricated:

Metal and dielectric thickness all change!



Leads up to 30% difference in resistance and capacitance!

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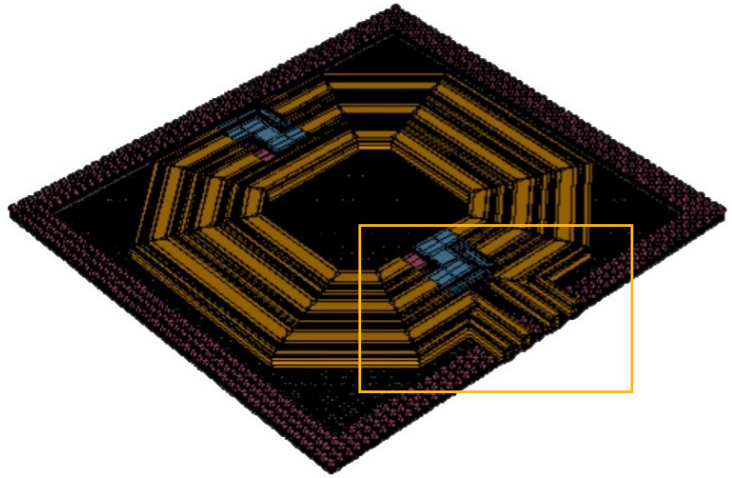
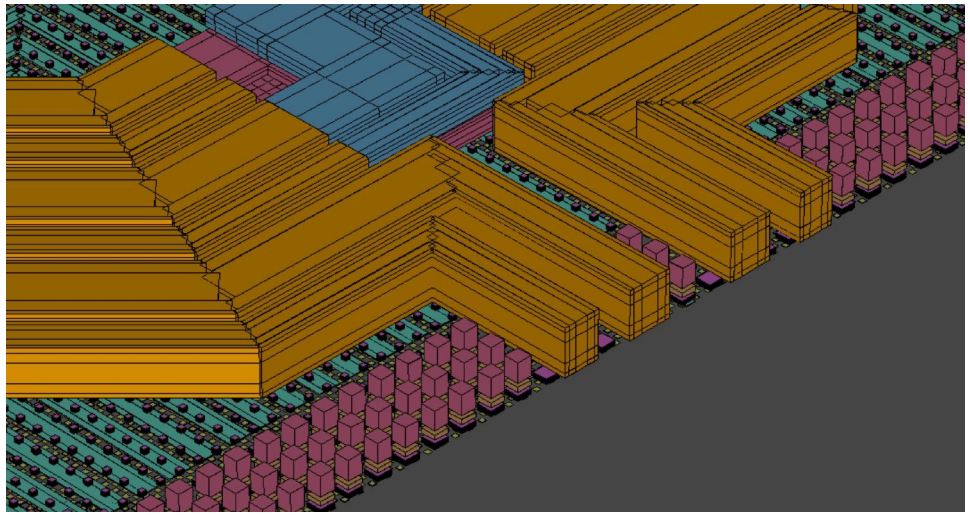
Mechanical Reliability with Metal Dummy Fill

- Unused area must be filled by dense array of "dummy metal tiles“
  - Necessary to ensure functional and reliable chips on each silicon wafer
- Electromagnetic performance is affected by dummy fill but…
- Design complexity explodes
  - Millions of dummy tiles!
    - Even on a device level layout (e.g. spiral inductor)





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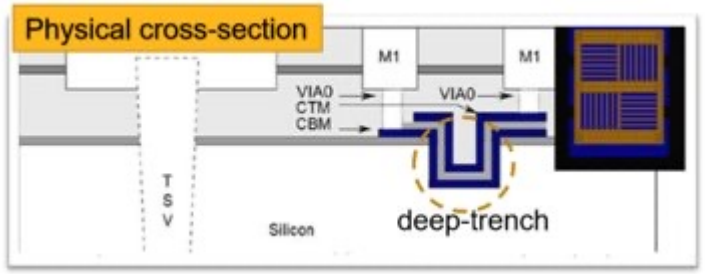
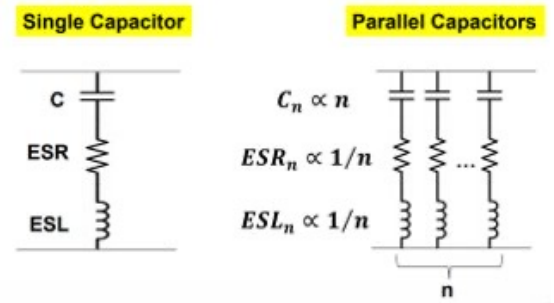
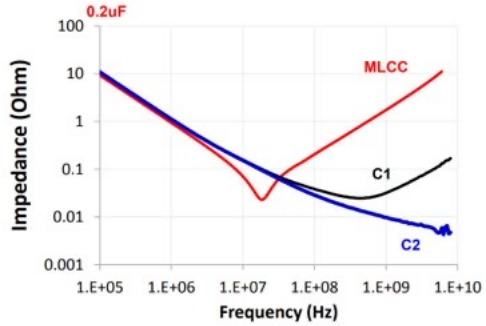
Heterogenous Design w/ Silicon Interposers

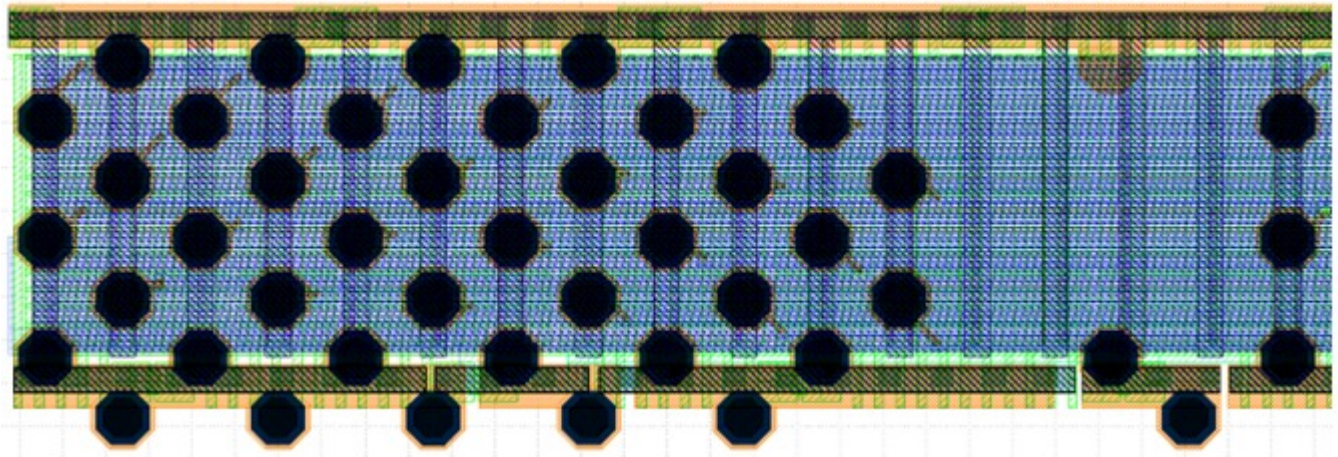
- Heterogenous design allows for process selection and optimization
  - Each part of system can have an optimized process
- Incorporate Ultra high-density capacitors for power integrity
  - Interposer Capacitors (iCAPs)
- Chiplets assembled to form entire system
- Interposer allows for system assembly







Surface Mount Capacitor
iCap Design 1
iCap Design 2



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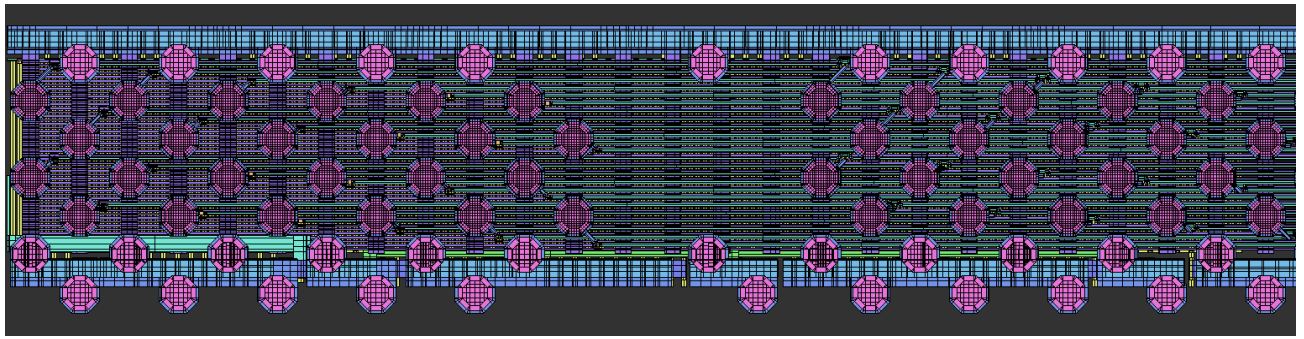
Interposer Example

- Layout used is a ~5mm lane of HBM I/O with 48 signal and VSS/VDD nets
- No manual layout work required to simplify the design
- Layout preprocessing automatically applied by RaptorX or RaptorH
- Size is ~0.3mm x 5mm

11 signals	RaptorX
Extraction time	5h 40m
Peak memory	170 GB
CPUs	16

48 signals	RaptorX
Extraction time	15h 2m
Peak memory	262 GB
CPUs	16



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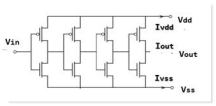
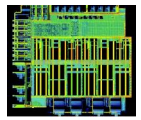
CSM System Signal Integrity Analysis Flow

IO Circuit

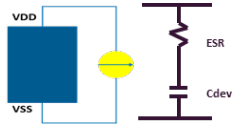


Chip



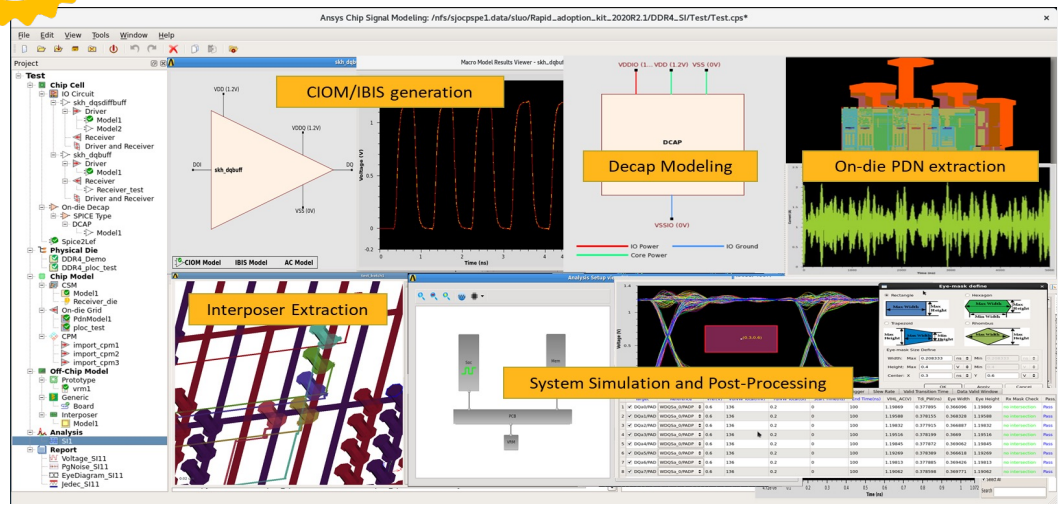
Interposer

On-die Decap Circuit



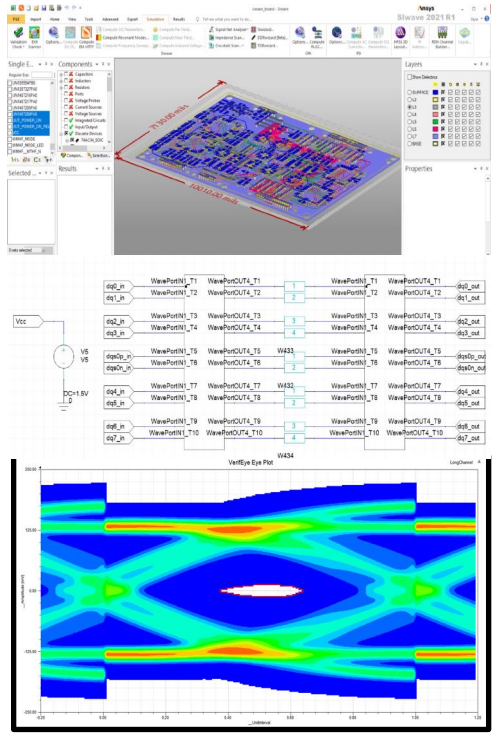
CSM Chip Modeling Flow for SI analysis

Powered by RaptorX



Deliver CSM model as a chip model in PKG/PCB system SI analysis

SIwave/AEDT



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Conclusion

- Heterogenous designs requires multidisciplinary approach to design to squeeze out the best performance possible
- Signal and power nets must be analyzed together in single EM simulation
- Many issues must be addressed for advanced silicon node sizes
  - Advanced Fabrication Effects
  - Interposer
- Need a way to analyze the different parts of the heterogenous design together
- A comprehensive and fast solution is needed for all these challenges

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