KEYSIGHT

Digital Twins for 5G and 6G

Phil Sohn, Keysight Technologies

Changes from 4G to 5G

Test Requirements and Instrumentation

Requirements:

- Component carrier bandwidths increased from 20 MHz to 400 MHz
- New frequency bands from 24 GHz to 52 GHz +
- More connections for FR1 (8 -> 64)
- Phased arrays (analog beam forming) and no connectors at FR2 driving more OTA testing

Instrumentation:

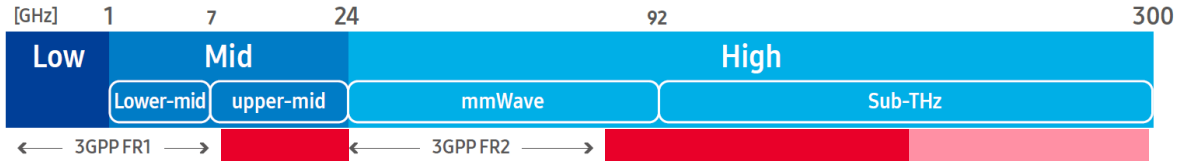
- Migration of mid-performance instruments from boxes to modules
  - Easier support for multi-channel instruments
- Bandwidths increased from 160 MHz to 1 GHz
- Switch matrixes to handle higher port count
- Remote transceivers to cover FR2 and OTA test requirements
  - New Solutions
  - Addition to existing customer instrumentation

❖Common software and APIs between new instruments and previous generation instruments

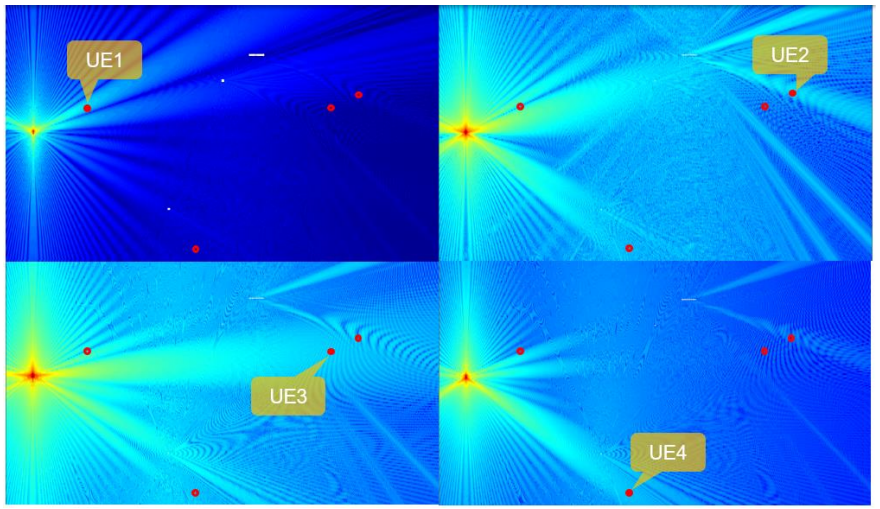
New Requirements for 6G

Based on Current Research Topics and new KPIs

- New Sub-THz frequency bands
  - Carrier frequency from 90 GHz to 170 GHz ++
  - Component carrier bandwidth 2 GHz to 4 GHz
  - Total aggregated bandwidth 10 GHz ++
- “Mid-band” frequency band
  - Carrier Frequency from 7 GHz to 24 GHz
  - Bandwidths comparable to FR2
  - Very high channel and antenna count
- AI RAN



- True massive MIMO and reconfigurable surfaces
  - FR1 and “mid-band” frequency ranges
  - Unknowns:
    - Connectors available?
    - Functional or parametric test?
    - How much test?



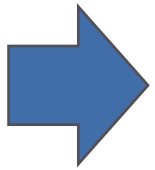
Voice of the Customer Challenges

These workflow challenges are NOT addressed very well by <u>any T&M or EDA vendor</u>

Addressing Product Development Cost drivers

Cost Drivers:

- Design spins
- Sheer effort
- Insufficient spec margins



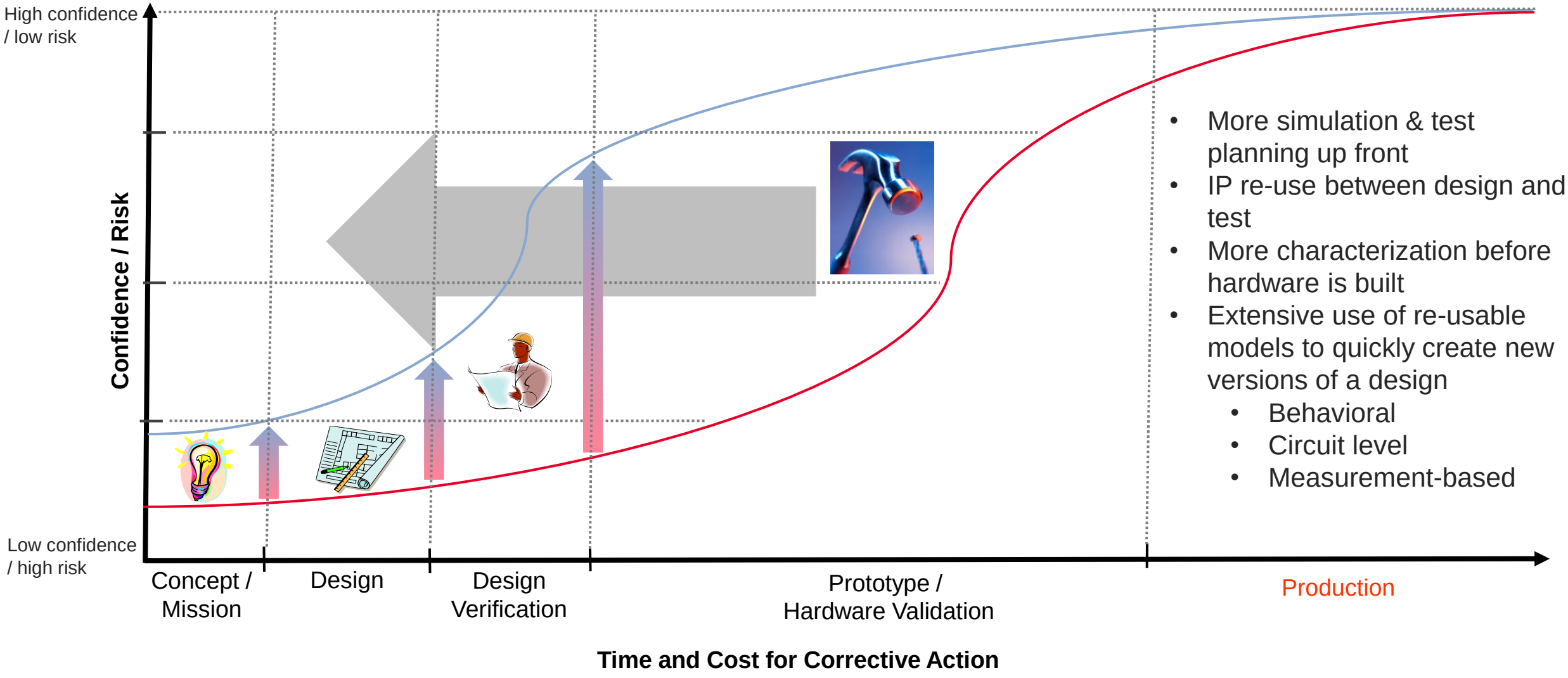
Root Causes:

- Manual processes
- Mistakes
- Insufficient design characterization
- Lack of IP and data reuse
- Process variations

Remedies:

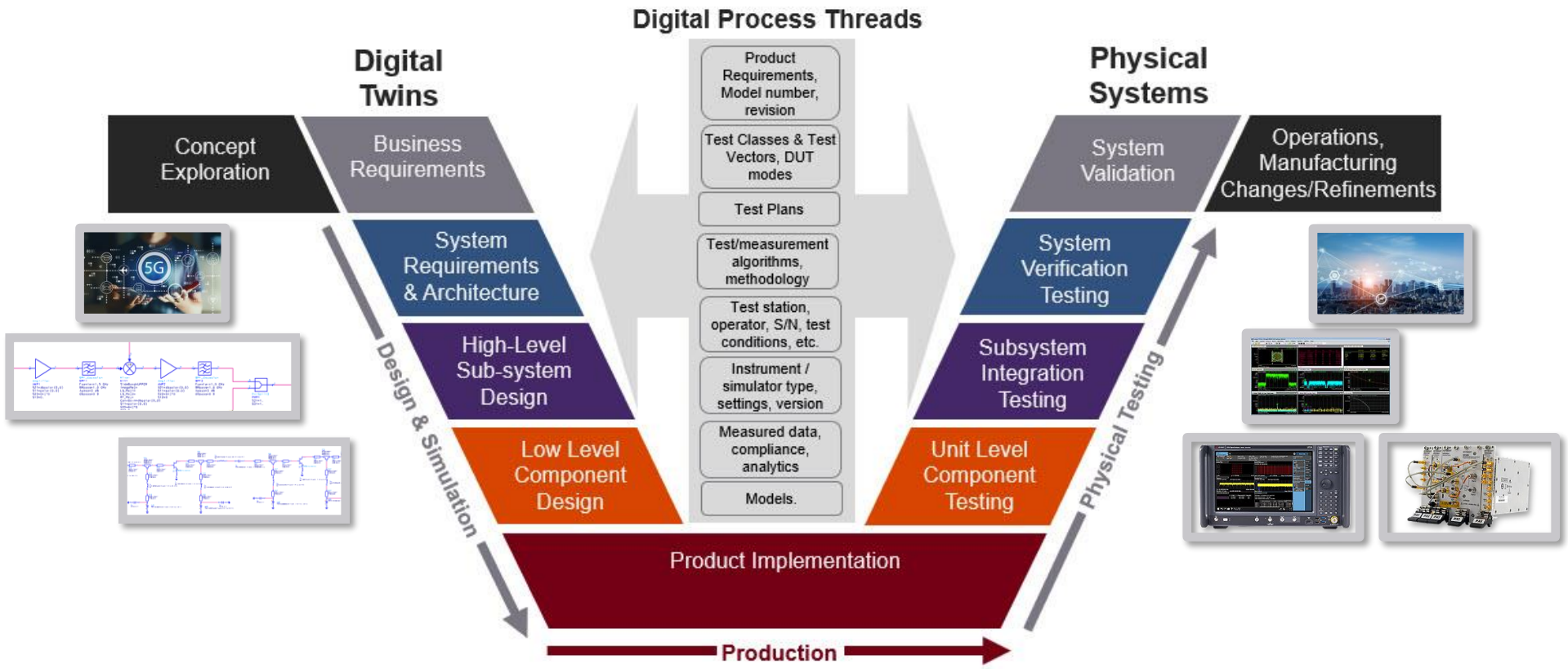
- Consistent, automated workflow
- Data traceability
- “Shift Left” – more verification
- Techniques to reduce design and test correlation differences
- Design and Test analytics
- Statistical design methods/HPC

Industry Mega- trend: “Shift Left” Effort



- More simulation & test planning up front
- IP re-use between design and test
- More characterization before hardware is built
- Extensive use of re-usable models to quickly create new versions of a design
  - Behavioral
  - Circuit level
  - Measurement-based

Linking Physical Systems to Digital Twins



- Digital twins has been an effective way of managing complex products
- Customers must manage processes and data for both design and test
- Physical Systems and Digital Twins must be linked by digital threads

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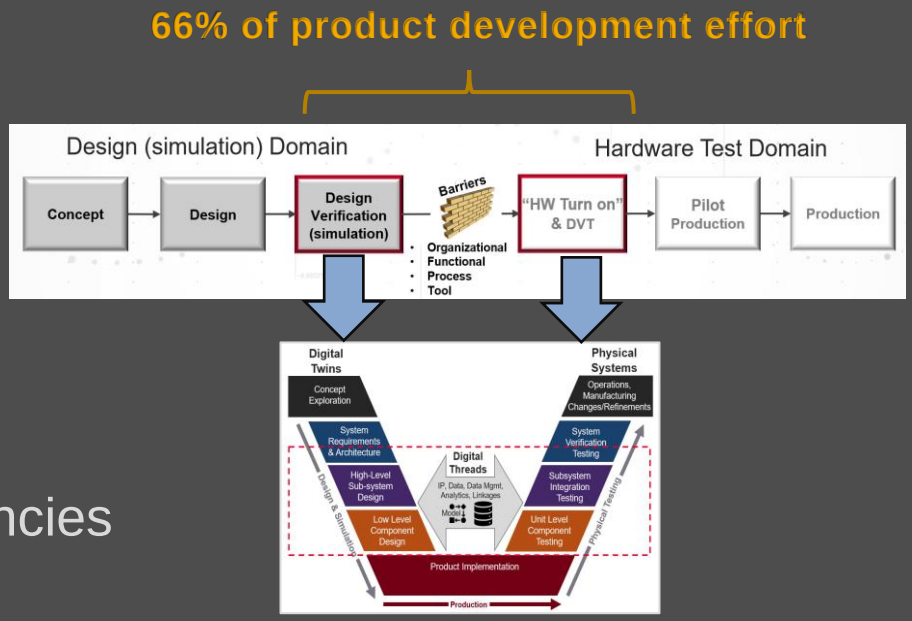
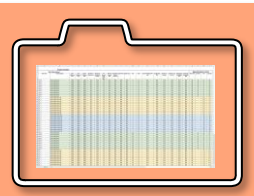
***Simulation and Test* Process and Data Management - Strategy**



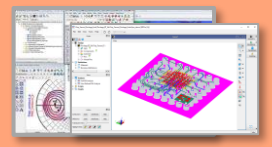
- Focus on design and hardware verification – core competencies
- Manage simulation/test plans, processes
- Supply reference IP for measurements which is consistent between simulation and test
- Manage simulation/test data acquisition
- Provide comprehensive design and test compliance analytics
- Automate processes!

Verification Challenge: 5G RF Analog Mixed Signal SoC Transceiver

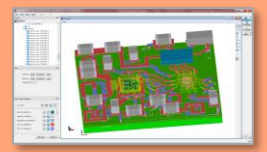
Design Verification Process → **Physical Test Verification Process**



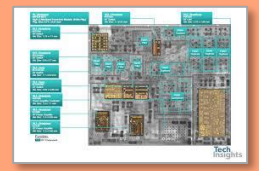
Overall Product Requirements
2100 requirements



IC Level Simulations & corner analysis
800 requirements to verify



Board application
200 requirements to verify



Chip level characterization
64K requirements to verify

Statistical / corner wafer characterization
100K requirements to verify

ATE characterization
5M requirements to verify

Board application verification
300 requirements to verify

Situation Today:

- Verification occupies 2/3 of the engineering effort
- 1000's of requirements to verify over operating modes
- Manual efforts, semi-automated homegrown tools
- 30% of time analyzing/managing/correlating data

How DaT Helps:

- Automates workflow processes, reduces mistakes
- Establishes digital threads to provide traceability, consistency
- Directly addresses the compliance and correlation bottleneck
- 20-50% projected savings in cost and time

By tying the definition of what is to be delivered (requirements) to the most critical downstream process meta–data, a Digital Thread create the ability to understand the state of the product development process, what risks are visible and what corrective actions should be considered. Without a Digital Thread, a company is flying blind in terms of the risks it faces in product development. - Jama

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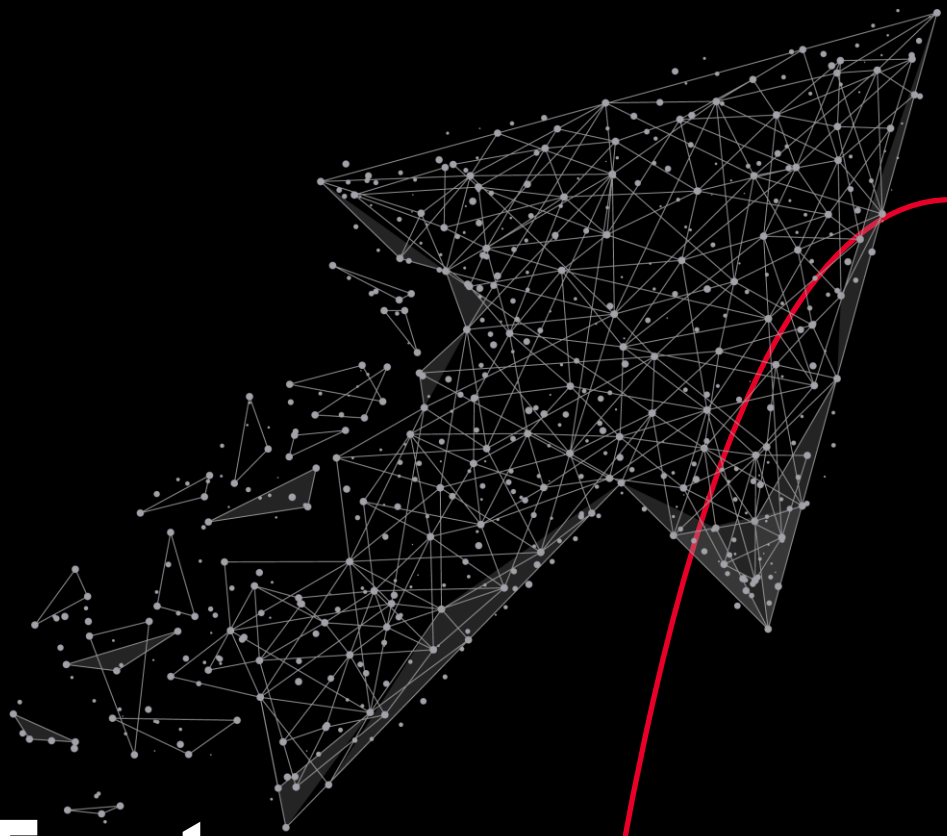
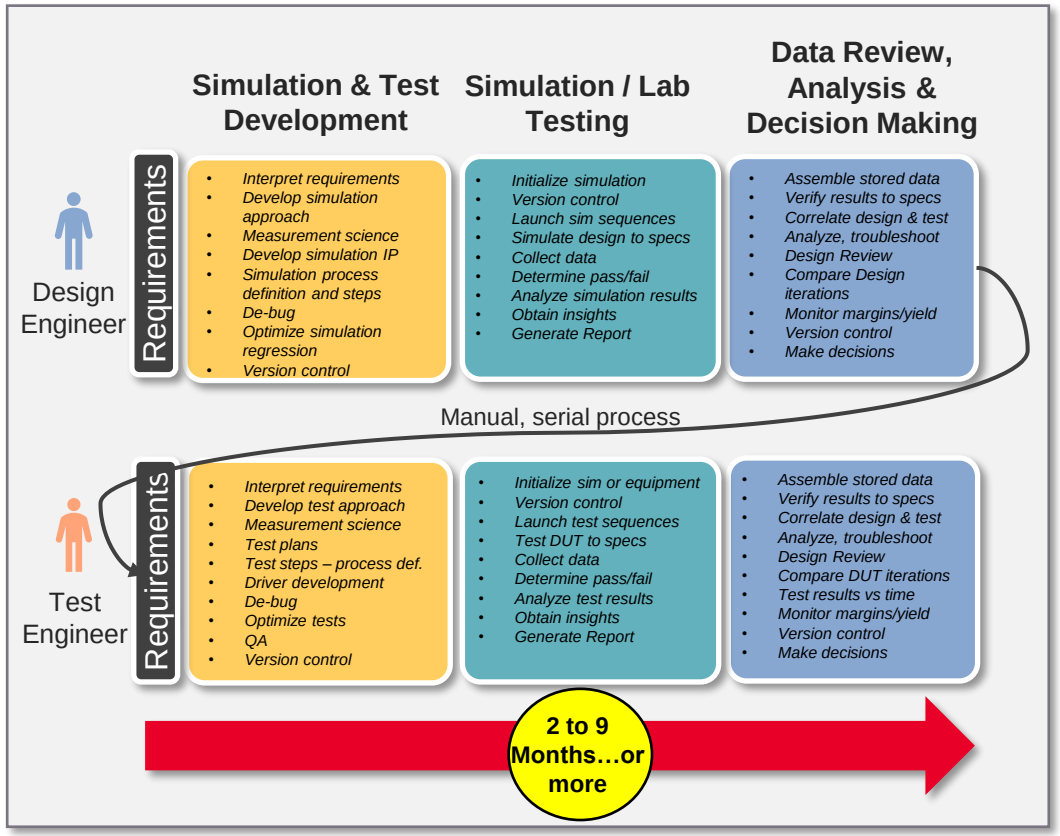


PathWave Design and Test

Digital Engineering Workflow Solution

Digital Workflow Transformation

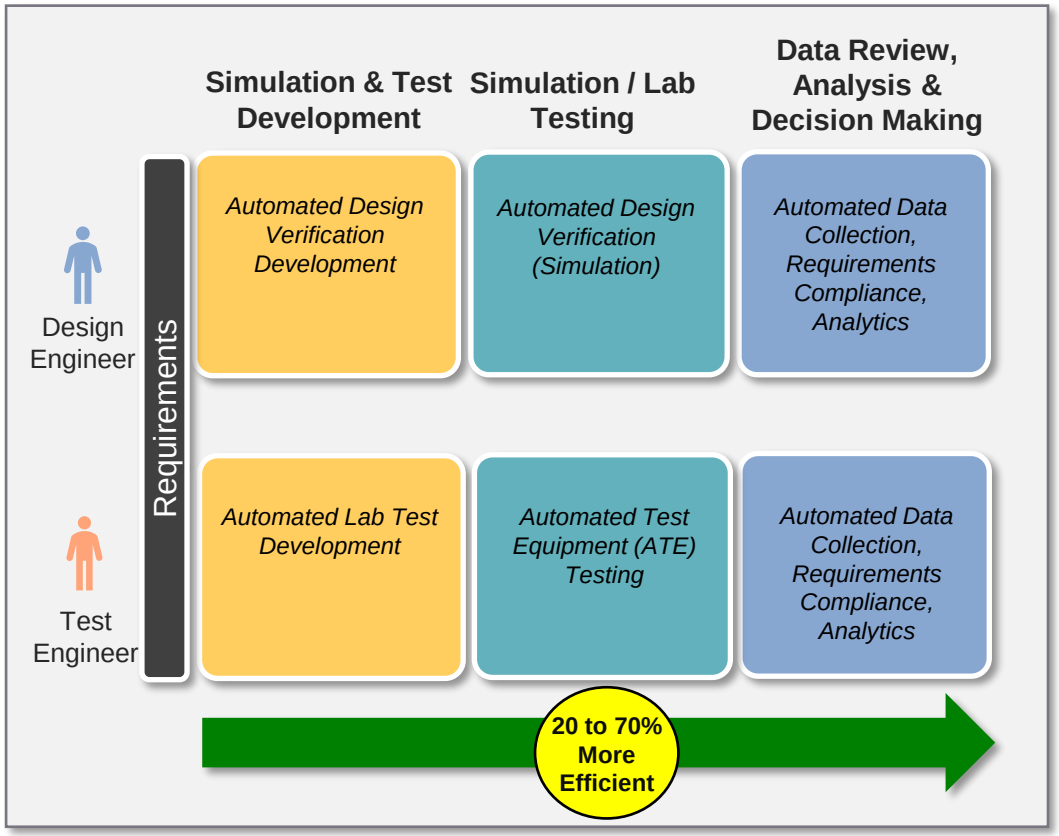
Traditional Verification Process



- Isolated serial Design and Test verification processes
- Error prone, time-consuming manual processes
- Inconsistent, lack of traceability, little IP re-use

Digital Transformation

DaT Process and Data Management



- **Automated workflow processes**
- Traceability, consistency
- Concurrent and collaborative design and test verification
- More insights

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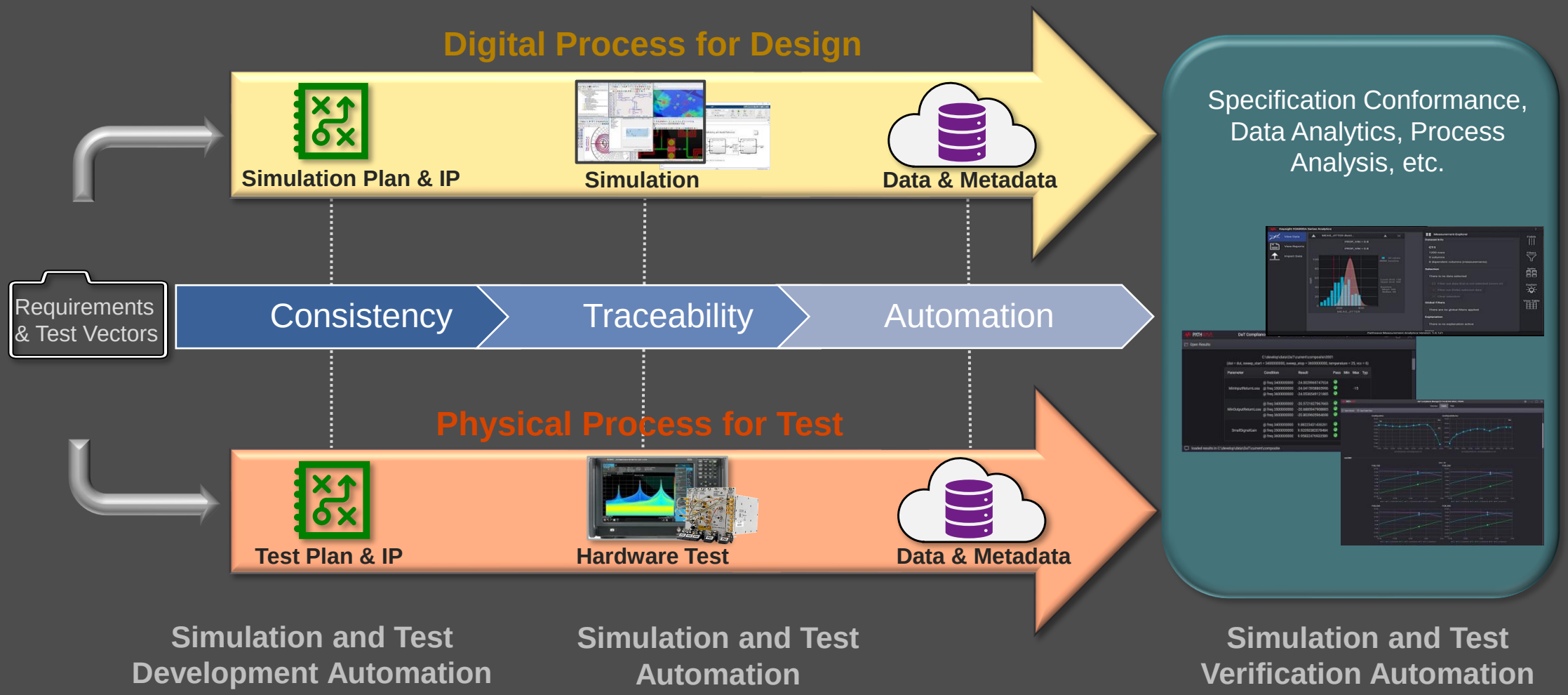
Physical and Digital Process Twins



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Design and Test Digital Engineering Workflow

Simulation and Test Development Automation

Central Engineering / Engineering Support Team

Requirements & Test Vectors

SysML, Excel, .csv

Sim/Test Development Automation

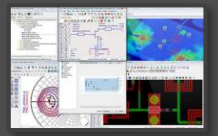
Inputs: Sources of Truth

(application specific IP, measurement science, drivers, etc.)

Keysight Trusted Test Libraries

Simulation and Test Automation

Design Engineering Team



Simulation automation IP

Simulation data and metadata

Repository

Simulation/Test IP, test plans, & recipes

Test automation IP

Test results data and metadata

Test Engineer / technician / operator

Multi-Discipline Optimization and Model Updates

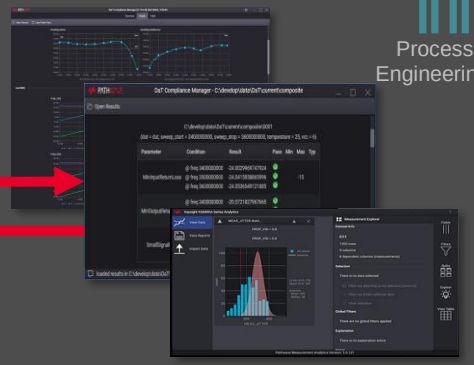
Data & Metadata

Data queries & Analysis reports

Simulation and Test Verification Automation

Design Engineering Team

Process & QA Engineering Team



Central Engineering / Engineering Support Team

Test Engineering Team

Management Team

Digital thread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