When Chips Become 3D Systems…The Challenges of 3DHI

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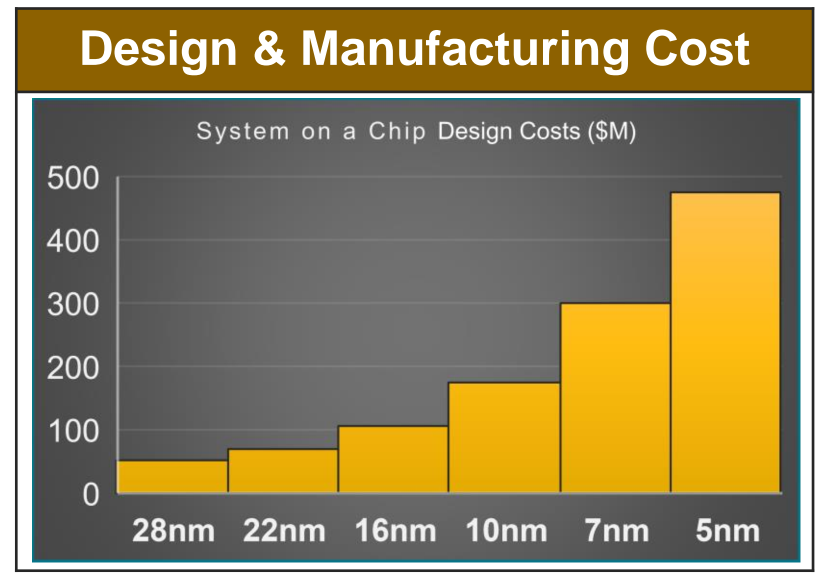
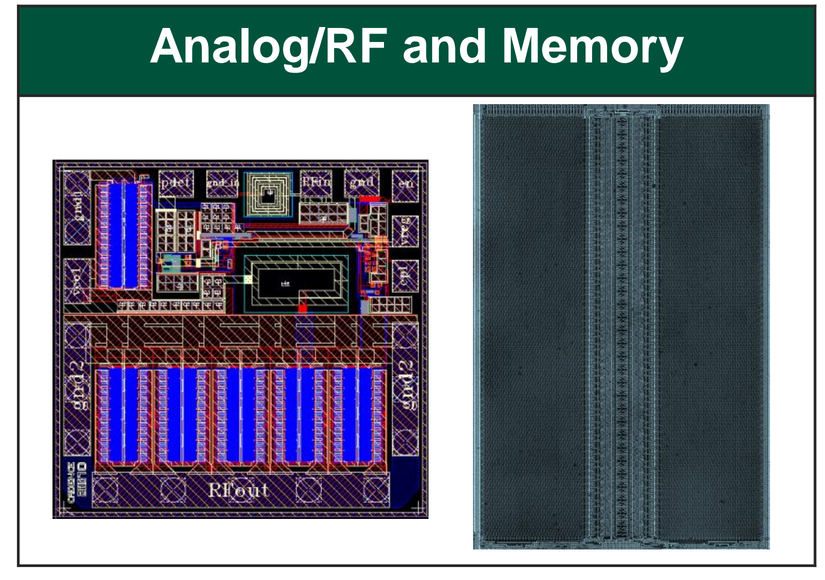
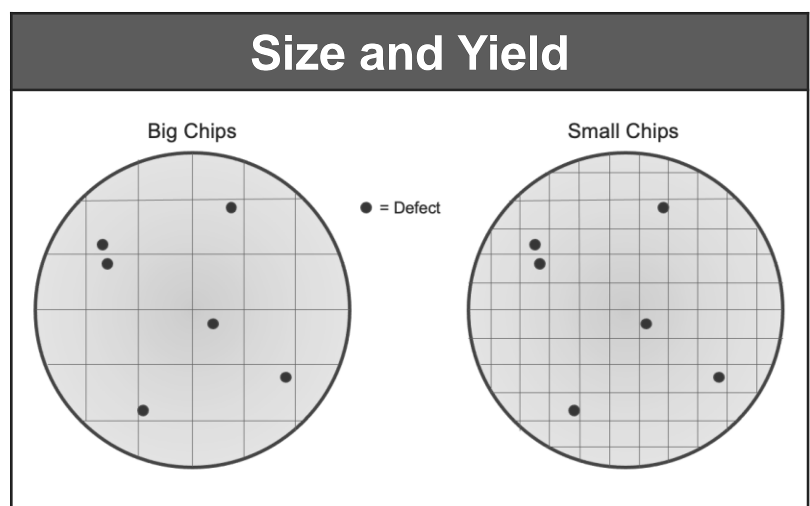
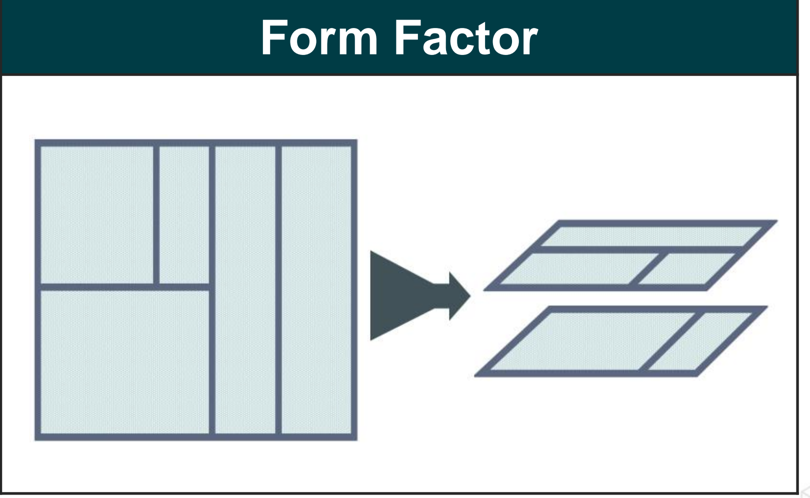
Simply Following Moore's Law Alone is No Longer the Best Technical and Economical Path Forward









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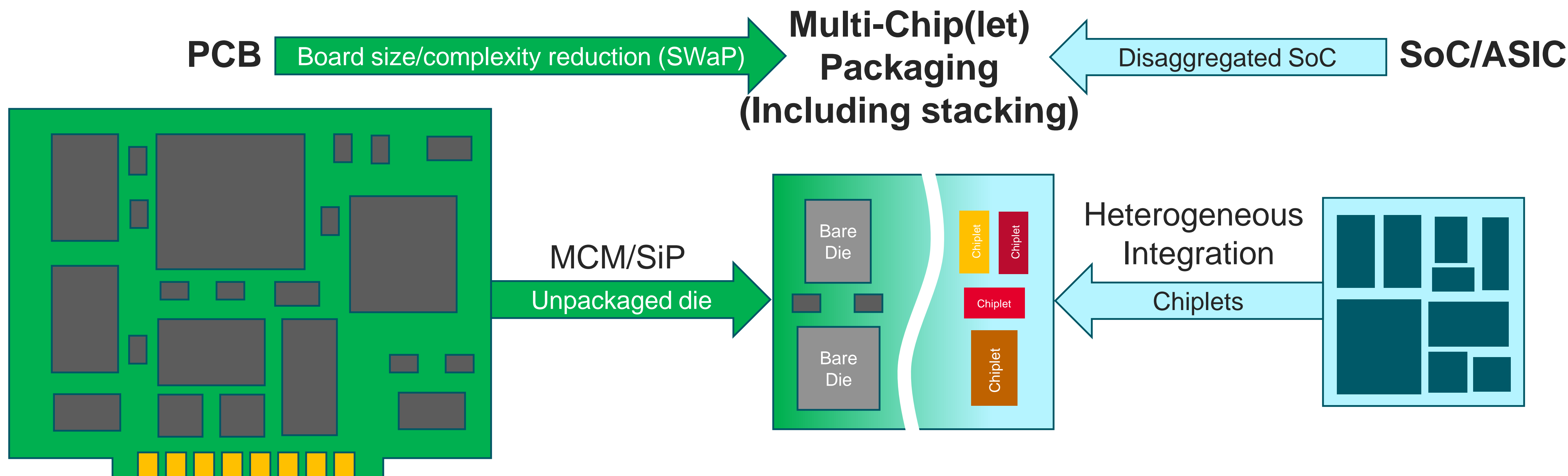
SiP/MCM vs. Chiplet-Based (Heterogeneous Integration) Architectures

The transition from system on a chip (SoC) to system in a package (SiP)



PCB to MCM/SiP Benefits
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

SoC to HI Benefits
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible IP use-model

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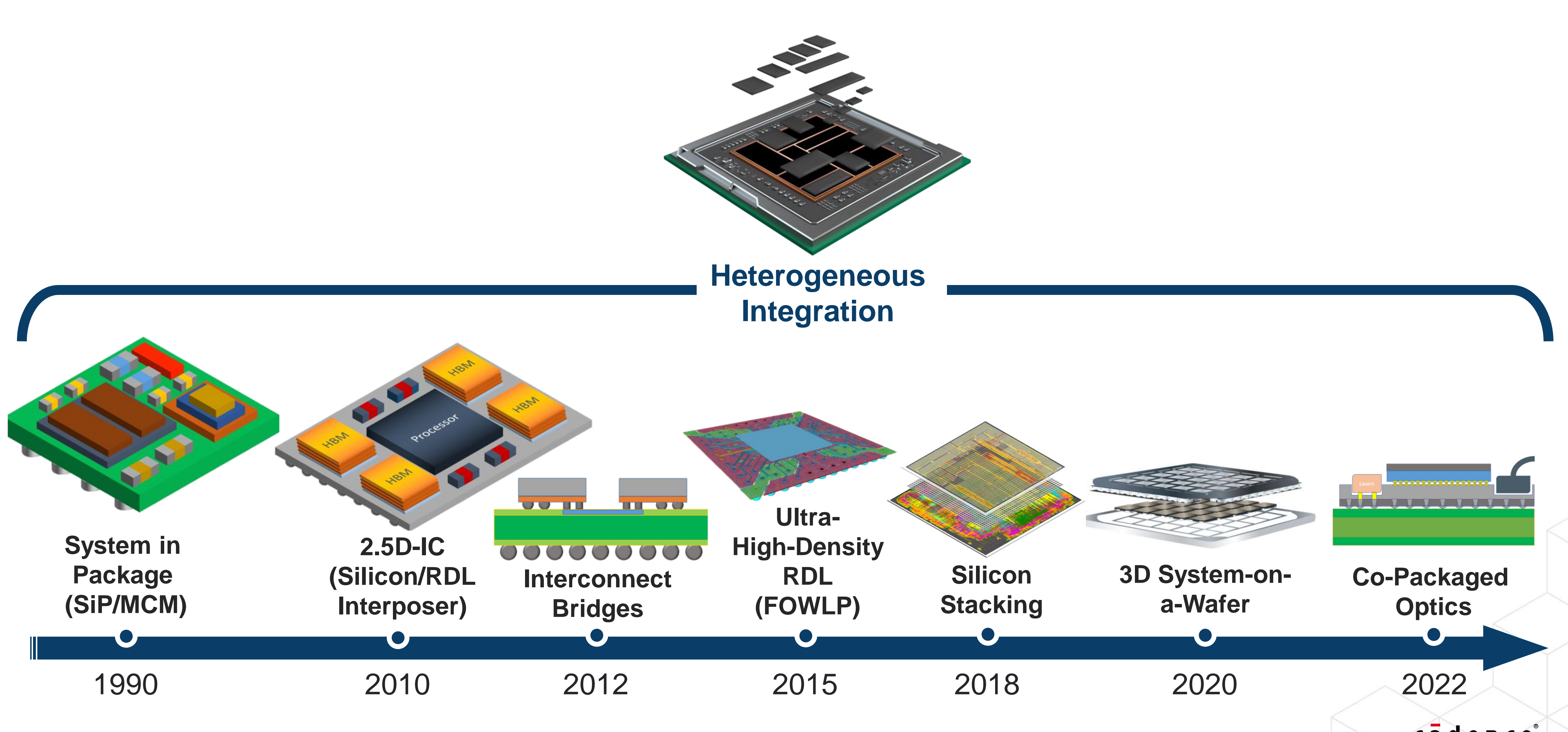
Heterogenous Integration Leverages Multiple Packaging Technologies



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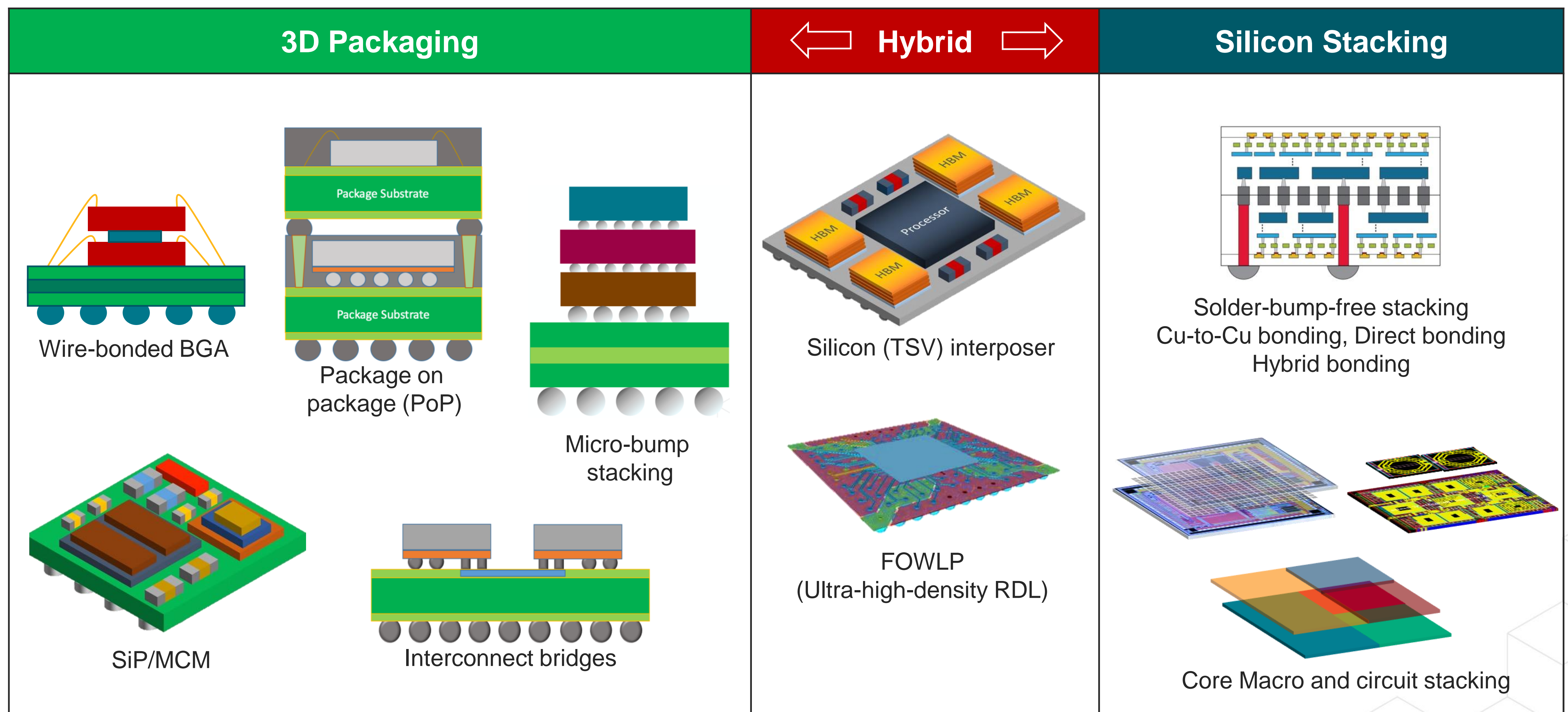
The Nuances of 3DHI Packaging



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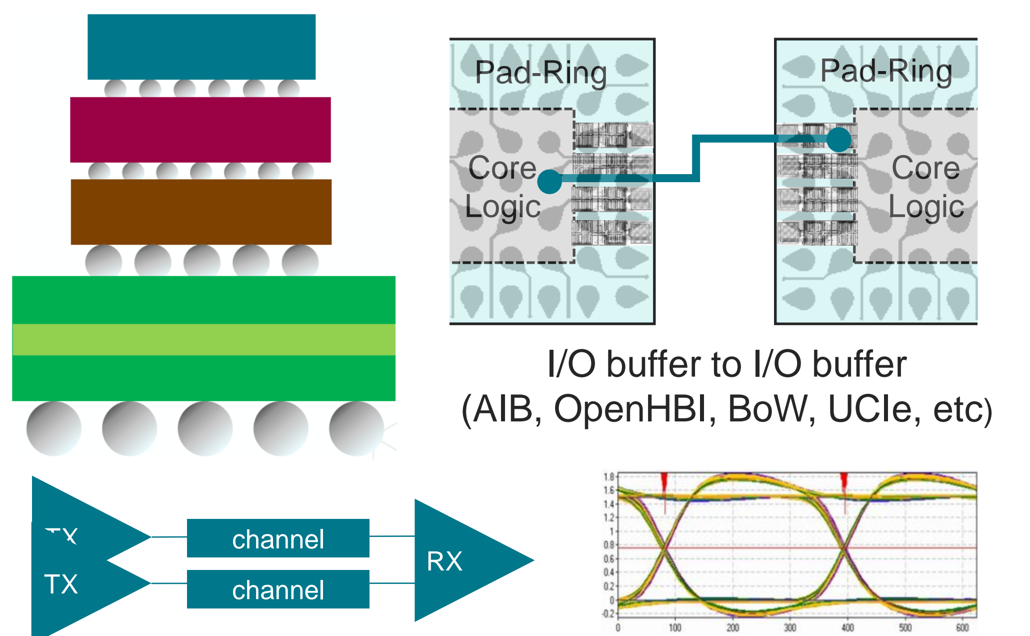
3D Packaging Versus Silicon Stacking (3DHI)

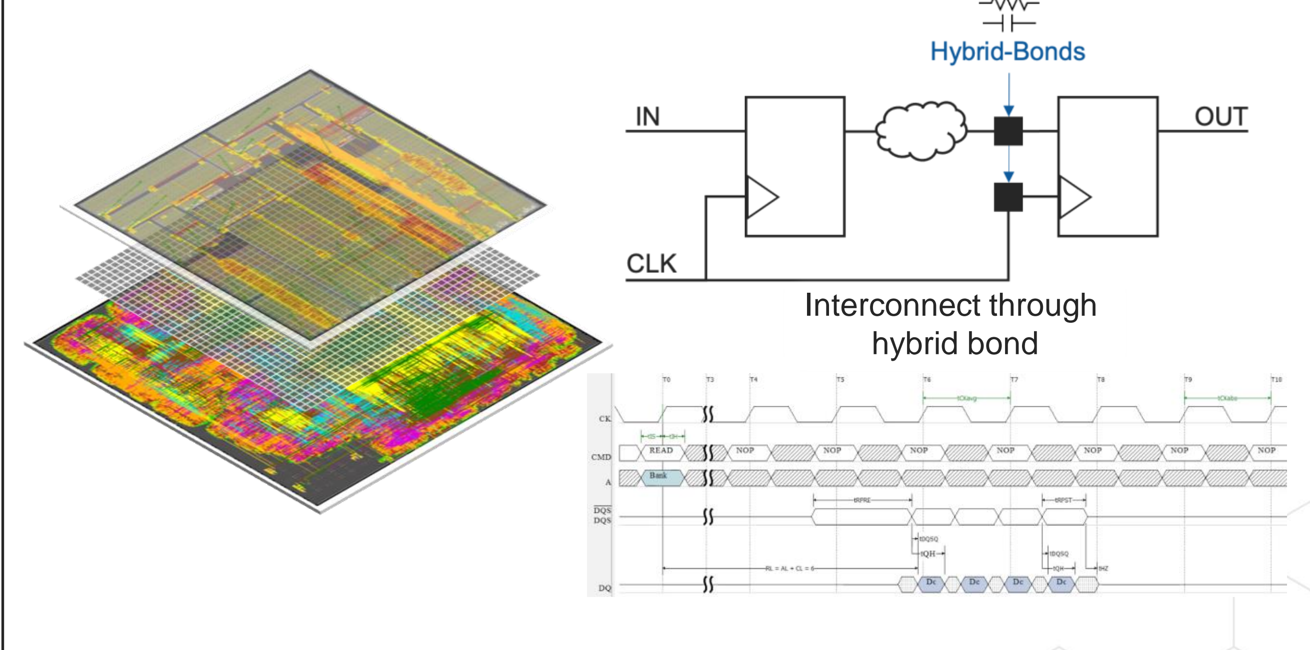
3D Packaging

- Solder-based connections
- Each die designed independently
- I/O buffer to I/O buffer signaling



Silicon Stacking

- Solder-free connections
- Single RTL partitioned at implementation
- DBI, hybrid-bond, cu-to-cu, direct connection



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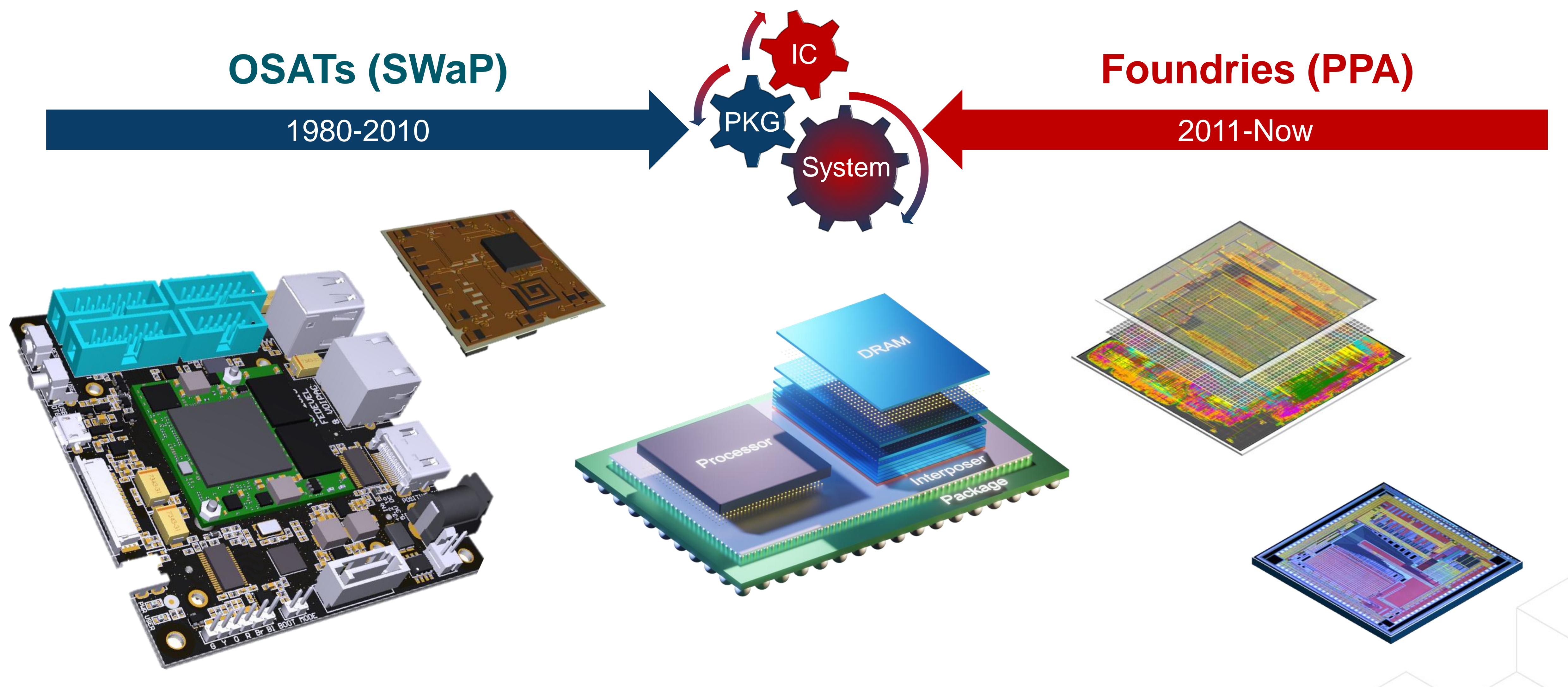
The Needs of IC and Systems Designers are Converging



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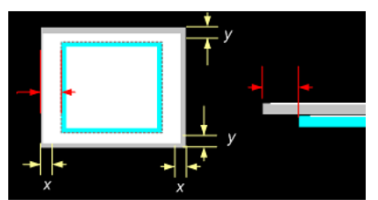
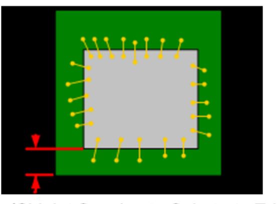
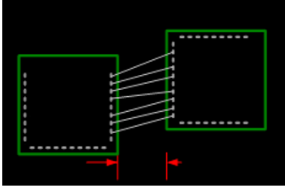
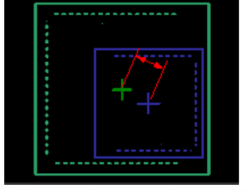
Multi-Chiplet 3D Ecosystem Challenges

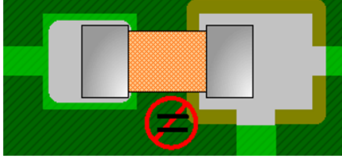


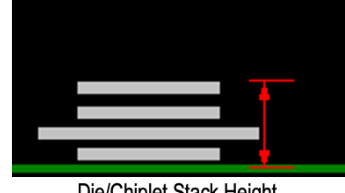
Die/Chiplet Overhang

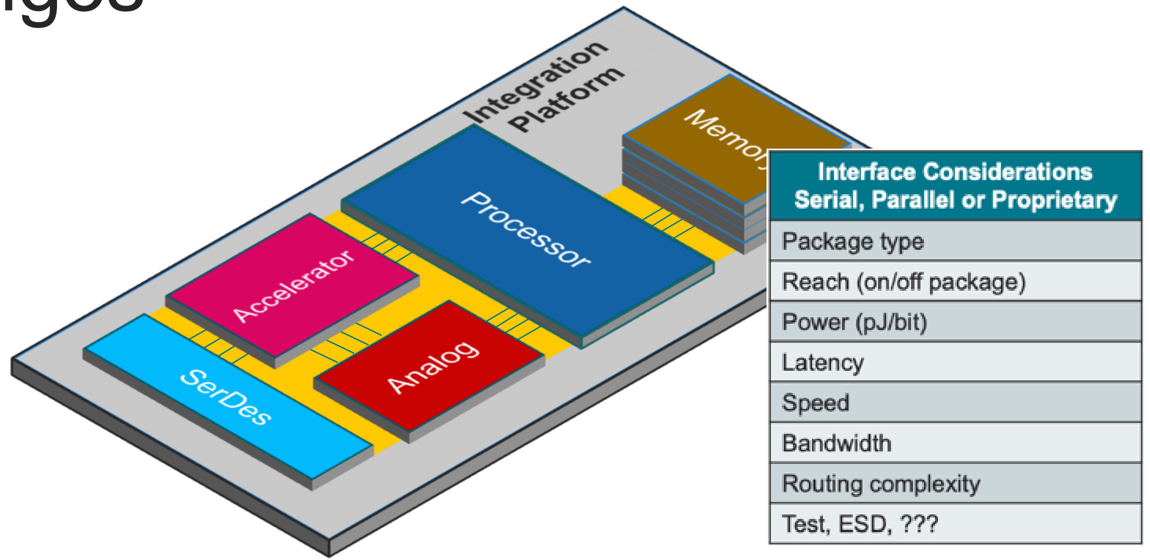

Die/Chiplet Spacing to Substrate Edge


Die/Chiplet to Die/Chiplet Spacing


Die/Chiplet Center to Center Offset


Tombstone Effect (% size diff)


Die/Chiplet Stack Height



Interface Considerations Serial, Parallel or Proprietary
Package type
Reach (on/off package)
Power (pJ/bit)
Latency
Speed
Bandwidth
Routing complexity
Test, ESD, ???

Assembly Design Kits

- PDK equivalent for the entire multi-chiplet assembly
- Historically, OSATs have not provided sufficient data to package designers
  - OSATs have large design centers to off-set this limited formal sharing of design requirements
- Foundries are helping to drive the concept of a PDK into the packaging world

COTS Chiplets

- Most chiplet-based designs are in a closed ecosystem
- Business case for IP companies to provide 3rd type of IP
- Standard exchange formats are lacking
- Common communication interface
  - AIB, UCIe, BoW, OpenHBI, …
  - Too many packaging options to standardize on a single interface

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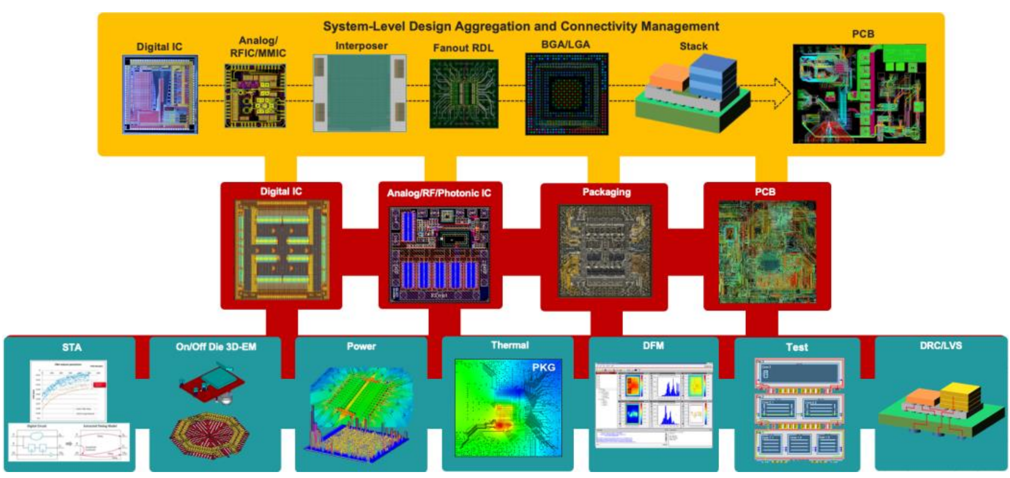
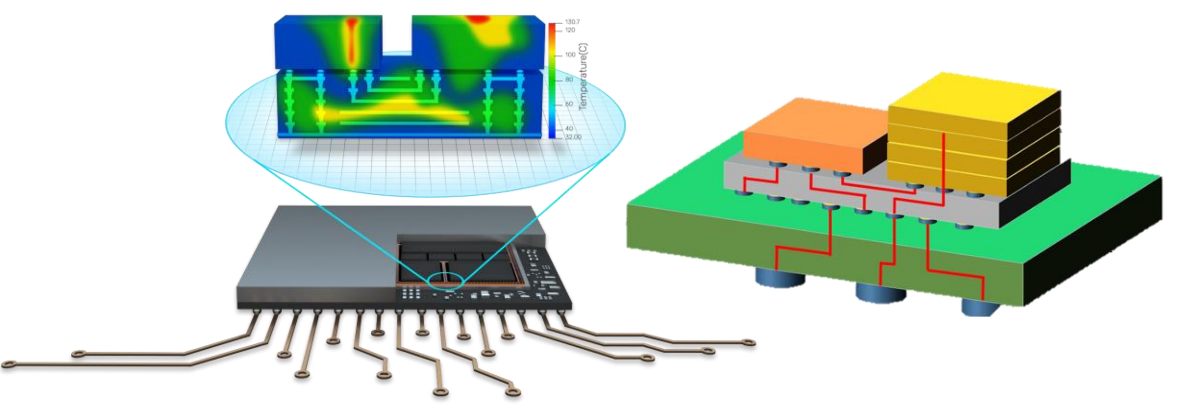
Multi-Chiplet 3D Challenges





Complex Design Flows

- Explosion in the number of design tools required
- System-level assembly planning, optimization and risk management
- Design partition strategies including D2D chiplets, thermal & off-package IO
- Need for common database for entire 3D-IC system
  - Chips, chiplets, tiles, packaging and PCB
- Early-stage Thermal and Electrical analysis

Analysis and Sign-Off

- STA with automated corner reduction
- Rule-deck-free systemLVS
  - Alignment and connectivity checking
- Multi-die EMIR
  - Accounting for dynamic loading across multiple die
- Comprehensive thermal stress and CMP planarity checks
- New 3D-IC test standards
- Very large structures (billions of instances) need 3D-EM modeling

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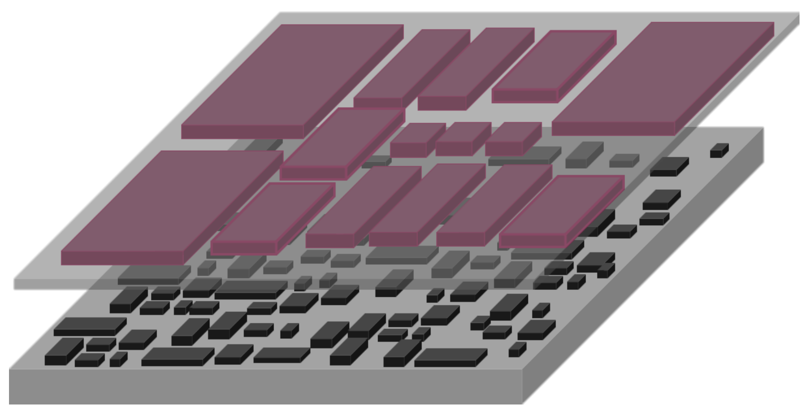
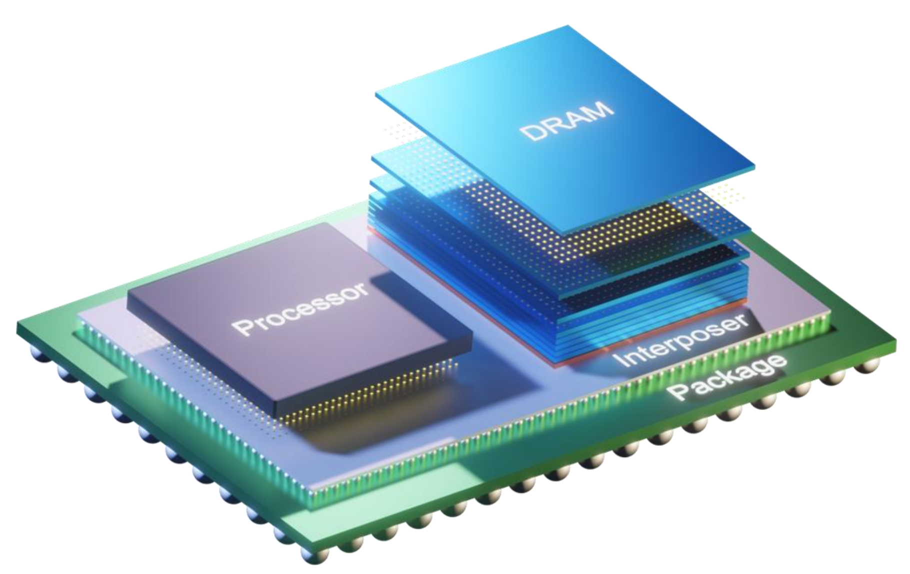
Multi-Chiplet 3D Challenges





3D Implementation

- Design size capacity
- Support for chiplets across multiple nodes/technologies (PDKs)
- Concurrent editing of multiple devices at full transistor-level detail
  - No abstraction
- On-the-fly die splitting and re-partitioning in Z direction
- Timing driven cross-chip(let) routing
- Co-design with packaging

Advanced Packaging

- Transitioning from laminate design to silicon design
  - Formal sign-off of DRC and LVS
- Differencing power/ground routing styles
  - Stripes/rails
  - Copper pour
- Advanced metal balancing
- Design capacity
  - Tens of thousands to hundreds of thousands (or more)

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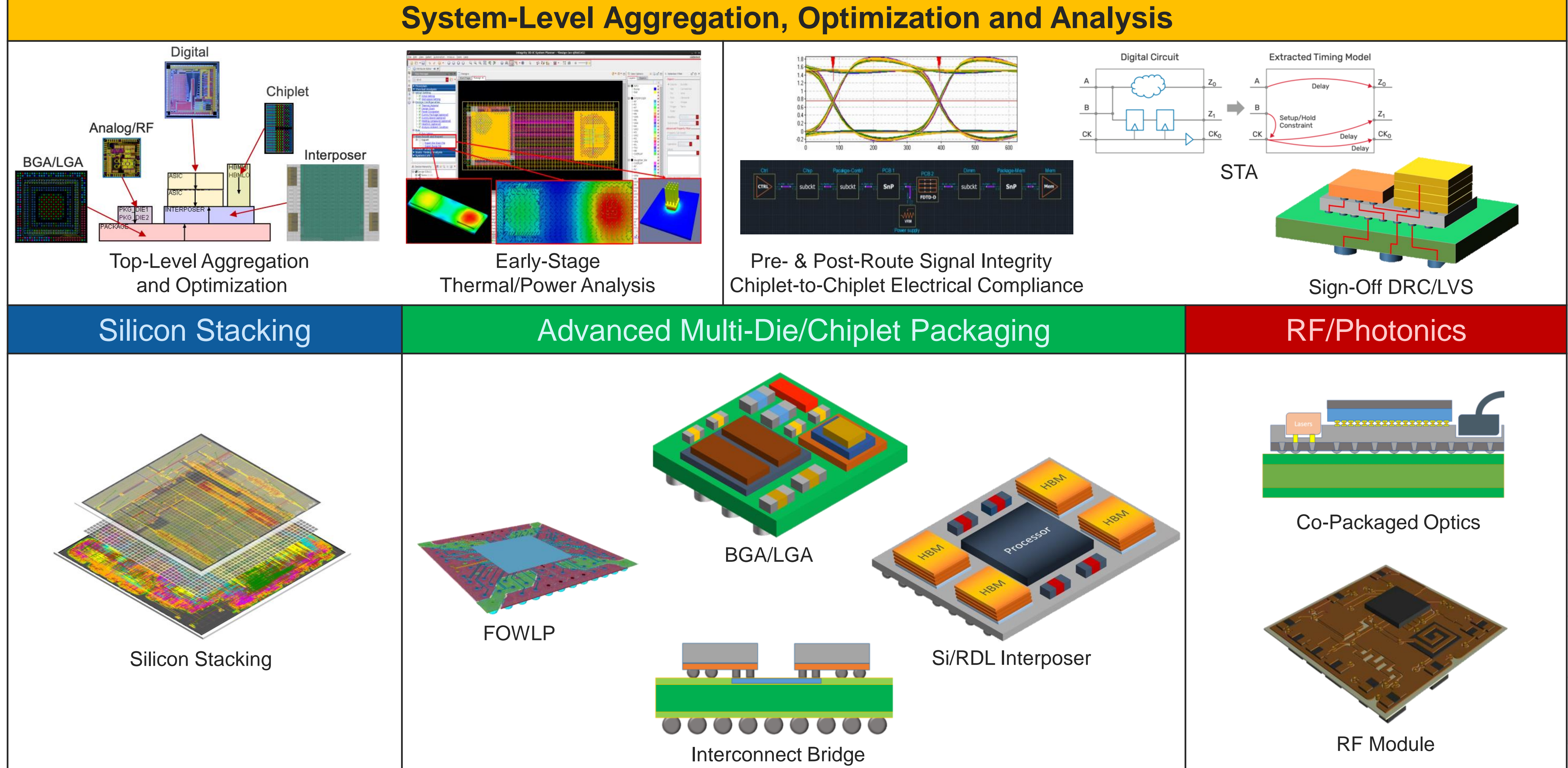
What to Look for in a Next-Generation 3D Integration Platform…



Summary

Advanced Packaging and 3DHI are Driving More-Than-Moore

Heterogenous Integration Leverages Multiple Packaging Technologies

Several New Challenges Facing Designers Moving to 3DHI

Is it Time to Reevaluate Your Design Methodology?

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