Realization of Multi-Die Systems in the SysMoore Era

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Outline

Market Trends

Multi-Die Design Challenges

The EDA Solution Driving Innovation

Summary

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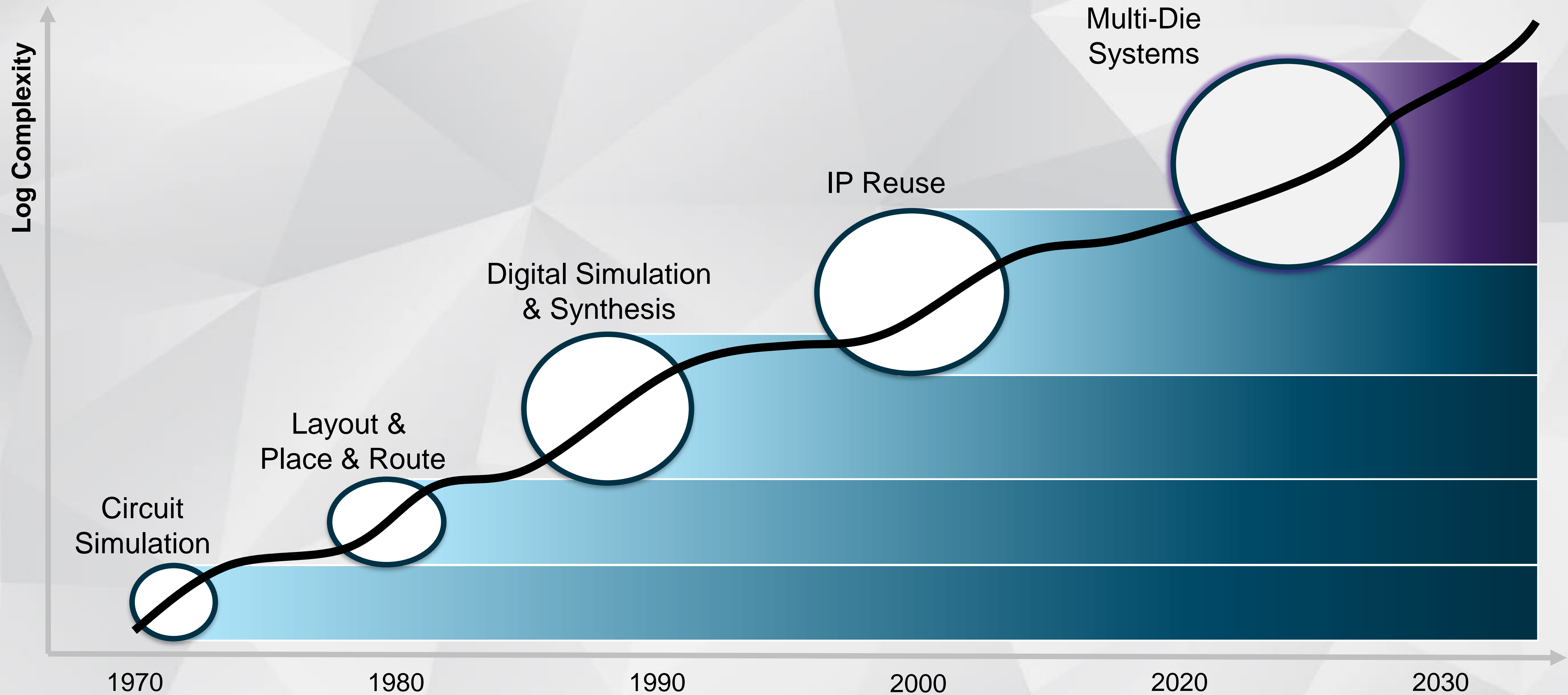
Semiconductor Design Productivity Waves

Multi-die system design: key enabler of the SysMoore era



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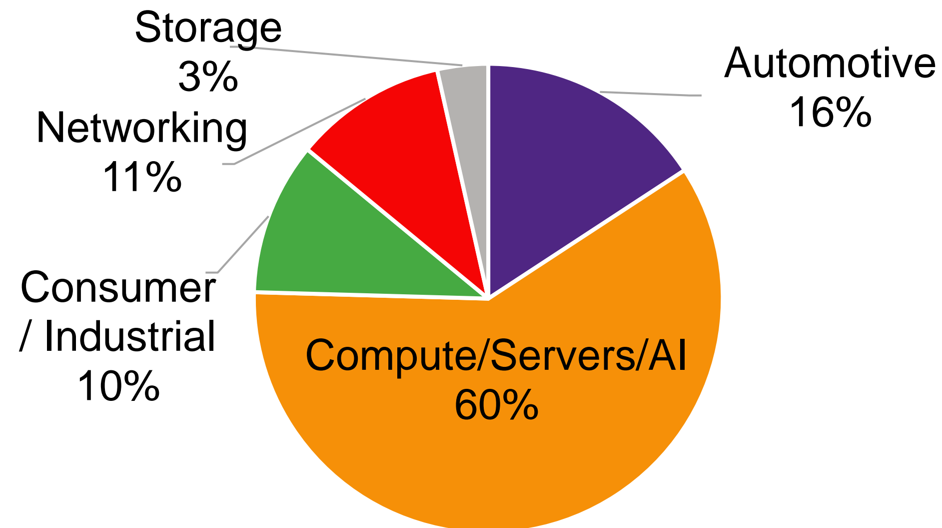
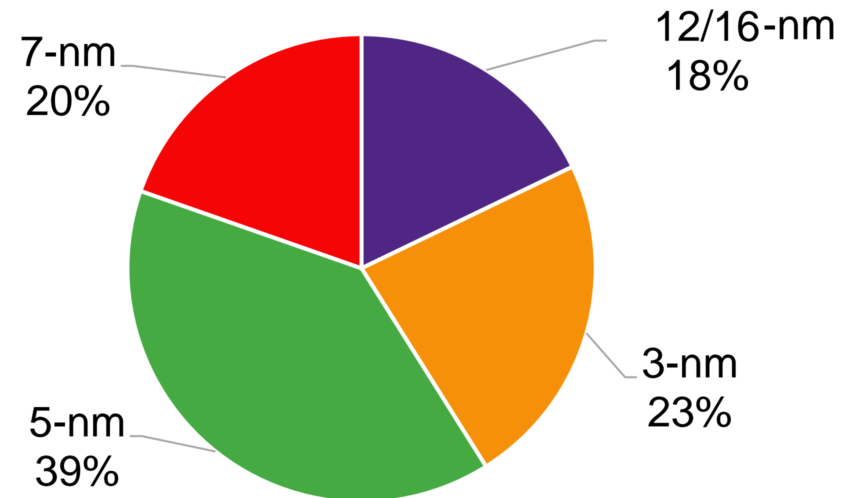
The Era of Multi-Die System Design is Already Here

Designs by Application



- The datacenter – Servers / AI – dominate
- NICs, Switches common use case
- Smartphone / Graphics / PC primarily proprietary
- Co-packaged Optics, Automotive ramping

Designs by Process Technology



- CPU/Processors driving down Moore's law
- I/O chiplets typically in N-2, N-1 processes (e.g., 7-nm or 12-nm)

Source: Synopsys (excluding proprietary interconnects)

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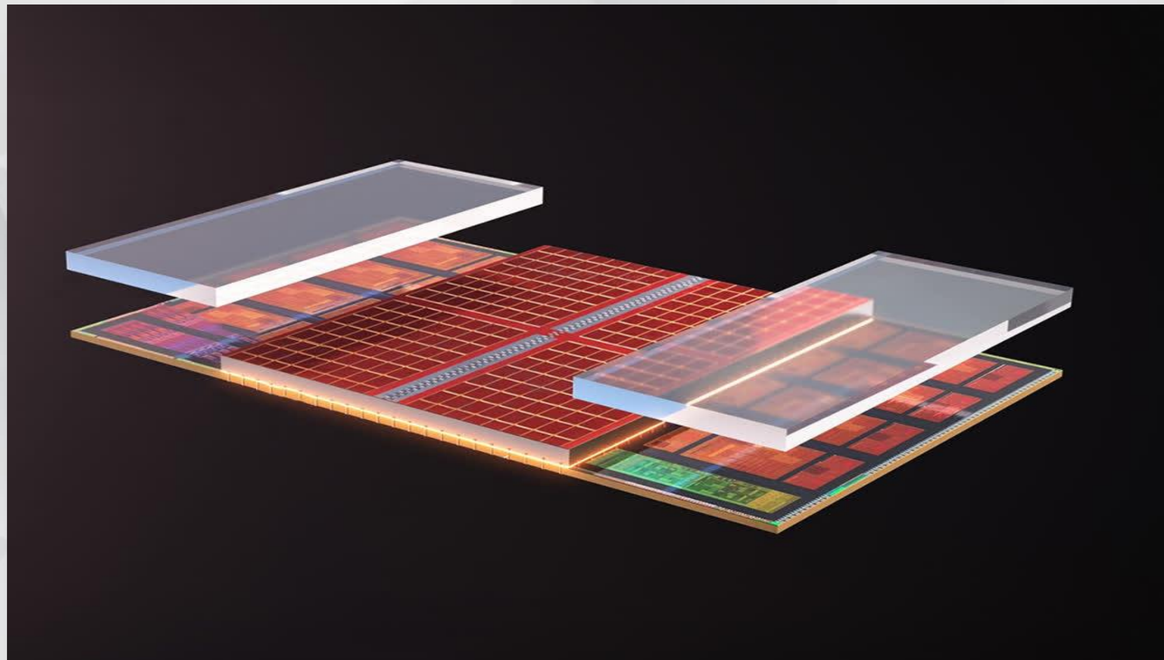
Enabling Truly Transformative Products

Examples of commercial high-performance, high-density multi-die systems

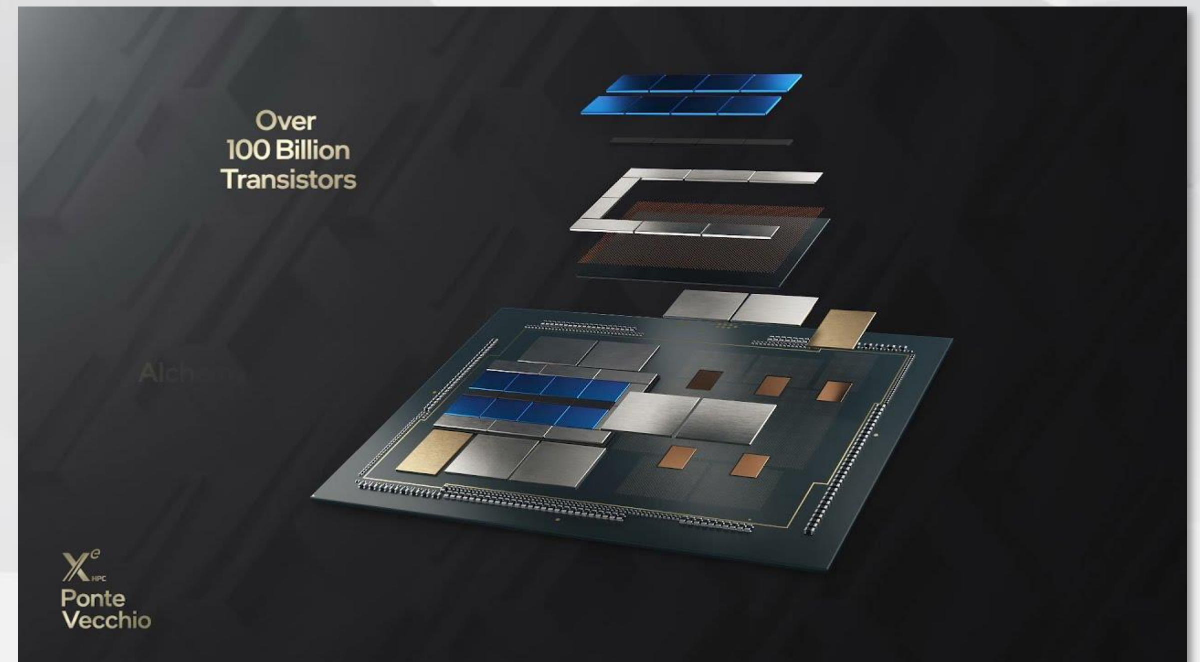
AMD



3D V-Cache: Hybrid Bonded

3x Energy Efficiency, 15x Interconnect Density
(vs. Micro-bumps)

INTEL



Exascale Computing / AI

100B+ Transistors, 47 Active Tiles, 5 Process Nodes

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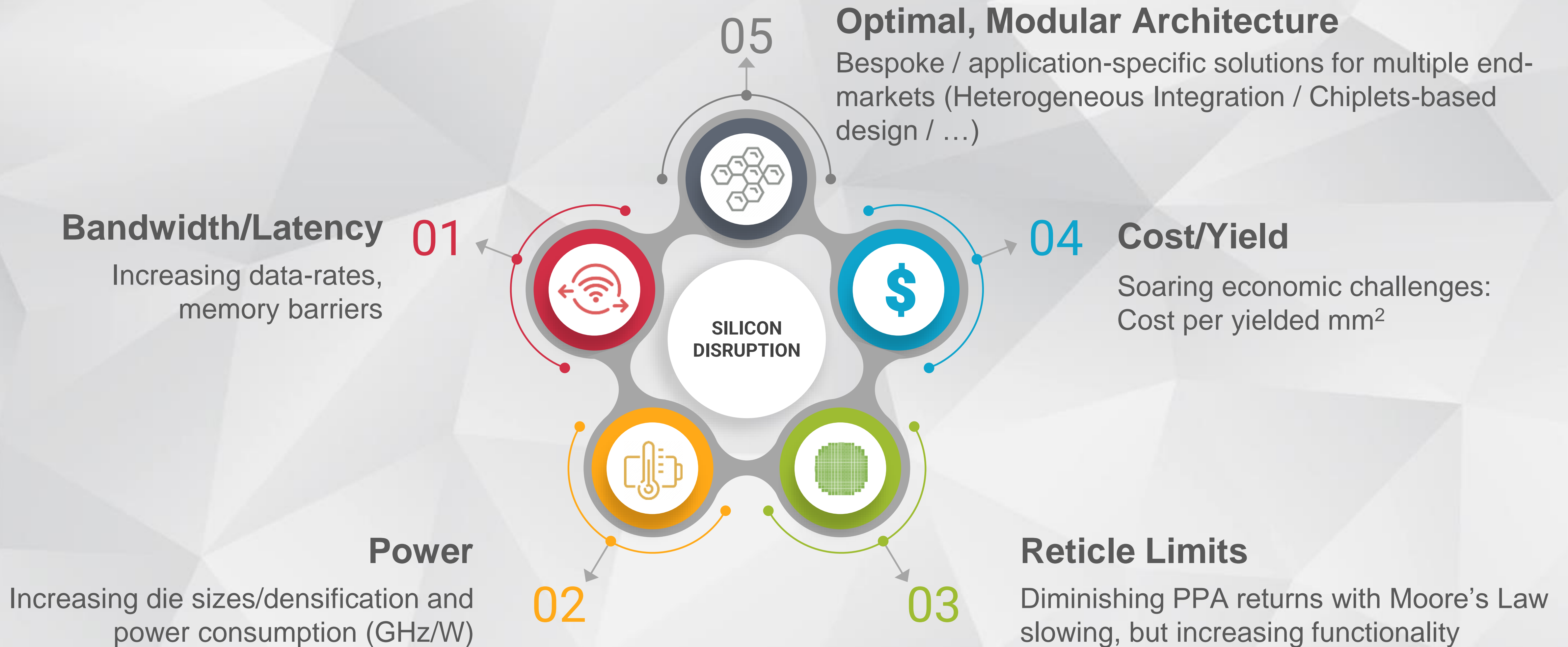
The Drivers of Multi-Die System Design



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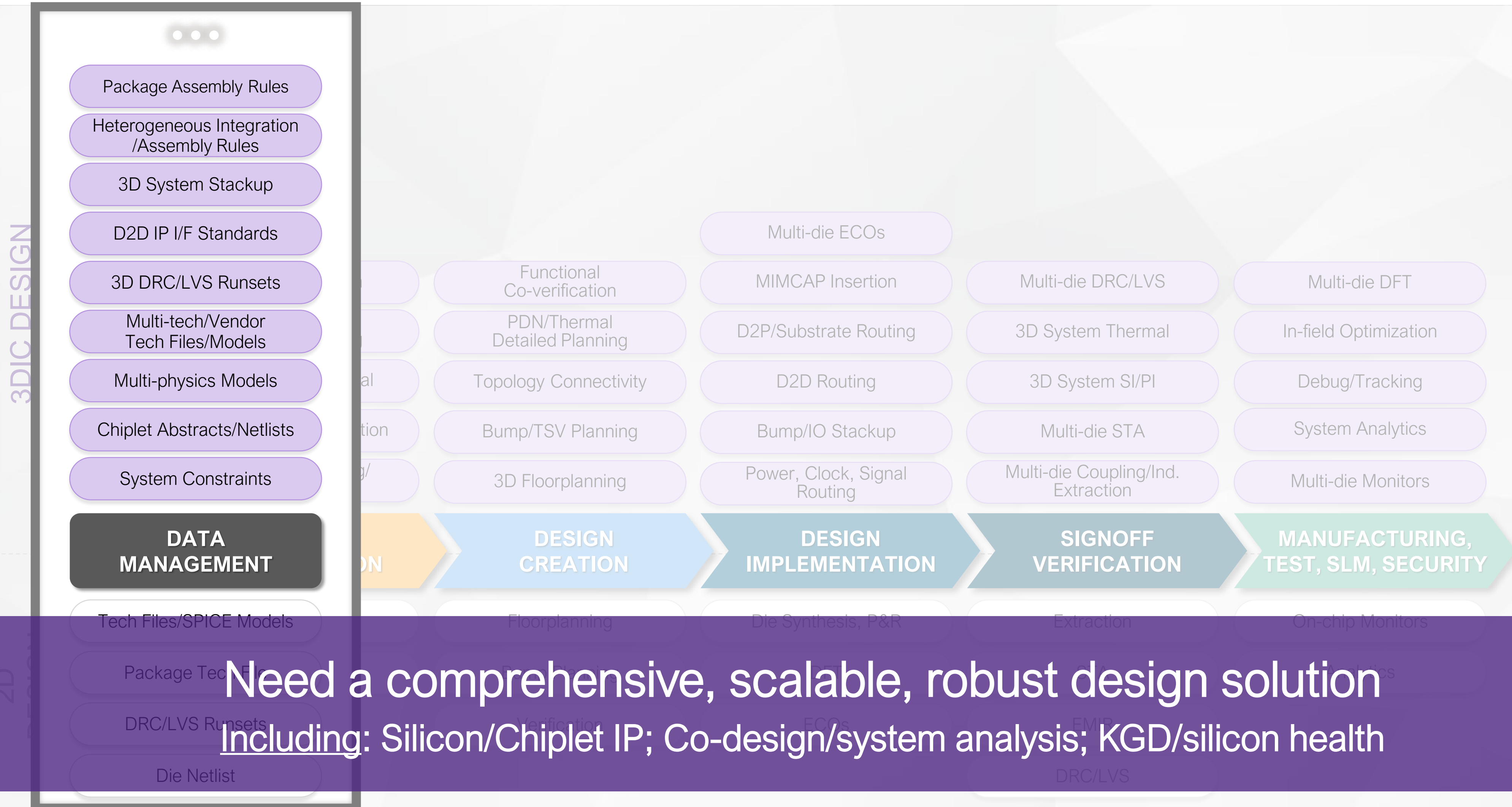
New Dimensions Bring New Opportunities… and Challenges

The multi-die/3DHI design flow is expansive – data consistency is critical



Need a comprehensive, scalable, robust design solution

Including: Silicon/Chiplet IP; Co-design/system analysis; KGD/silicon health

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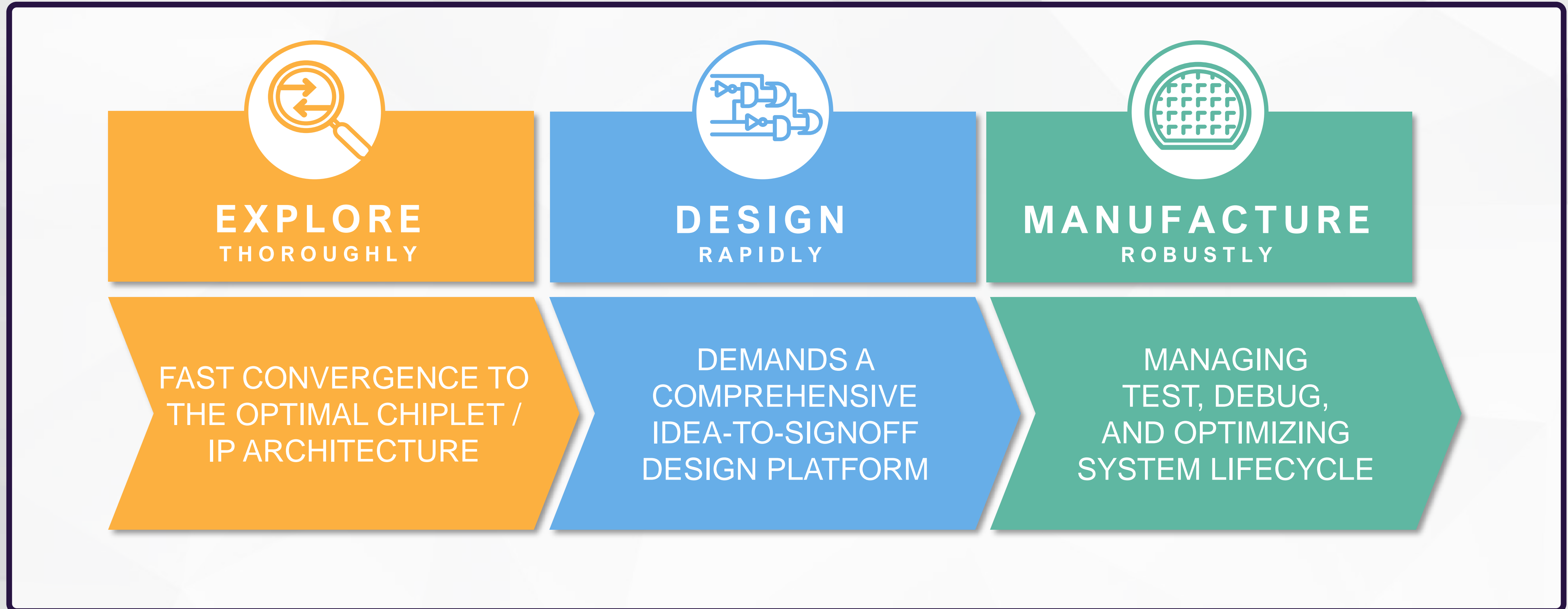
Key Facets of a Multi-Die System-Design Solution



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Robust Die-to-Die Interface IP at the Heart of Multi-Die Growth

UCIe: Emerging as a preferred D2D I/F

- **Technical Merits** (Most compelling PPAs)
  - Energy efficiency <0.3pJ/Bit
  - Edge efficiency >5Tbps/mm
  - Latency ~2ns from pin to FDI
- **Comprehensive and Futureproof**
  - All use cases
  - All package types
  - Complete protocol stack
  - Future proof with support up to 32Gbps data rate per pin
- **Broad Ecosystem**
  - Wide range of promoters and contributors spanning all industry segments

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Robust Die-to-Die Interface IP at the Heart of Multi-Die Growth

Synopsys' IP solutions for broad-market applications

IP PORTFOLIO

- Silicon proven
- High quality
- Secure

Foundation IP | **Interface IP** | Security IP | Processor IP

IP SUBSYSTEMS

Configured Interfaces
(PCIe Subsystem)

- Pre-validated
- Integration-ready

Test Bench Environment

VIP | Controller IP | RAMs | Custom logic | PHY IP | Clock & Reset | Register Interface | Control Registers | Debug Module

IP CHIPLETS

Ethernet IO Chiplet

Memory Expander Chiplet

AI Accelerator Chiplet

D2D Interface

...

SYNOPSYS IP CHIPLETS

- Built on Synopsys' silicon-proven, high-quality IP portfolio
- Flexibility to support multiple package types
- Customizable to target application
- Key features
  - Standards-compliant interfaces
  - Hierarchical test
  - Built-in security
  - SLM support
  - Yield enhancement functionality

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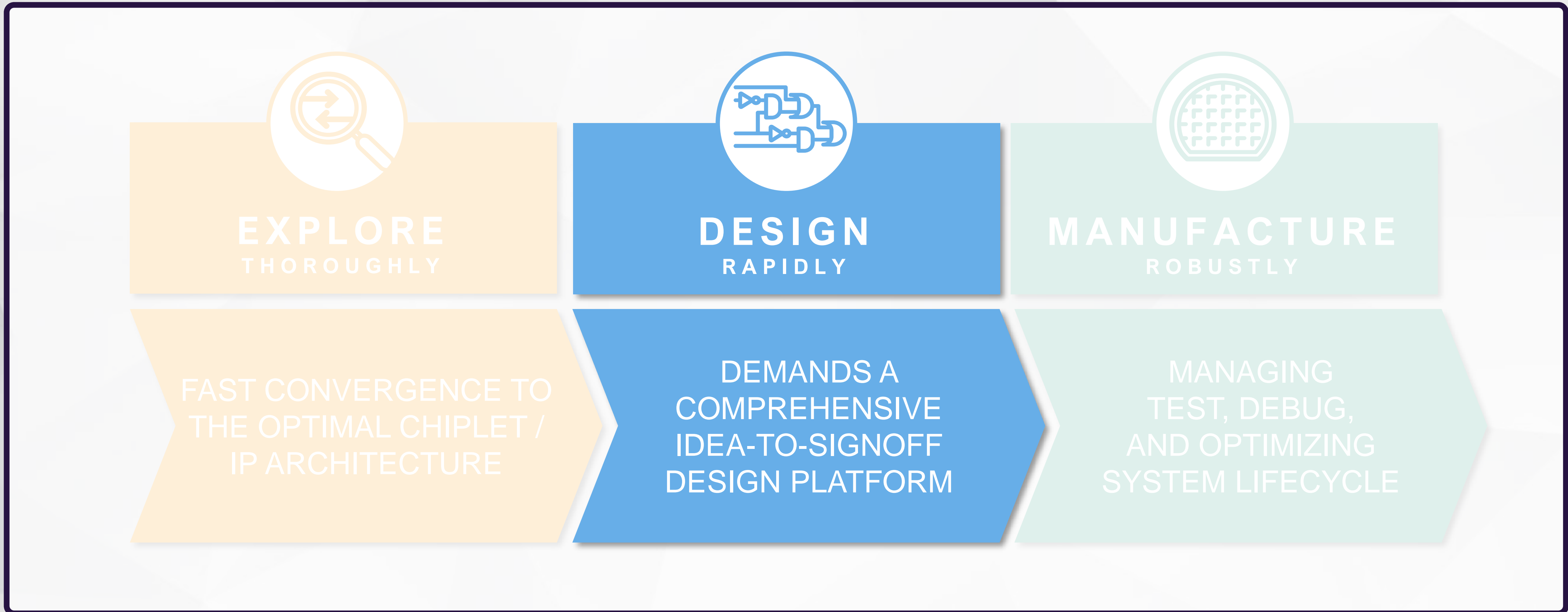
Key Facets of a Multi-Die System-Design Solution



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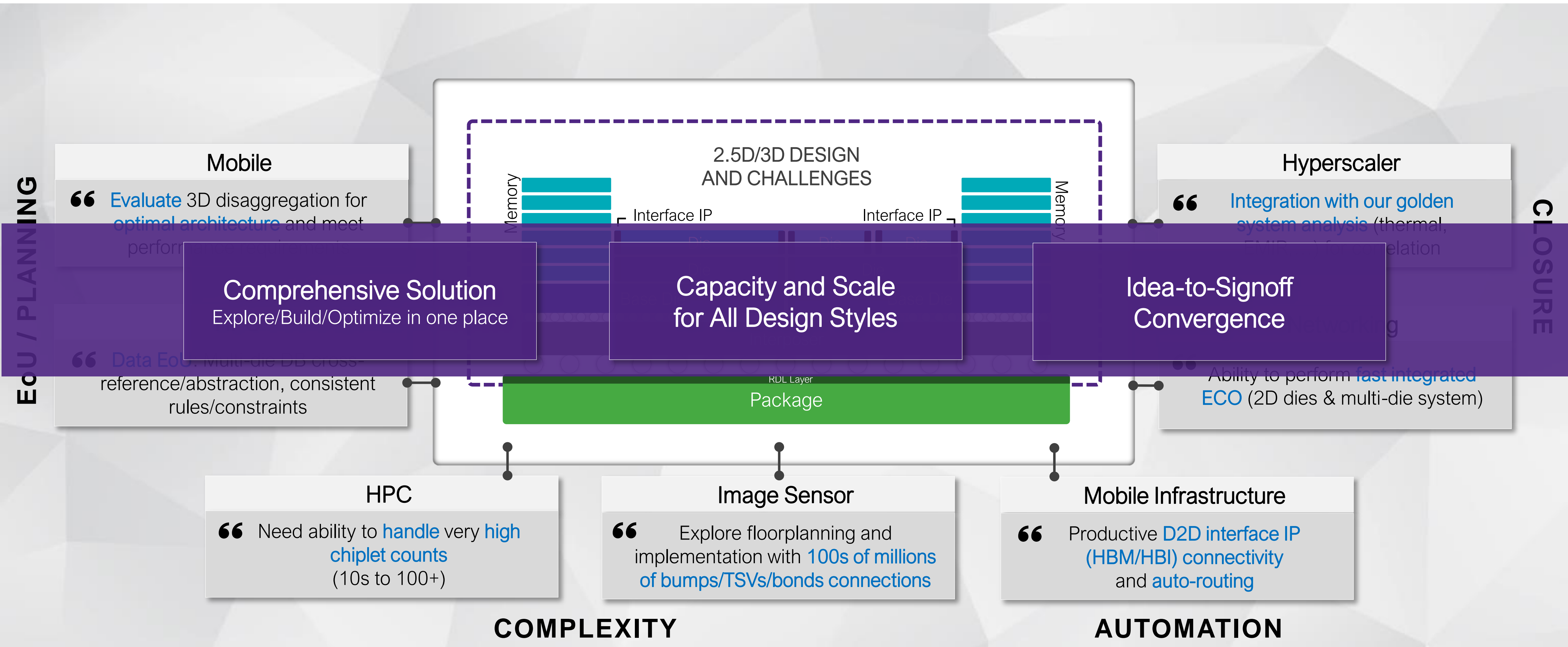
Multi-Die Design Requires a Re-Evaluation of Needs

A broader scope of challenges and demands



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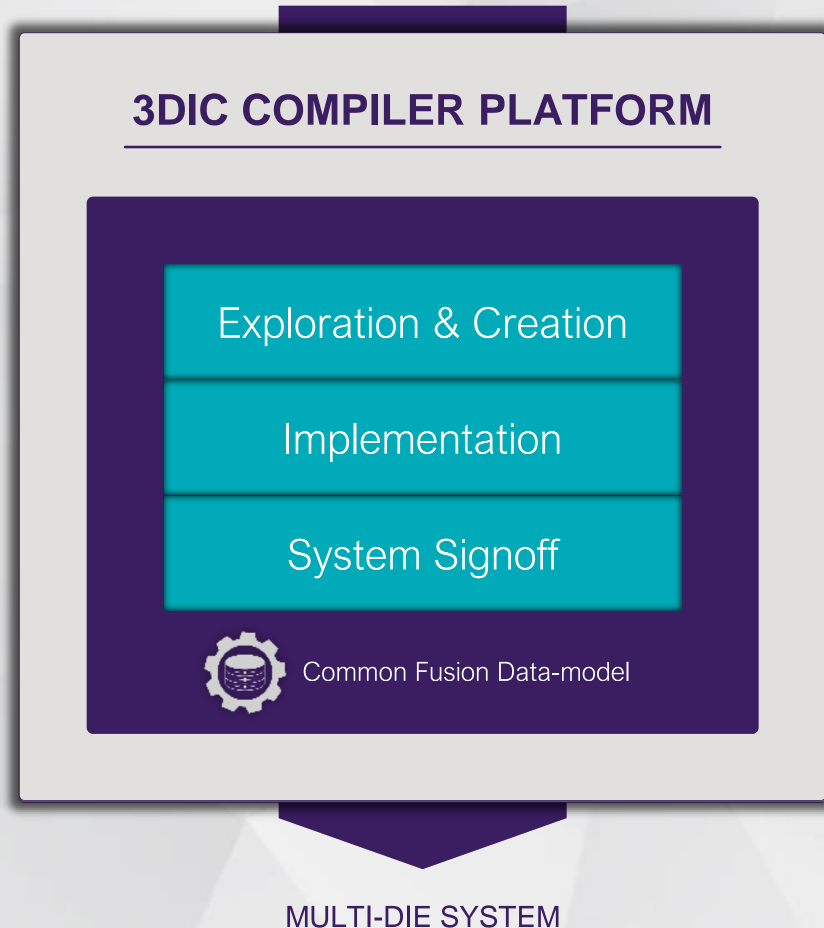
The Synopsys Unified Platform for Multi-Die System Design

Full-scope system-level co-design and analysis



A Highly Scalable Platform

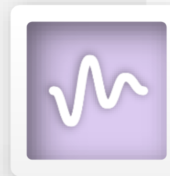
Heterogeneous integration of 100s of billions of transistors
Billion+ inter-connections in a few hours

Seamless 2D to 3D Design Continuity

Common data-model and tech-files
Efficient, concurrent workflow for faster closure

Unified Full-Flow Productivity

Single environment for full system design
Full breadth engines: design, test, analysis, verification



Trusted, Golden-Signoff Analysis

Industry-leading technologies – STA, Thermal, EMIR, SI/PI
Fast convergence to optimal PPA/mm^3, accelerate tapeout

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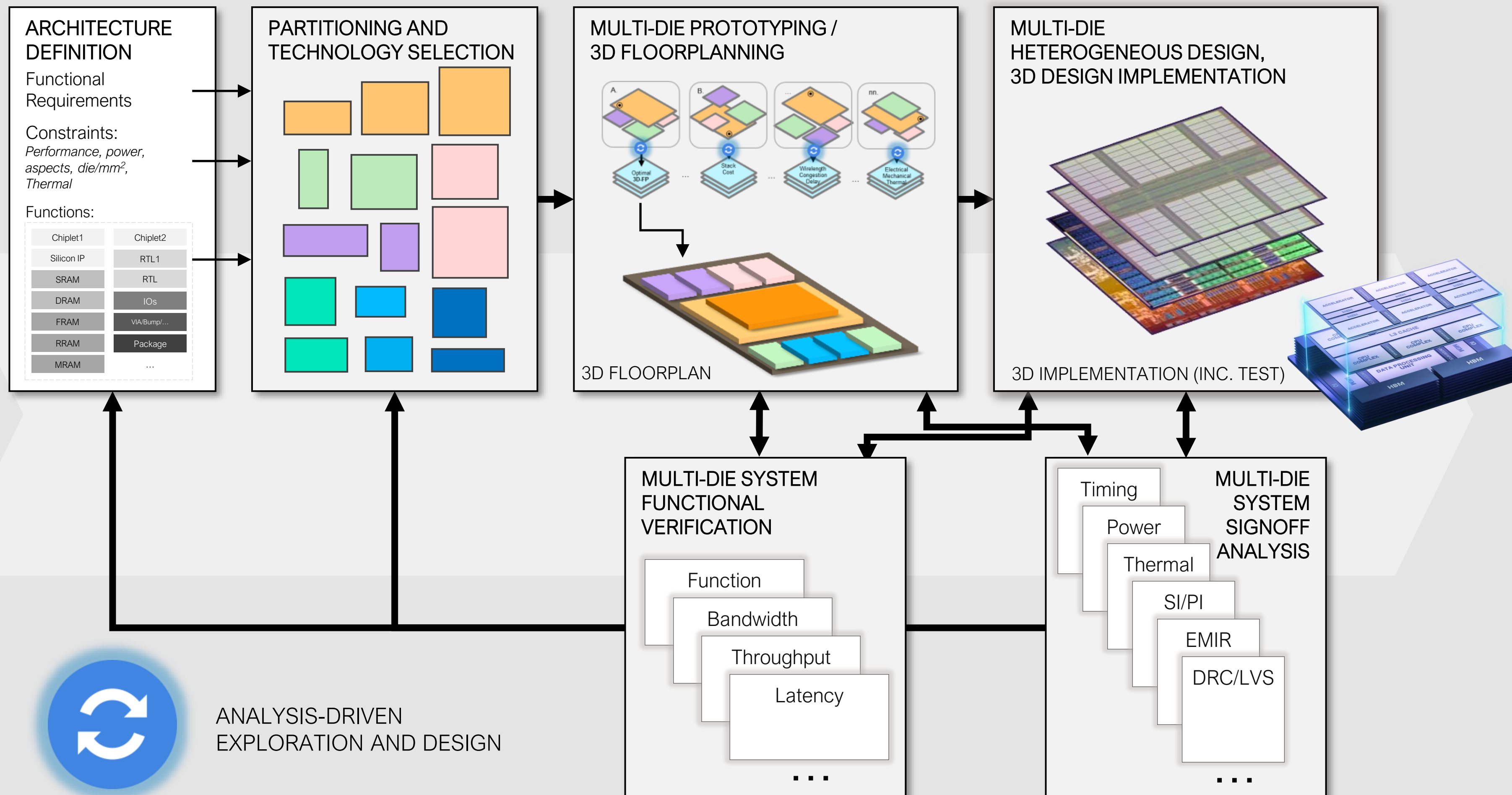
Convergence and Closure Demands Analysis-Driven Design

Create, Implement, Refine, Converge – A 3DHI example



- Full, partial, or zero netlist design entry for multi-die feasibility analysis
- Auto extraction / abstraction of IP and connectivity from existing 2D dies/modules
- Multi-fab/-node IP and block management support
- Fast floor-planning and connectivity optimization using 3D analytical assessment

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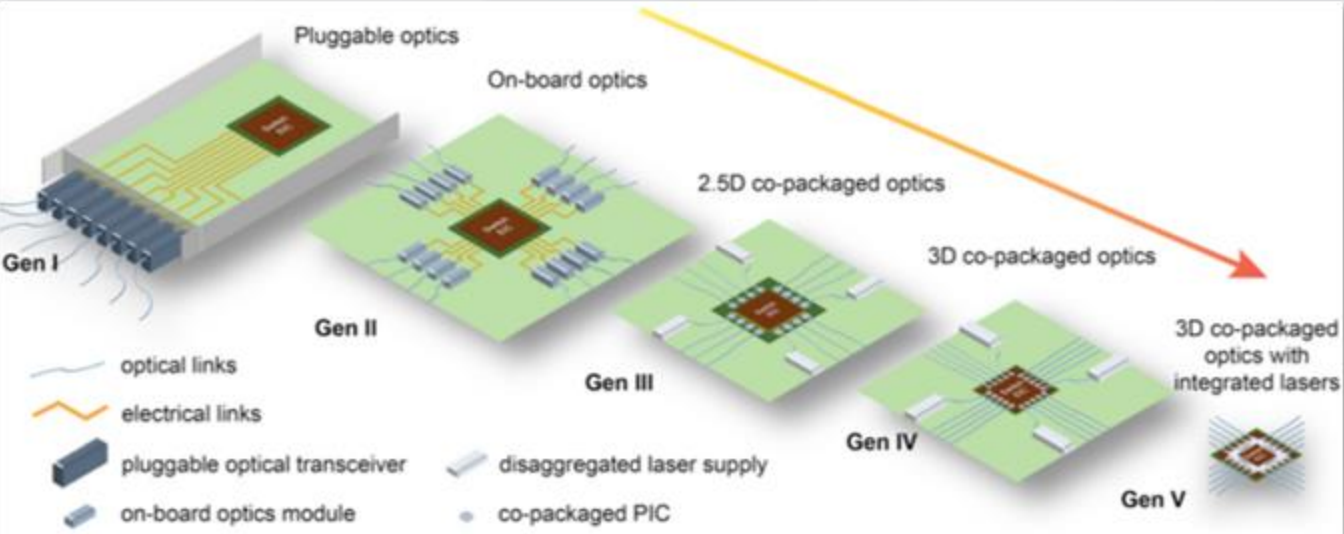
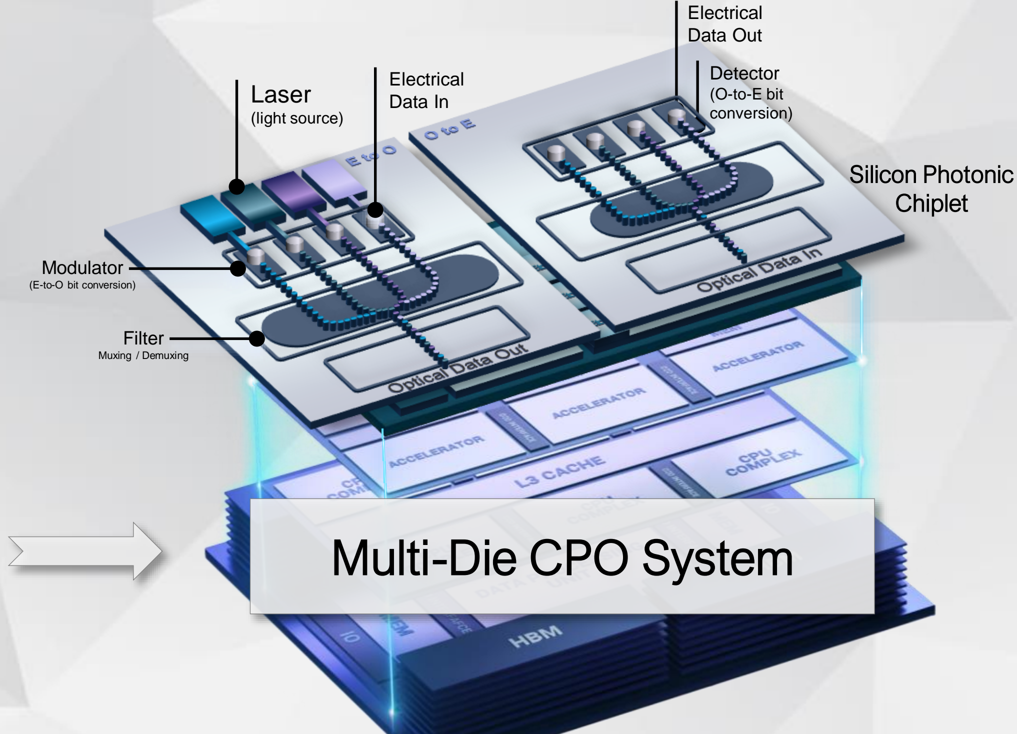
The Co-Packaged Optics (CPO) Solution to Performance

The silicon-photonic chiplet – Another die in a multi-die system

Generational progression:
Tighter integration between Datacenter Switches and Optical IO





Source: John Bowers, UCSB

3DIC COMPILER
Multi-Die Heterogeneous-Integration Platform

OPTO COMPILER
Photonic Chiplet Design

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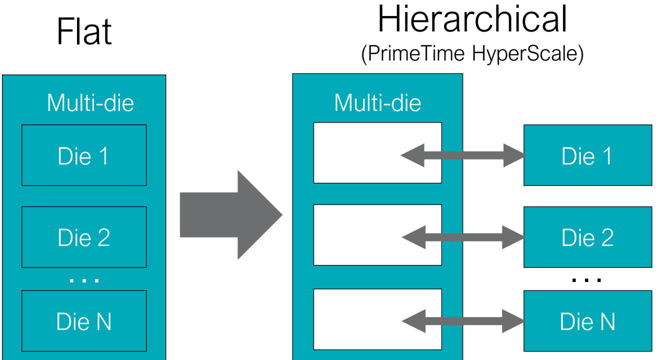
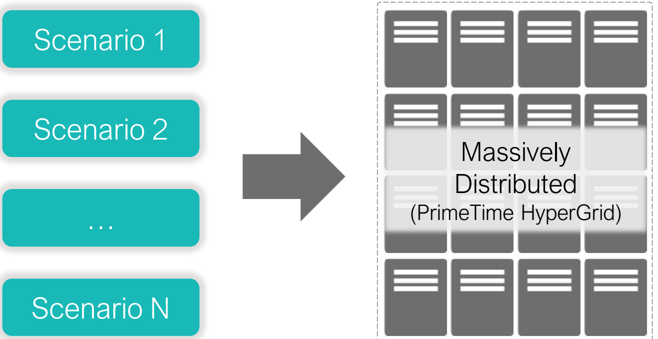
Achieving Golden Signoff for Multi-Die Systems

STATIC TIMING ANALYSIS AT SCALE



Hierarchical Signoff

Runtime and memory efficiency with full flat accuracy

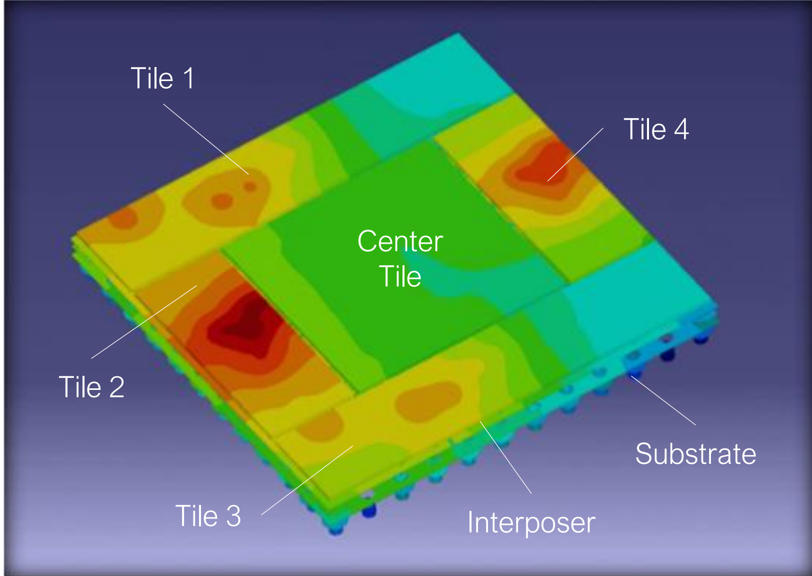


Resource Maximization

Multi-scenario/corner, cloud native
+
Smart corner reduction (10x)

THERMAL ANALYSIS AT SCALE

Integrated System-level Hierarchical Thermal Analysis



Courtesy: Ansys

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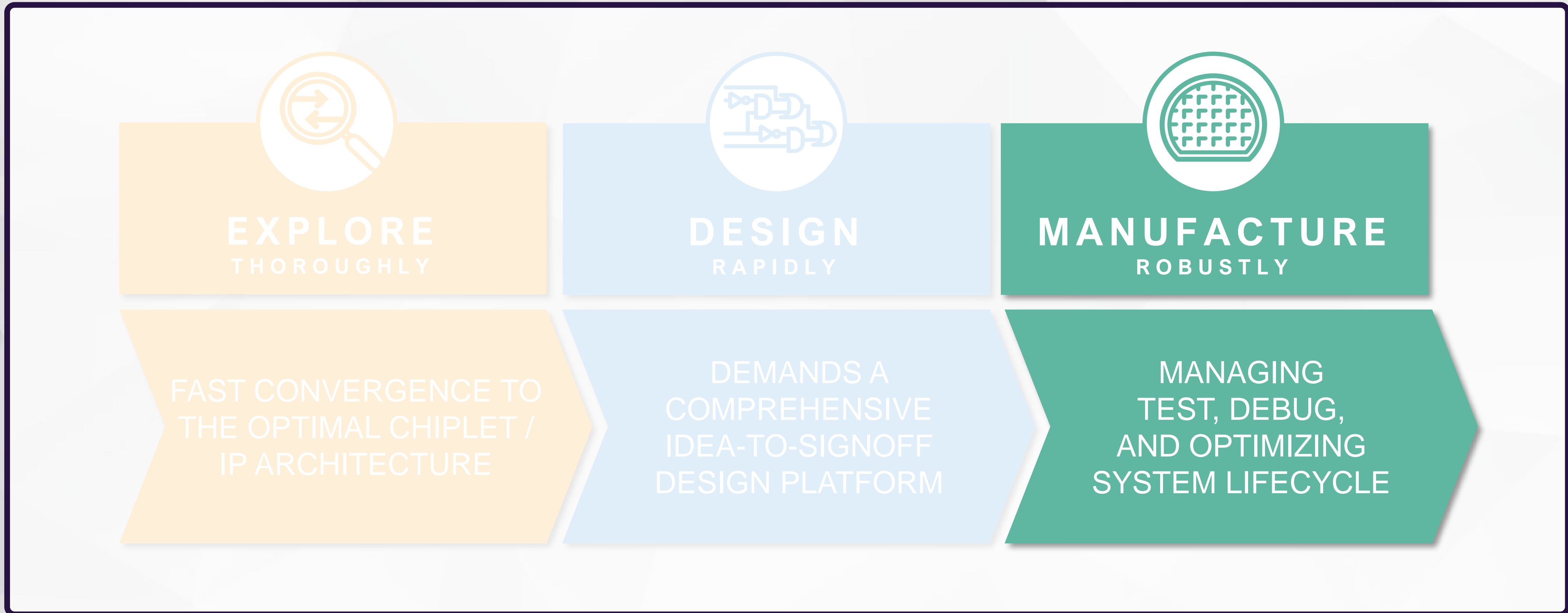
Key Facets of a Multi-Die System-Design Solution



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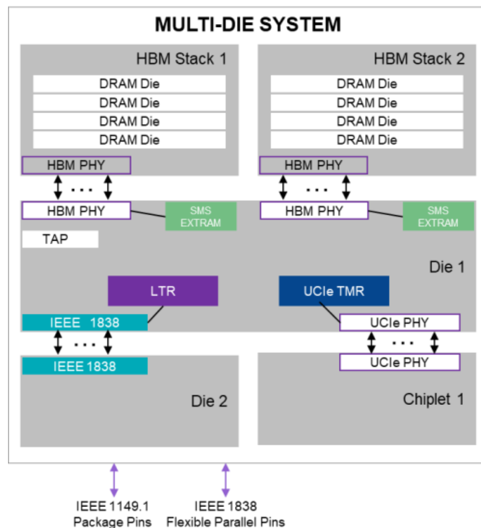
Enabling the Manufacturing Ramp and Product Reliability

Synopsys' TestMAX and the SLM Family of products

MULTI-DIE SYSTEM TEST AND REPAIR

PRODUCT QUALITY (KGD, Package, System)



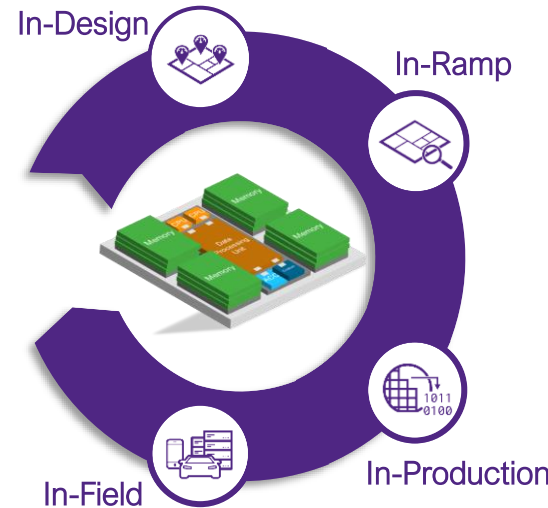
Ensure quality with comprehensive test, debug, repair for multi-die systems

Integrated Test for:
Multiple Dies, Memories, Interconnects, and Full-system

Test Access	Logic-to-Logic	Logic-to-Memory	Via / Bump / Interconnect
IEEE 1838	PHY Monitor, Test & Repair	Ext. Memory BIST & Repair	High volume Lane Test & Repair

SILICON LIFECYCLE MANAGEMENT

RELIABILITY, YIELD, HEALTH



Enhance multi-die system operational metrics through environmental, structural, functional monitoring

Solution comprises:
Silicon IP
EDA Software, and
Analytics Insights

In-Design	In-Ramp	In-Production	In-Field
Power/Performance Optimization	Yield, Failure Diagnosis	Volume Test, Quality and Traceability	Optimization, Safety, Security, Maintenance

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Summary

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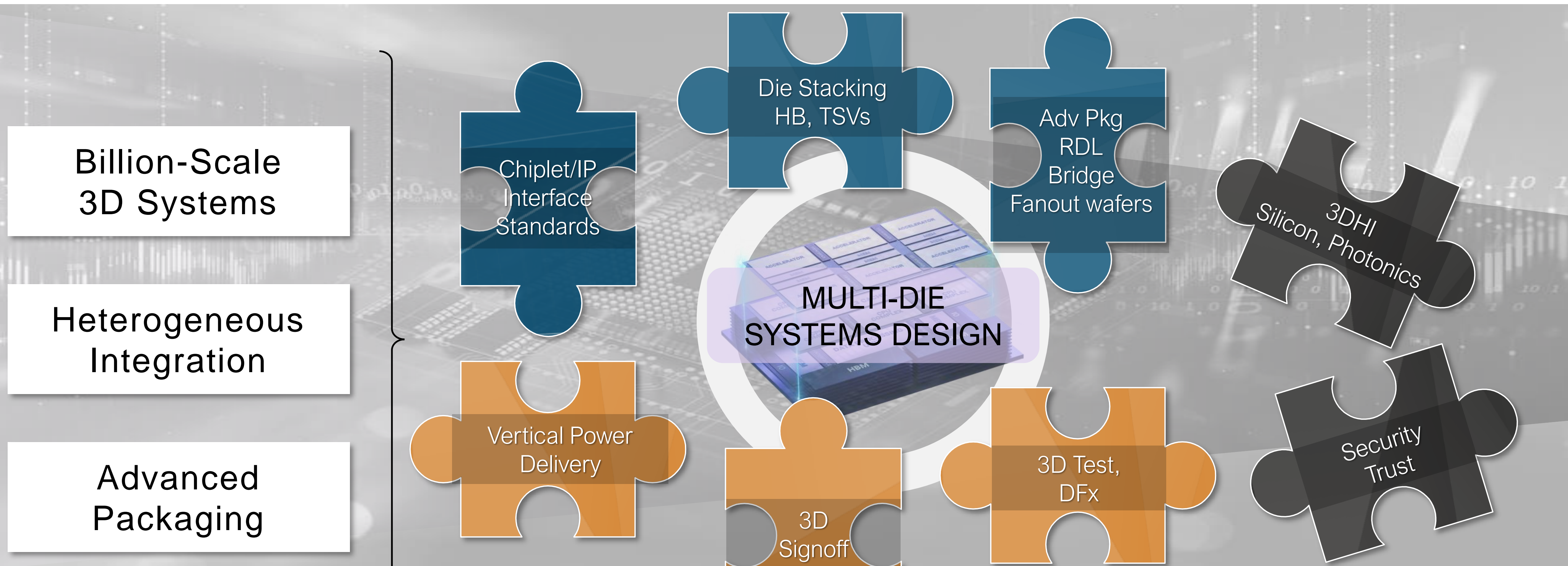
Multi-Die Systems: The Next Wave in Semiconductor Design

New Dimensions, *New Challenges*, **New Opportunities**…



Need a holistic solution for efficient multi-die system design, and industry-wide collaborations to catalyze *SysMoore Era* innovations

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THANK YOU

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