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System Foundry and the Chiplet Revolution

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IEEE EDPS 2022

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Outline

- System Foundry Overview (IFS)
- Industry Vision & Motivation
- Technology Needed – Architecture, Design, Debug & Test
- Industry Case Studies

IFS Overview

From Wafers to System

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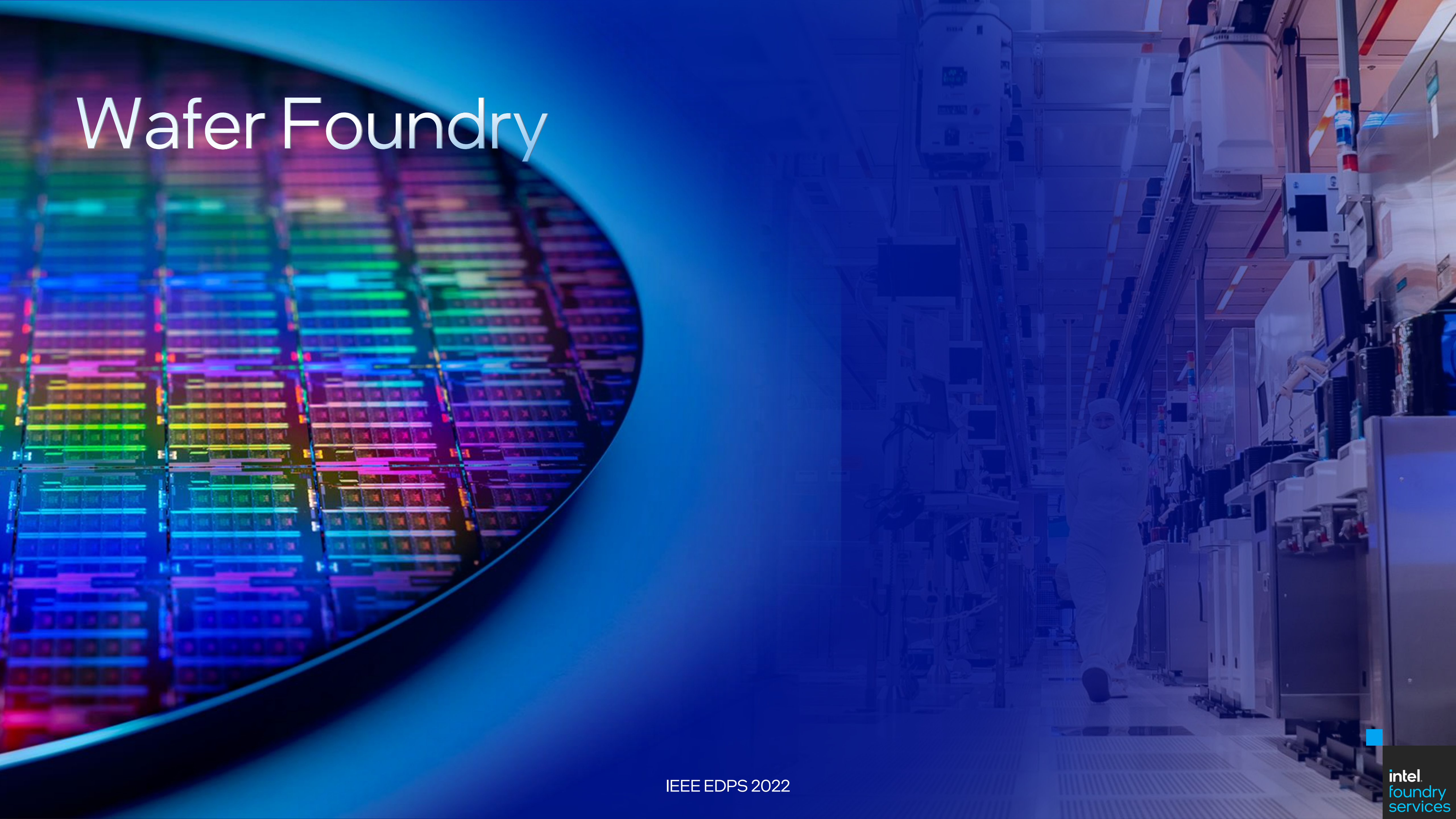
Wafer Foundry
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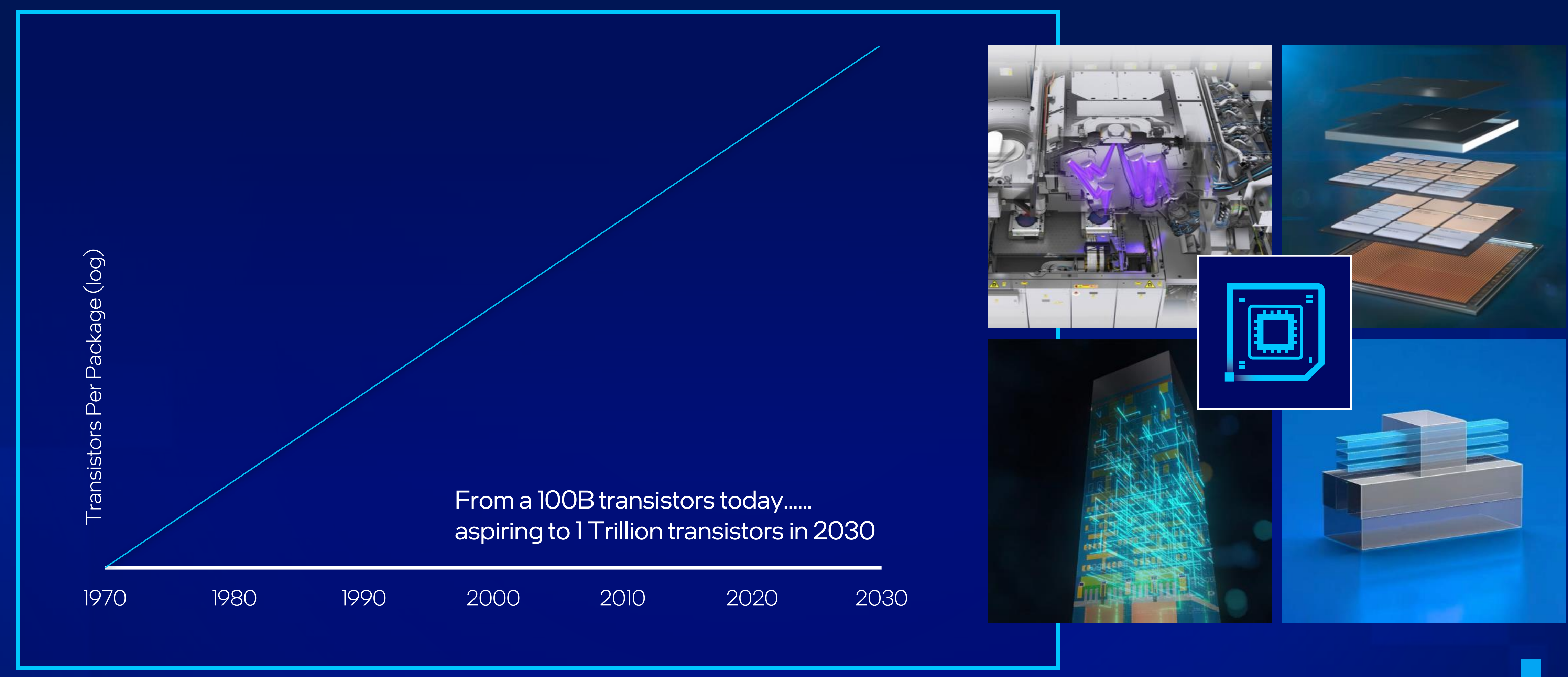
Moore's Law Alive and Well



Future projections based on products still in design. Future transistor counts are projections and are inherently uncertain

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We will not rest until the periodic table is exhausted

1 H Hydrogen 1.008																	2 He Helium 4.002602
3 Li Lithium 6.94	4 Be Beryllium 9.0121831											5 B Boron 10.81	6 C Carbon	7 N Nitrogen 14.007	8 O Oxygen 15.999	9 F Fluorine 18.998403163	10 Ne Neon 20.1797
11 Na Sodium 22.98976928	12 Mg Magnesium 24.305											13 Al Aluminium 26.9815385	14 Si Silicon 28.085	P Phosphorus 30.973761998	16 S Sulfur 32.06	17 Cl Chlorine 35.45	18 Ar Argon 39.948
19 K Potassium 39.0983	20 Ca Calcium 40.078	21 Sc Scandium 44.955908	22 Ti Titanium 47.867	23 V Vanadium 50.9415	24 Cr Chromium 51.9961	25 Mn Manganese 54.938044	26 Fe Iron 55.845	27 Co Cobalt 58.933194	28 Ni Nickel 58.6934	29 Cu Copper 63.546	30 Zn Zinc 65.38	31 Ga Gallium 69.723	Ge Germanium 72.630	As Arsenic 74.921595	34 Se Selenium 78.971	35 Br Bromine 79.904	36 Kr Krypton 83.798
37 Rb Rubidium 85.4678	38 Sr Strontium 87.62	39 Y Yttrium 88.90584	40 Zr Zirconium 91.224	41 Nb Niobium 92.90637	42 Mo Molybdenum 95.95	43 Tc Technetium (98)	44 Ru Ruthenium 101.07	45 Rh Rhodium 102.90550	46 Pd Palladium 106.42	47 Ag Silver 107.8682	48 Cd Cadmium 112.414	49 In Indium 114.818	50 Sn Tin 118.710	51 Sb Antimony 121.760	52 Te Tellurium 127.60	53 I Iodine 126.90447	54 Xe Xenon 131.293
55 Cs Caesium 132.90545196	56 Ba Barium 137.327	57 - 71 Lanthanoids	72 Hf Hafnium 178.49	73 Ta Tantalum 180.94788	74 W Tungsten 183.84	75 Re Rhenium 186.207	76 Os Osmium 190.23	77 Ir Iridium 192.217	78 Pt Platinum 195.084	79 Au Gold 196.966569	80 Hg Mercury 200.592	81 Tl Thallium 204.38	82 Pb Lead 207.2	83 Bi Bismuth 208.98040	84 Po Polonium (209)	85 At Astatine (210)	86 Rn Radon (222)
87 Fr Francium (223)	88 Ra Radium (226)	89 - 103 Actinoids	104 Rf Rutherfordium (267)	105 Db Dubnium (268)	106 Sg Seaborgium (269)	107 Bh Bohrium (270)	108 Hs Hassium (269)	109 Mt Meitnerium (278)	110 Ds Darmstadtium (281)	111 Rg Roentgenium (282)	112 Cn Copernicium (285)	113 Nh Nihonium (286)	114 Fl Flerovium (289)	115 Mc Moscovium (289)	116 Lv Livermorium (293)	117 Ts Tennessine (294)	118 Og Oganesson (294)

57 La Lanthanum 138.90547	58 Ce Cerium 140.116	59 Pr Praseodymium 140.90766	60 Nd Neodymium 144.242	61 Pm Promethium (145)	62 Sm Samarium 150.36	63 Eu Europium 151.964	64 Gd Gadolinium 157.25	65 Tb Terbium 158.92535	66 Dy Dysprosium 162.500	67 Ho Holmium 164.93033	68 Er Erbium 167.259	69 Tm Thulium 168.93422	70 Yb Ytterbium 173.045	71 Lu Lutetium 174.9668
89 Ac Actinium (227)	90 Th Thorium 232.0377	91 Pa Protactinium 231.03588	92 U Uranium 238.02891	93 Np Neptunium (237)	94 Pu Plutonium (244)	95 Am Americium (243)	96 Cm Curium (247)	97 Bk Berkelium (247)	98 Cf Californium (251)	99 Es Einsteinium (252)	100 Fm Fermium (257)	101 Md Mendelevium (258)	102 No Nobelium (259)	103 Lr Lawrencium (266)

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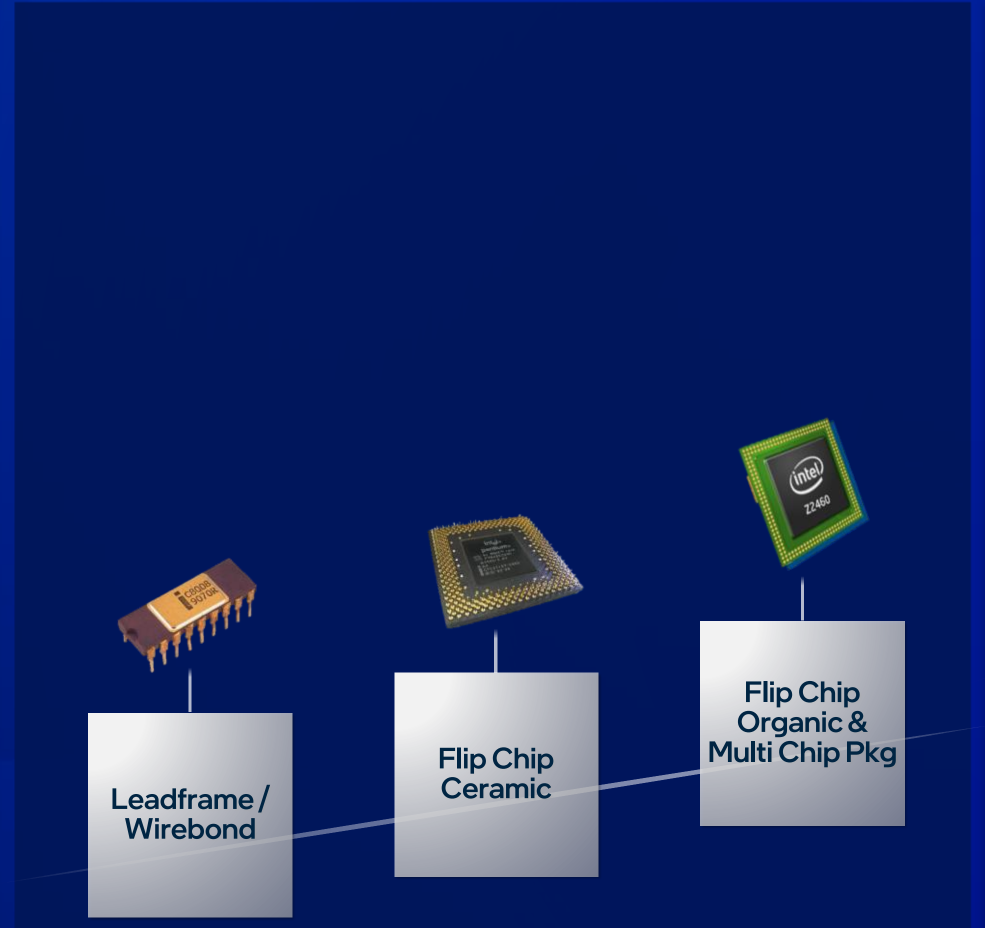
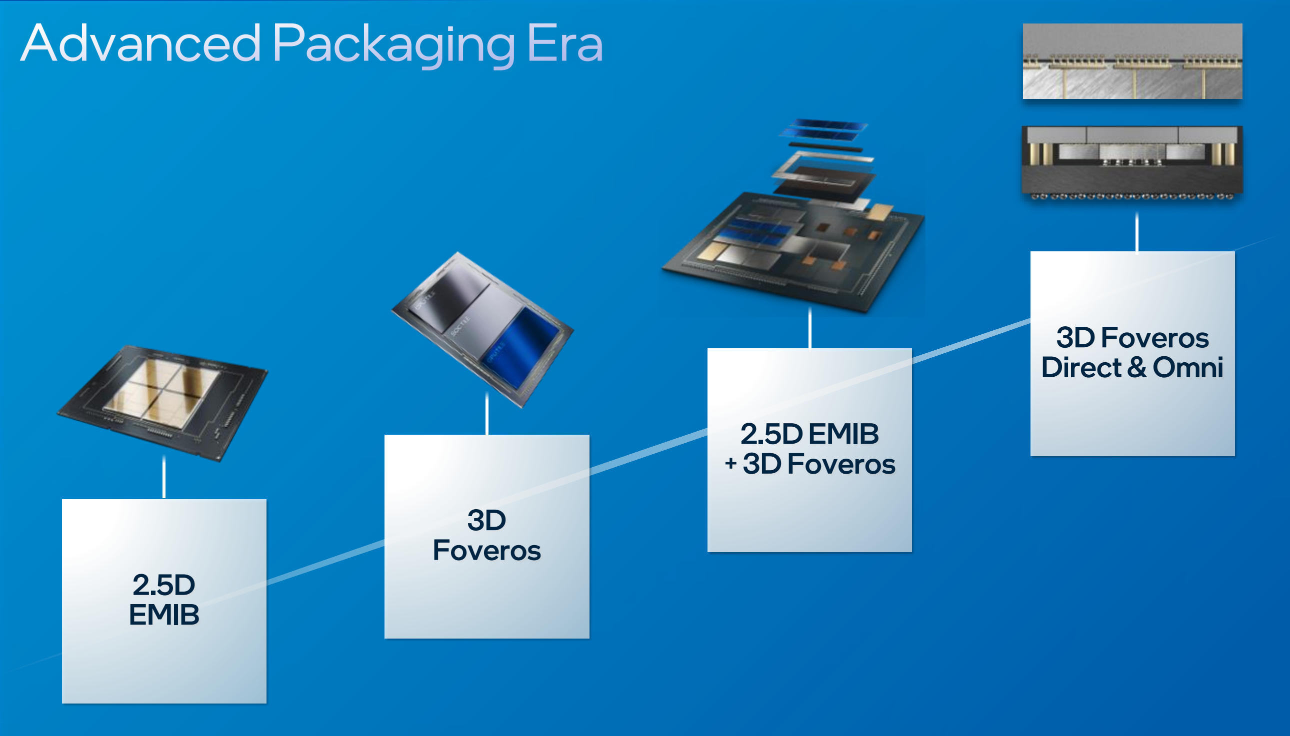
Intel Package Technology





Package main function: provide power and signaling from motherboard to die

Added Package value: high density interconnects that enable larger die complexes from multiple process nodes

*Graphic is for illustrative purposes only and is not to scale

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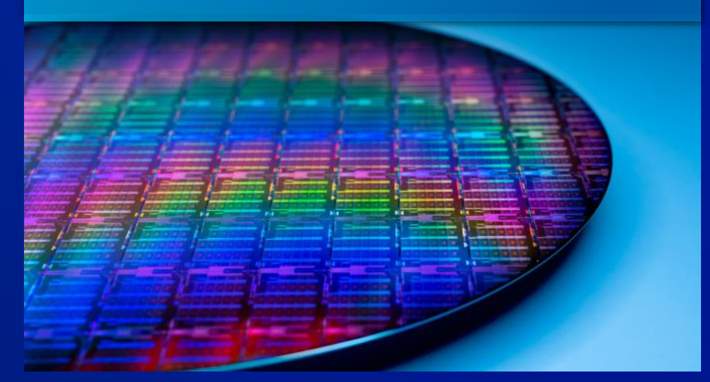
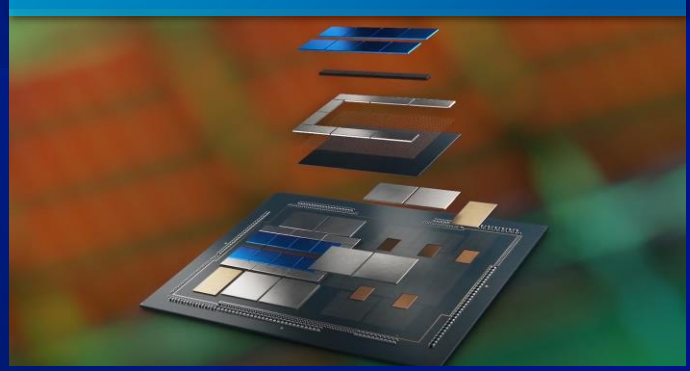
Systems Foundry

Wafers



Packaging

Chiplets



Software

IFS as an Open System Foundry

Secure Solution

System Software	x86, arm, RISC-V, oneAPI; Open SW Stack: Operating System, Virtualization, BIOS, Firmware, Tools & Compilers; Intel® Simics®
System of Chips	System Partitioning; Intel® Chiplet Studio™ Suite
Accelerated Silicon Services	Architecture; Intel® Docea™ Thermals; Intel® Cofluent™ Performance; Security – Manageability - Test/Debug (Differentiated IP); ASIC; Validation
Package & Interconnect Optimization	UCIe Universal Chiplet Interconnect Express; EMIB; Foveros
Silicon	Intel 16; Intel 3; Intel 18A

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Industry Vision

Moore's Predicted "Day of Reckoning"

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1]."

-Gordon E. Moore

Image: Intel®

[1]: "**Cramming more components onto integrated circuits**", Electronics, Volume 38, Number 8, April 19, 1965

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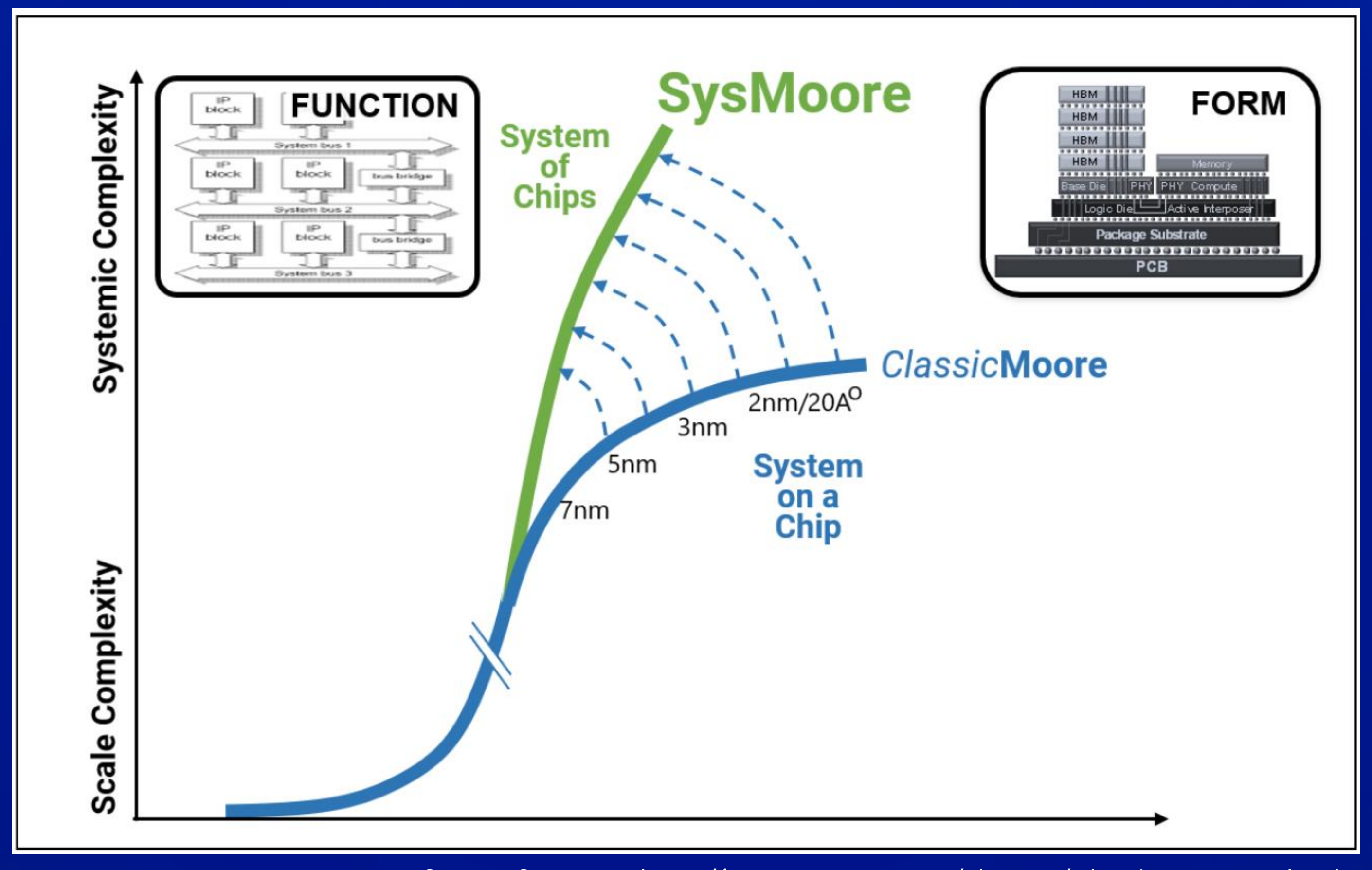
System on Chip -> System of Chips

"Catalyzing the Impossible: Silicon, Software, and Smarts for the SysMoore Era" – Dr. Aart de Geus



Source: Synopsys, https://www.synopsys.com/glossary/what-is-sysmoore.html

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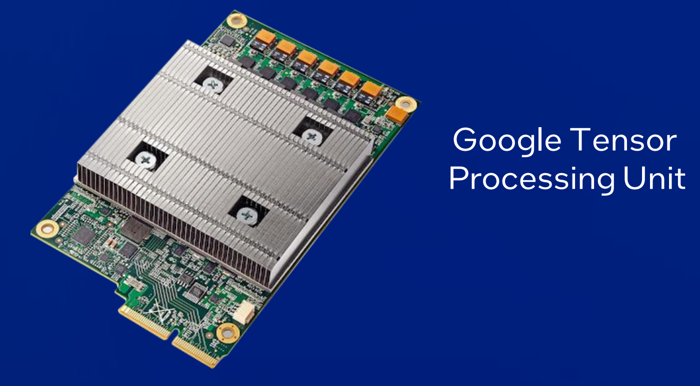
Google Cloud Blog*: A Chiplet Innovation Ecosystem for a New Era of Custom Silicon

Growing Demand for AI



Google Tensor Processing Unit

Growing Demand for Video

(YouTube, Live Streaming)

Google Video Coding Unit

Image credit: Google

What's needed:

- Modularity
- Optimized Silicon and Package
- Open Standards, examples:
  - IO
  - Protocols
  - Security
  - Management

*https://cloud.google.com/blog/topics/systems/open-chiplet-ecosystem-powering-next-era-of-custom-silicon

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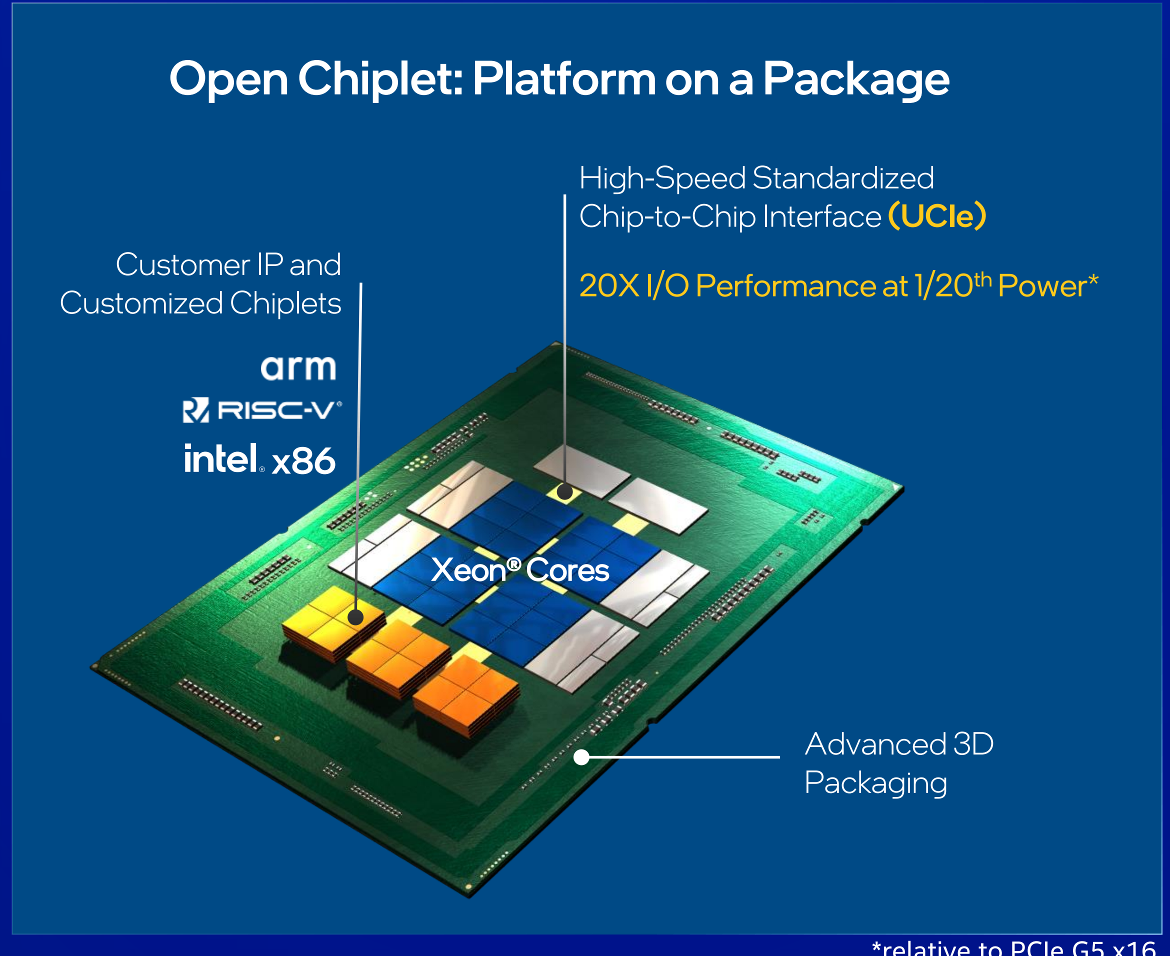
Intel® Vision : The "Chiplet Revolution"



*relative to PCIe G5 x16

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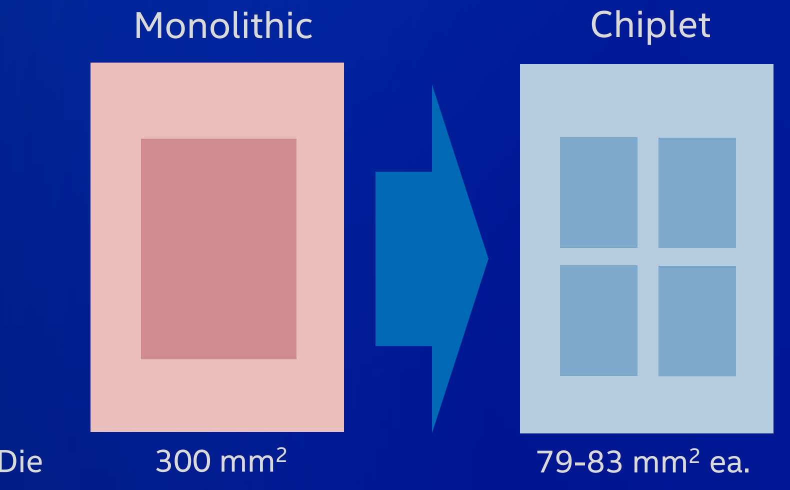
Industry Inflection Points

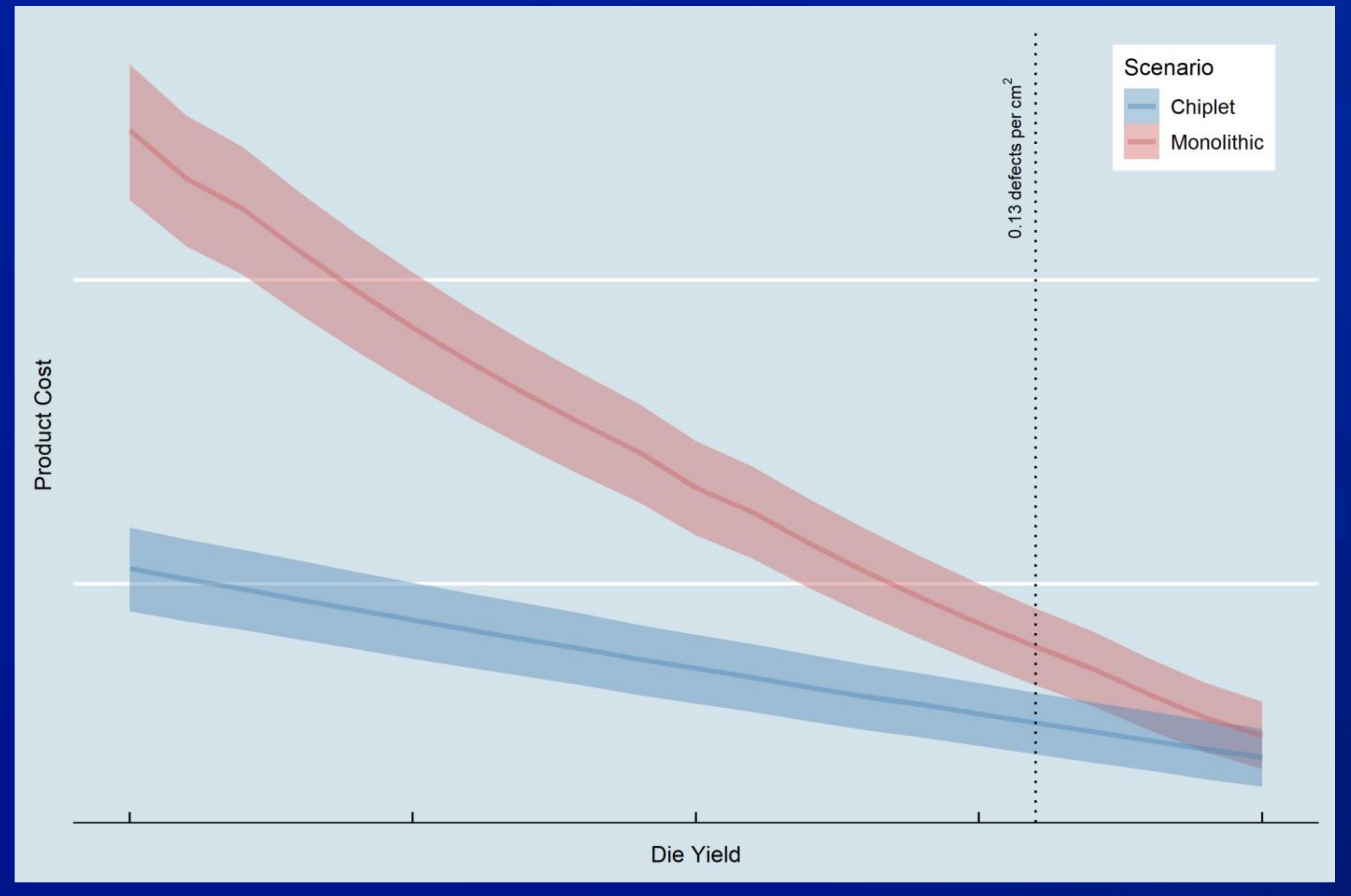
Motivation : Cost & Manufacturing Optimization



Die 300 mm² 79-83 mm² ea.

Input Variables:

- Die Area
- # of Chiplets
- Wafer Cost
- Defect Density
- Package/Assembly/Test
- Known Good Die
- Die Area Tax & Overhead



*Probabilistic trend by 1std dev

Source: Intel® Model

Reference: https://ieeexplore.ieee.org/document/9758914
"Heterogeneous Integration of Chiplets: Cost and Yield Tradeoff Analysis"

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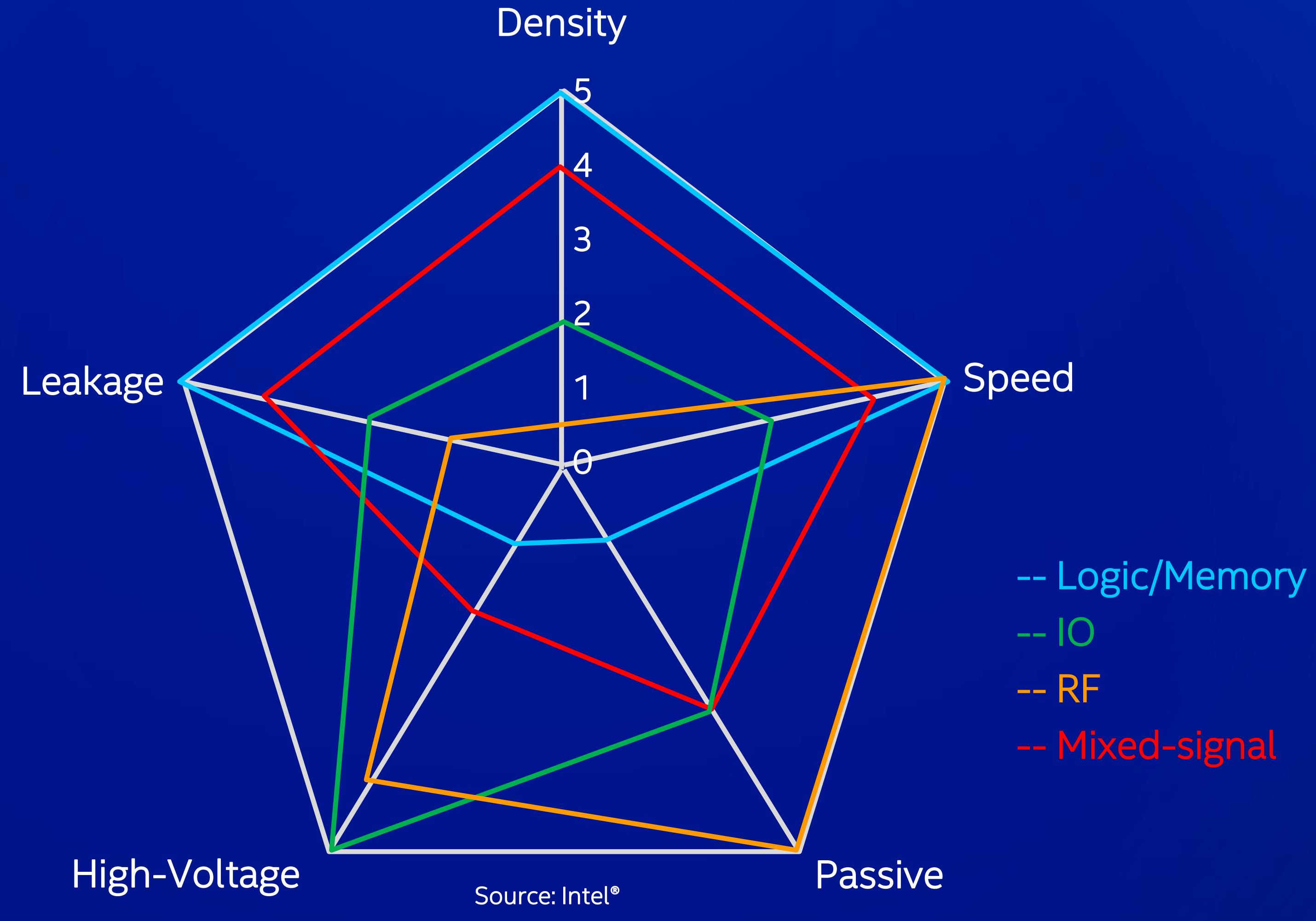
Motivation : Process Technology Optimization



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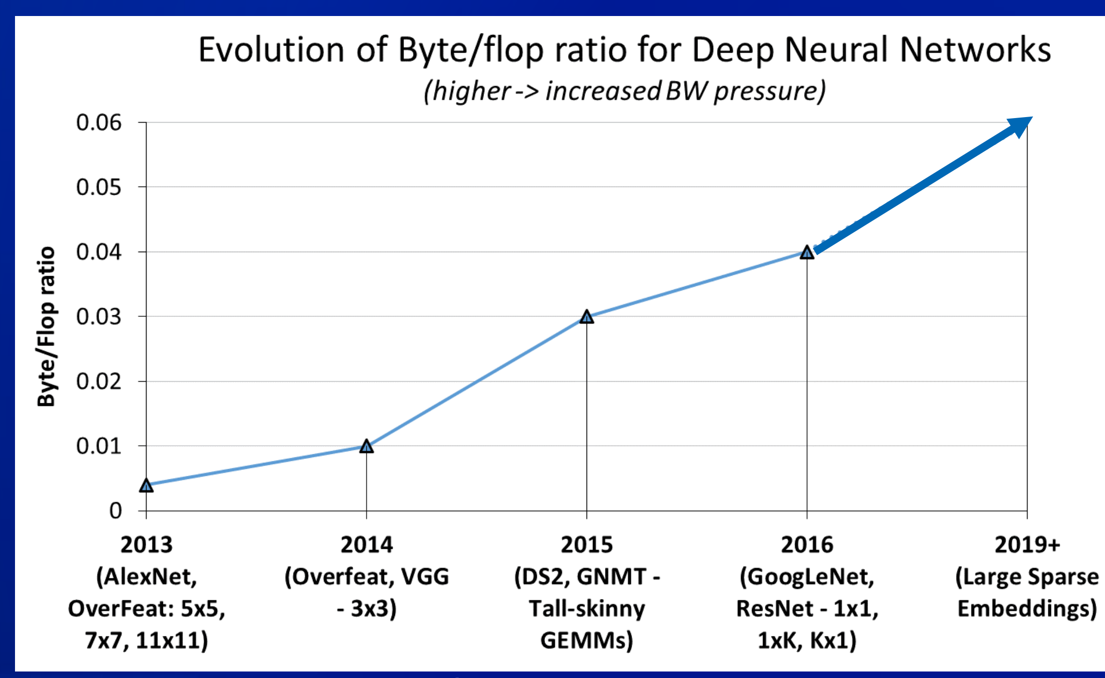
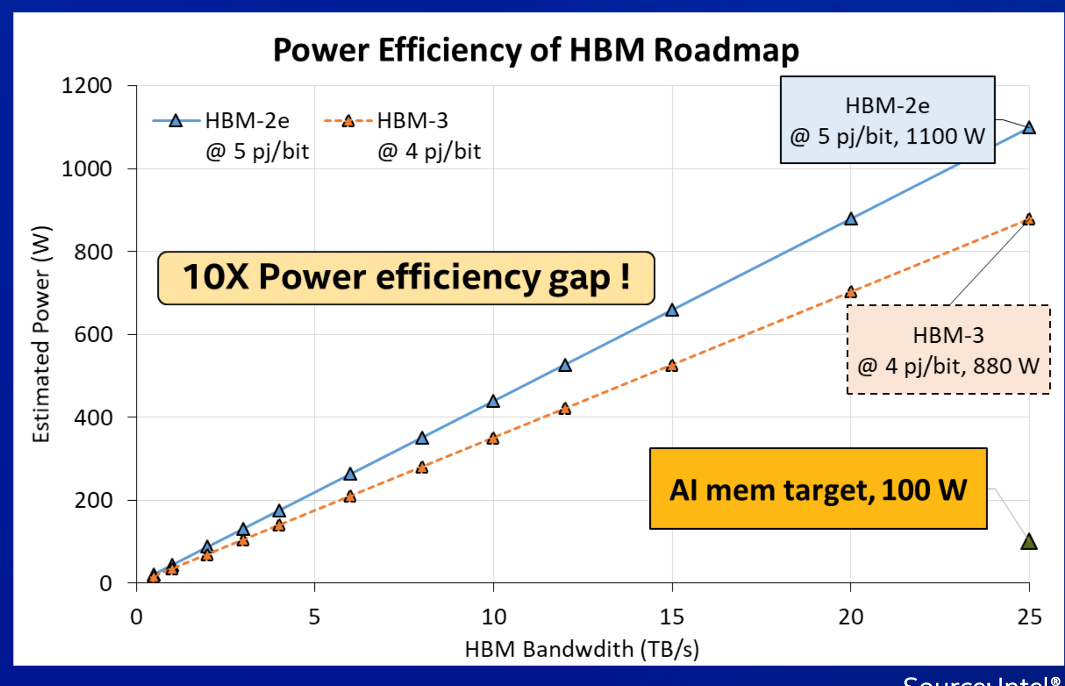
Motivation : AI Memory BW/Power Gap



2020 AI Compute ~ 400 Tops
0.06 B/F → 25 TB/s

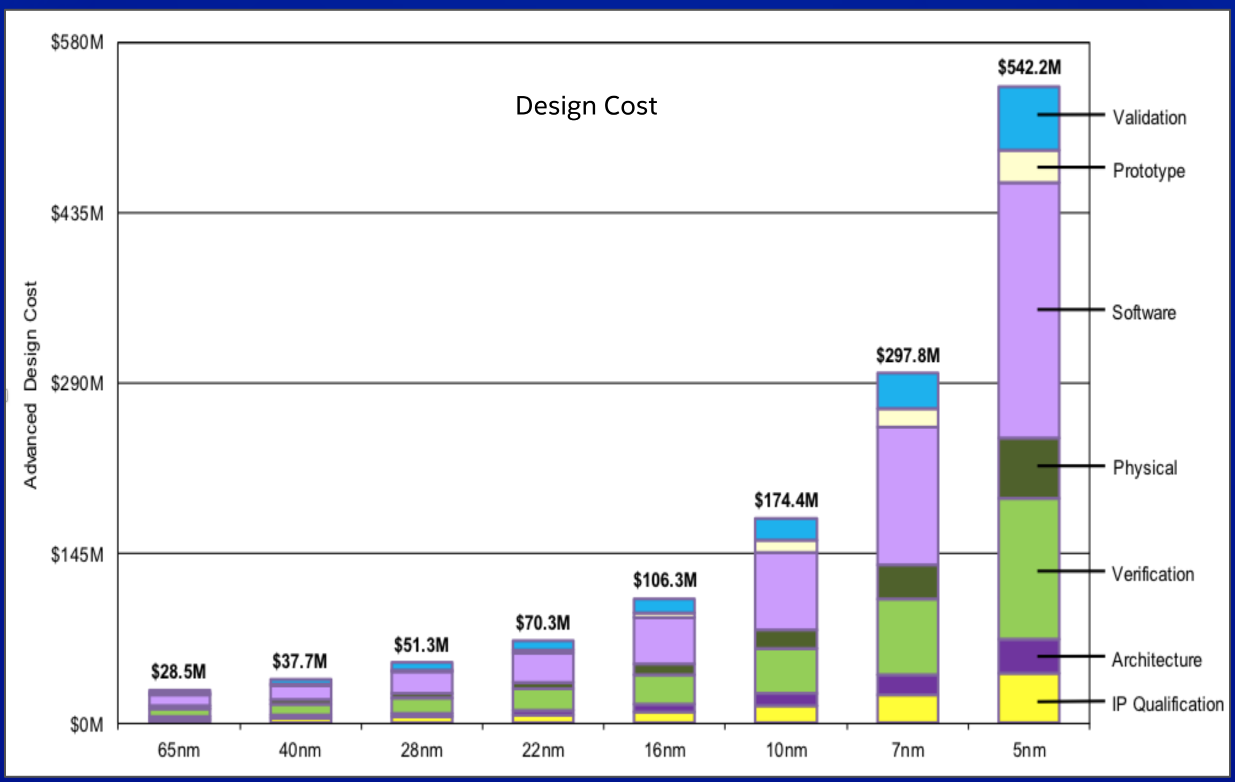
Source: Intel®



Source: Intel®

- ☐ Insatiable Memory Bandwidth
- ☐ The energy efficiency gap is getting bigger

Motivation: R&D Cost and Product Velocity



Source: Lapadeus, M., "Big Trouble At 3nm", Semiconductor Engineering, June 21, 2018
cited in IEEE Heterogeneous Integration Roadmap
https://eps.ieee.org/images/files/HIR_2020/ch02_hpc_1.pdf

Move from Exponential -> Linear with modularity and reuse

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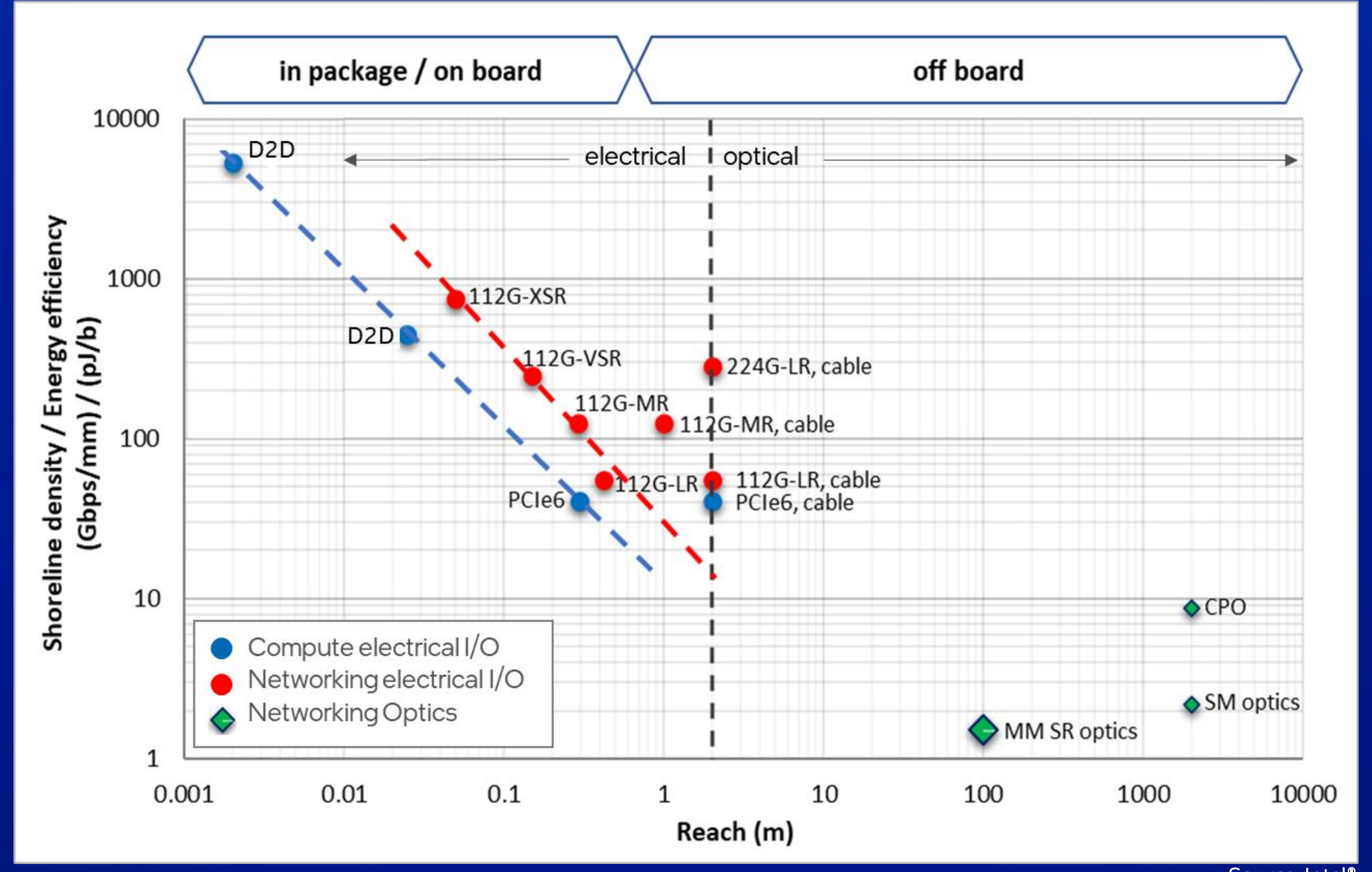
Motivation: Optimize System Level High Speed IO



Source: Intel®

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Technology Needed

Some EDA Challenges

New Development Model : System on Chip -> System of Chips

Platform & SW/HW Co-Design

Architecture Perf. Modeling

RTL Design & Verification

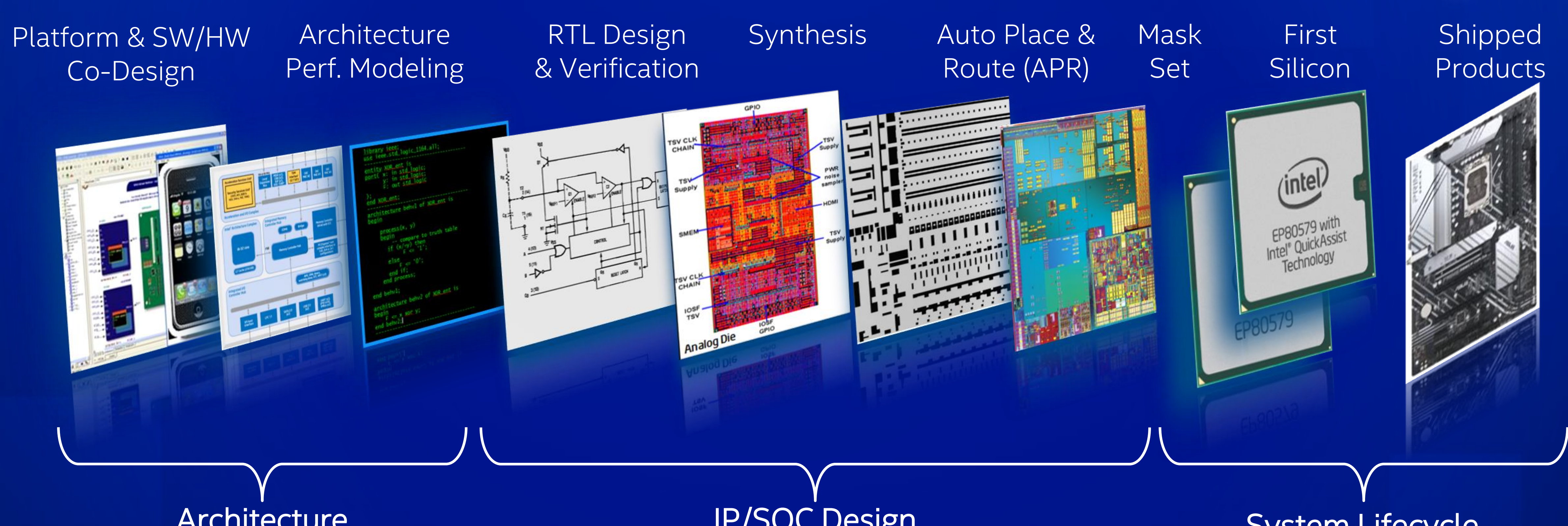
Synthesis

Auto Place & Route (APR)

Mask Set

First Silicon

Shipped Products



Architecture

IP/SOC Design

System Lifecycle Management

Post-Si & Test

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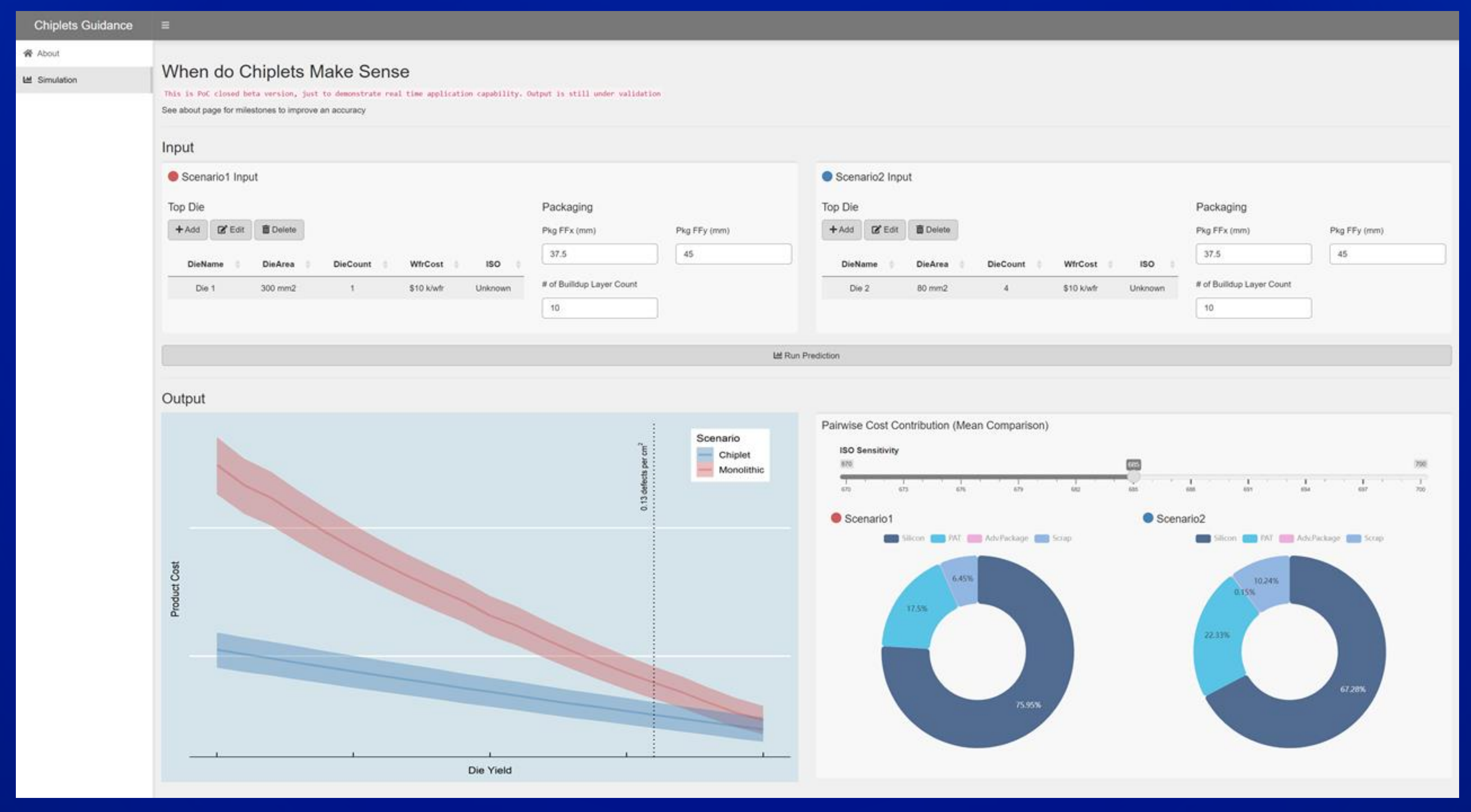
Architecture: Optimal Silicon Partitioning

Comparative/pairwise analysis for any homogeneous or heterogeneous implementations



Source: Intel® Model

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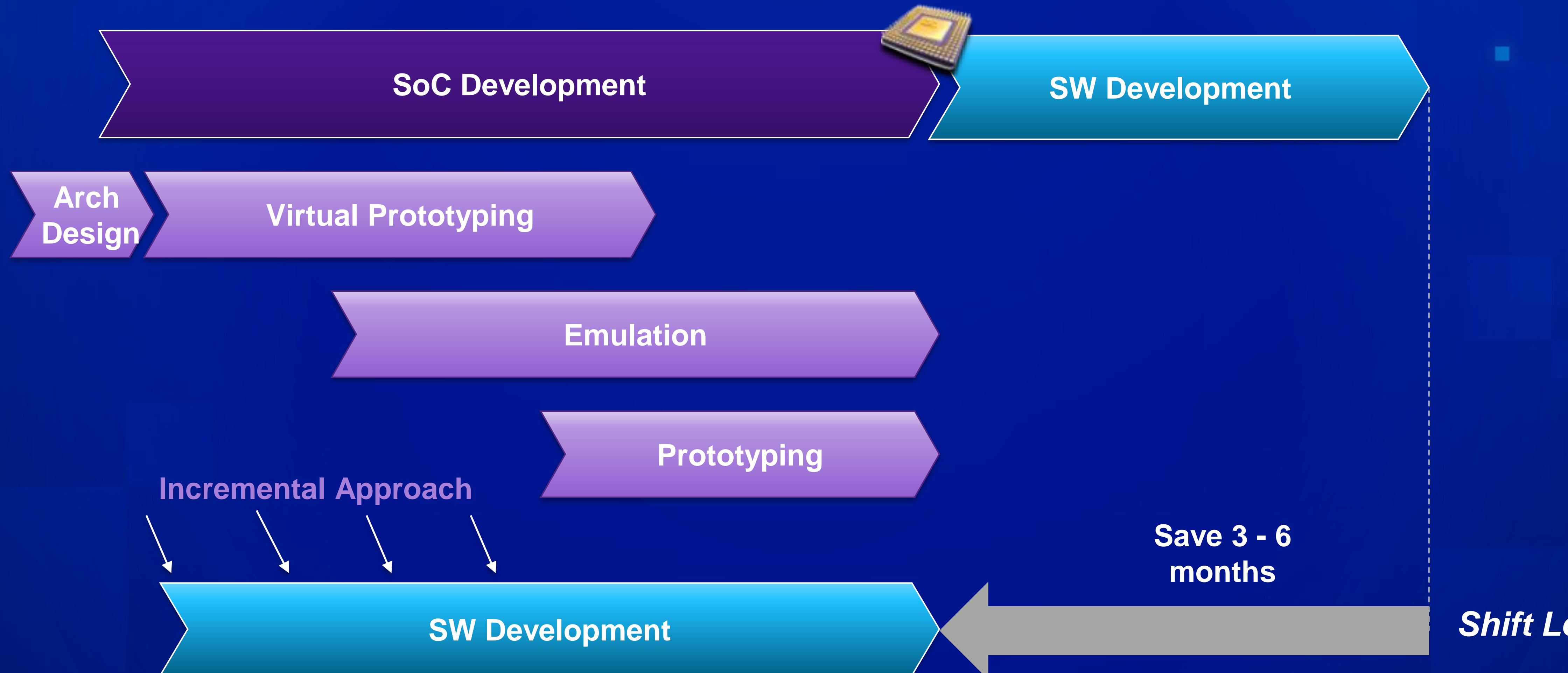
Shifting Left with SW/HW Co-Design



Credit: Synopsys

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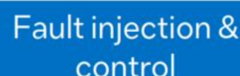
Shifting Left with SW/HW Co-Design

Ex. Intel® Simics® Virtual Platforms

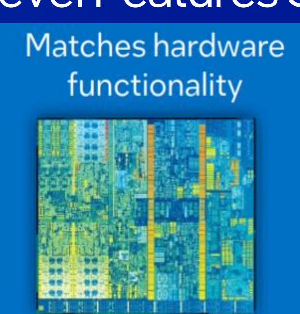
System Level Features Support

Scripting

```
con0.wait-for-string "$"
con0.record-start
con0.input "./ptest.elf 5\n"
con0.wait-for-string "."
$r = con0.record-stop
if ($r == "fail.") {
   echo "test failed"
}
```



Matches hardware functionality



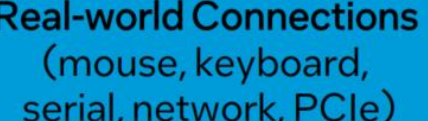
Real-world connections

Fault injection & control

Multicore & -machine multithreading

Modular & user-extensible

Integration of 3rd party entities



Real-world Connections (mouse, keyboard, serial, network, PCIe)

External SW Tools (Intel System Debugger, GDB, WinDBG, Lauterbach, …)

Simics®

Other Simulators (VCS, Cadence, Synopsys, Matlab, C, …)

RTL Emulation / FPGA (Synopsys HAPS & ZeBu, Intel® systems, …)

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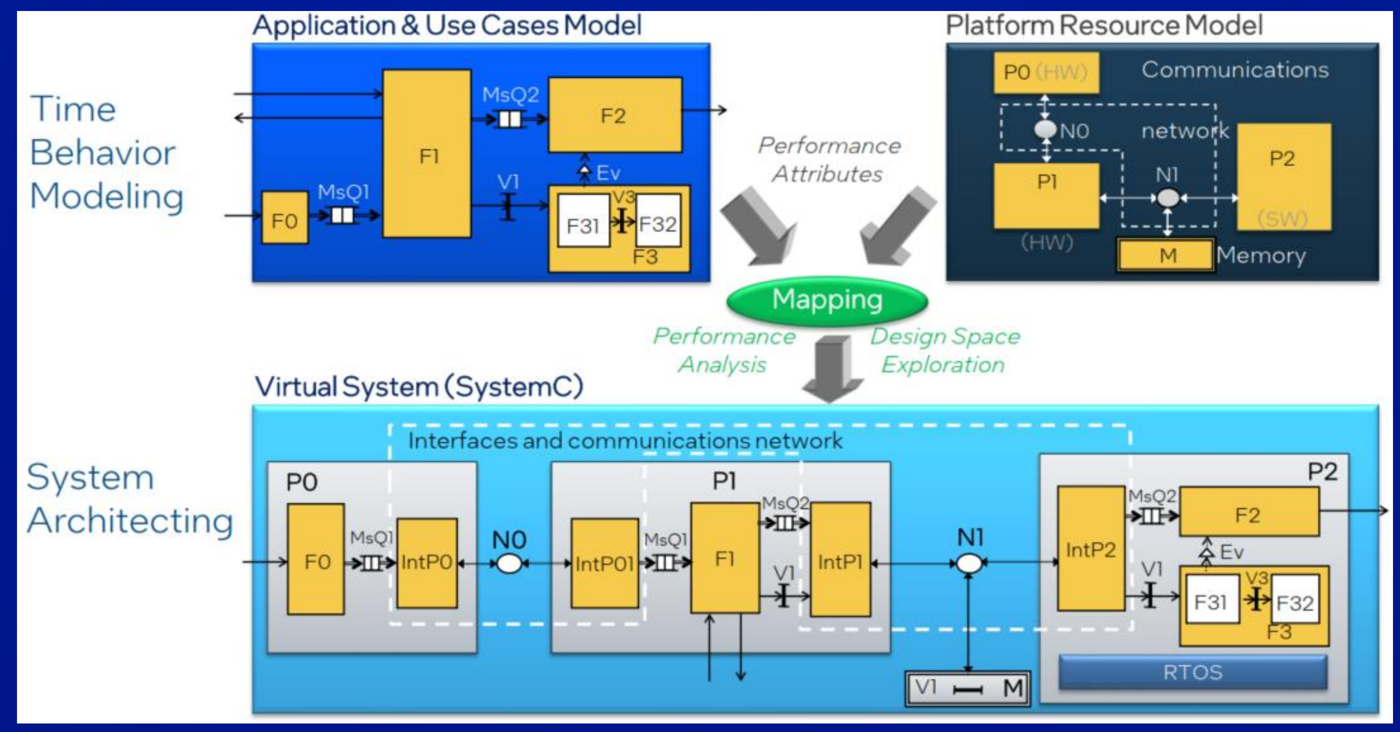
Architecture: System of Chips Performance Modeling

Ex. Intel® CoFluent™ Technology

Execute real SW workloads



Shape Micro-architectural details

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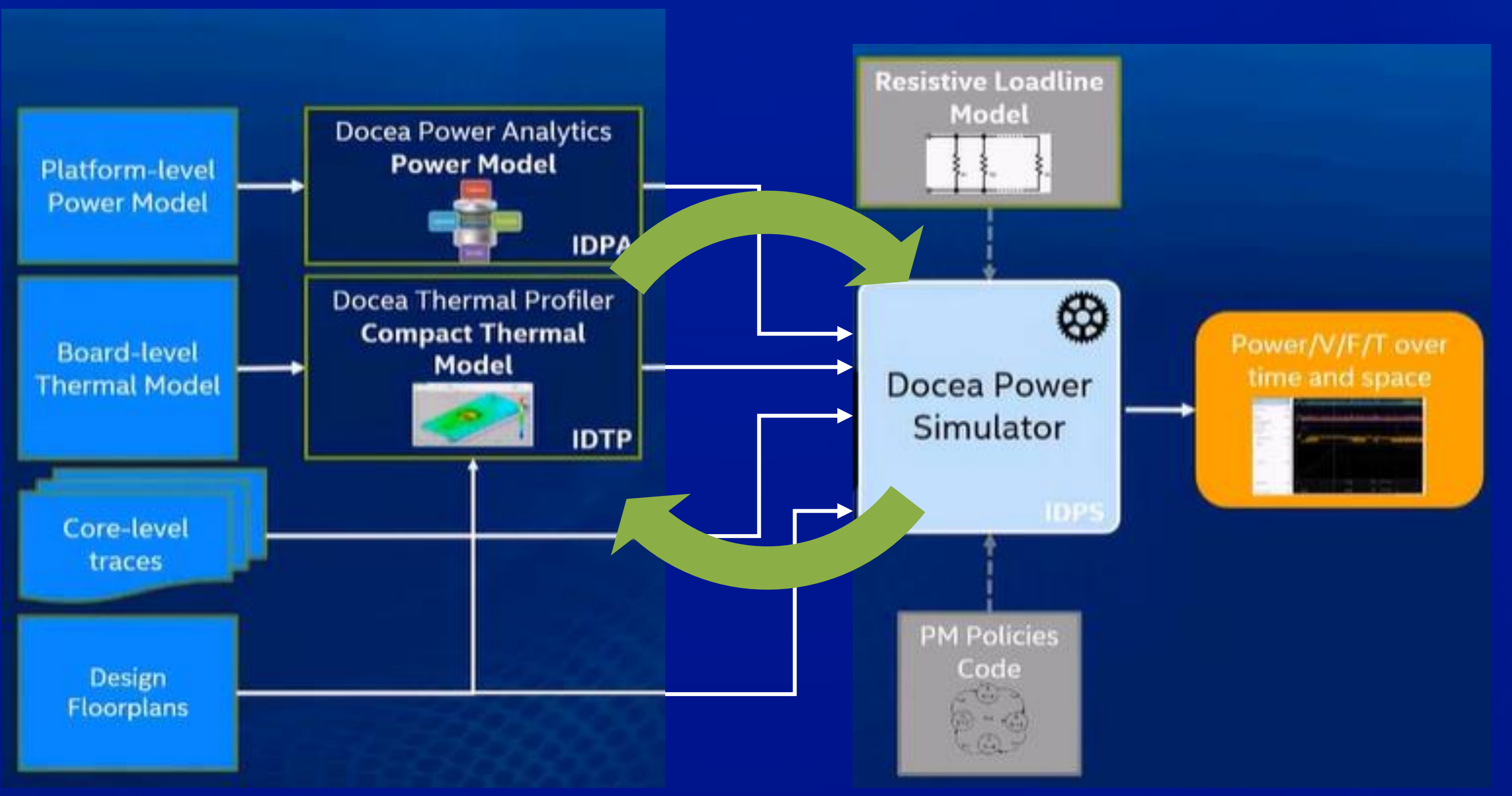
Architecture: System Power & Thermal Optimization

Ex. Intel® Docea™ – System Thermal Analysis -> Quick Iteration (Arch, Design, Power, Thermal)



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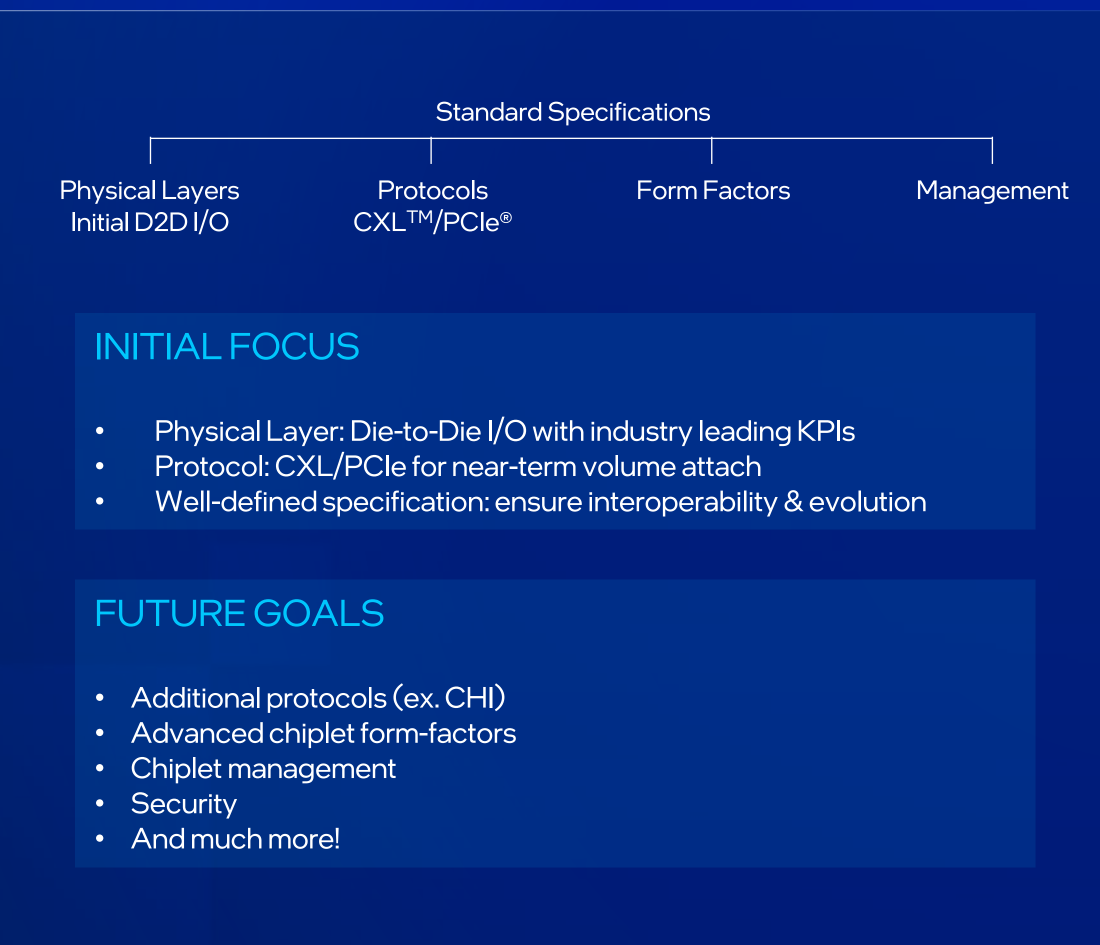
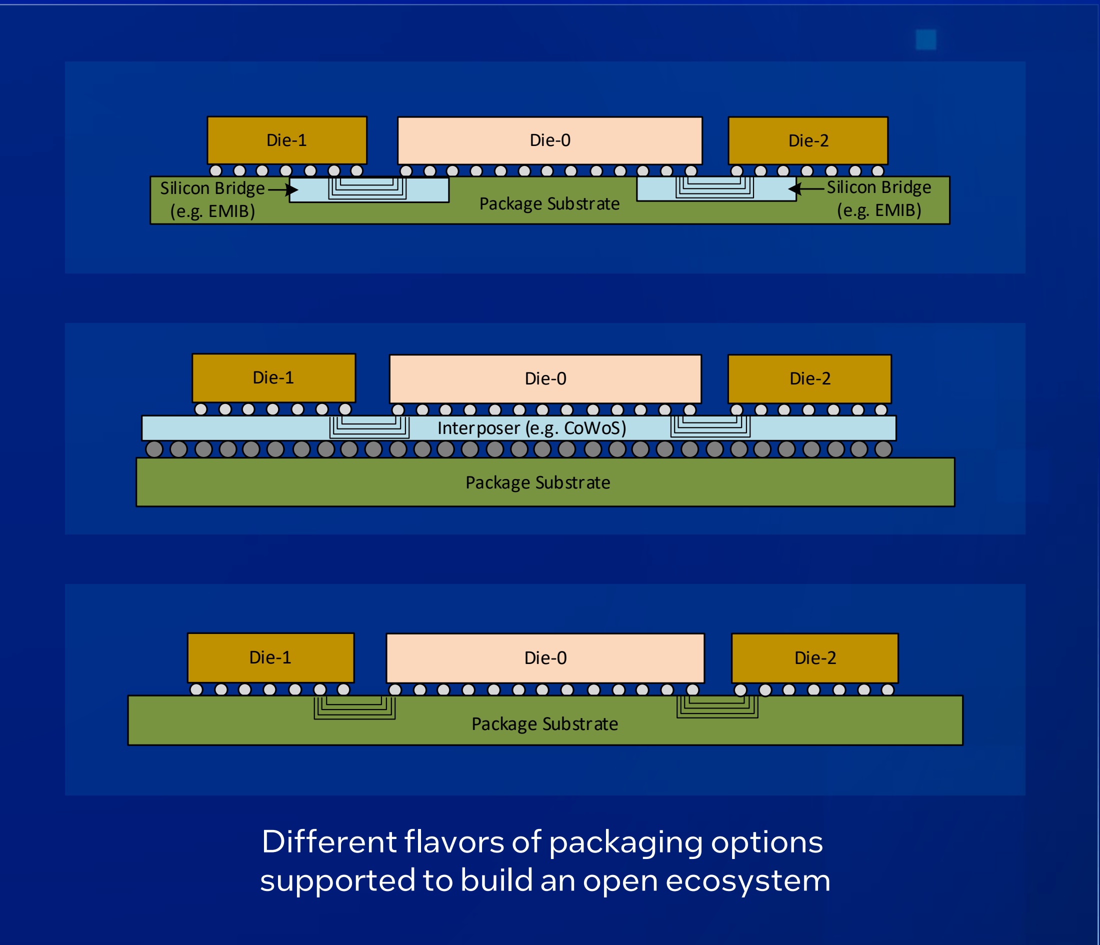
Design: Standardized IP : HIP and SIP

Ex. UCIe Open Interconnect





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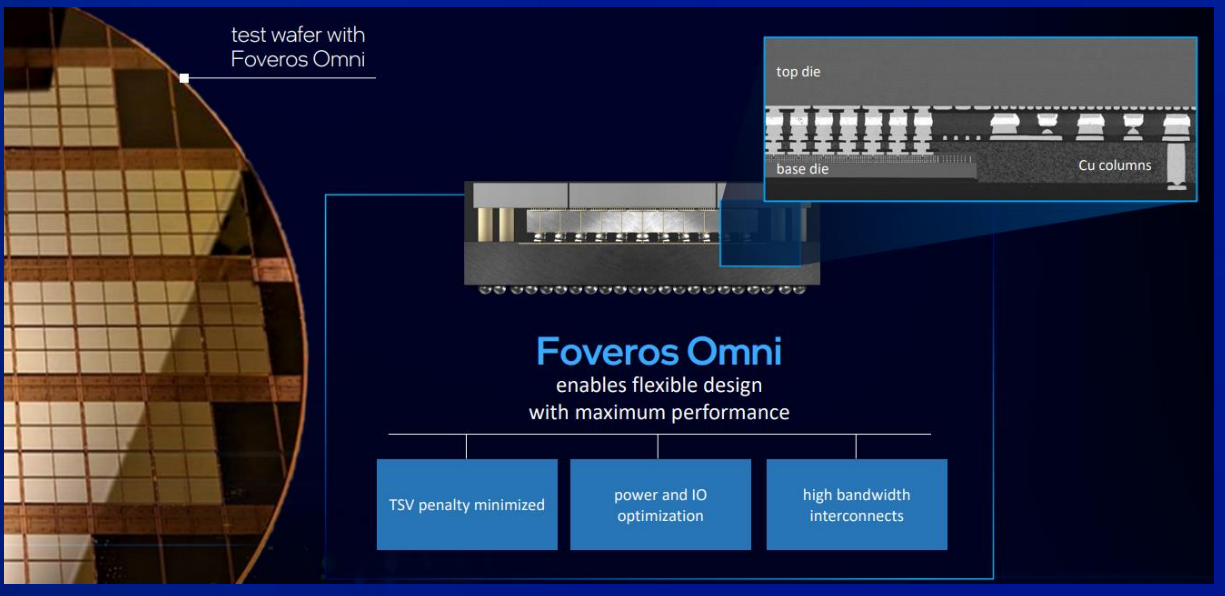
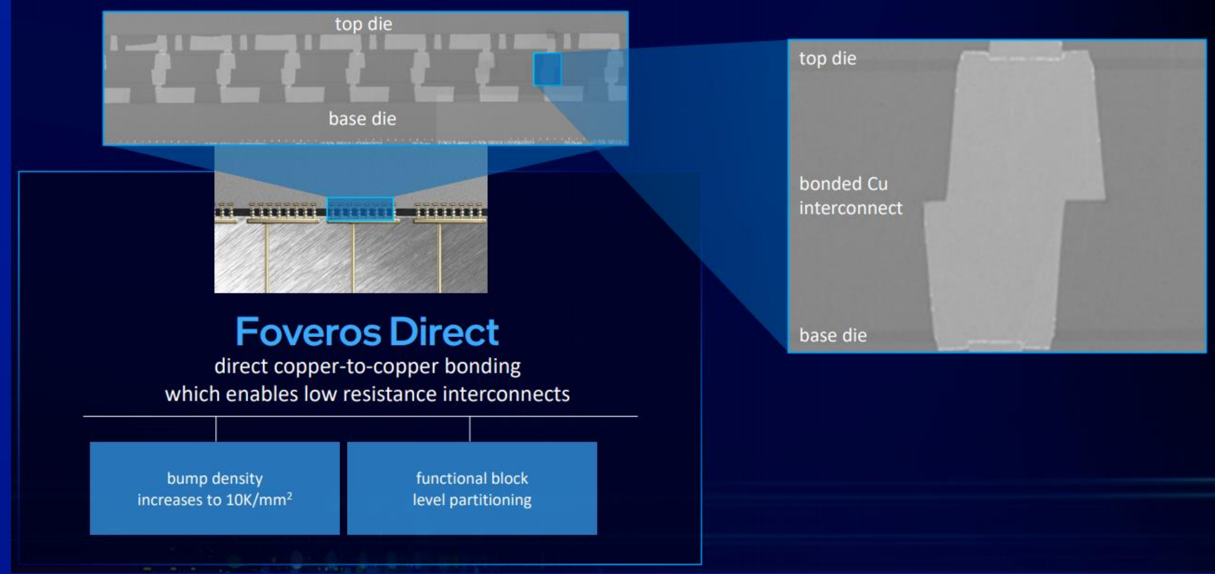
Design: DTCO & STCO Silicon + Package

PPAC Silicon Optimization, Package-Silicon Optimization





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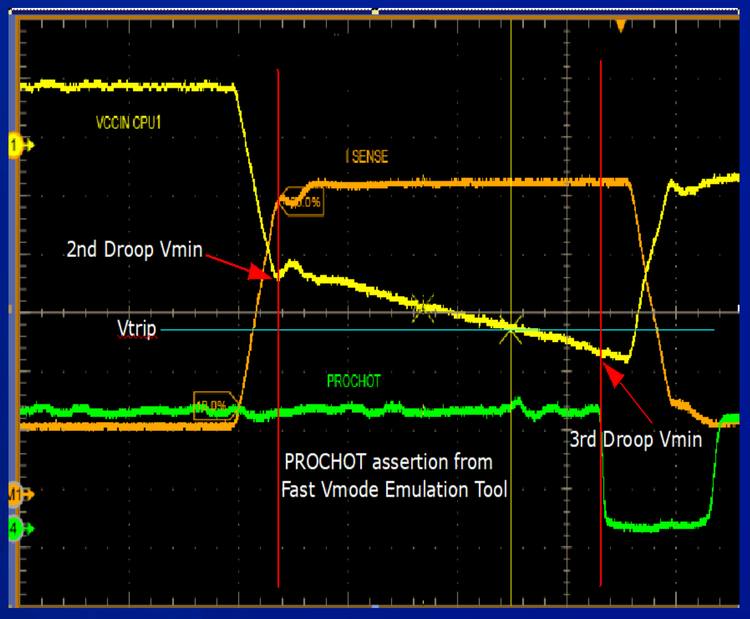
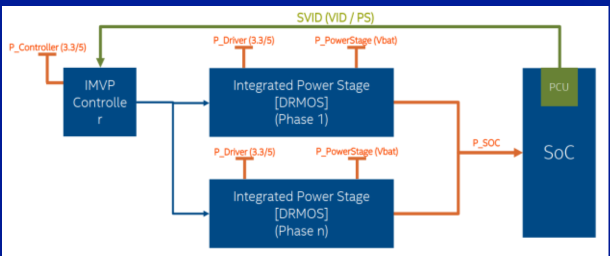
Design: Power Delivery

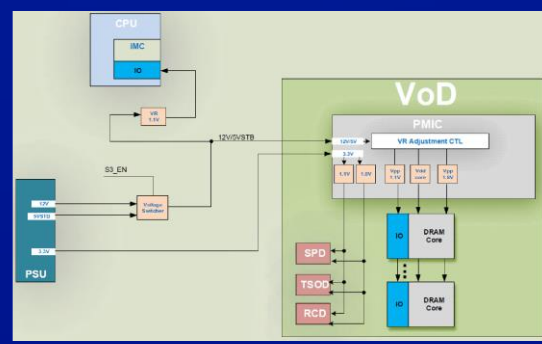
Power to the Platform – clean & efficient



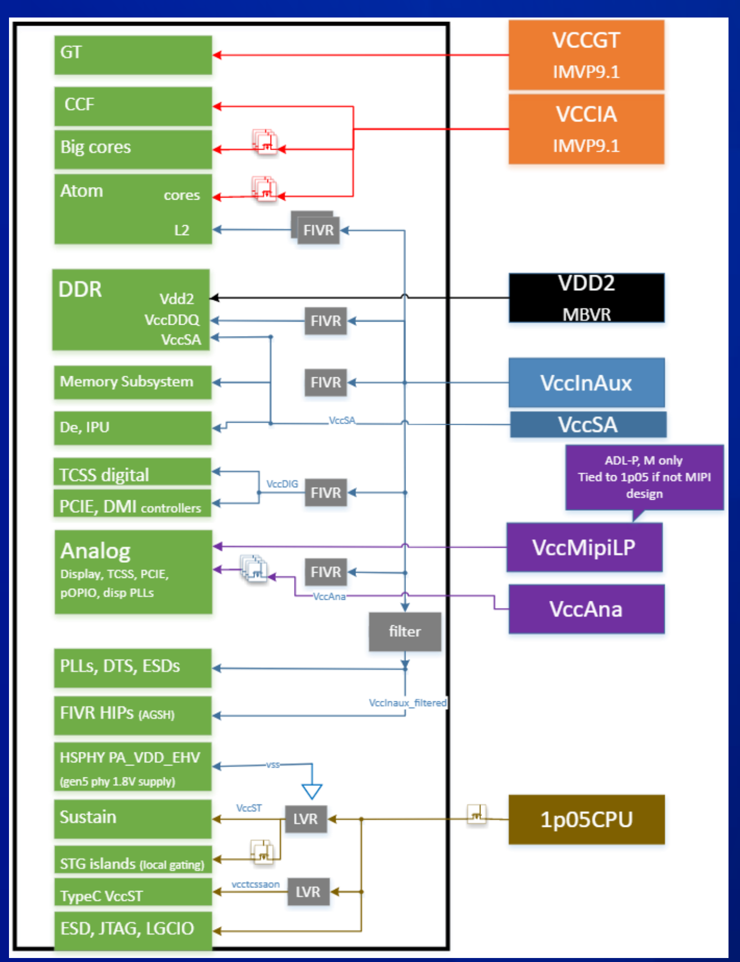
Distributed Power Delivery Droop



Optimize Voltage Regulators



Distribute Power Delivery



Optimized
Power Management IC (PMIC)

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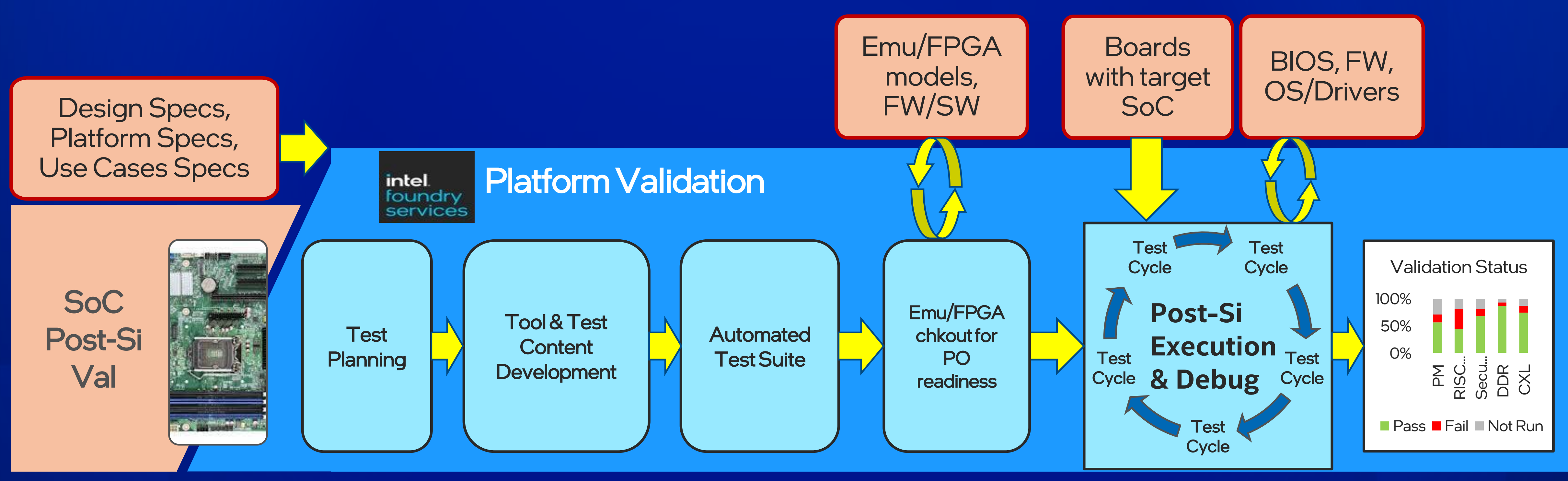
Post-Si: Platform Validation and Debug

New Post Silicon Multi-Die Tools/Flows/Methods, new Design for Debug Architecture



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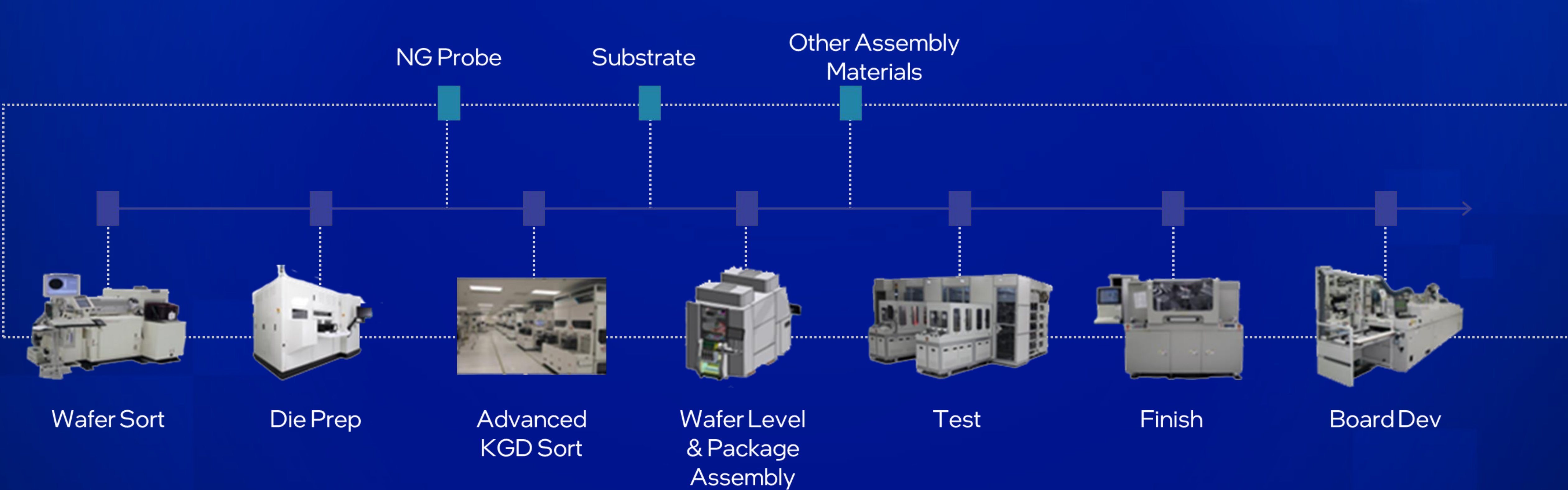
Post-Si: Manufacturing and Test

New Test Architecture & Capabilities : Known Good Die-> Known Good Multi-Die



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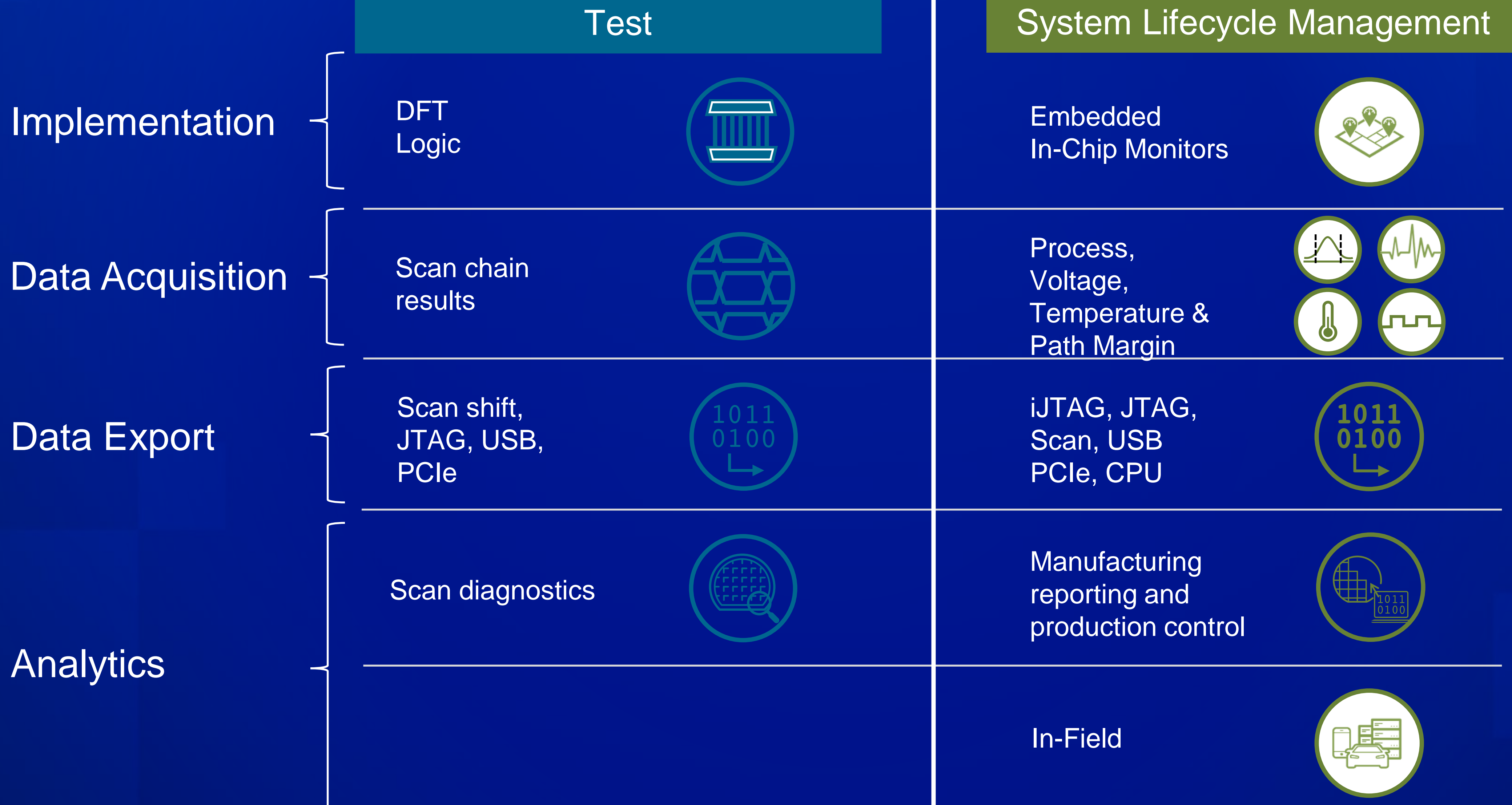
Test & Life Cycle Management



Credit: Synopsys

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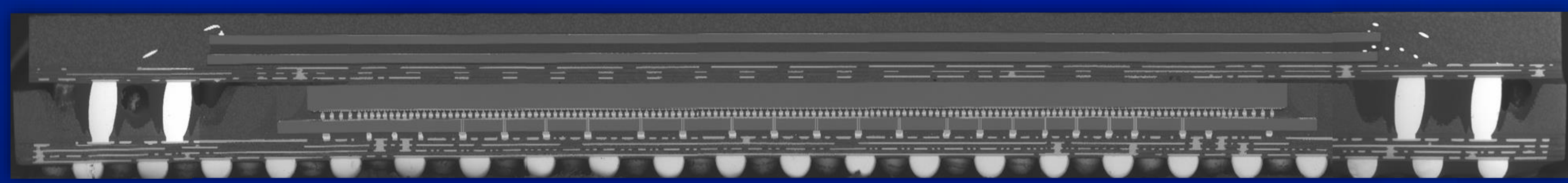
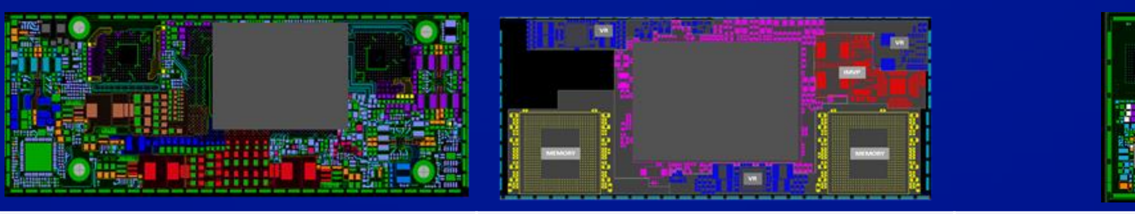
Chiplets

Industry Case Studies & Representative Applications

Case Study: Intel® Client, Lakefield 3D Foveros

Ex. Market Segmentation (GFX, Memory), Process Optimization

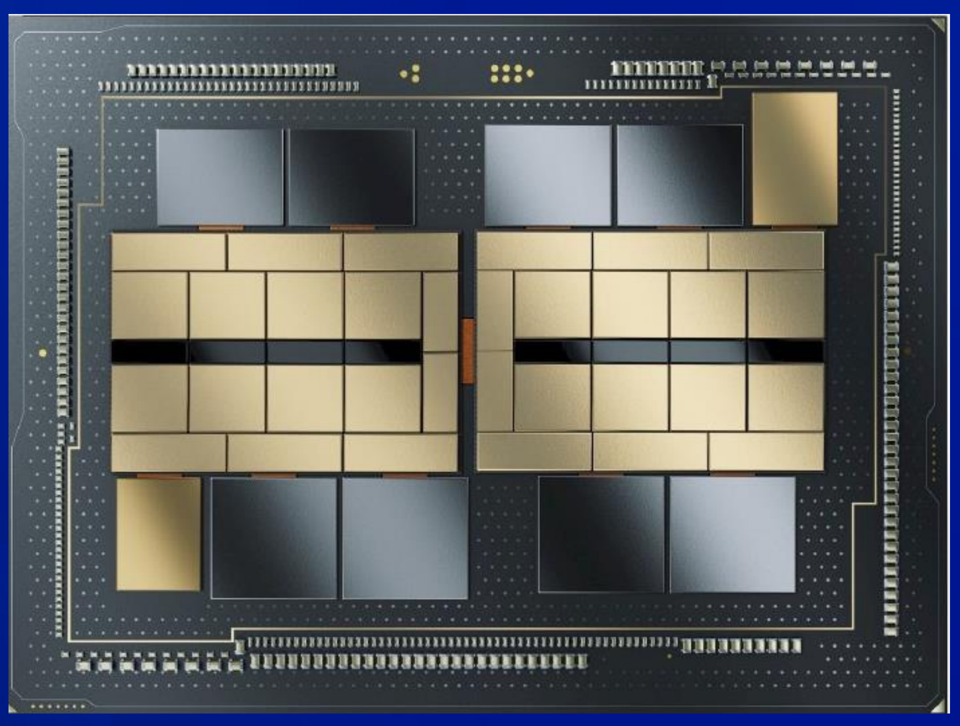


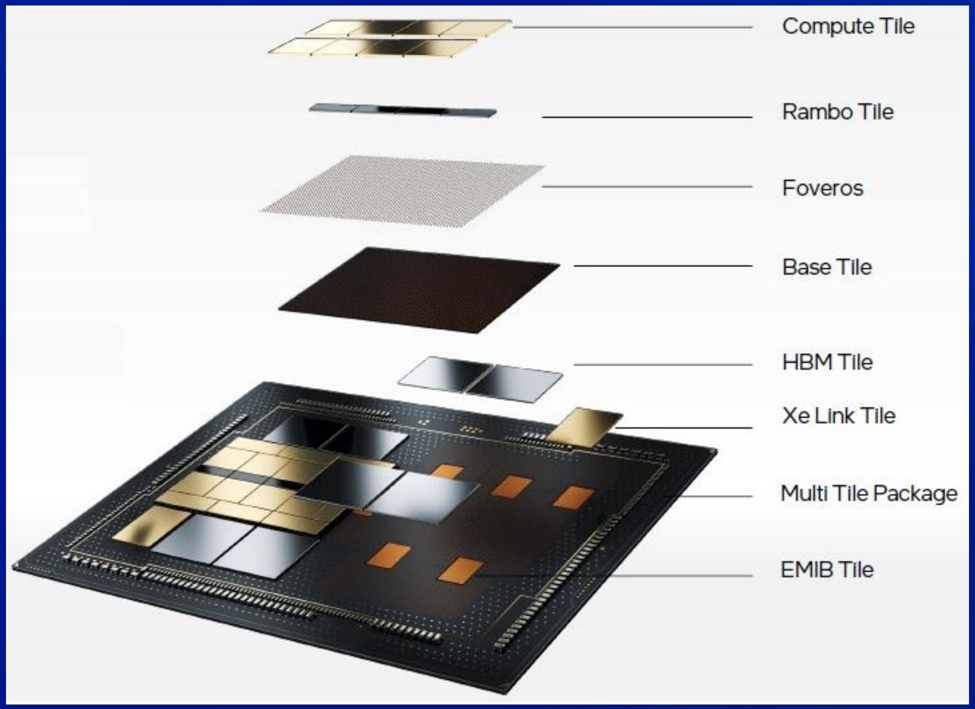


	Y SKU Gen-1	Y SKU	LKF
Package	20.5x16.5	26.5x18.5	12x12
Memory	LP3 11x11.5	LP4-4x 12.5x12.5	LP4-4x POP

Case Study : Intel® HPC - Ponte Vecchio

Ex. Complexity Management, Process Optimization





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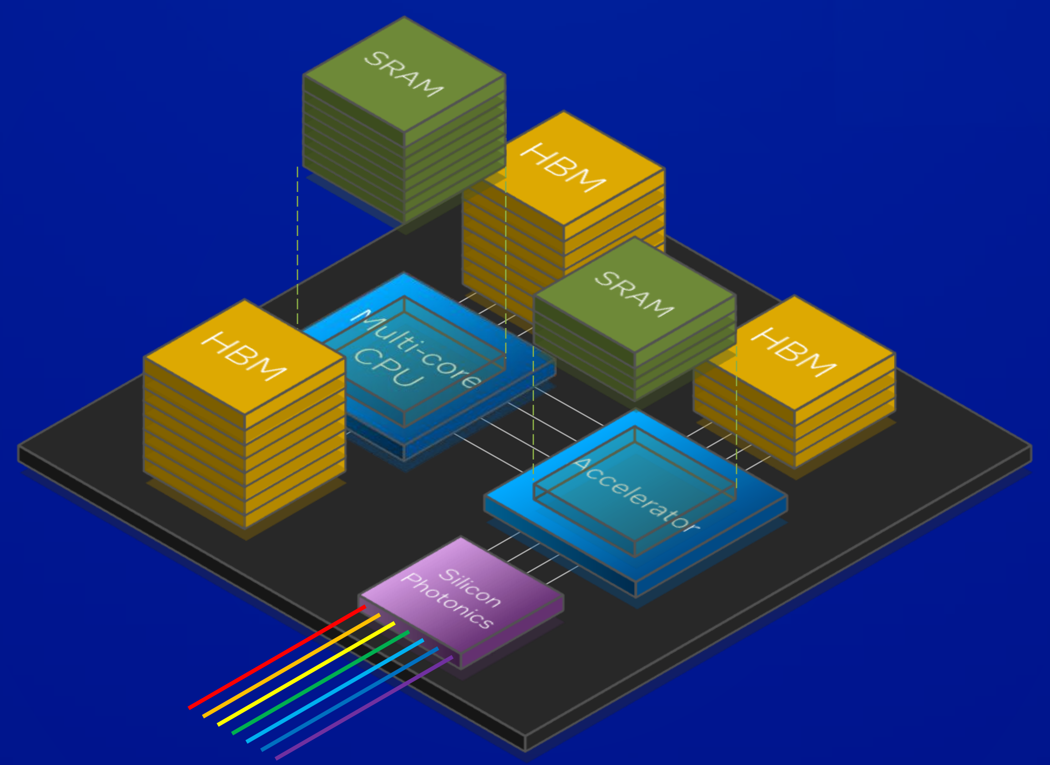
HPC Case Study



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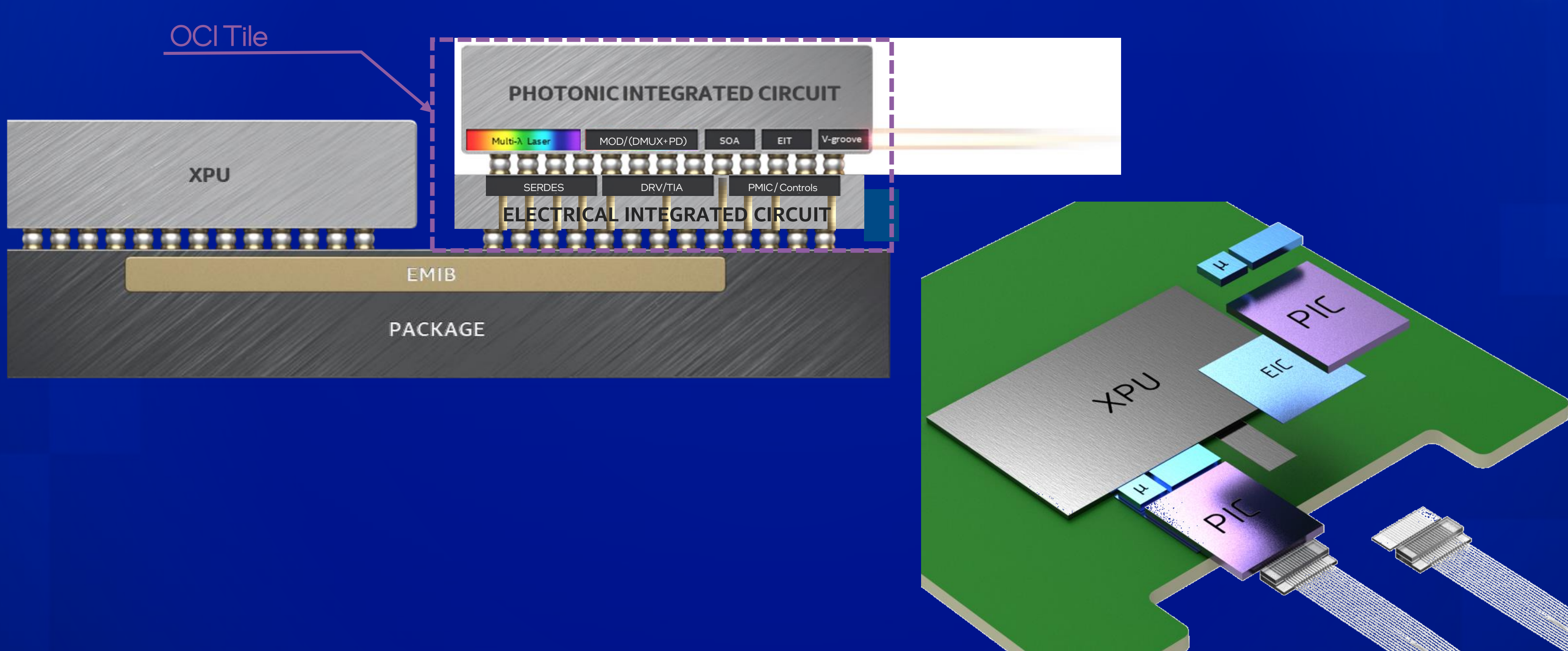
IO Optimization: Intel® Optical

Ex. Network Optimization through Modularity



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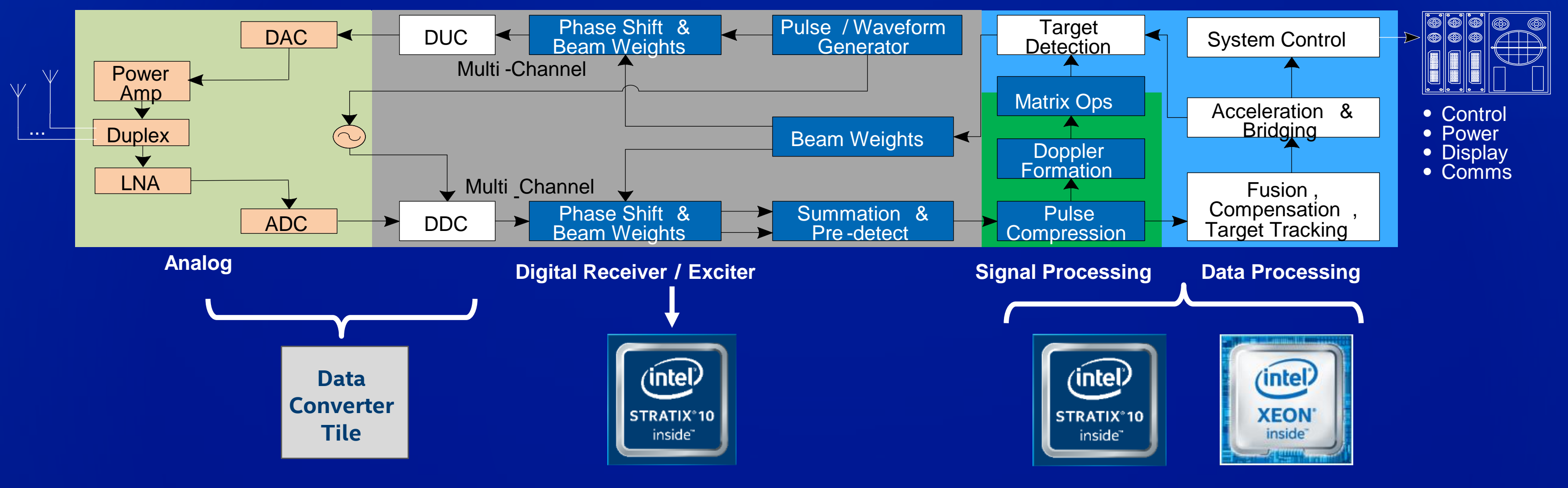
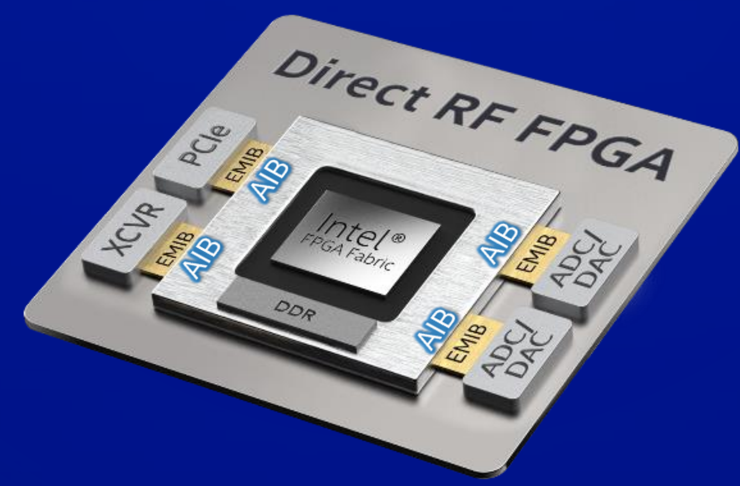
Sensor Case Study: Radar Beamforming Application





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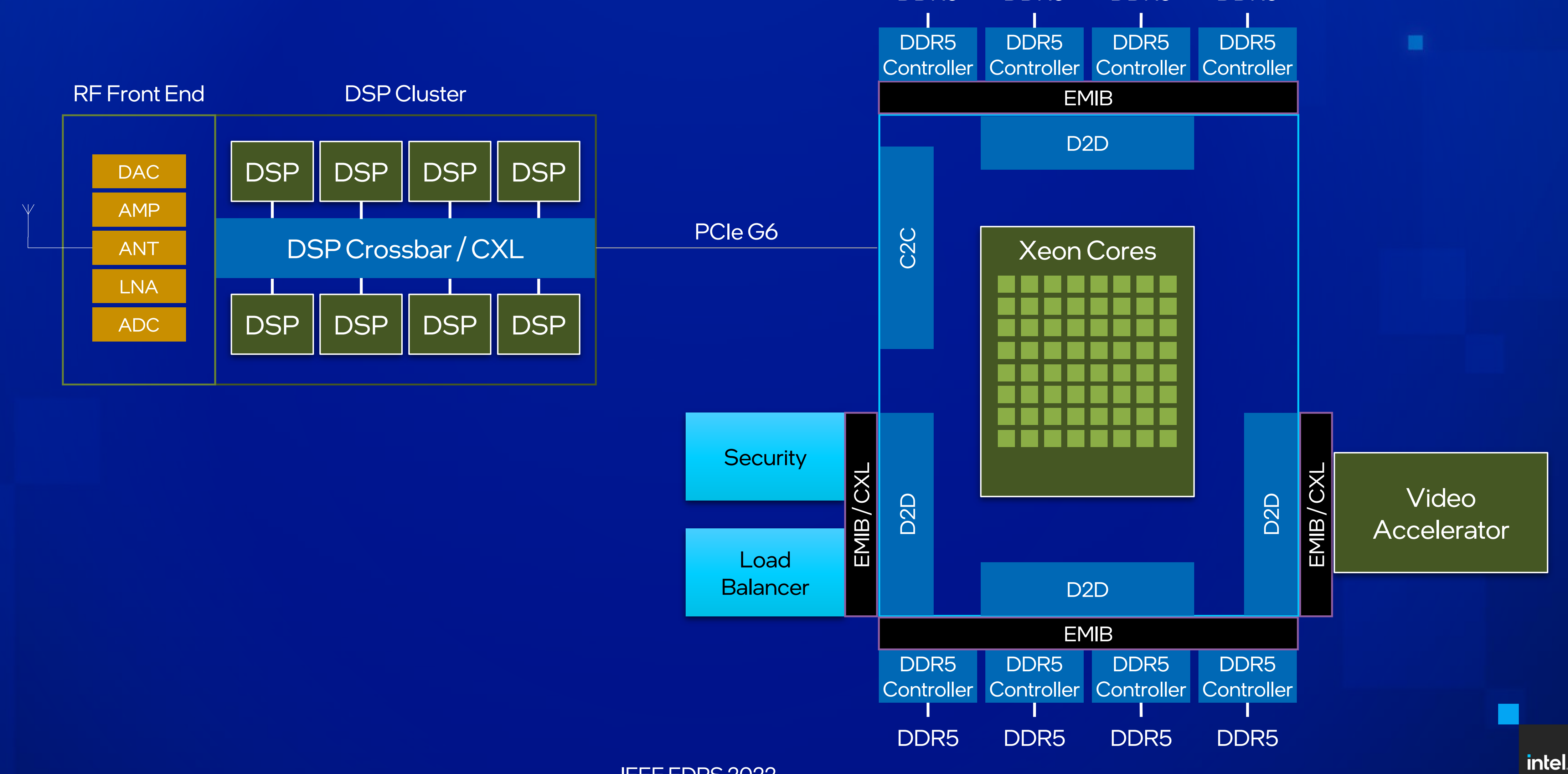
Future Telco Repartitioning (5G, 6G)



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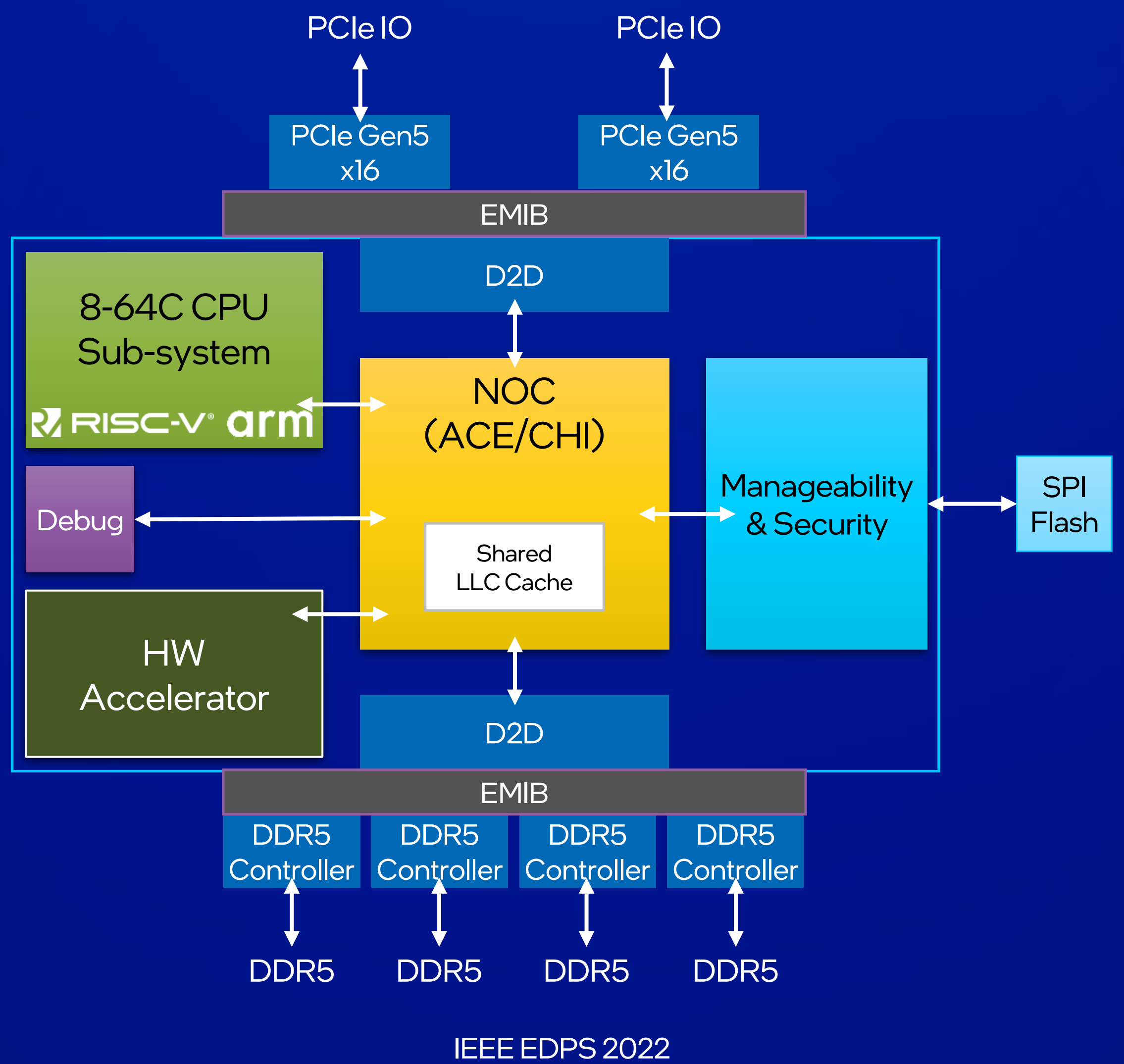
IO Case Study: Disaggregated PCIe & Memory

Ex. Optimization of Process (ex. Analog), Supply Chain



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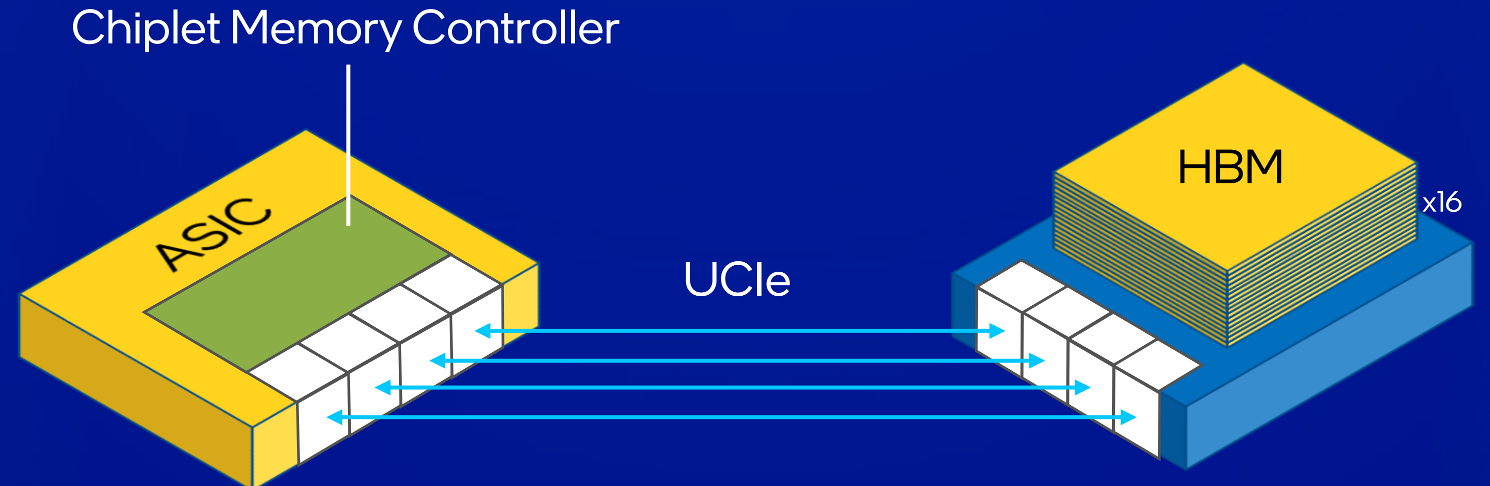
IO Case Study: Possible HBM Architecture

Optimize : AI Bandwidth/Power Density, AI Thermals



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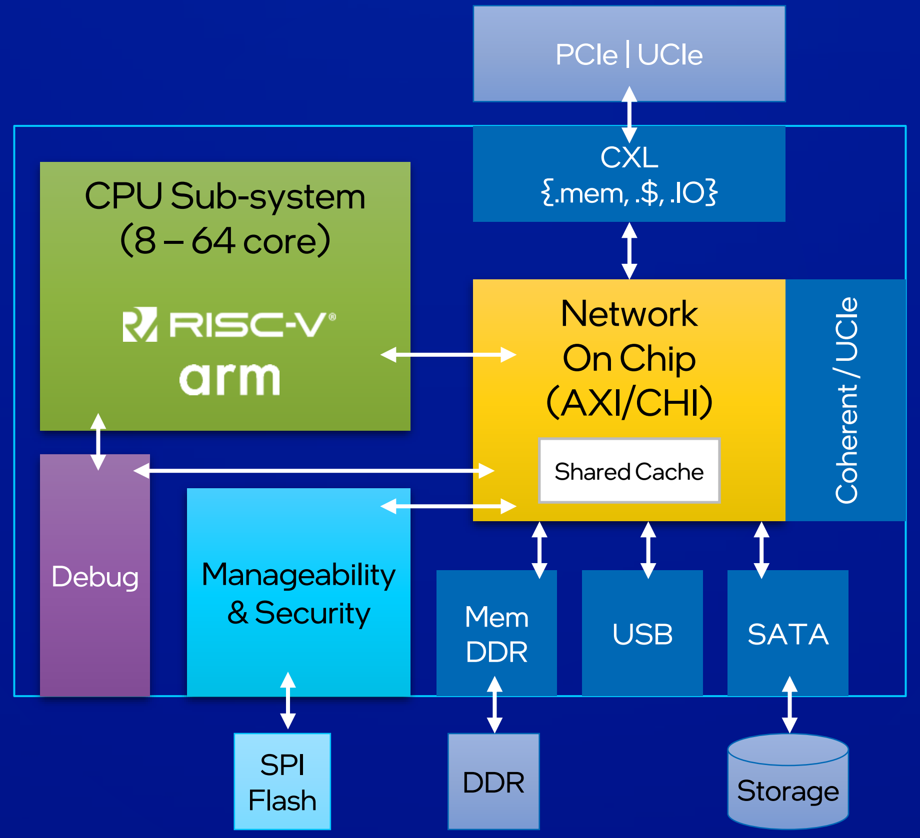
Server Case Study: Multi-core uServer

Ex. Multi-Protocol Architecture : CXL/UCIe and CHI/UCIe



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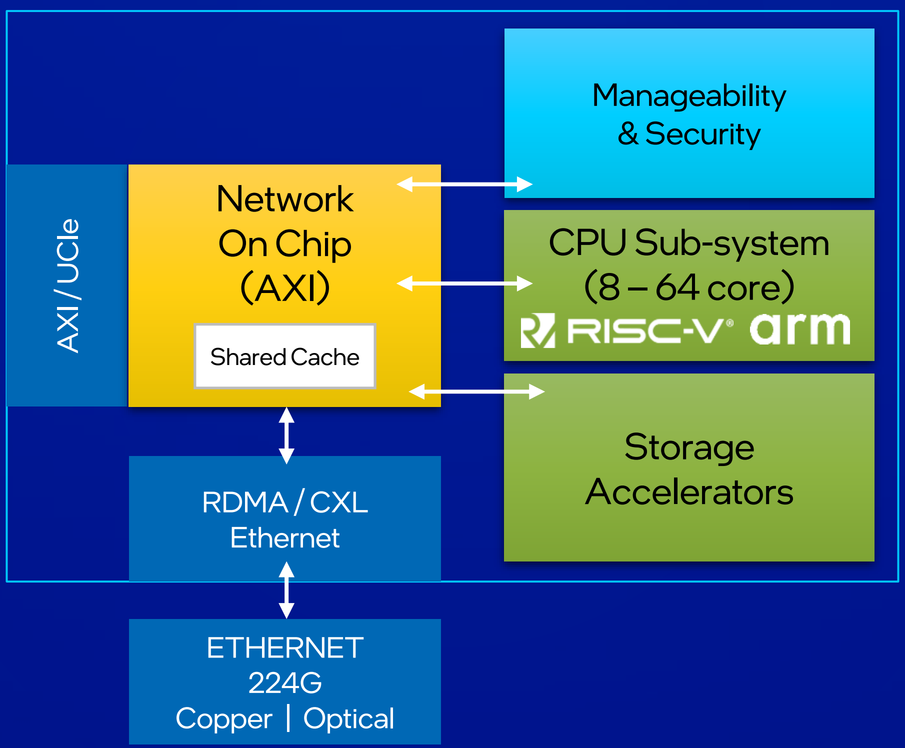
Networking/Storage Case Study: IPU/DPU

Ex. Multi-Protocol Architecture : AXI/UCIe ; Networking Modularity



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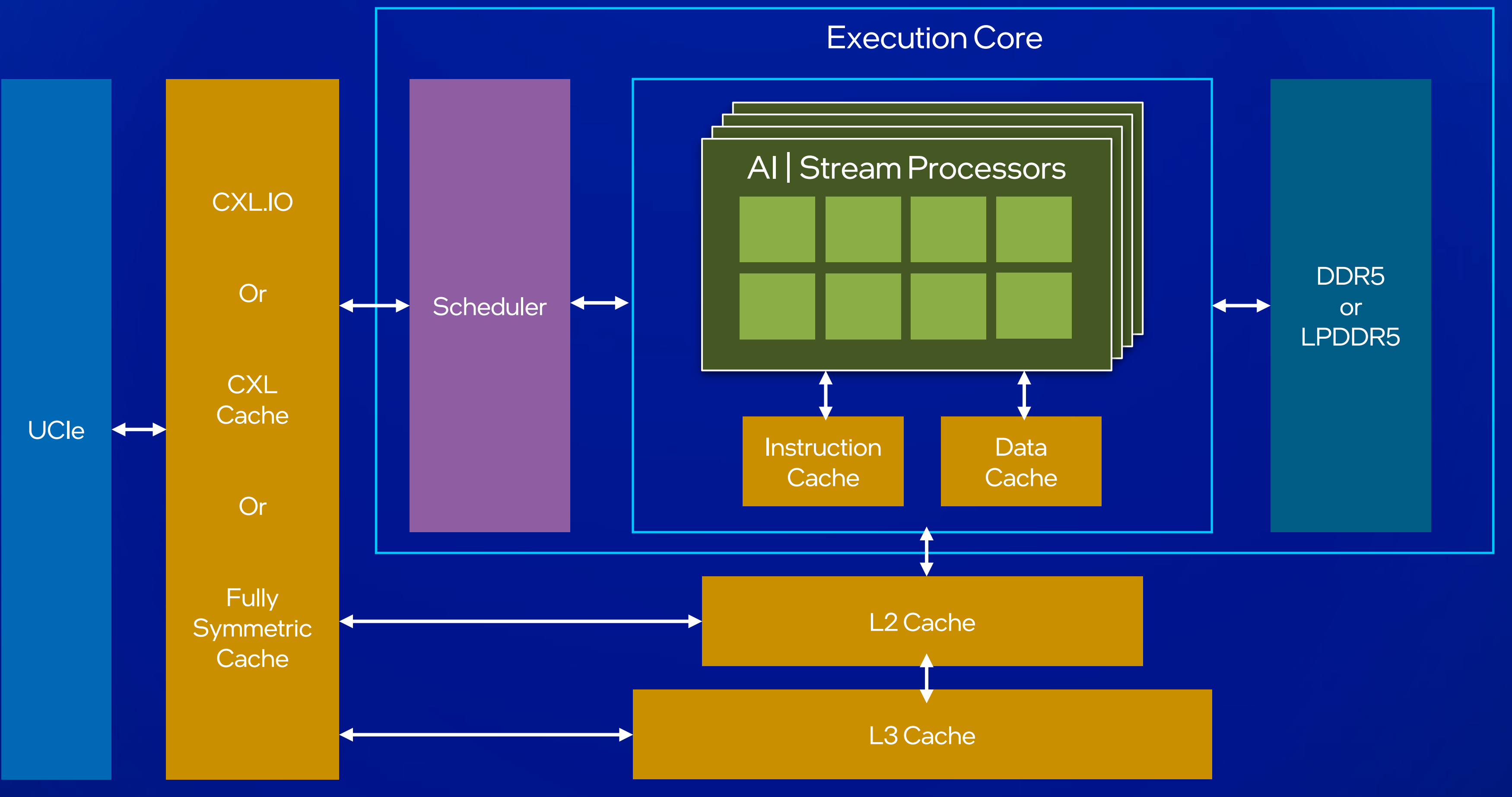
AI Case Study: Caching Inference Architecture

Ex. DMA, Asymmetric Coherence, Symmetric Coherence



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Summary

- Industry Vision – we are at an inflection point
- Technical Challenges – die size, process, IO, and R&D $ optimization
- Technology Needed – new tools in Architecture, Design, and Debug & Test
- Commercial Case Studies – many new emerging architectures, it's just the beginning, let's collaborate!

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