

Modeling Photonic Integrated Circuits in Synopsys Photonic IC Platform: OptoCompiler

Custom Design and Electronic-Photonic Cosimulation

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5th November 2021



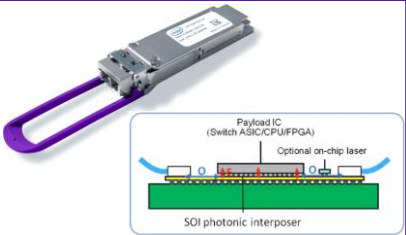
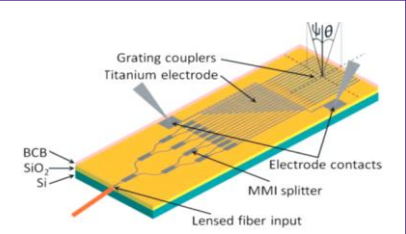

Outline

- Photonic Toolset and Photonic IC Design Platform
- Custom Photonic Design
- E/O Co-design
- Summary

Photonic Toolset and Photonic IC Design Platform



Photonics and PIC Technologies Emerging in many Areas

Technology	Market Segment	Hyperscale networks for Cloud	Cellular networks for 5G/IoT	Computing	Military / Aerospace	Automotive	Consumer	Energy
 <p>Pluggable and co-packaged optics</p>	Optical data communication	●	●	●	●	●	●	
 <p>VCSELs, fiber sensors, LiDAR</p>	Sensing				●	●	●	●
 <p>Wearables, Lab on a Chip</p>	Bio-photonics						●	

● current ● prospective

Key Challenges In Photonic IC Design & Manufacture

For the Tool

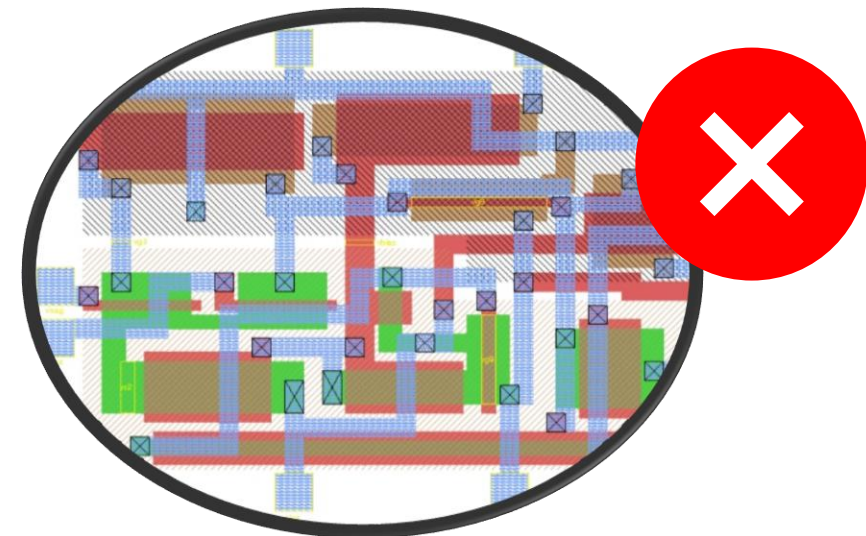
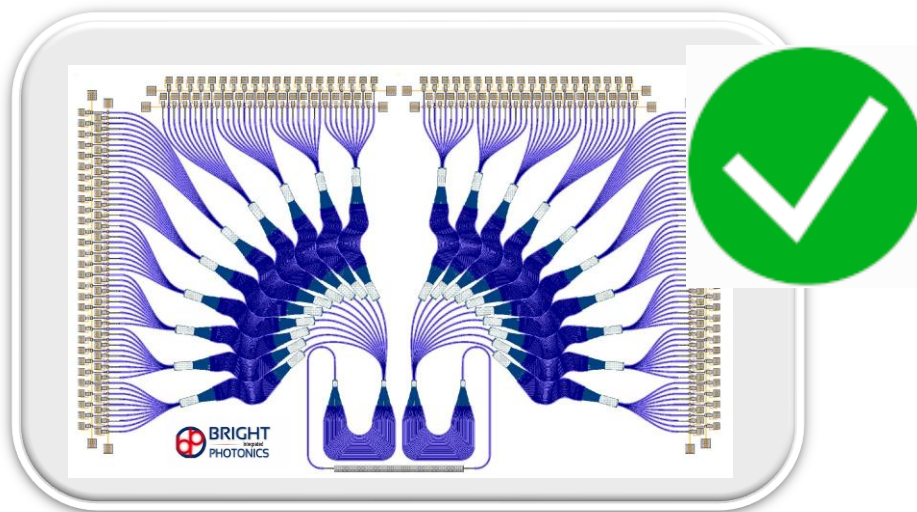
- Photonics has “RF-like” behavior
- Needs curves, not corners
- Uses waveguides, not wires
- Unique physics and signal attributes

For the Designer

- Historically the “domain of experts”
 - Electrical models and simulators are inadequate for photonic devices
 - Manual layout
 - Fragmented flows
- Low Productivity
→ Human Error

For the Foundry

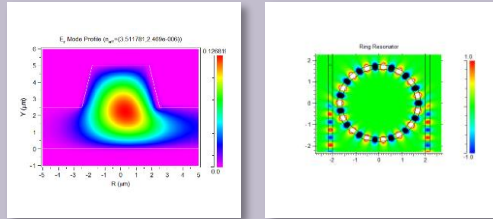
- Photonics process and PDKs are immature
 - Curvy data impacts layout, OPC and mask-prep
- Low Performance and Yield



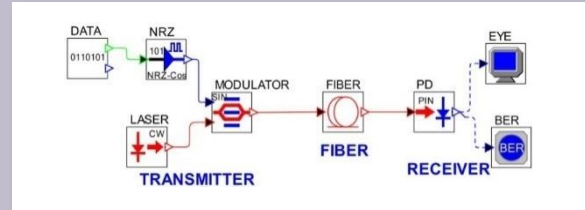
Synopsys Photonic Design Automation Solutions

Increasing quality of results, reducing errors and improving efficiency of photonics design

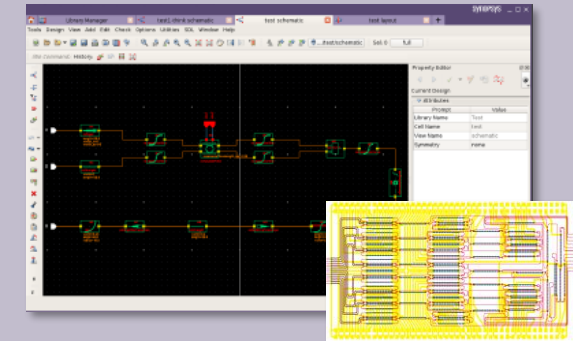
RSoft Photonic Device Tools



OptSim



PIC Solutions



Photonic
Devices

Photonic
Systems

Photonic
ICs

Synopsys provides Industries first Unified E/O co-design Solution

OptoCompiler – interactive design cockpit

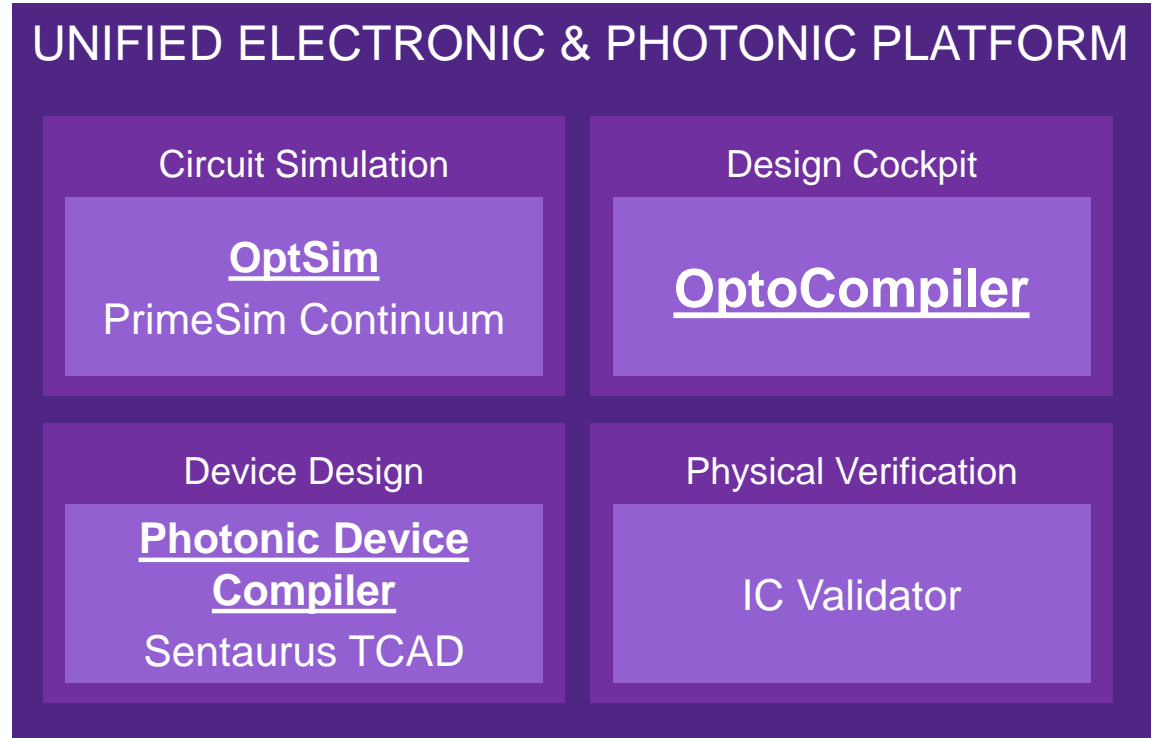
- Complete custom/AMS capability
- Photonic-aware layout synthesis
- Exclusive Photonic Design Features
 - Seamless abutment
 - Photonic auto-align
 - Assisted Waveguide Routing
- Photonic DRC & LVS with **IC Validator**

OptSim – photonic circuit & system simulation

- E/O co-simulation with **PrimeSim**

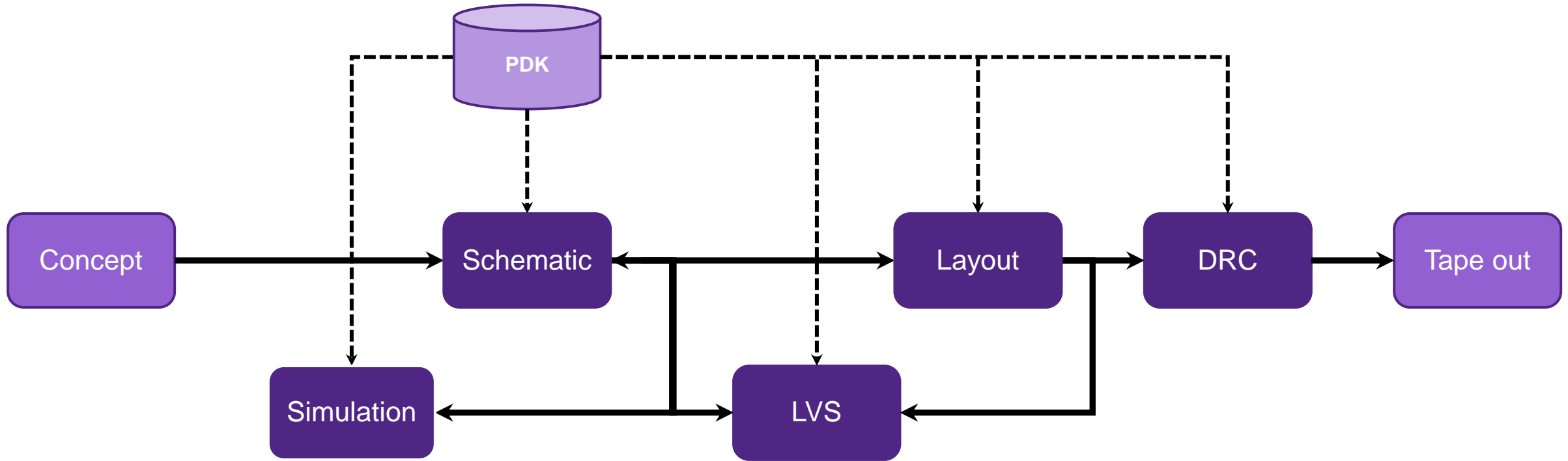
Photonic Device Compiler – device design

- E/O co-simulation with **Sentaurus TCAD**
- Automated photonic PDK and library development



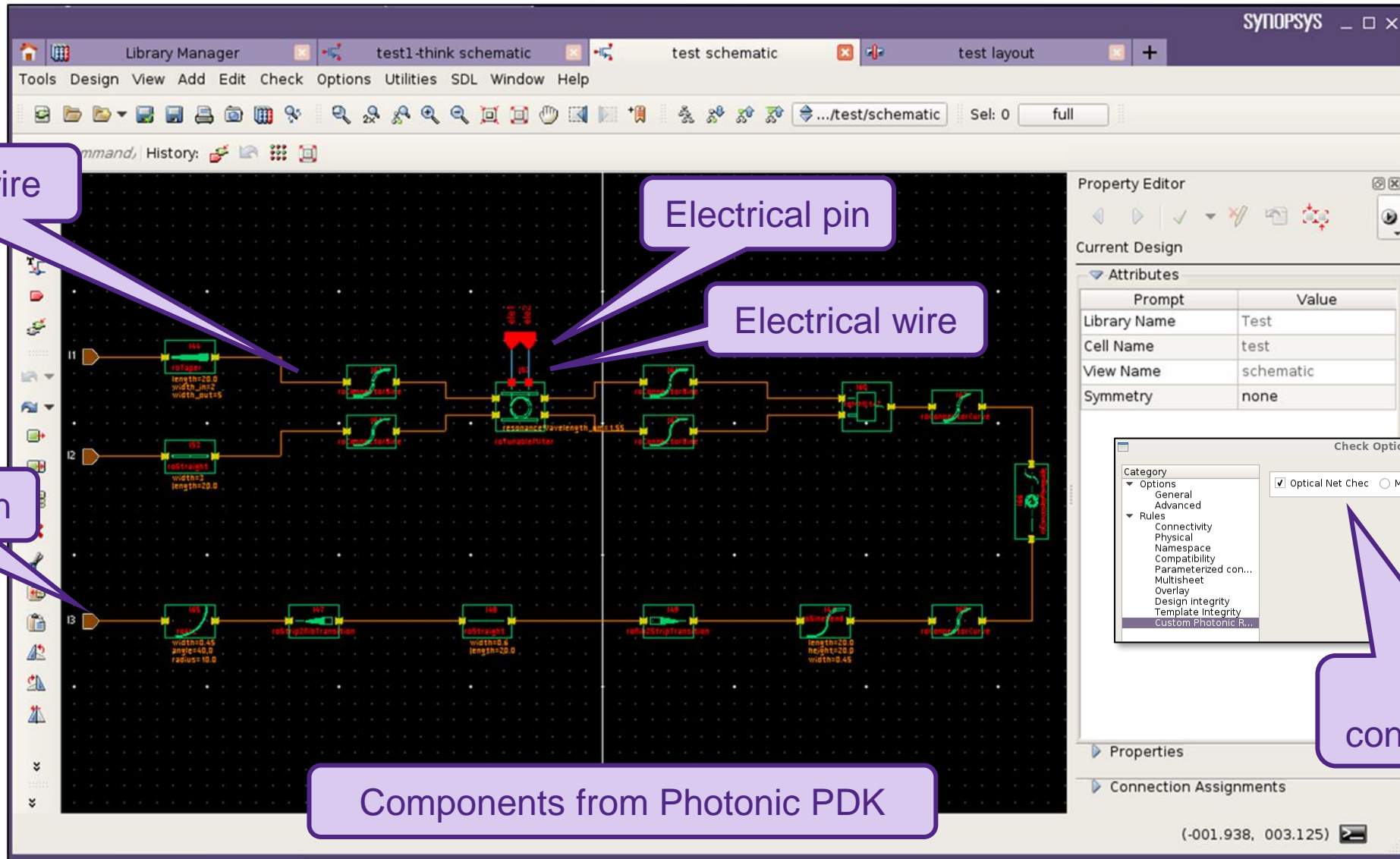
The industry's **only unified** electronic & photonic platform

OptoCompiler provides PDK driven Schematic Driven Layout (SDL) Design Flow



1. Schematic capture and simulation
2. Layout implementation
3. Back annotation and re-simulation
4. Design rule checking and layout versus schematic verification

OptoCompiler uses modern and easy to use design environment, familiar for IC designers



Photonic wire

Electrical pin

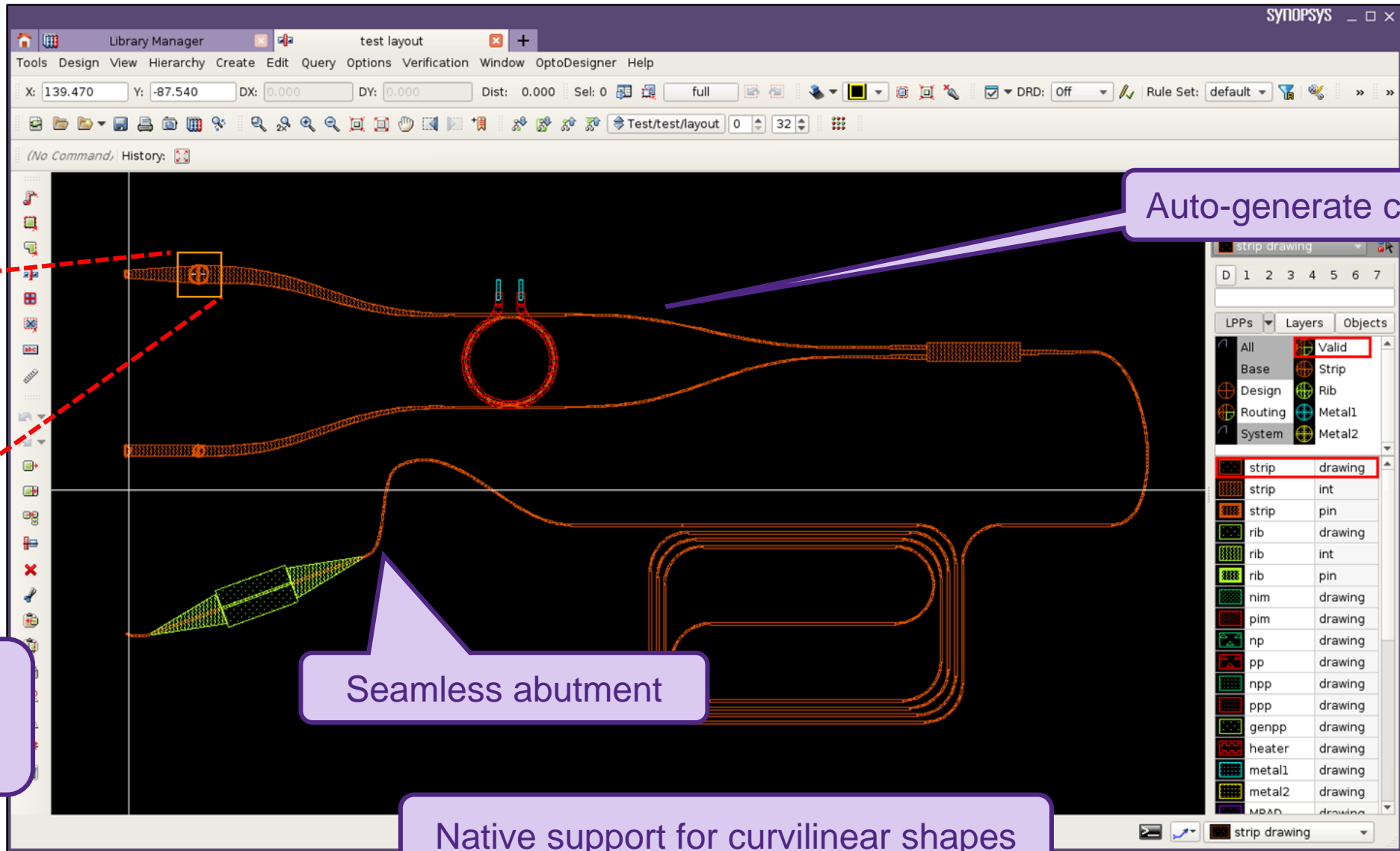
Electrical wire

Photonic pin

Photonic connection check

Components from Photonic PDK

OptoCompiler provides interactive layout with productivity features for photonics



Auto-generate connectors

$w = 5.0$ $w = 5.0$
 $a = 180.0$ $a = 0.0$

Display of photonic pin properties

Seamless abutment

Native support for curvilinear shapes

OptoCompiler provides back annotation to enable post layout verification

Identify and solve
mismatch of
photonic parameter
in schematic

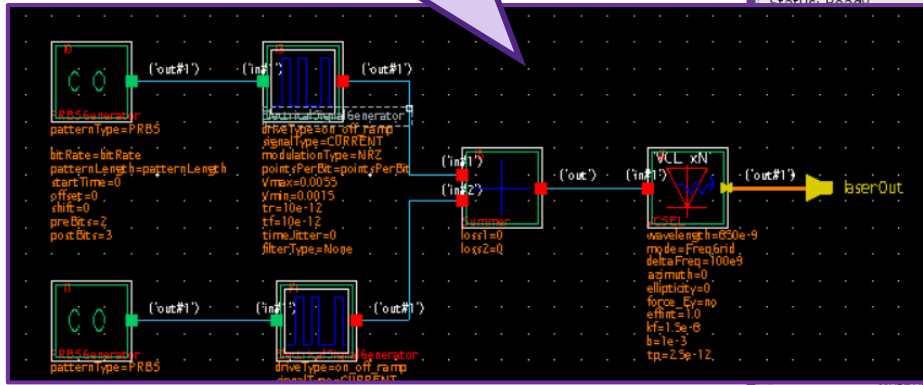
The screenshot displays the Synopsys OptoDesigner interface. The main window is titled 'test layout' and shows a photonic layout with orange waveguides and a red circular component. A context menu is open over the layout, listing various actions such as 'Symbolic Editor with Chaining', 'Pick and Place', 'Manual Correspondence', 'Instance Mapping...', 'Fit', 'Select in Design', 'Fix Mismatch', 'Back Annotate Parameter', 'Fix Soft Macro Mismatch', 'Flatten', 'Recover', and 'Create Template'. A purple callout box points to the 'Back Annotate Parameter' option. Another purple callout box points to the 'Mismatch' column in the 'Insts' table below.

Insts	Master	Parameter	Mismatch
I61	roConnector...	crossSection...	
I62	roConnector...	crossSection...	
I63	roConnector...	crossSection...	
I64	roConnector...	crossSection...	
I65	roArc	crossSection...	
I66	roComposite...	crossSection...	

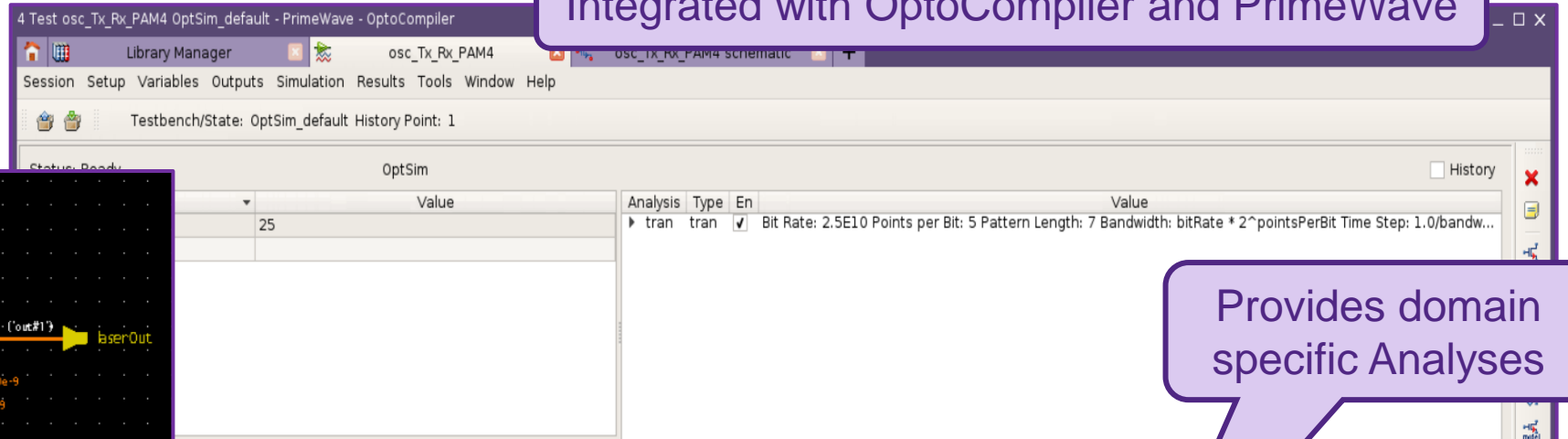
Back annotation
from layout to
schematic

OptSim enables seamless circuit and system simulation and analysis

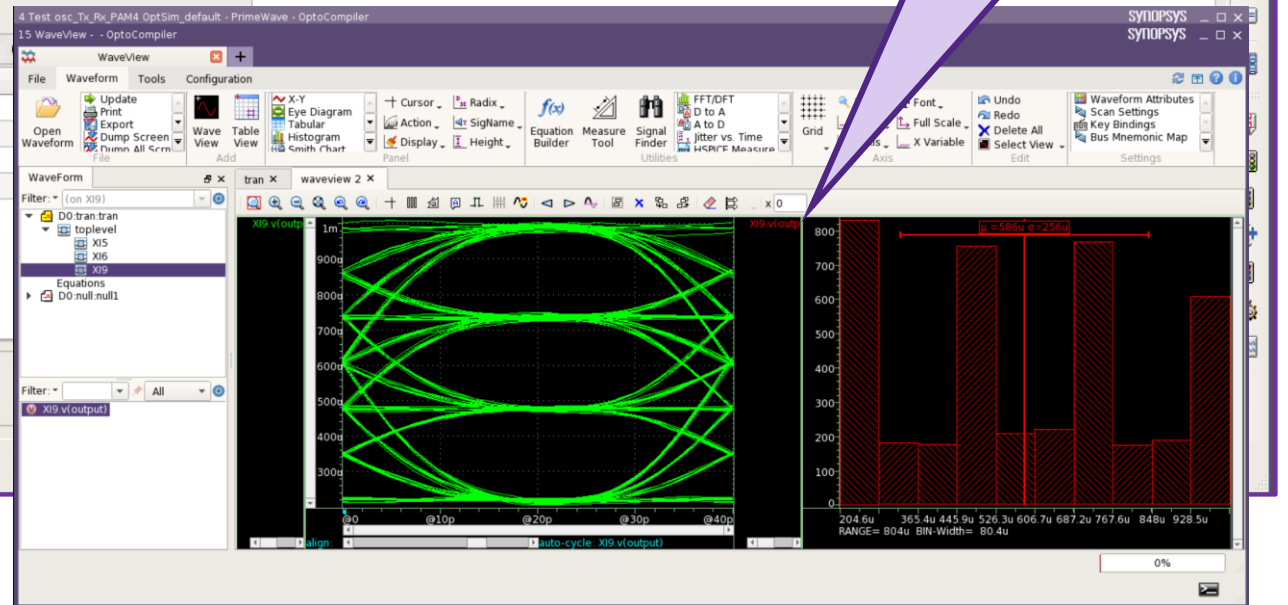
Supports Optical, Electrical and Logical Signals



Integrated with OptoCompiler and PrimeWave



Provides domain specific Analyses



Electro-Optical co-simulation

Enable

Netlist Format: HSPICE Spectre

Electrical Simulator: PrimeSim HSPICE
PrimeSim HSPICE
FineSim
PrimeSim SPICE

E/O co-simulation with domain specific engines

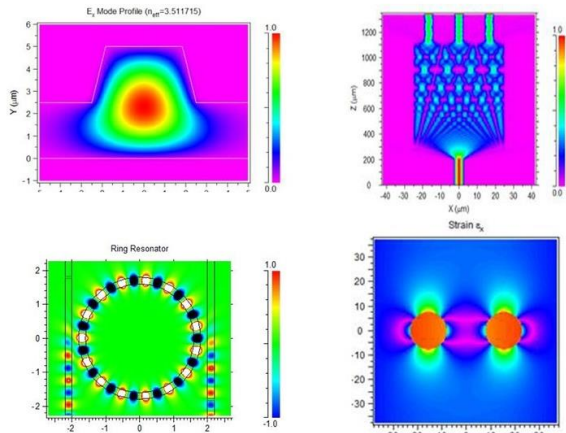
Custom Photonic Design



Photonic Device Compiler supports Photonic device design, PDK and custom library development

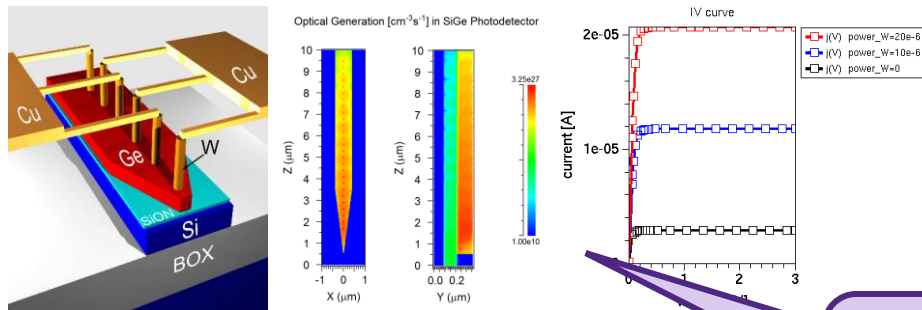
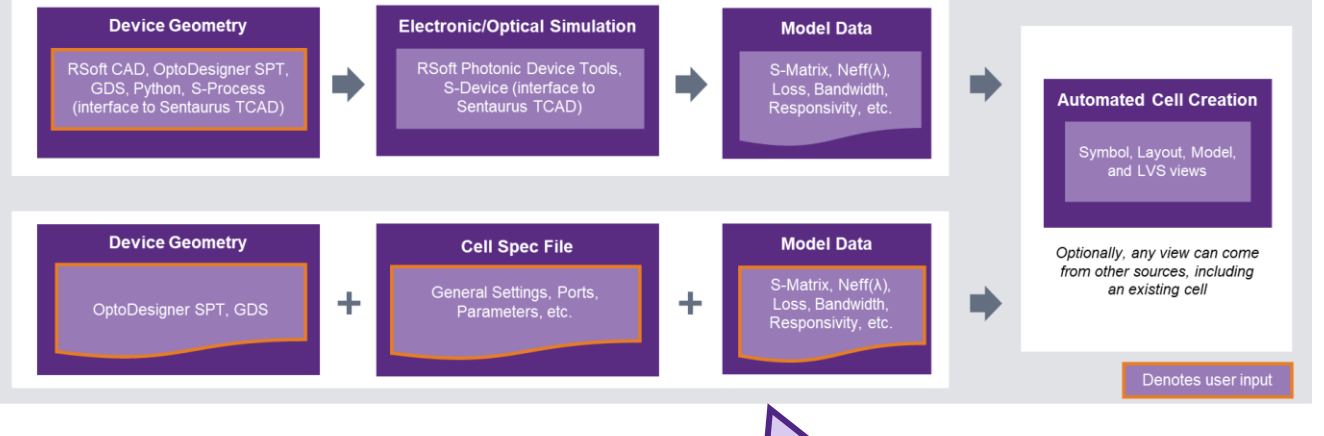
Design, simulate, and optimize passive and active photonic devices

Create Symbols, Layouts, Simulation Models and LVS information



Industries largest set of tools and methods, including BPM, FDTD, RCWA

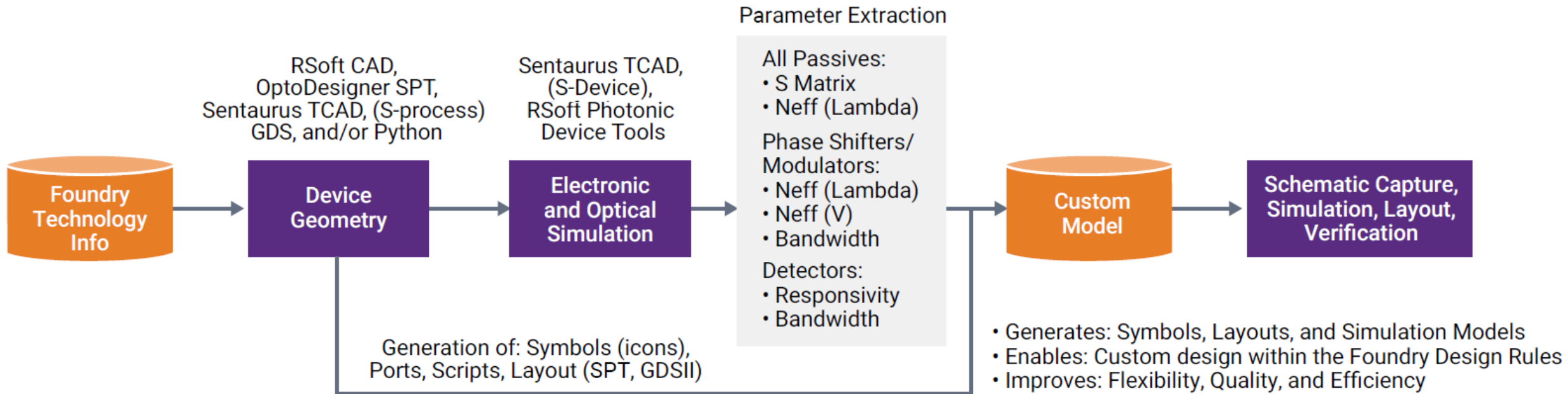
Custom PDK Utility: Component Cell Creation and Automation Flows



Interfaces with Sentaurus TCAD, CODE V and LightTools

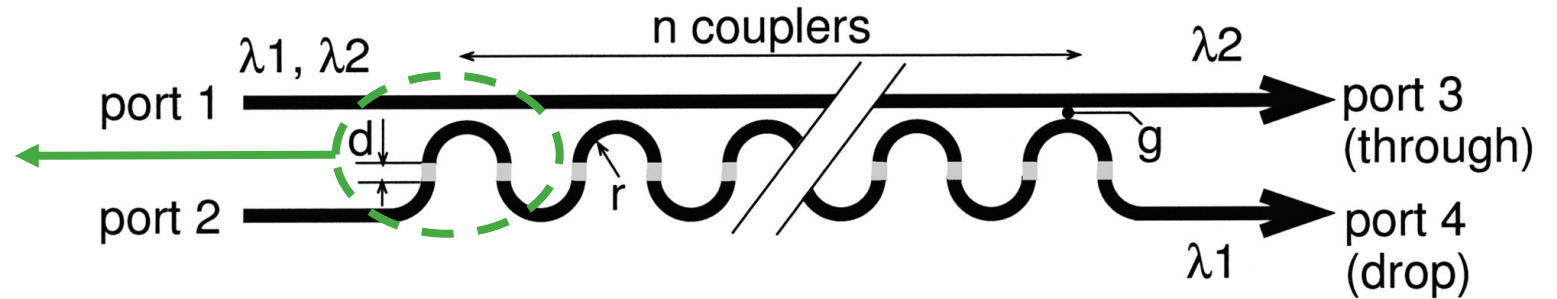
Automation for PDK and custom device creation

Photonic Device Compiler supports Photonic device design, PDK and custom library development



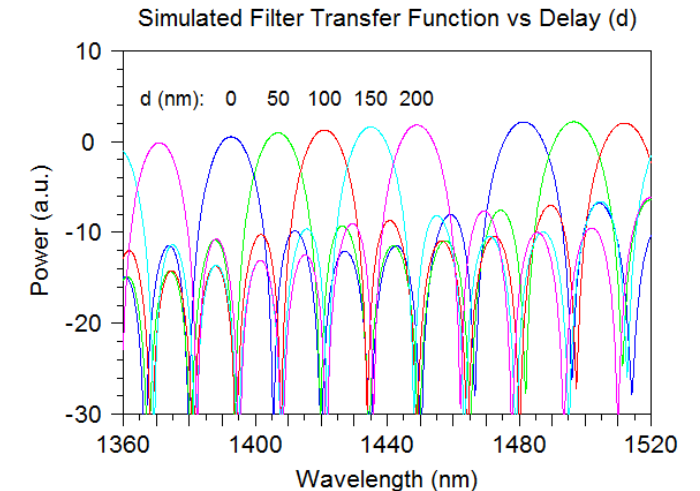
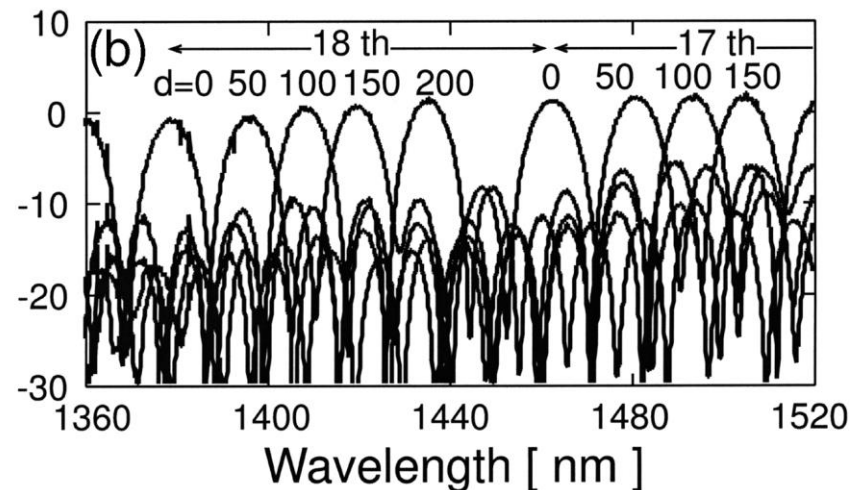
Example: Tunable Lattice Filters for Detector Array

- Cascaded MZI coupler elements can be tuned to different wavelengths via adjustable delay length d



Koji Yamada, *et al*, "Silicon-wire-based ultrasmall lattice filters with wide free spectra ranges," *Optics Lett.*, vol. 28, No. 18, pp. 1663-1664, Sept. 2003.

- Different cascade designs can be used as optical filters before detectors to create a multi-channel detector array

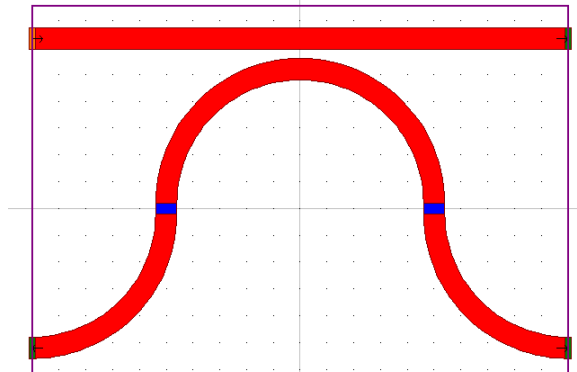


Example : Tunable Lattice Filters for Detector Array

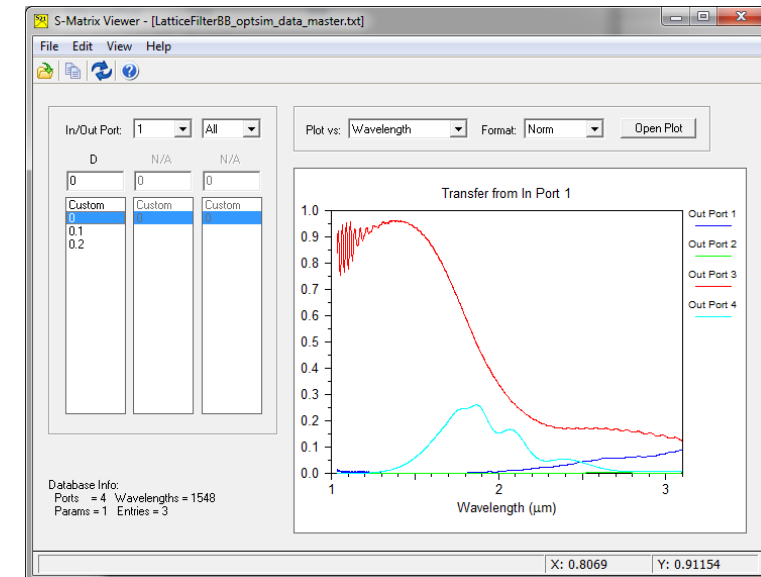
Device Overview

- The Building Block (BB) to construct the device is a single MZI coupler shown on the right.
- Synopsys Photonic Device Compiler used to generate transfer function for BB.
- Filter formed by cascading several coupler BBs
- 6-stage cascaded MZI couplers are used to balance ER and bandwidth requirements
- Resulting device:
 - Is tunable: Adjusting delay line length (d) changes dropped wavelength
 - Is small: A $2.5\mu\text{m}$ bend radius \rightarrow overall length less than $100\mu\text{m}$
 - Has a large free spectral range (FSR)

Component Model of Single Coupler (BB)



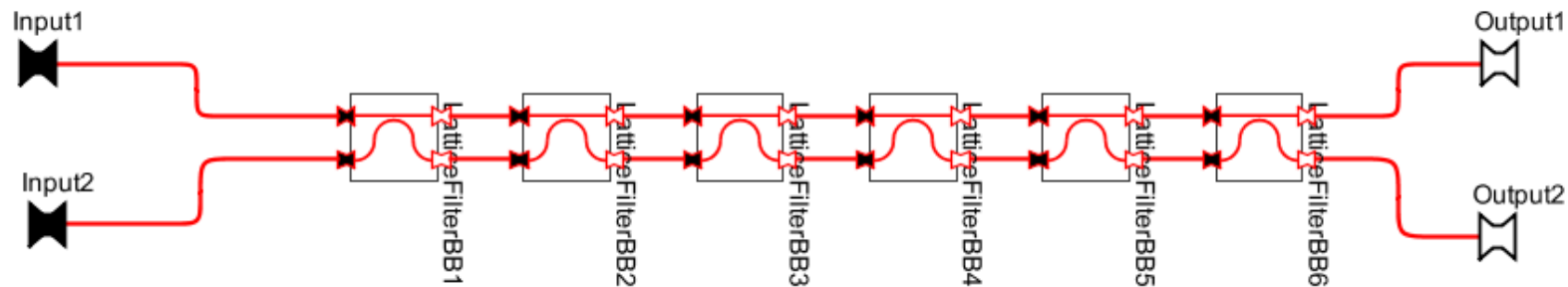
Generated S-Matrix for the BB



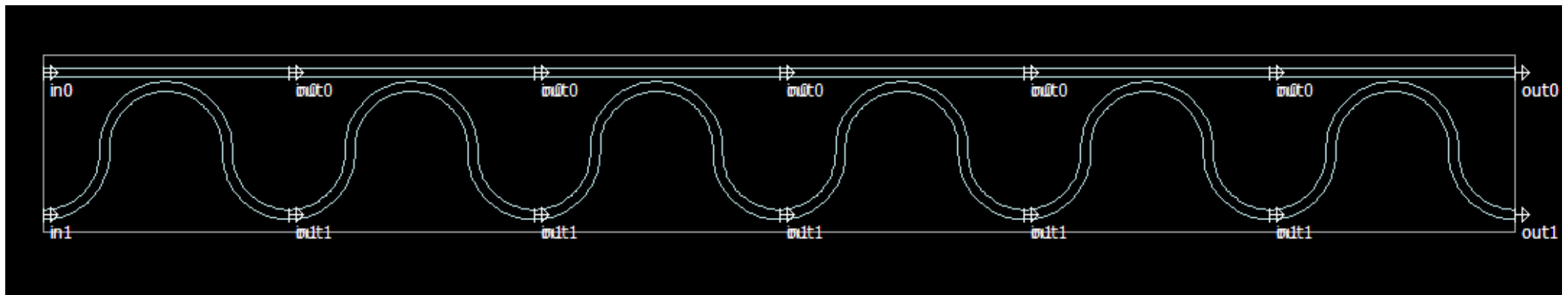
Example : Tunable Lattice Filters for Detector Array

Circuit Schematic and Layout: OptoCompiler

- Schematic



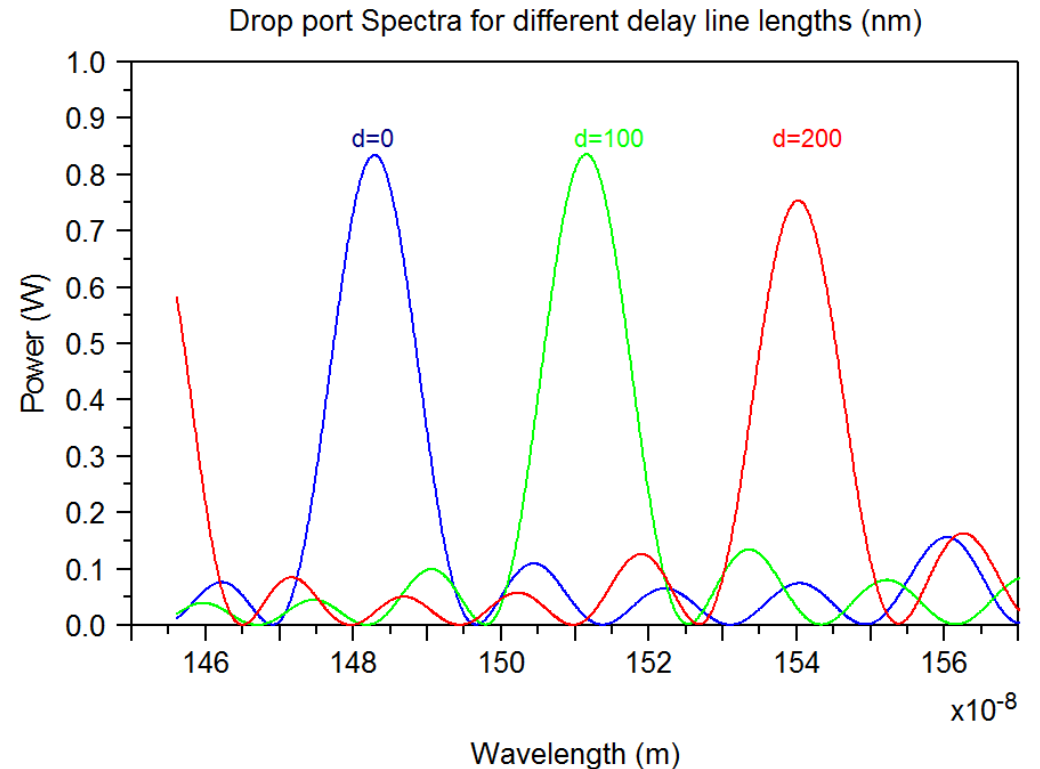
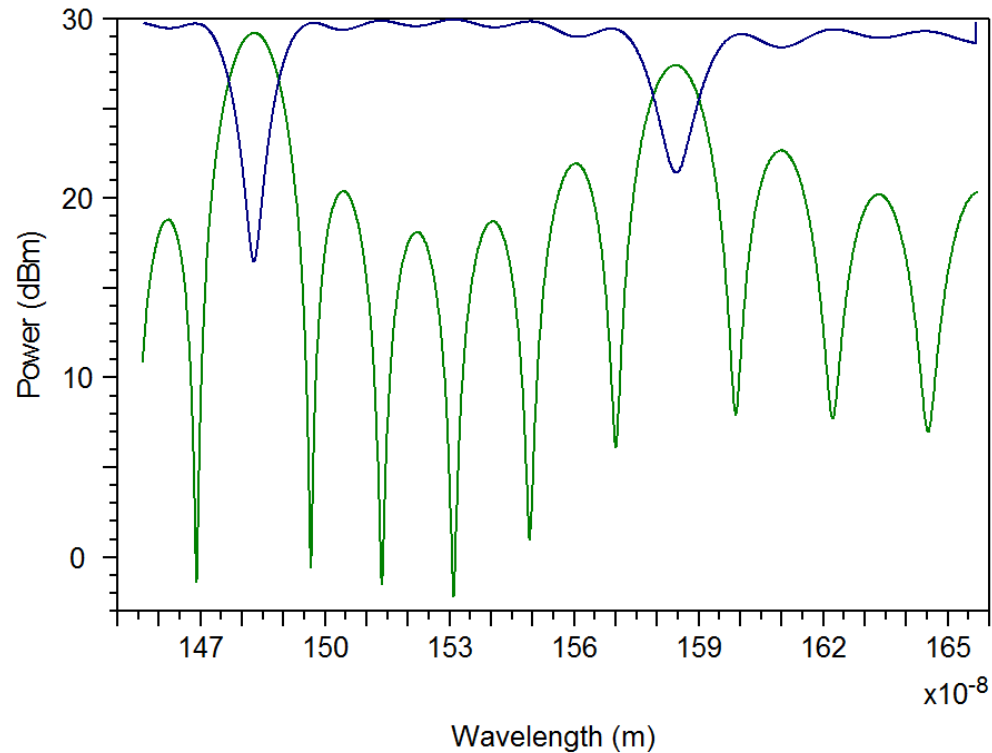
- Layout



Example : Tunable Lattice Filters for Detector Array

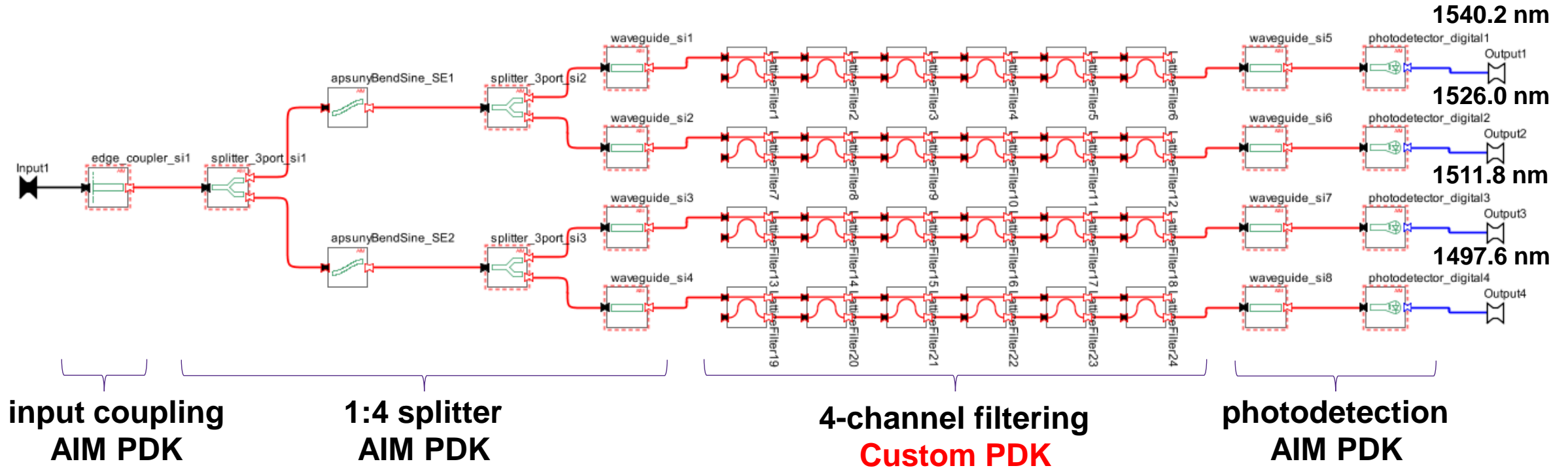
OptSim Simulation Results (Using S-Matrix data from FullWAVE)

- Left: Through and Drop port Spectrum with FSR $\sim 100\text{nm}+$ (at delay length $d=0$)
- Right: Drop port Spectra for various delay line lengths



Example: Tunable Lattice Filters for Detector Array

4-channel Detector Array using both Foundry and Custom PDK Elements

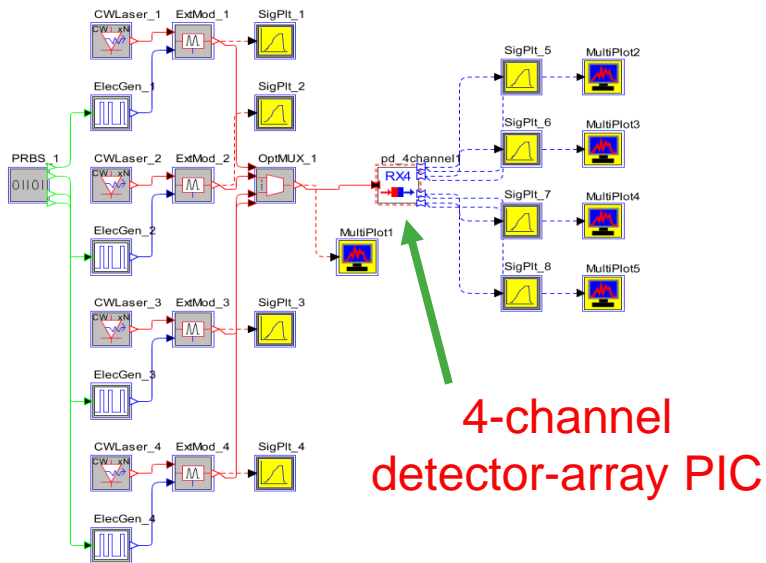


- 6-stage cascaded MZI couplers are used to balance ER and bandwidth requirements
- Adjustable delay lengths $d = 50, 100, 150, \text{ and } 200$ nm accommodate center channels of 1497.6, 1511.8, 1526.0, and 1540.2 nm, respectively
- Standard AIM Photonics PDK elements provide input coupling, signal splitting, and photodetection

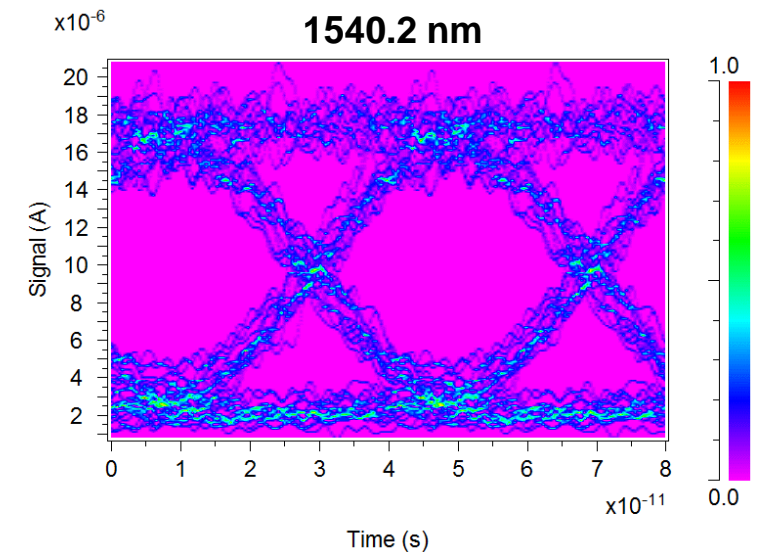
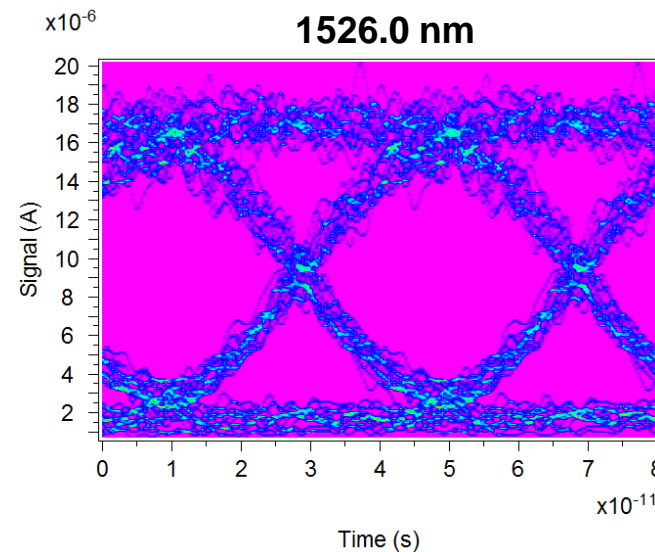
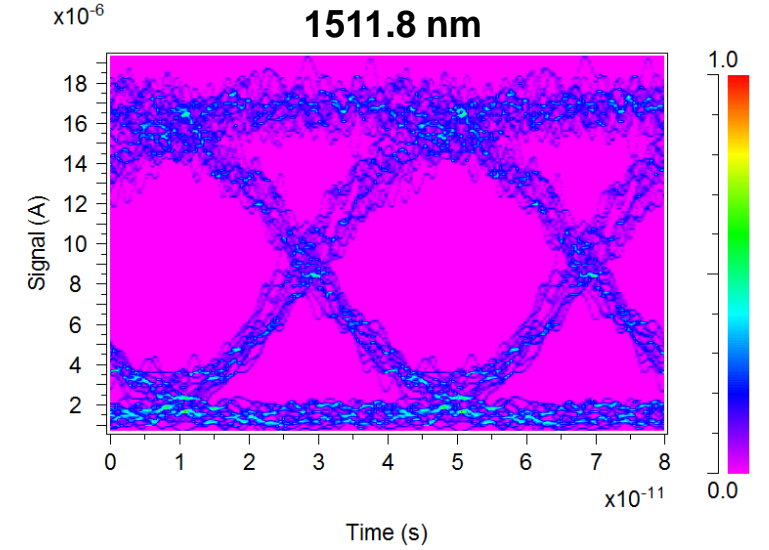
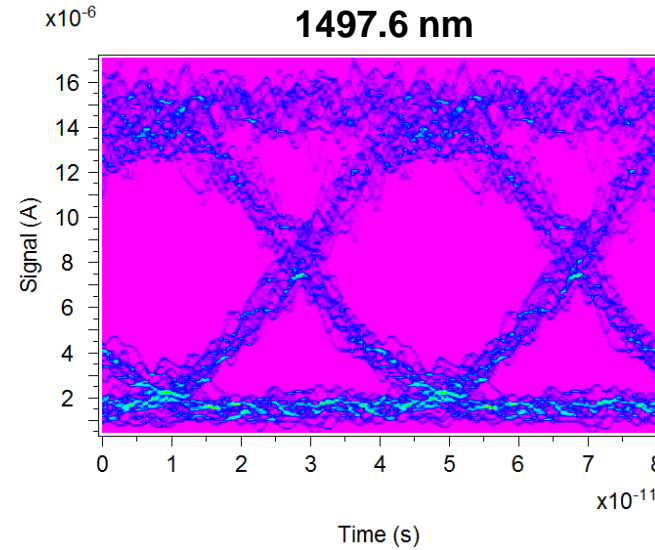
Example: Tunable Lattice Filters for Detector Array

4-channel Detector Array Eye Diagrams

Test Circuit:

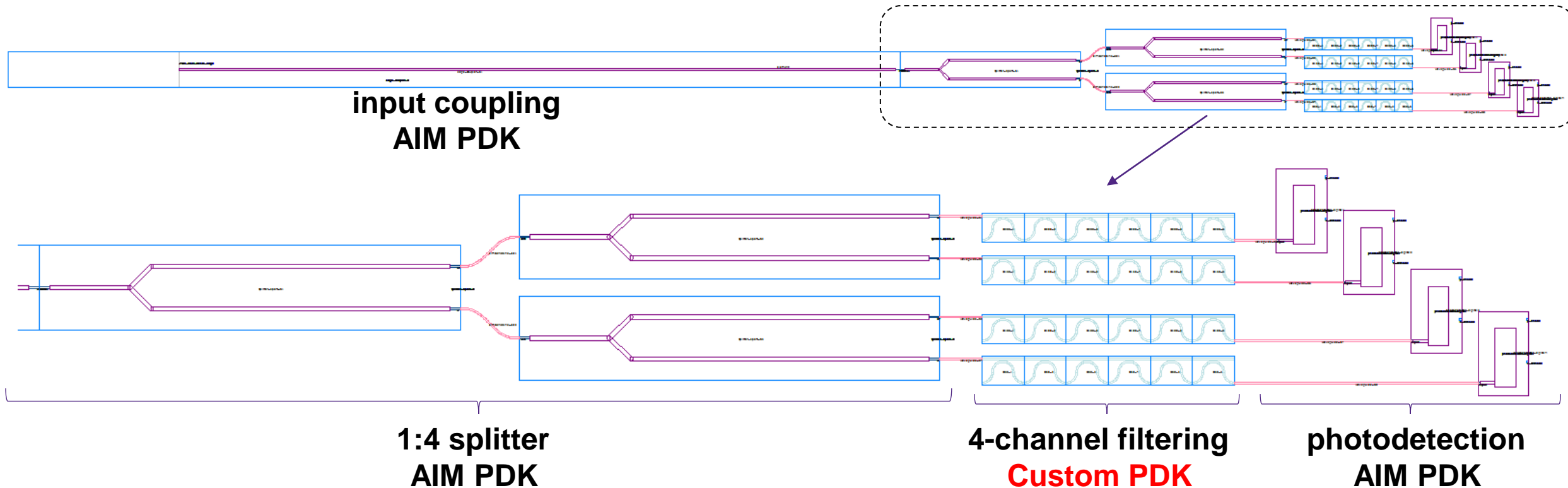


- 25 Gbps NRZ operation
- Approximately -8 dBm launch power per channel
- Open eye at all four wavelengths



Example: Tunable Lattice Filters for Detector Array

4-channel Detector Array Layout



- Custom photonic components behave like foundry PDK components and follow the same schematic-driven layout (SDL) flow

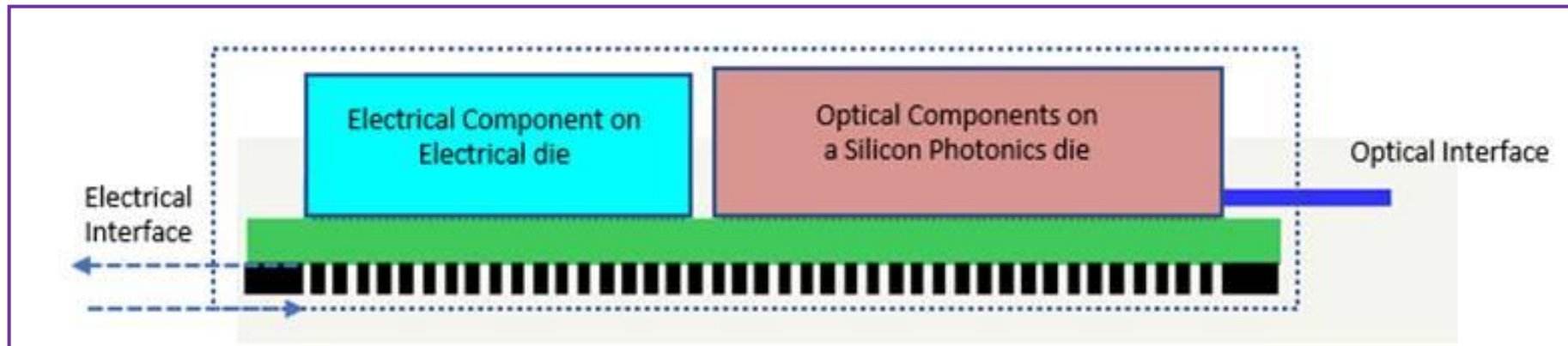
E-O Co-Design



Electronics-Photonics Cosimulation

- Motivation:

- Many applications require electronics to drive photonics (e.g., transceivers)
- The transition from pluggables to co-packaged optics is inevitable

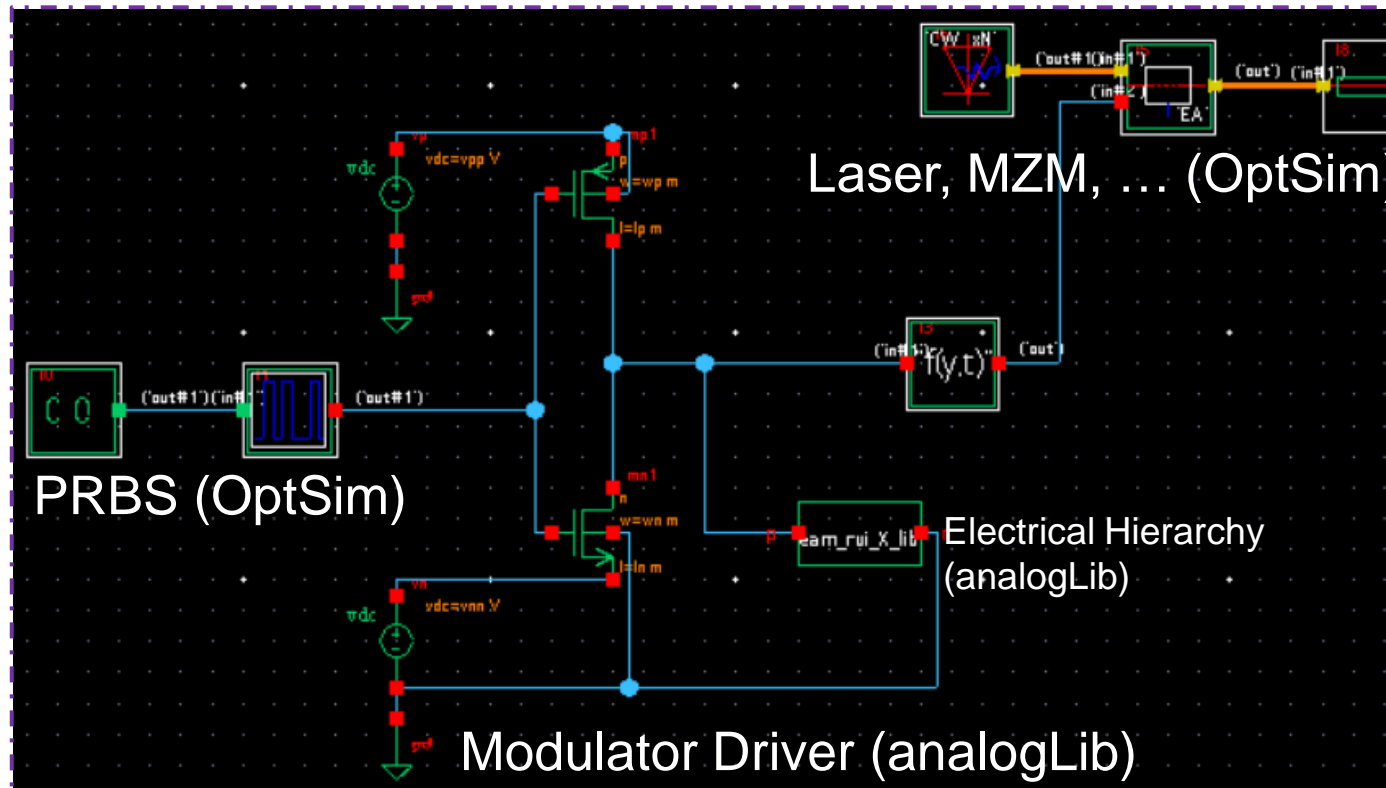


- Modeling bidirectional photonic circuits as electronic circuits (Verilog-A,...) is too much pain with too little gain
- Commercial electrical circuit simulators and photonic circuit simulators are mature today (i.e., no need to model photonics as electronics unlike in past)

OptSim: Electronics-Photonics Cosimulation

- Philosophy:

- Provide intuitive and seamless E-O schematic creation (Electrical + Photonic devices in the same Schematic)
- Free designers from manual, error-prone cross-domain interventions



Testbench: Setting up E-O Co-Simulation

- A testbench is a simulation setup for the schematic under test
- PrimeWave Design Environment enables management of testbenches

The screenshot displays the PrimeWave Design Environment interface. The top menu bar includes 'Setup', 'Variables', 'Outputs', 'Simulation', and 'Results'. The 'Setup' menu is open, with 'Simulator...' highlighted. A red circle highlights the 'Setup' menu item, and a red arrow points to it. A green circle highlights the 'Simulator...' menu item, and a green arrow points to it. The main window shows the 'PrimeWave Design Environment' with a status bar indicating 'Simulation Completed' and 'OptSim Jobs: 40 (Data Points: 40)'. The 'Design Variables' table is visible, listing variables like 'temp', 'L1_um', 'L2_um', and 'filter_center_nm'. The 'Analysis' table shows analysis types like 'corners', 'Monte Carlo', and 'tran'. The 'Probes at nodes and nets' table lists various output expressions and their corresponding plot types and colors. The 'Simulators' dropdown menu is open, showing options like 'OptSim', 'PrimeSim', 'FineSim', 'FineSim VCS', 'OptSim', and 'Spectre'. The 'Plots' table shows the configuration for each output, including plot type and color.

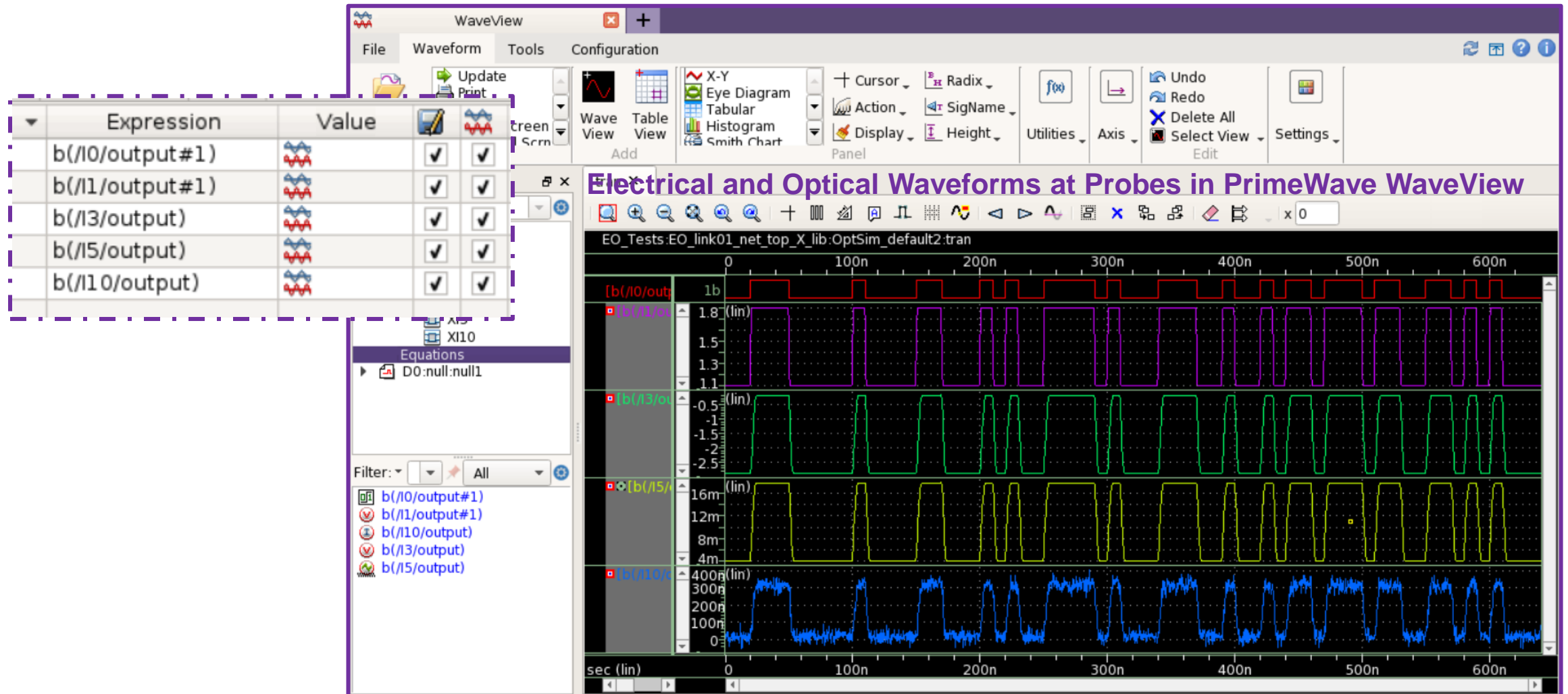
Variable	Value
temp	25
L1_um	100.0
L2_um	120.0
filter_center_nm	

Analysis	Type	En	Value
corners		✓	Total:2, enabled: 2
▶ Monte Carlo	Monte Carlo	✓	Iterations: 20 Start Iteration: 1
▶ tran	tran	✓	Bit Rate: 1E10 Points per Bit: 5 Pattern Length: 7 Bandwidth: bitRate * 2^pointsPerBit Ti...

Output	Expression	Value	Plot Type	Plot Color
	b(/I1/input#1)		auto	
	oc_opt_pow(attenOut, /I9/output#2)		scatter	
	oc_opt_pow(filterOut, /I7/output)		histogram	
	oc_opt_pow(m1, /I7/output)		scatter	

Simulator	Netlist Format	Results Directory
OptSim		
PrimeSim		
FineSim		
FineSim VCS		
OptSim		
Spectre		

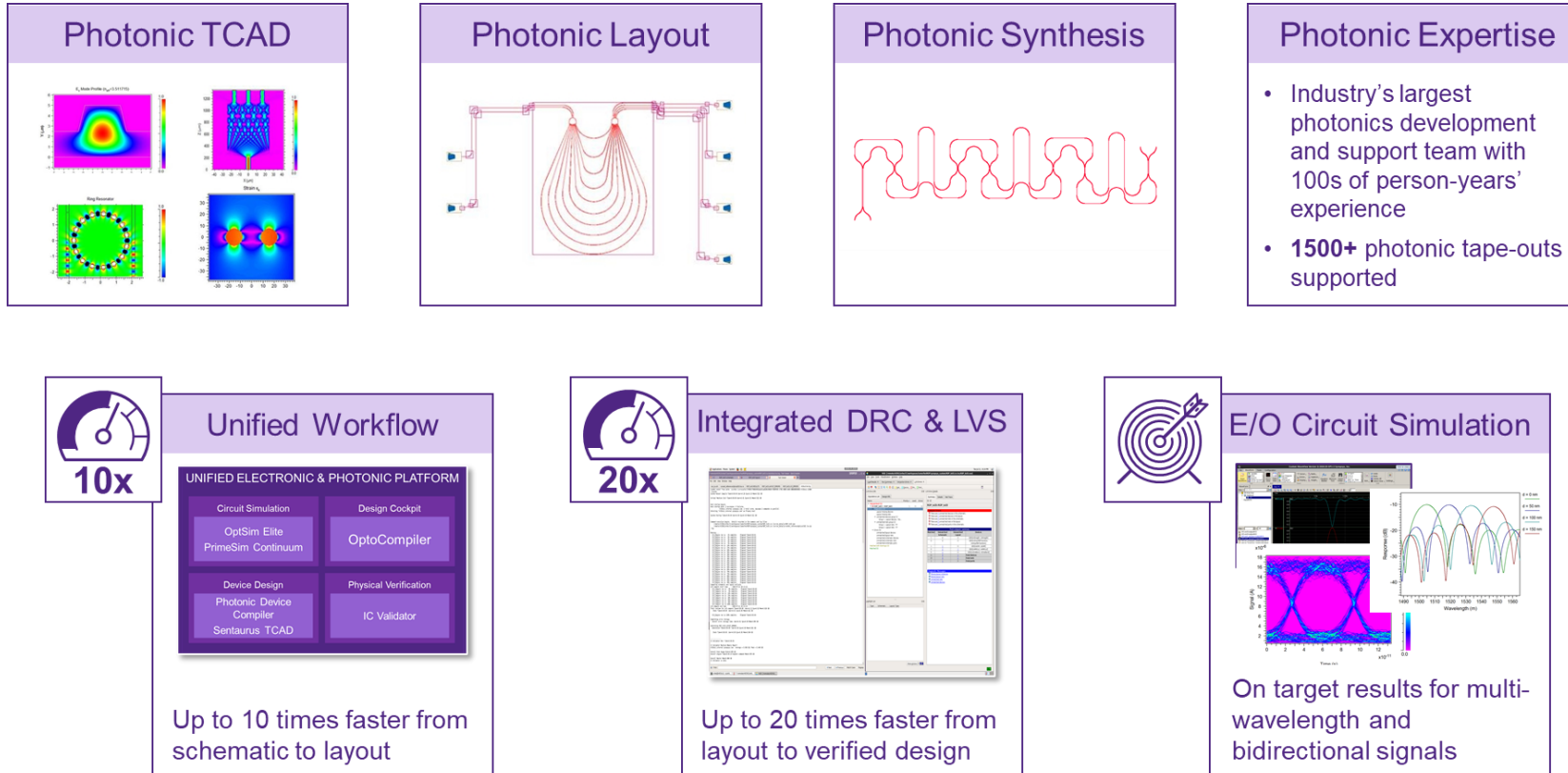
Results Analyzer and Waveform Viewer: E-O Waveforms



Summary



Synopsys' Differentiators Enable Fast & Accurate Results



"With the Synopsys platform, we were able to reduce the time from schematic entry to final test chip layout by nearly 4X over legacy tools," said Dr. Radha Nagarajan, CTO and SVP, Platforms at Inphi Corporation. "Due to its productivity features and ease of use, we have successfully used OptoCompiler for tape-outs."

"Rockley's unique photonic chipset technology with silicon photonics at its core is driving the growth of integrated optical components in healthcare, machine vision and data communications," said Andrew Rickman, chief executive at Rockley. "The PDA platform Rockley has created by utilizing OptoCompiler allows our engineers to define, simulate, lay out and verify Photonic ICs quickly and efficiently to meet our quality and schedule goals. Synopsys' technical support has been instrumental in ensuring Rockley met its tape-out goals. We look forward to additional efficiency gains by expanding our use of Synopsys' Photonic Solutions tools."

Thank You

