Hewlett Packard Enterprise

AN OPEN SILICON PHOTONICS ECOSYSTEM FOR COMPUTERCOM APPLICATIONS

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- SiPh ecosystem: Ashkan Seyedi (now at Nvidia)
- Process and verification: Peng Sun
- Design tools: Jared Hulme with Mentor Graphics and Lumerical
- 3D co-design: Jinsung Youn with Ansys/Lumerical
- PDK devices: Peter Rhim, Jinsung Youn, Jared Hulme
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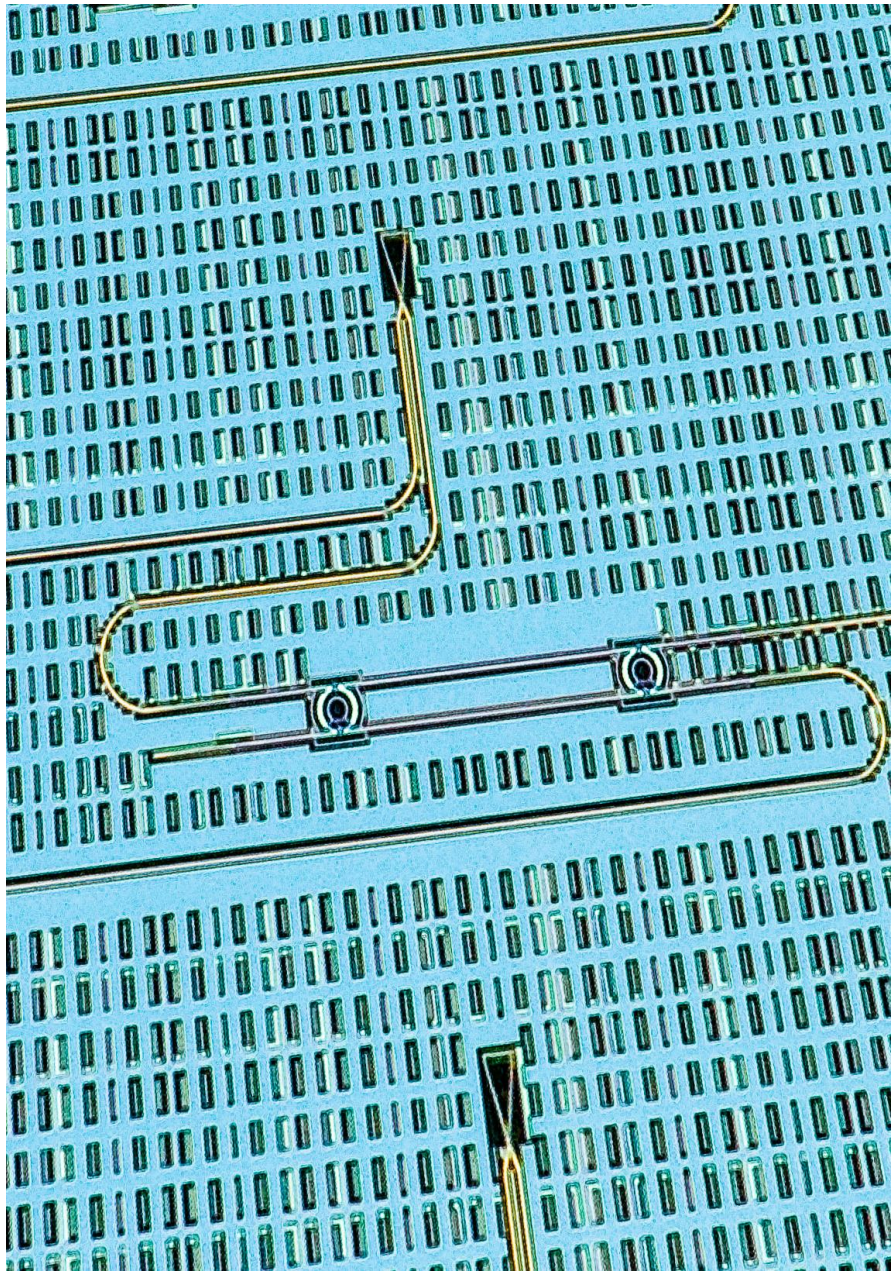
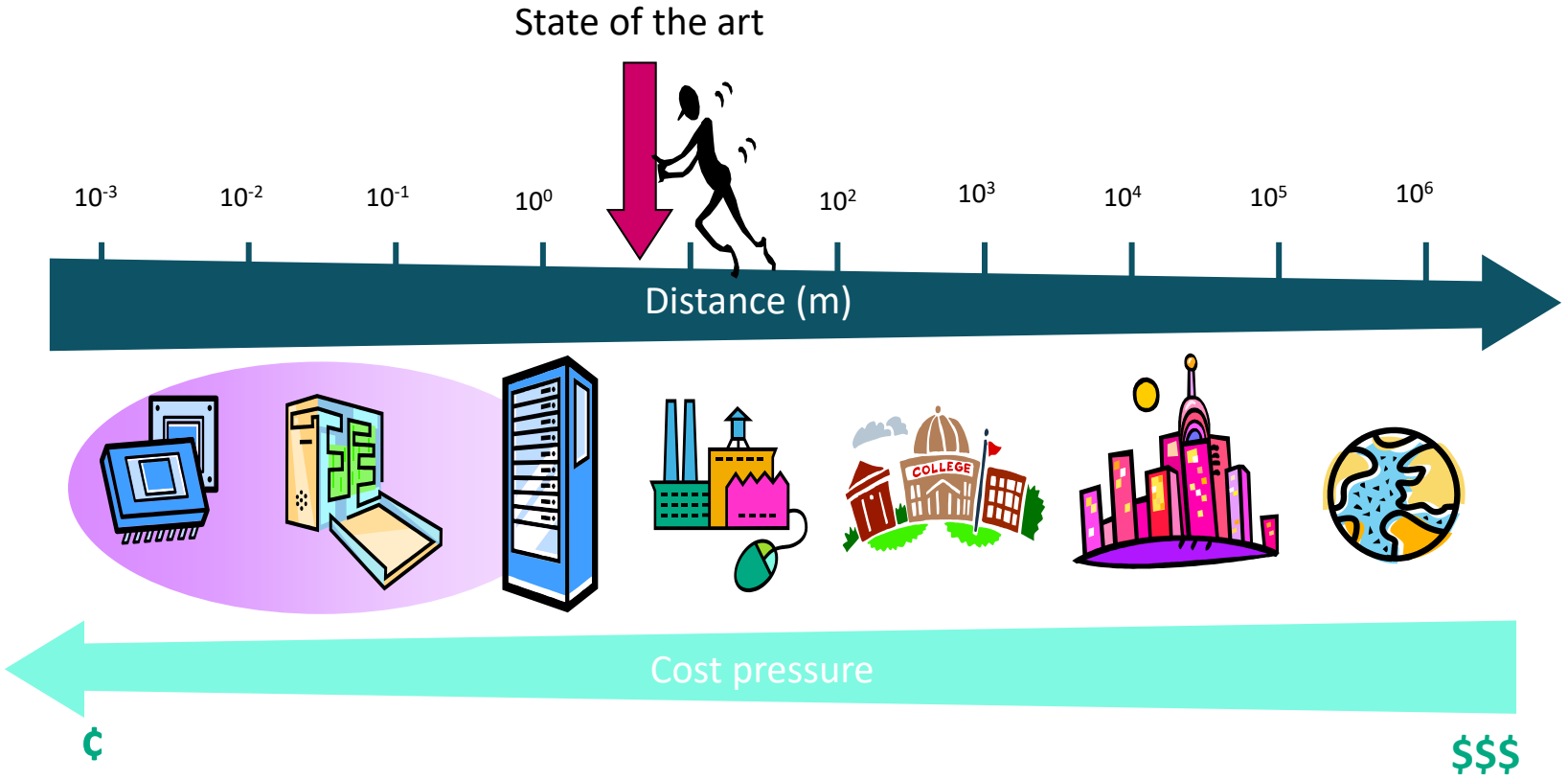
- Packaging: Sagi Mathai with US Conec



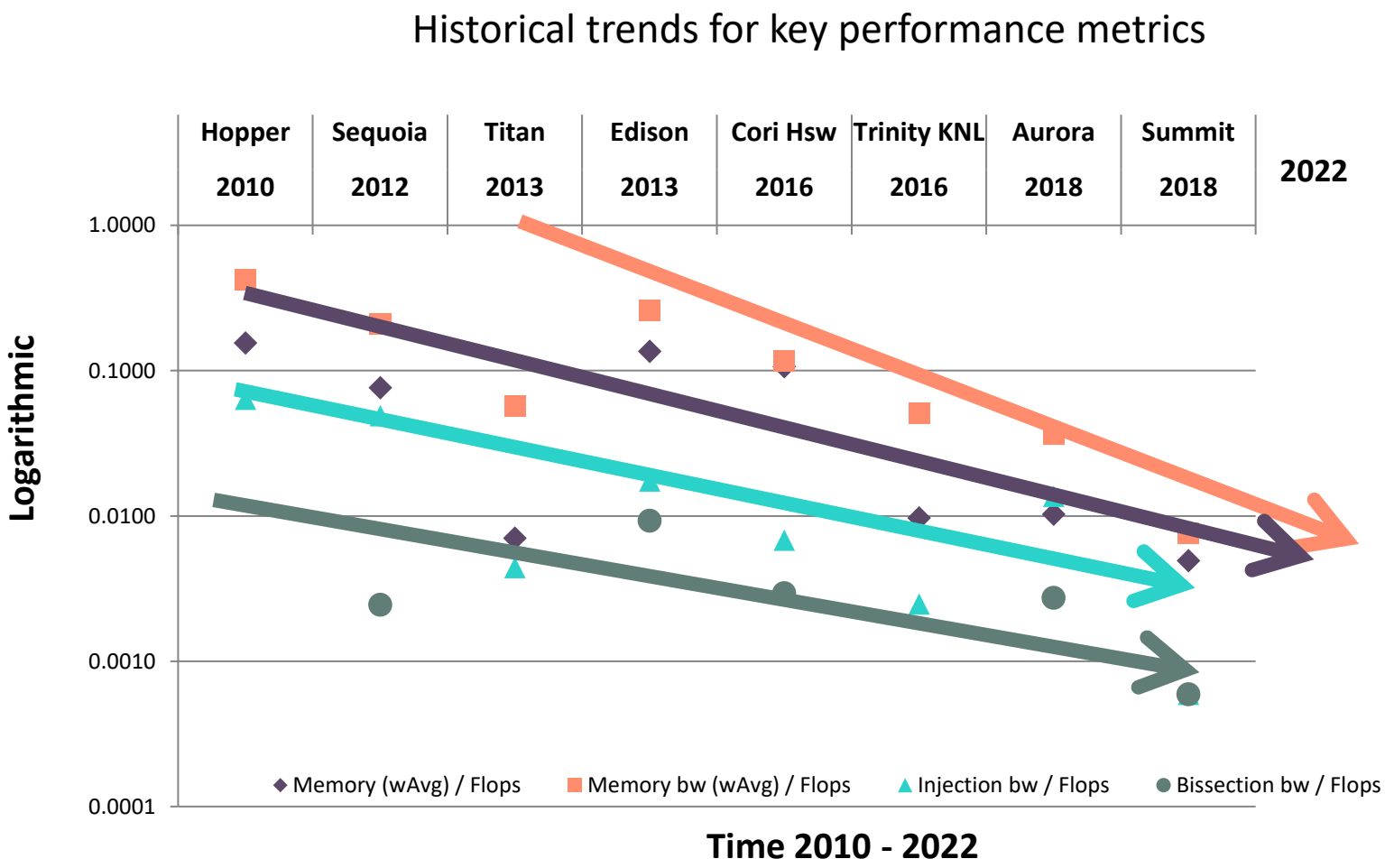
OPTICAL INTERCONNECTS



Advantages

More bits per “wire”	Less power per bit	Better signal integrity
New architectures		

SUPERCOMPUTER SYSTEMS TRENDS

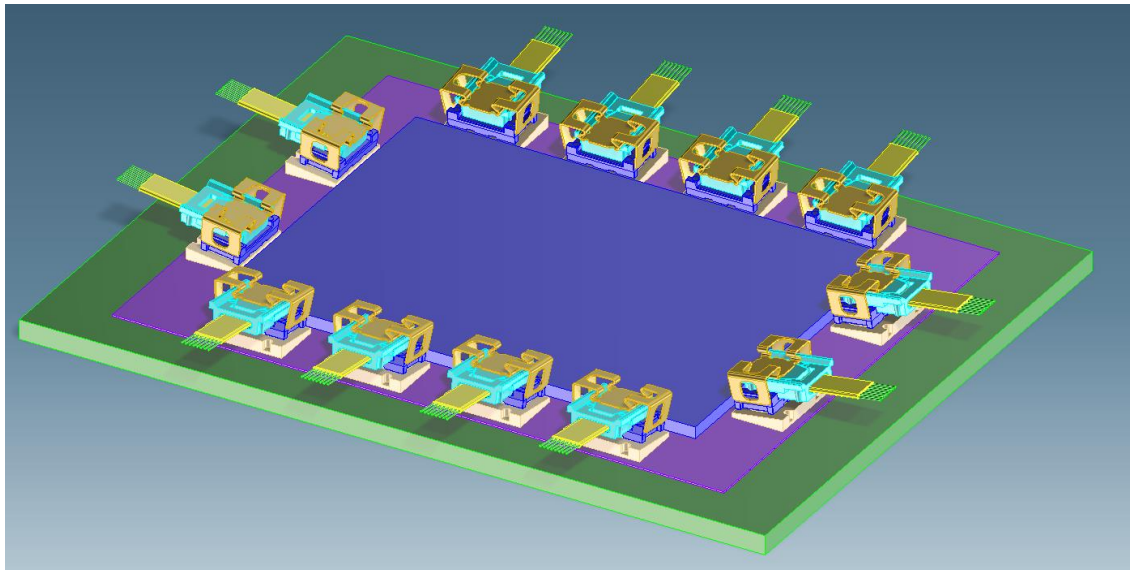


- **Balanced system architecture**
- **Memory-driven programming model**
- **Energy efficiency from chip to cooling tower**
- **Open architecture, open ecosystem**

..our ability to "service" the FLOPs is degrading

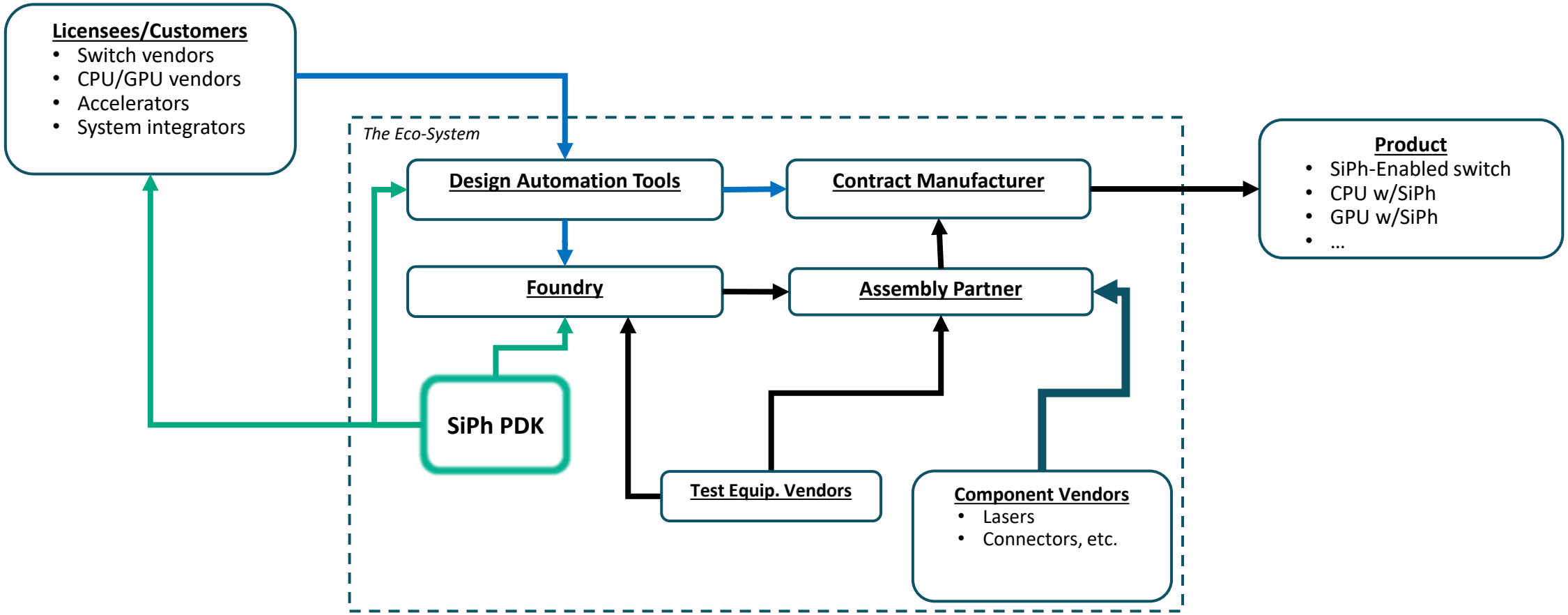
ECOSYSTEM REQUIREMENTS

- Current SiPh players own all the IP
  - “Vertical” model
  - Inefficient
  - High entry barrier
- “Horizontal” model
  - Licensable IP, off the shelf parts
  - Comprehensive catalog of tools, parts, and services
  - Quick time to market
- Targeted for high-volume
  - CPU, GPU, switch manufacturers
  - System integrators



A SILICON PHOTONICS ECOSYSTEM

How do we increase market penetration of SiPh?

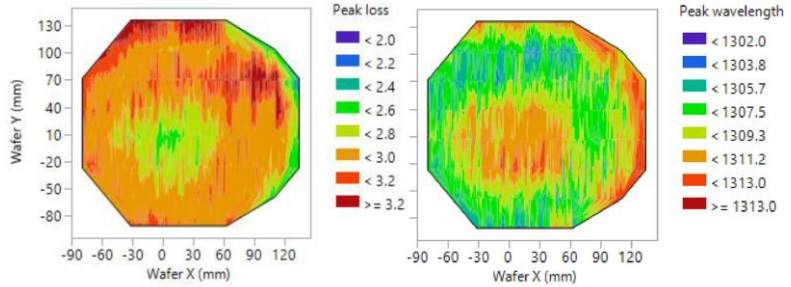


Fiorentino et al. "**An open Silicon Photonics ecosystem for computercom applications"** in Silicon Photonics IV, D. Lockwood and L. Pavesi eds. (in print)

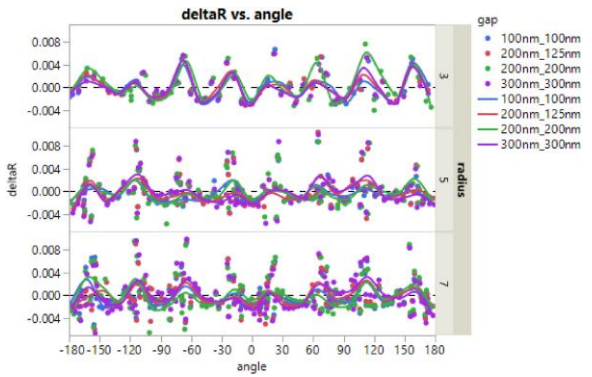
PROCESS & VERIFICATION

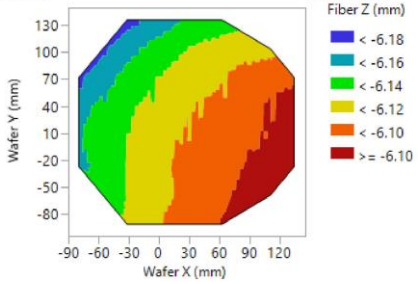
- Standard SiPh process
  - 300 mm wafers
  - 220 to 270 nm top silicon
  - 1-3 µm BOX
  - 3-4 etches
  - Implants
  - Ge process for PDs
- Expansion
  - Ge APD process
  - Laser heterogeneous integration
- Need reproducible results!
  - Parameter control
  - Verification

Grating properties

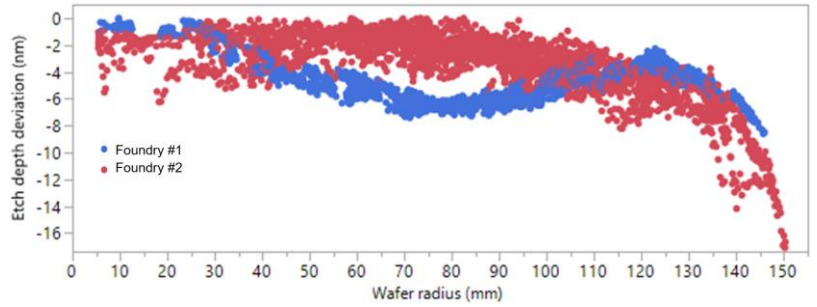


Sidewall roughness





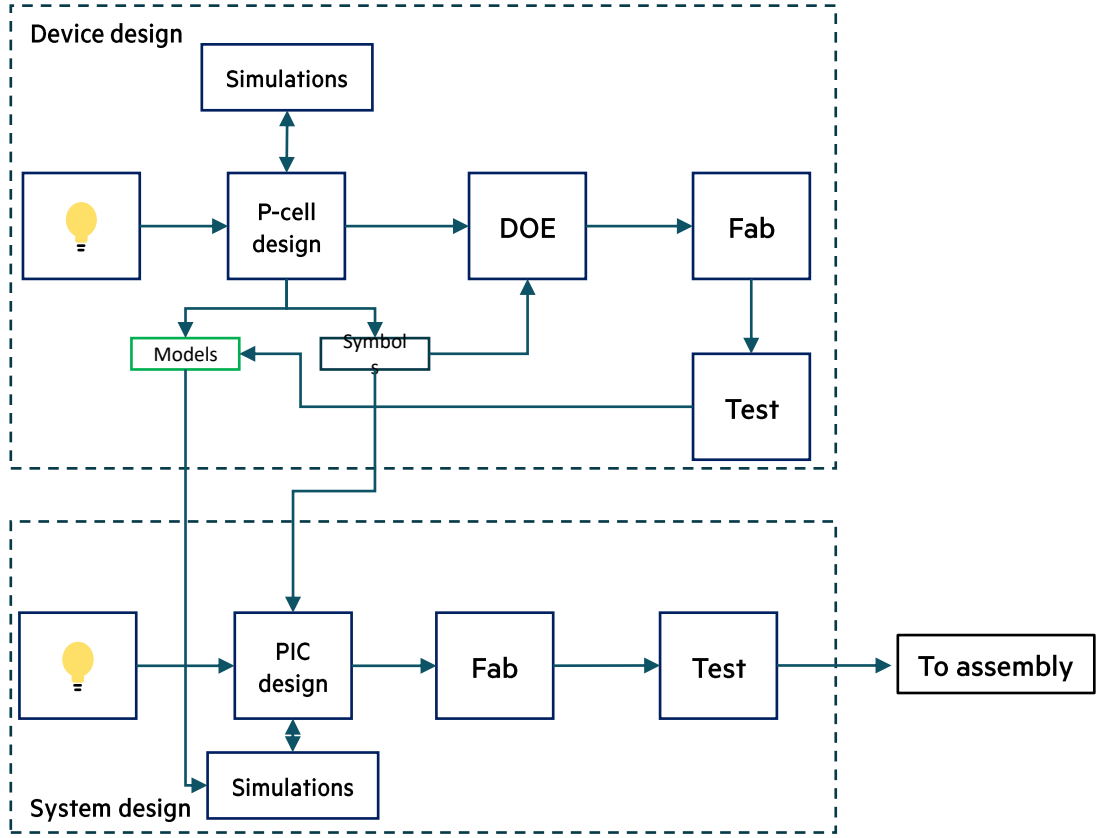
Etch dept control

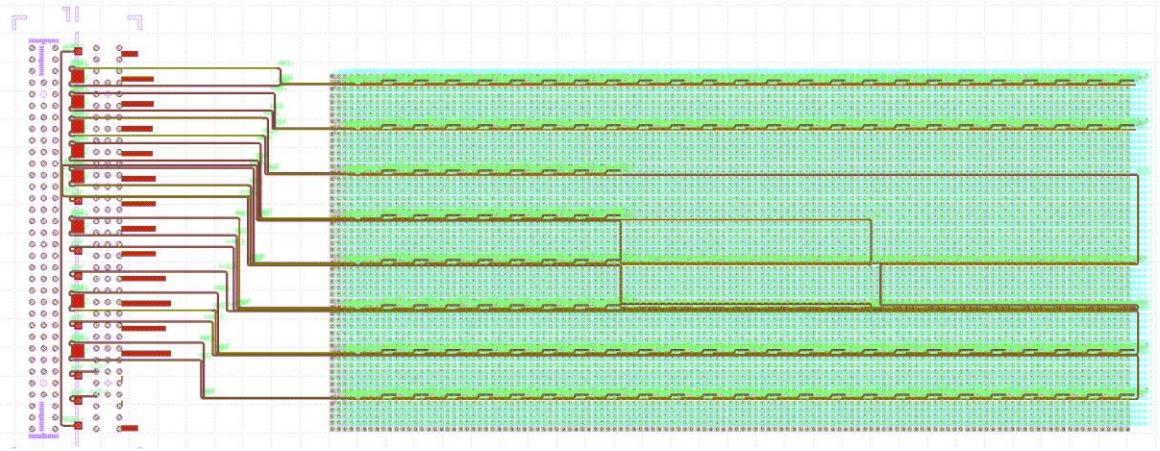


Sun, Peng, et al. "**Statistical behavioral models of silicon ring resonators at a commercial CMOS foundry**." IEEE Journal of Selected Topics in Quantum Electronics 26.2 (2019): 1-10.

DESIGN TOOLS

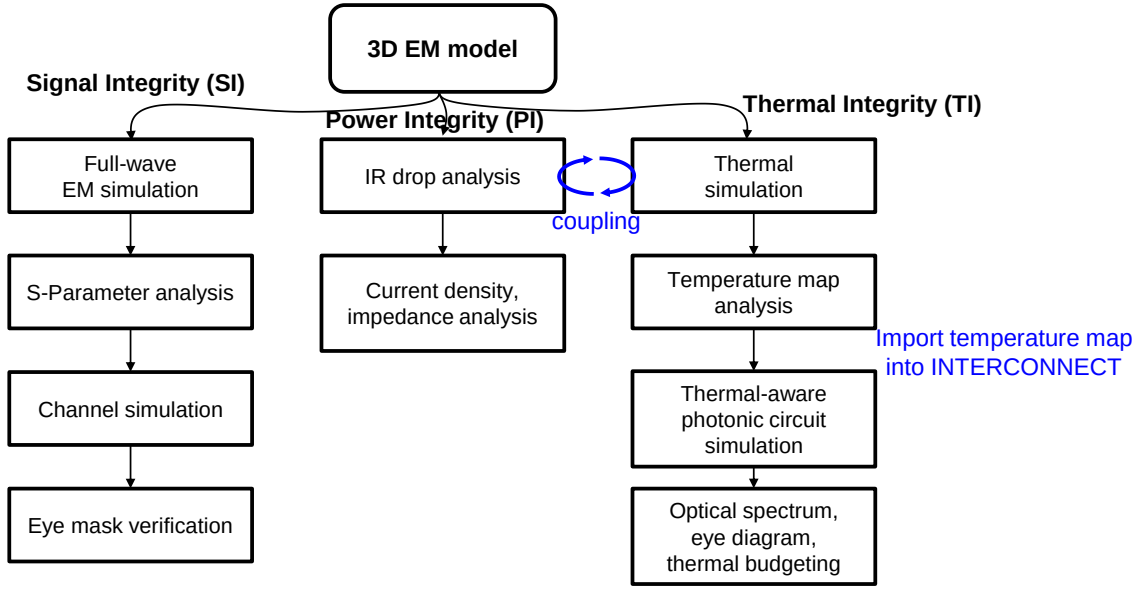
- Separate design cycles
- Device design tools
  - Required for photonics engineers
  - Python-based p-cells
  - Create symbols and models for system designers
- System design tools
  - Facilitate use for non-experts
  - Automated place and route
  - Integrated simulations
  - LVS

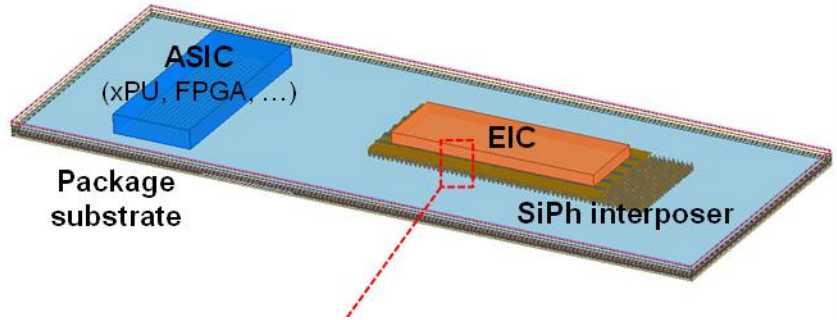


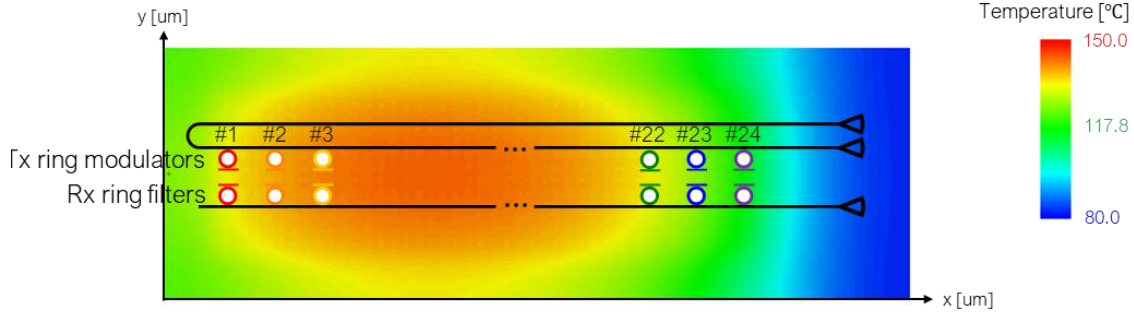


3D INTEGRATION CO-SIMULATION

- Co-Design Methodology for Silicon Photonics 3D IC
  - SI/PI using Ansys Electronics
  - also supports IR-Drop simulation
- Showed Thermal-Aware Photonic Circuit Simulation
  - Thermal Simulation using Ansys Icepak
  - Photonic Circuit Simulation using Ansys Lumerical INTERCONNECT
- Eliminate Design Issues in the Early Design Stages



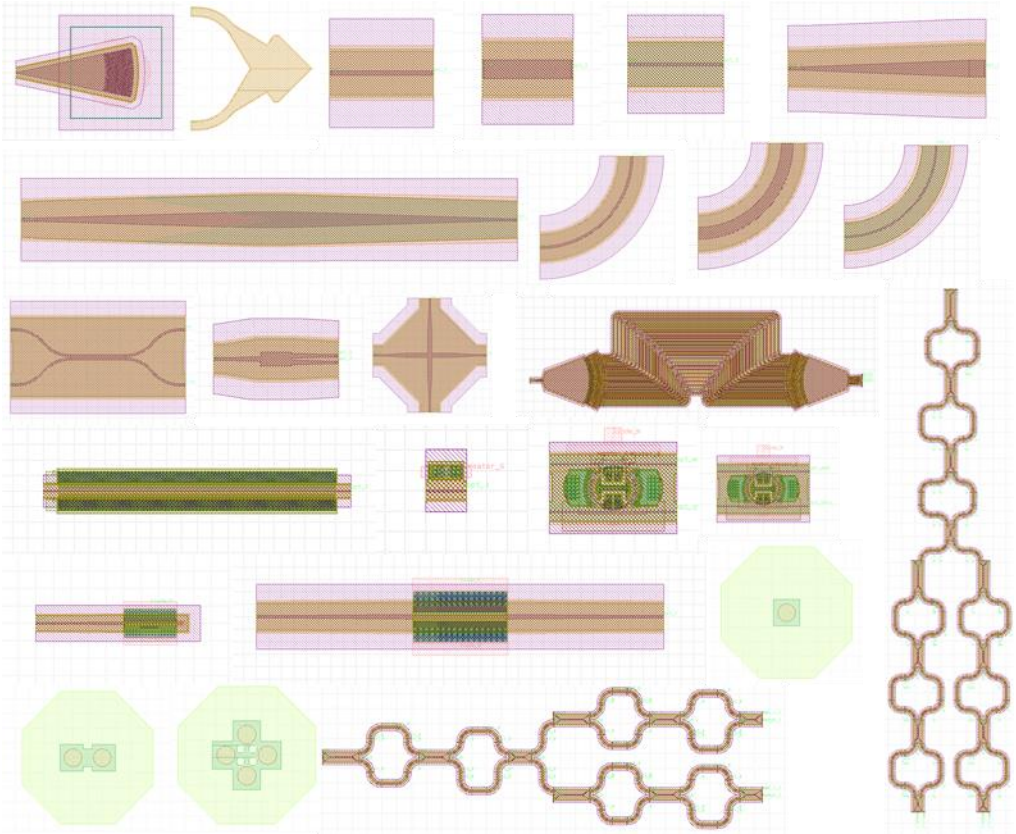




Jinsung Youn **"Electronic-Photonic IC Co-Design with Signal/Power Integrity and Thermal Simulation for Silicon Photonics 3D IC"** in DesignCon 2021.

DEVICES

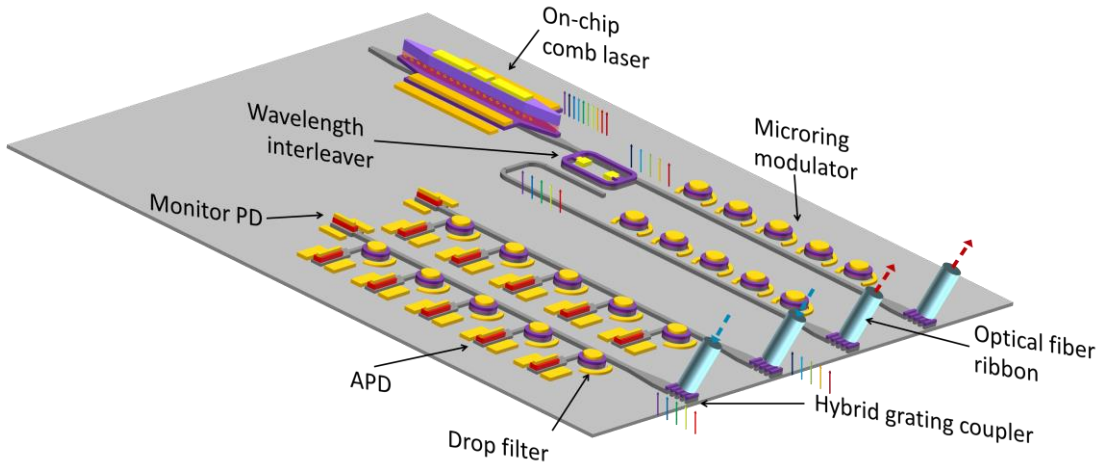
- Initial offering
  - Short- and long-reach WG
  - Transitions, splitters, and crossings
  - Gratings and edge couplers
  - AWG, interleaver and ring filter
  - Bias diode and heater
  - PIN and PN ring modulators
  - Ge PDs
  - TSV-ready
- Additions
  - Ge APDs
  - Integrated lasers



LASERS

Laser integration

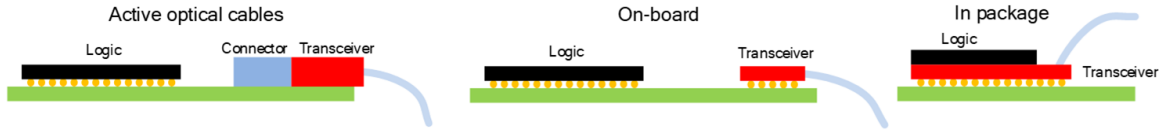
- Off-chip
  - Currently available
  - Field-replaceable unit
  - Comb lasers available
  - Expensive (~US$100/laser)
- On-chip
  - Adopted by some players
  - Lower cost (~US$10/laser)
- Heterogeneously integrated
  - Lowest cost (>US$0.1/laser)
  - Integration flow requires buy-in from foundries
  - Single point of failure/requires redundancy

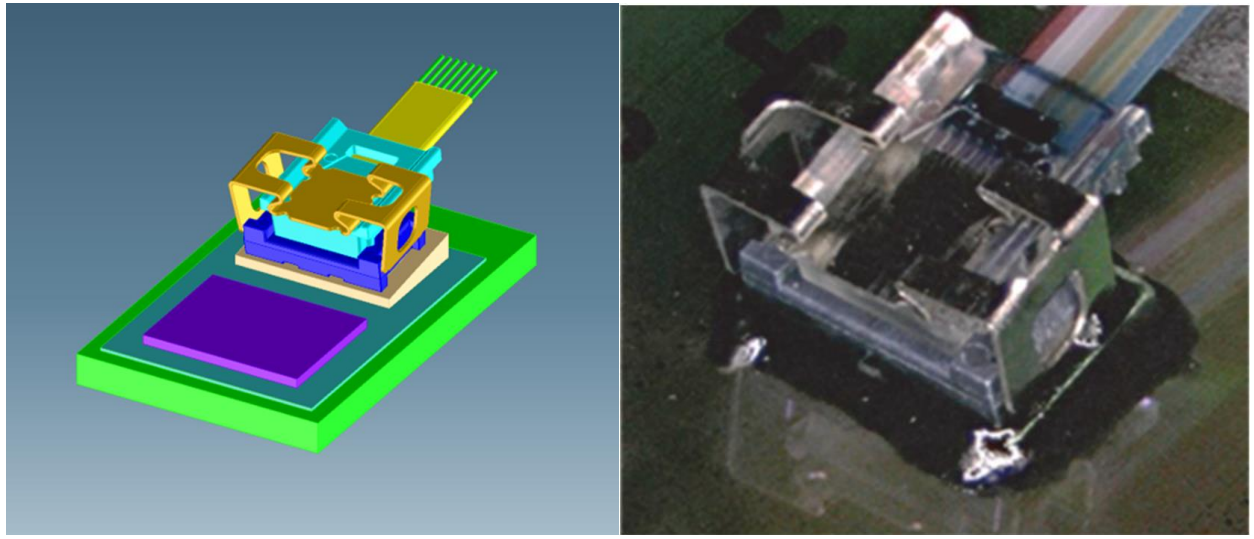


PACKAGING

Packaging evolution

- Front panel
  - Current solution
- On-board
  - Saves cost/power
  - Eliminates front panel BW bottleneck
- In-package
  - Further reduces cost/power
  - Eliminates pin BW bottleneck
  - Requires severable fiber attach
  - Requires TSVs
- Packaging has still a lot of issues
  - Develop photonics techniques that are robust
  - Adapt packaging to be compatible

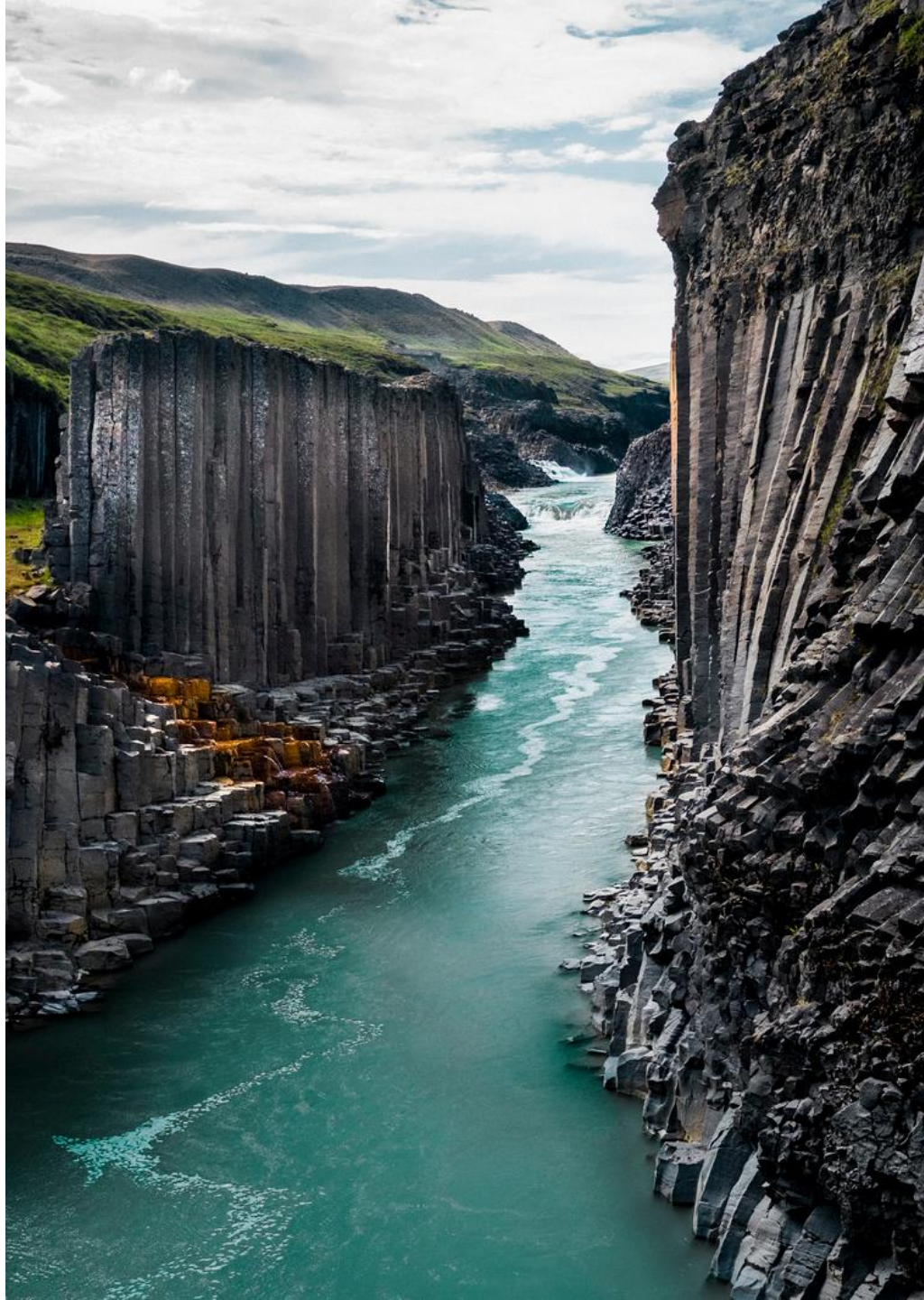


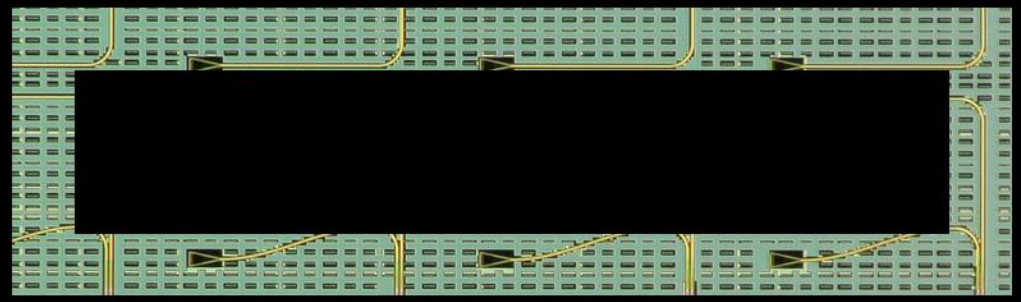


FUTURE WORK

Still much work to do!

- Continued technology improvement
  - At-scale demo of TSVs
  - Expand device portfolio with active components and APDs
  - Improve chip packaging
  - Develop high fiber count connectors
- Simplify supply chain
  - Consolidate suppliers
  - Simplify processes
- Continue recruiting partners/users





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