Design of Heterogeneous Chips - Chiplets and System Considerations

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Outline

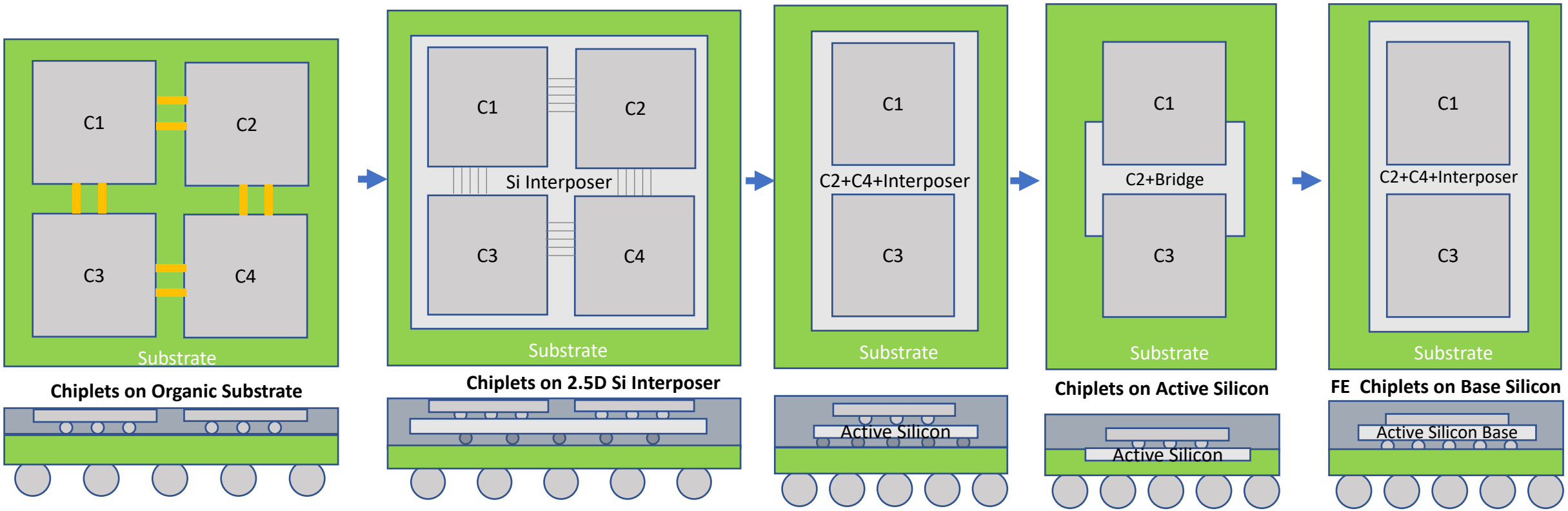
1. Chiplets
   - Heterogeneous Integrated Circuits with Chiplets
   - Chips vs Chiplets
   - Chiplet Models
   - Early-stage architecture and design For heterogeneous IC designs

2. Design of Heterogeneous ICs
   - Design Steps and Workflow
   - Power Mechanical and Thermal

3. System and Technology Co-optimization
   - Requirements for System Design Kits

4. Summary

Integrated Circuits With Chiplets

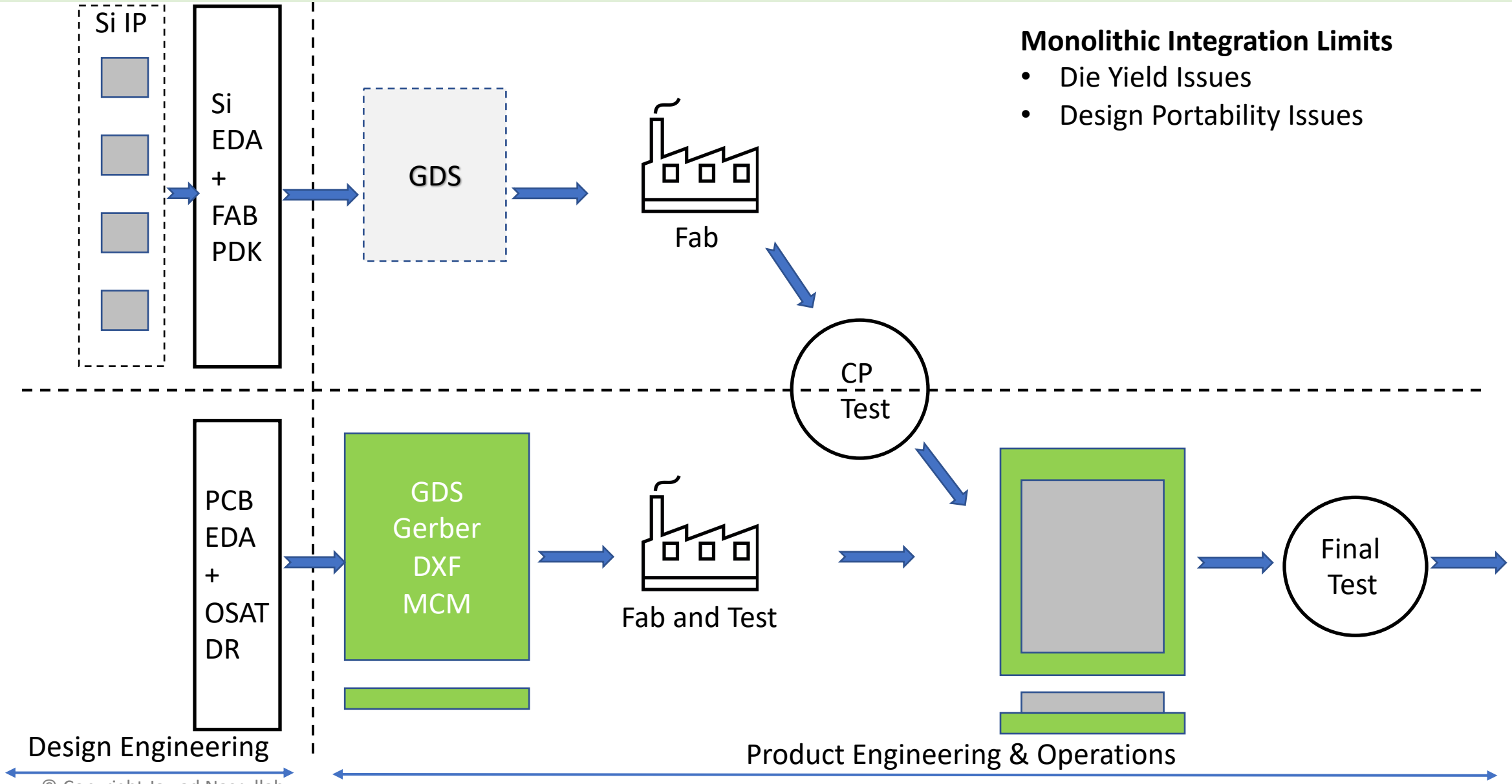


Chiplet on Organic	2.5D Chiplets	Active Interposer	Si Bridges	FE Chiplets
Substrate/Fanout, Si (--)	Si, Substrate/Fanout (++)	Si, Substrate/Fanout (++)	Substrate/Fanout, Si (-)	Si, Substrate/Fanout (++)
$	$$$	$	$$	$
Value	Value++	Value++	Value+	Value+++

Chips vs Chiplets

	Chips	Si Hard/Soft IP	Chiplets
State	Physical Goods	IP	Physical Goods
Trading	Buy/Sell with Warranty	Buy/Sell with Warranty	Buy/Sell with Warranty
Warranty	Warranty for DPPM	N/A	Warranty for DPPM
2L Assembly	SMT Capable	N/A	SMT or Wire-bond
Packing	Tape & Reel	N/A	Tape & Reel or Wafer Sale
Verification	Verified by Vendor	Supply verification models	Supply verification models
Testing	Testable by Manufacturer. Some have JTAG boundary scan.	N/A	Testable by Customer. Need boundary scan at least.

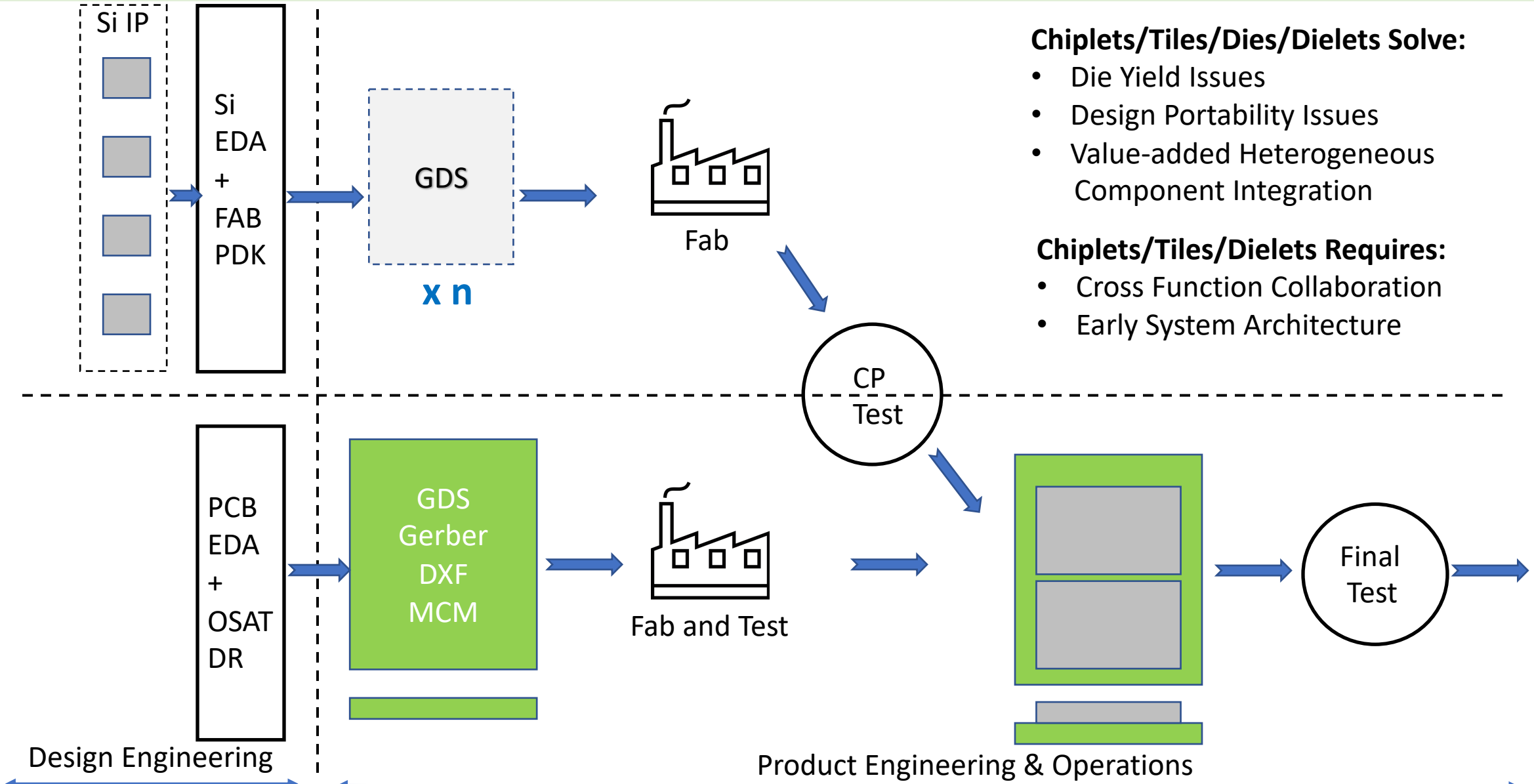
Chips vs Chiplets



Monolithic Integration Limits

- Die Yield Issues
- Design Portability Issues

Chips vs Chiplets



Chiplets/Tiles/Dies/Dielets Solve:

- Die Yield Issues
- Design Portability Issues
- Value-added Heterogeneous Component Integration

Chiplets/Tiles/Dielets Requires:

- Cross Function Collaboration
- Early System Architecture

Chiplet Models

Models	Chips	Si Hard/Soft IP	Chiplets
Mechanical	Data Sheet	N/A	MCM, DIE, XDA, AIFF, LPB, ZEF, GDS, Gerber, DXF
Thermal	Data Sheet	N/A	ECXML
Behavioral	Data Sheet	Verilog/System C	Verilog/System C/Data Sheets/ESL
IO	Data Sheet	Verilog A/AMS	IBIS
Electrical	Data Sheet	Data Sheet	Machine Readable SOA/EC Tables
PI/SI	Data Sheet/CPM		CPM
Test	Data Sheet/JTAG	Verilog	IEEE 1149.1/1149.6/1500/1838/…

Design and Manufacturing Steps—Chips / Chiplets

DESIGN STEPS

1- Architecture

2- Design
- IO Planning
- RTL Design and Verification
- Schematic Capture
- DFT/BIST

3- Chip Layout / Routing / Package Layout

4- Verification
- Functional/Formal
- Electrical
- Thermal/Structural

5- Send to Manufacturing

MANUFACTURING STEPS

1- Wafer Fab, Contact Probe

2- Substrate Fab, e-test

3- uBump/Assembly/CSP/BGA

4- Packaged Part Test

5- ESD and Latchup Tests (sampling)

6- Reliability Tests (sampling)

7- Infant Mortality Burn-in

8- Final Test

Design and Manufacturing Steps—Chiplet Integration

DESIGN STEPS

1- Architecture, Chiplet selection/design, Package Technology Selection

2- Design
- IO Planning
- RTL Design and ESL Verification
- Schematic Capture/Netlist Gen
- Component Placement

3- Substrate/Interposer Routing and Layout

4- Verification
- Thermal
- Functional
- Electrical

5- Send to Manufacturing

MANUFACTURING STEPS

1- Interposer Fab, Contact Probe

2- Substrate Fab, e-test

3- Chiplet Assembly/Packaging

4- Package System Level Test

5- ESD and Latchup Tests

6- Reliability Tests

7- Infant Mortality Burn-in?

Development Activities for Chiplet Integration

Architecture

Choose Multi-Die Technology
Choose Chiplets and Signaling
Cost Analysis
Performance Modeling
Early Power Estimation
Choose A Thermal Solution
Design For Structural Integrity
Design For Testing
System Level Test Development

Design

Multi Die Design
System Connectivity
Power Delivery Integrity
Signal Integrity
Cross-Die Timing
Noise Analysis, EMI, IR, XTalk
Detailed Power Model
Thermal Analysis
Structural Analysis
Verification
Design Sign Off

Manufacturing

Wafer Probe
Organic Material Testing
Bring Up Testing
System Level Test
Environment Reliability
Later Life Failure Testing
HVM

Power, Mechanical, and Thermal

“Power Is Everything”

Power Profile	10^{-1} W	10^{0} W	10^{1} W	10^{2} W	10^{3} - 10^{5} W	10^{6} W
Applications	AIoT, Trackers, Wearables	Mobile	Laptops Pads	Servers	Racks	Data Centers
Energy Efficiency Challenge	✓	✓	✓	✓	✓	✓
Thermal Design Challenge		✓	✓	✓	✓	✓

Chip Active Power Top Usage: IO/SerDes/Optical/RF, Compute, Storage

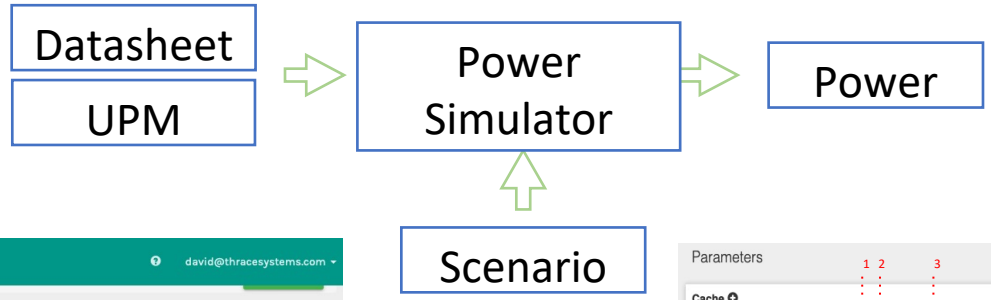
Chip Static Power Top Usage: Transistor Leakage, DC Biasing

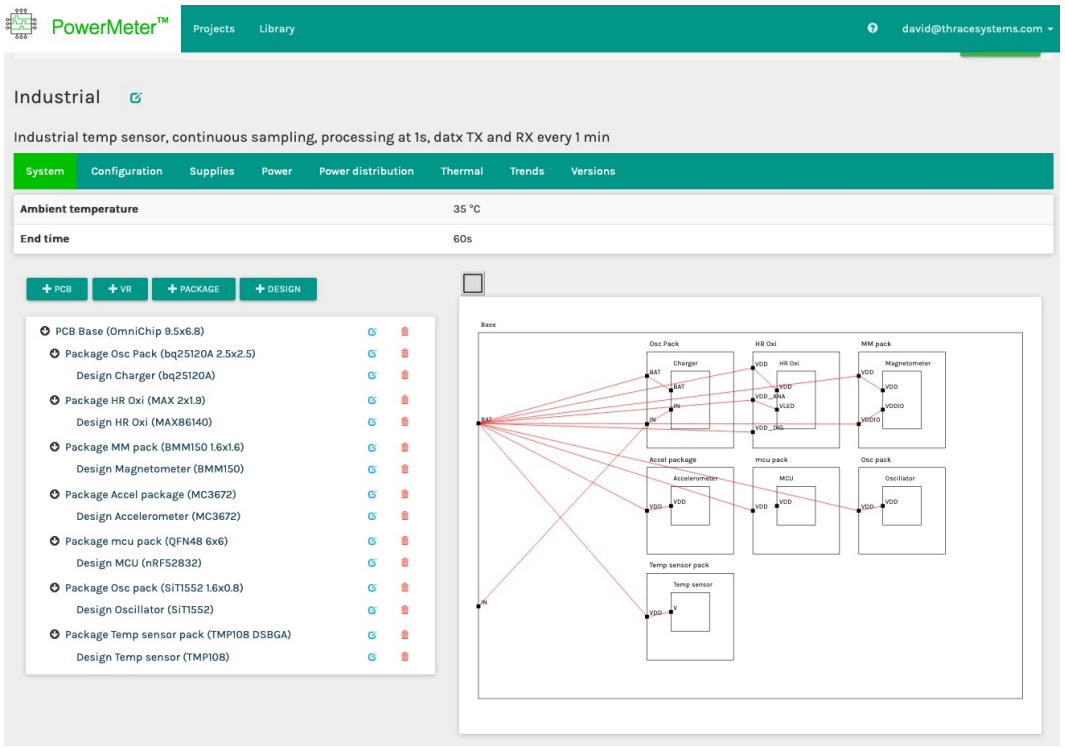
Chip Thermal Design Range: 1mW-1000W

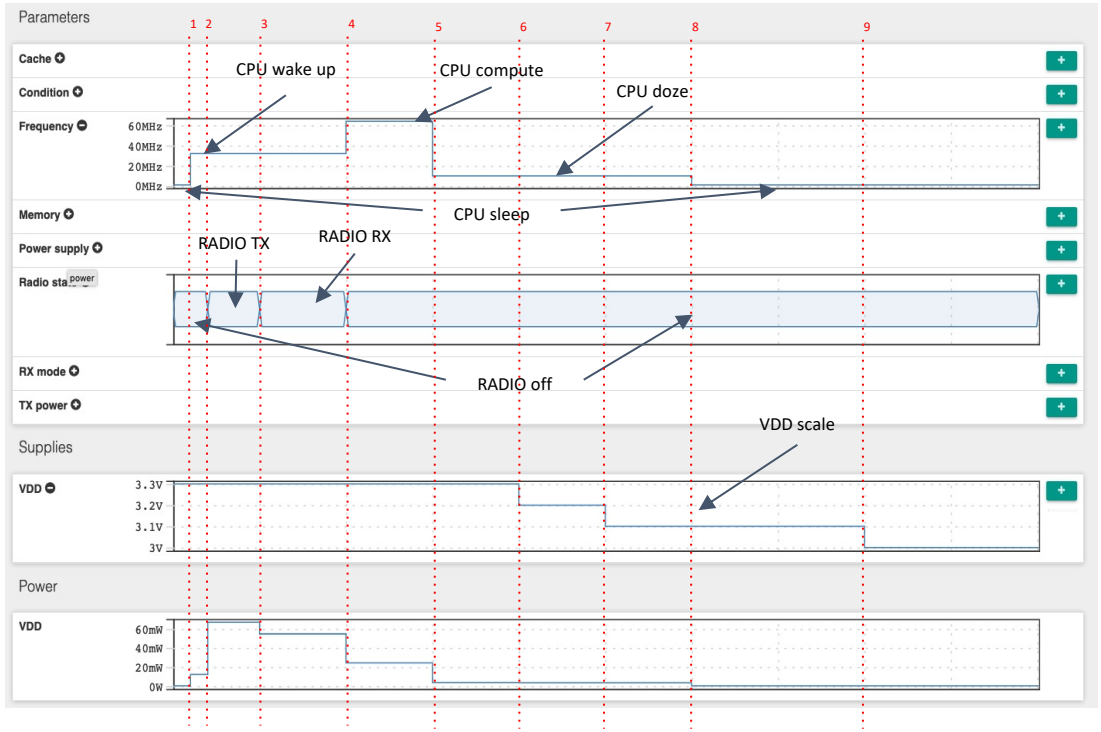
Chiplet System Power Estimation

OPEN DOMAIN SPECIFIC ARCHITECTURE

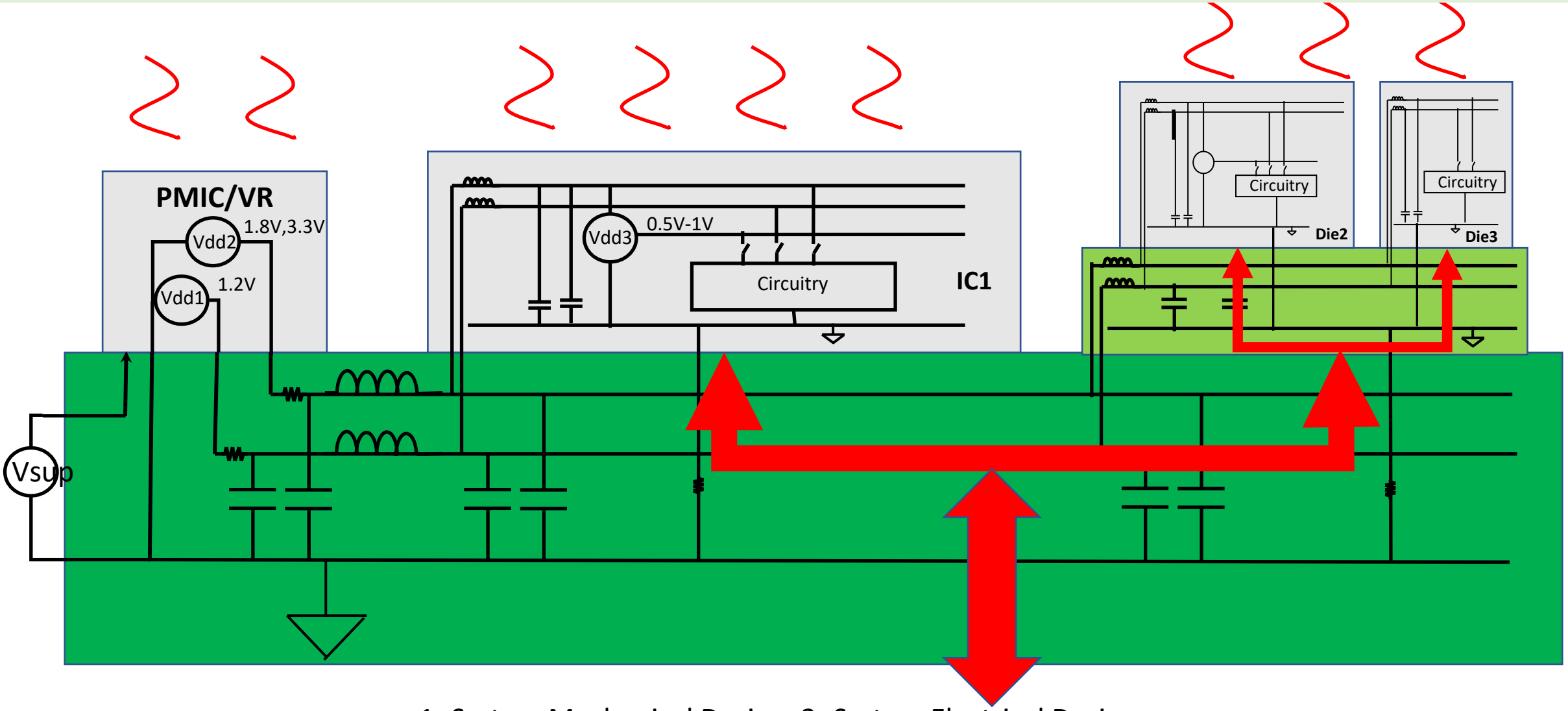
CDX







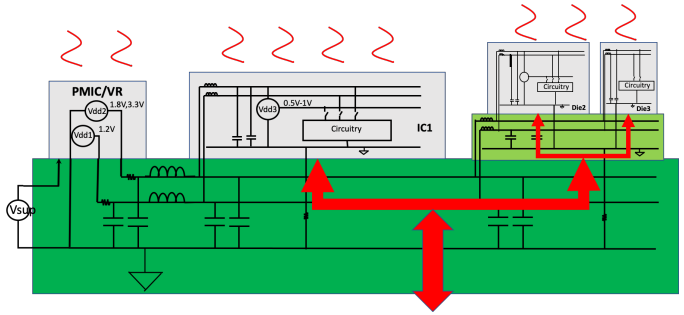
Design for Chiplet Based Systems



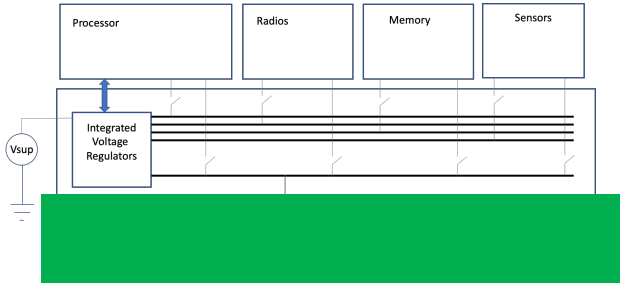
1- System Mechanical Design 2- System Electrical Design

Need for Early Power Modelling

- Side-by-Side Placement (Cheaper and Good-Enough Performance)
  - Easier Shrink of the System (Improves IO Power Dissipation somewhat)
  - Critical Dimensions Shrinking (cost advantage)

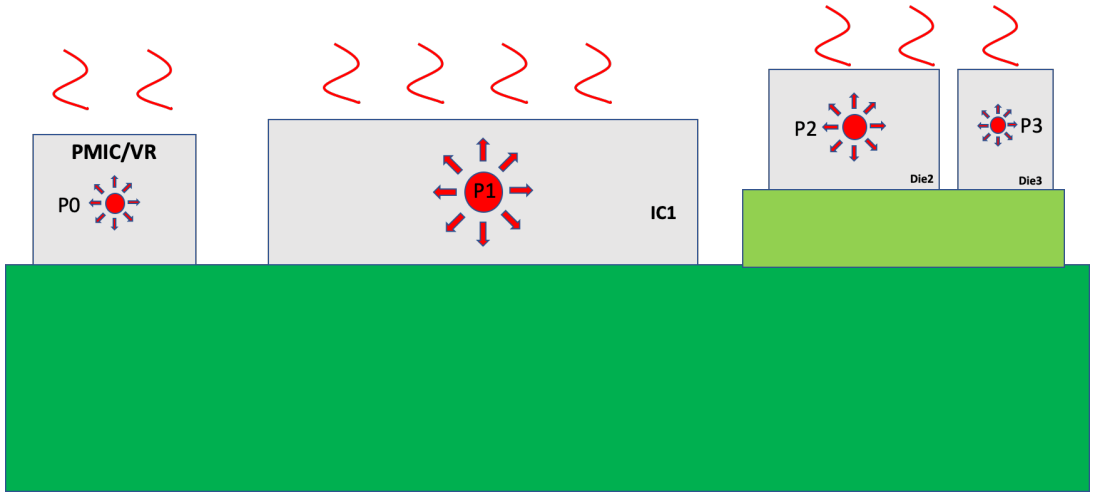


- Vertical Stacking (New Technologies)
  - Vertical Interconnect (Significantly Improves performance and power)
  - Vertical Power Management (Significantly Improved Co-designed Power Management)



Mechanical and Thermal Design

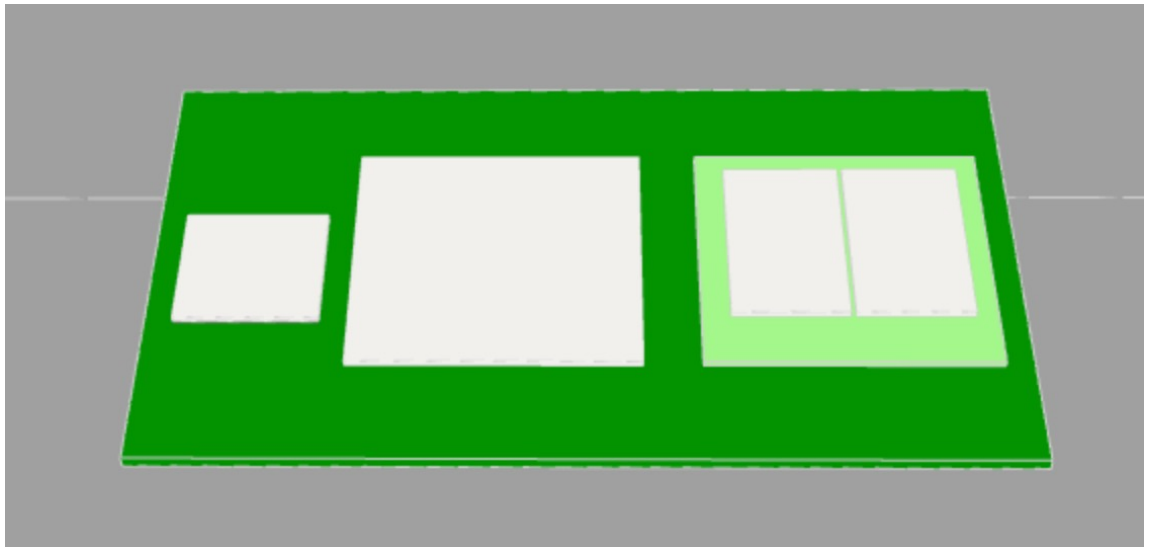
- Thermal and Floor planning
  - Technology Selection
  - Vertical OR Side-by-Side Integration



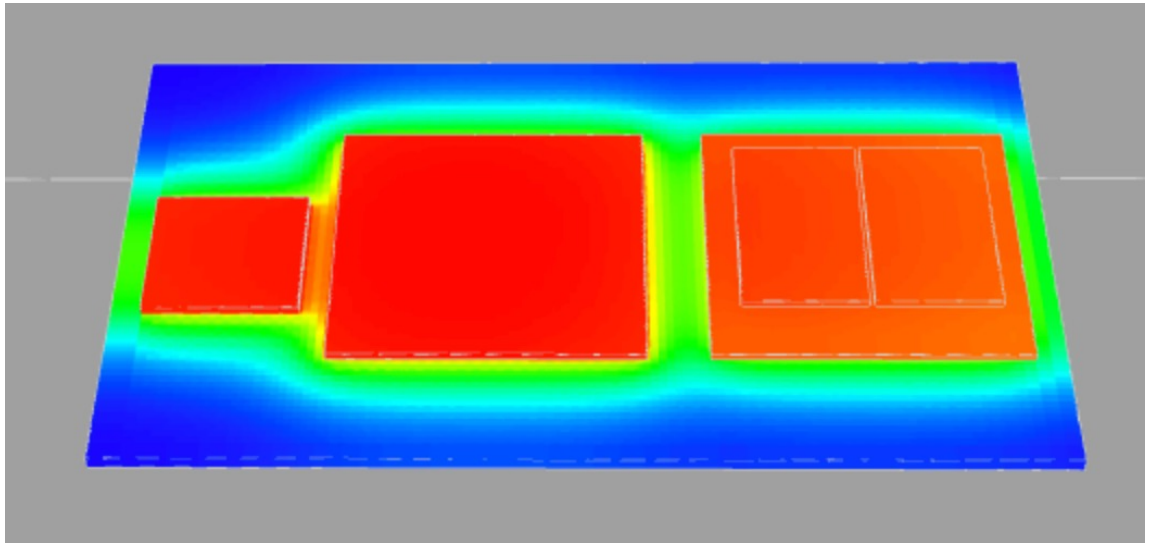
- Power Dissipation Design
  - Heat Spreader, Heat Sink Design
  - Accurate power model is needed for accurate power model (recursive)

  (Leakage model depends on temperature which depends on accurate leakage model among others)

Mechanical and Thermal Design

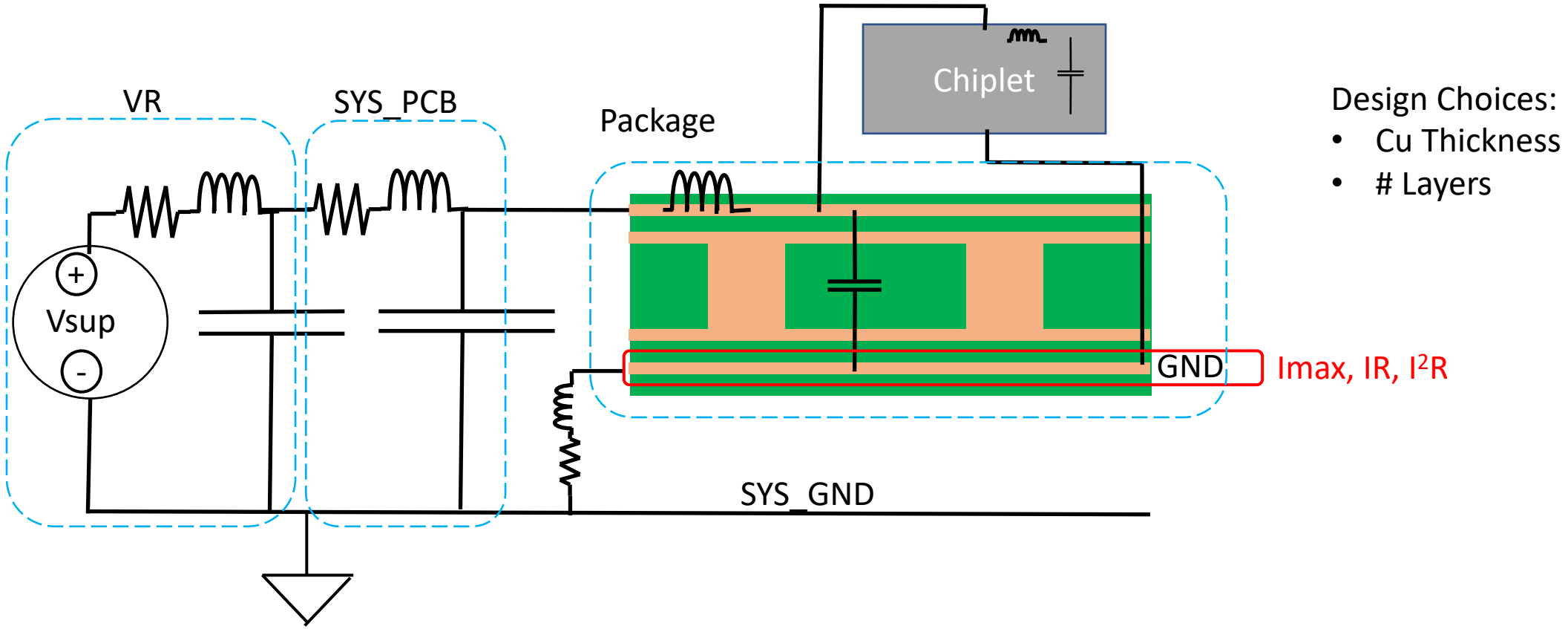


Courtesy: Anemoi Thermal Solver
Anemoisoftware.info



Thermal Cross Talk and Desensitization
Thermal Run Away
Architecture Power Modulation
Package DVFS

Power Delivery Network Design

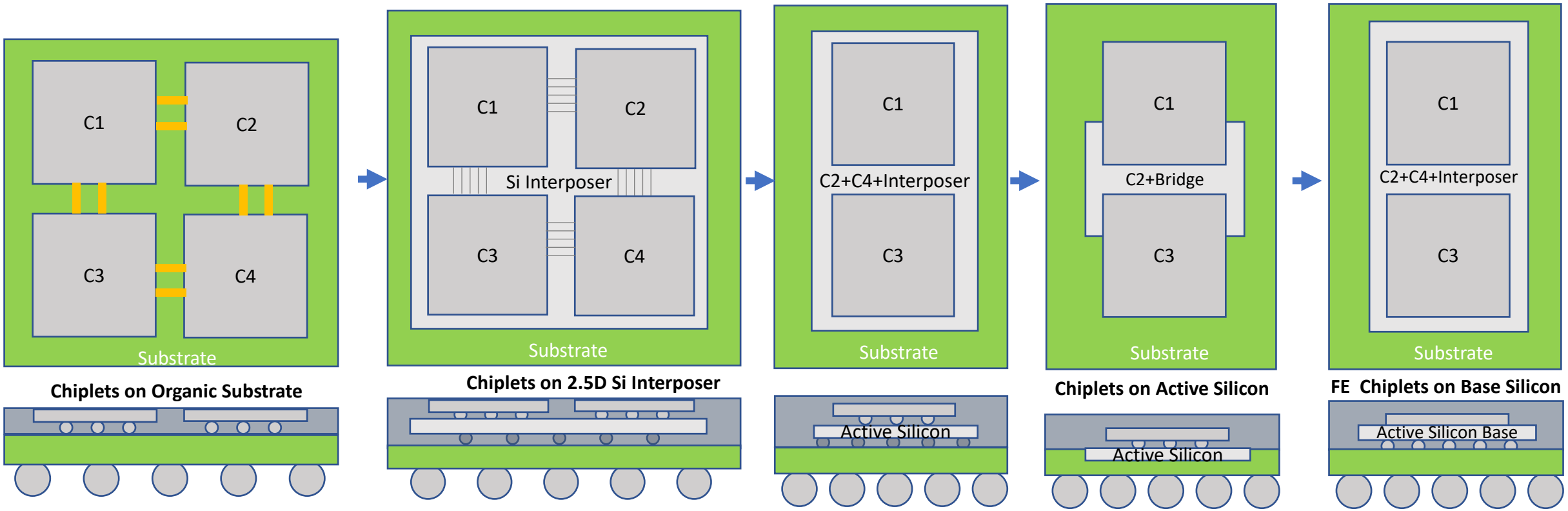


Design Choices:
- Cu Thickness
- # Layers

- Ground and Power Planes Need to Support IR, I^2R, Droop. Decoupling Capacitors help Volage Droop.
- Cu Thickness Helps IR.
- Little Room for Overdesigning.

System Design and Technology Co-optimization

Design Automation Needs



Chiplet on Organic	2.5D Chiplets	Active Interposer	Si Bridges	FE Chiplets
Chiplet PDK	Chiplet and Interposer PDK	Chiplet and Interposer PDK	Chiplet and Bridge PDK	PDK
Assembly DK	Assembly DK	Assembly DK	Assembly DK	
Package DK	Package DK	Package DK	Package DK	

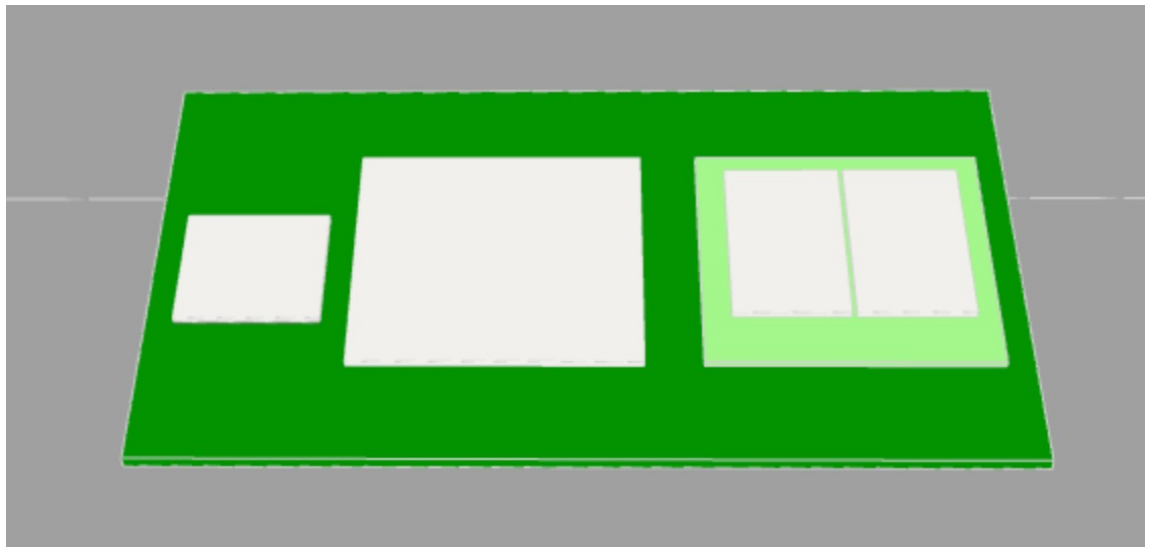
Requirements For Design Kits

Fab Process Design Kits:

- DRC, LVS, Extraction R,C Rulesets
- Spice Models
- Derivative collaterals (IO, ESD, Library, Timing, Power, Bumping, Stacking Cu-Cu)
- DFM

Package Rule Sets:

- R, L, C Extraction
- Impedance Estimation
- S-parameter Estimation
- Thermal Design Rules (Material Dk, Df, K, c)
- Structural Analysis Rule (Modulus, Tg)



Assembly Rule Sets:

- Chiplet Spacing
- Clearances
- Stack-up Artwork Rules
- Assembly Warpage
- Die pad shrink
- TXV Rules
- Wire-bond Rules
- Molding Rules
- Underfill Rules
- DFM Rules

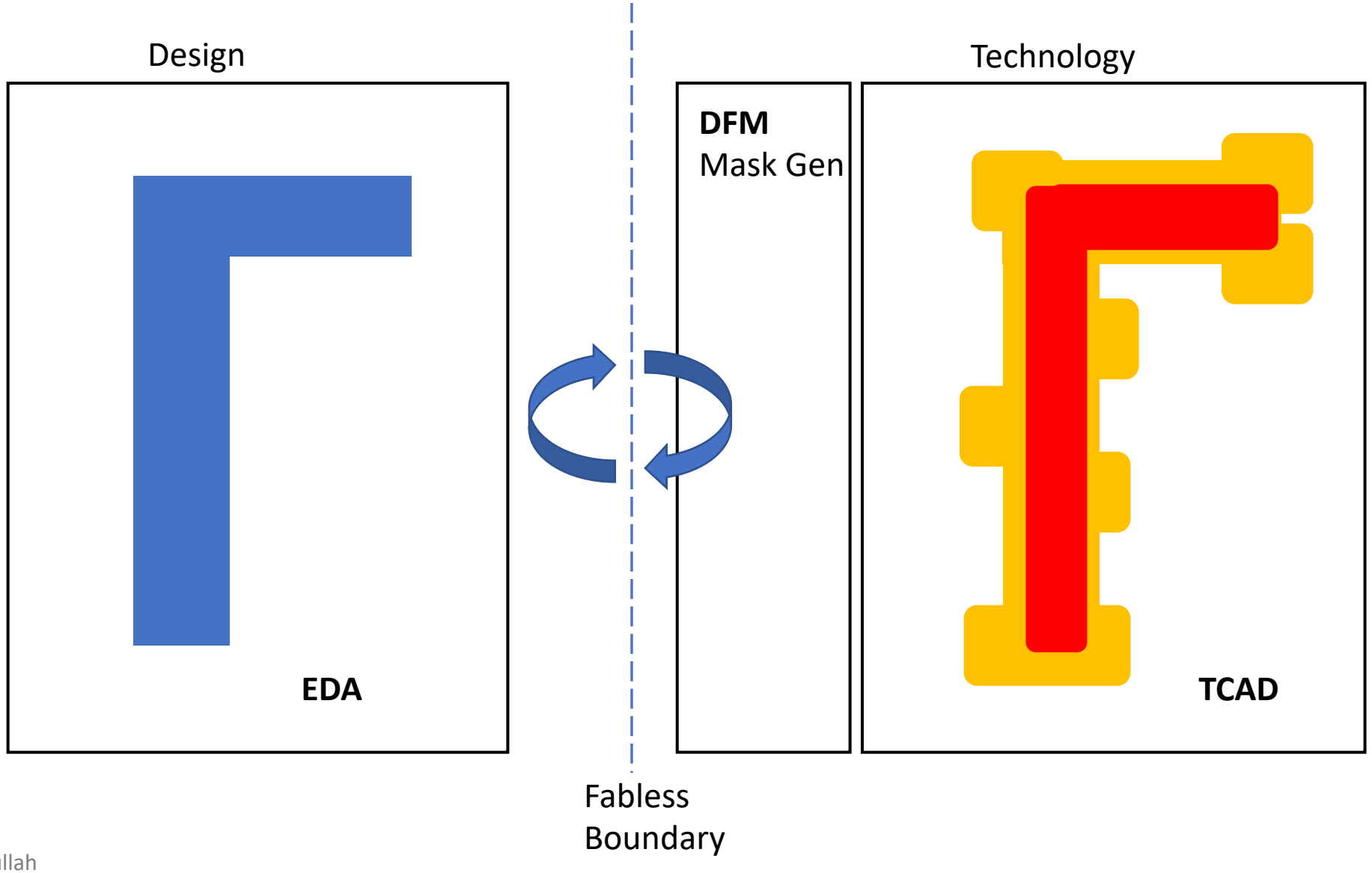
Testing:

- IEEE 1149.x, IEEE 1500, IEEE 1836, IEEE 1801, ATPG
- Chiplet vendors will need to provide enough models to support SiP level debug.

Design-Technology Co-Optimization (Legacy)

Characterize Design Collaterals:

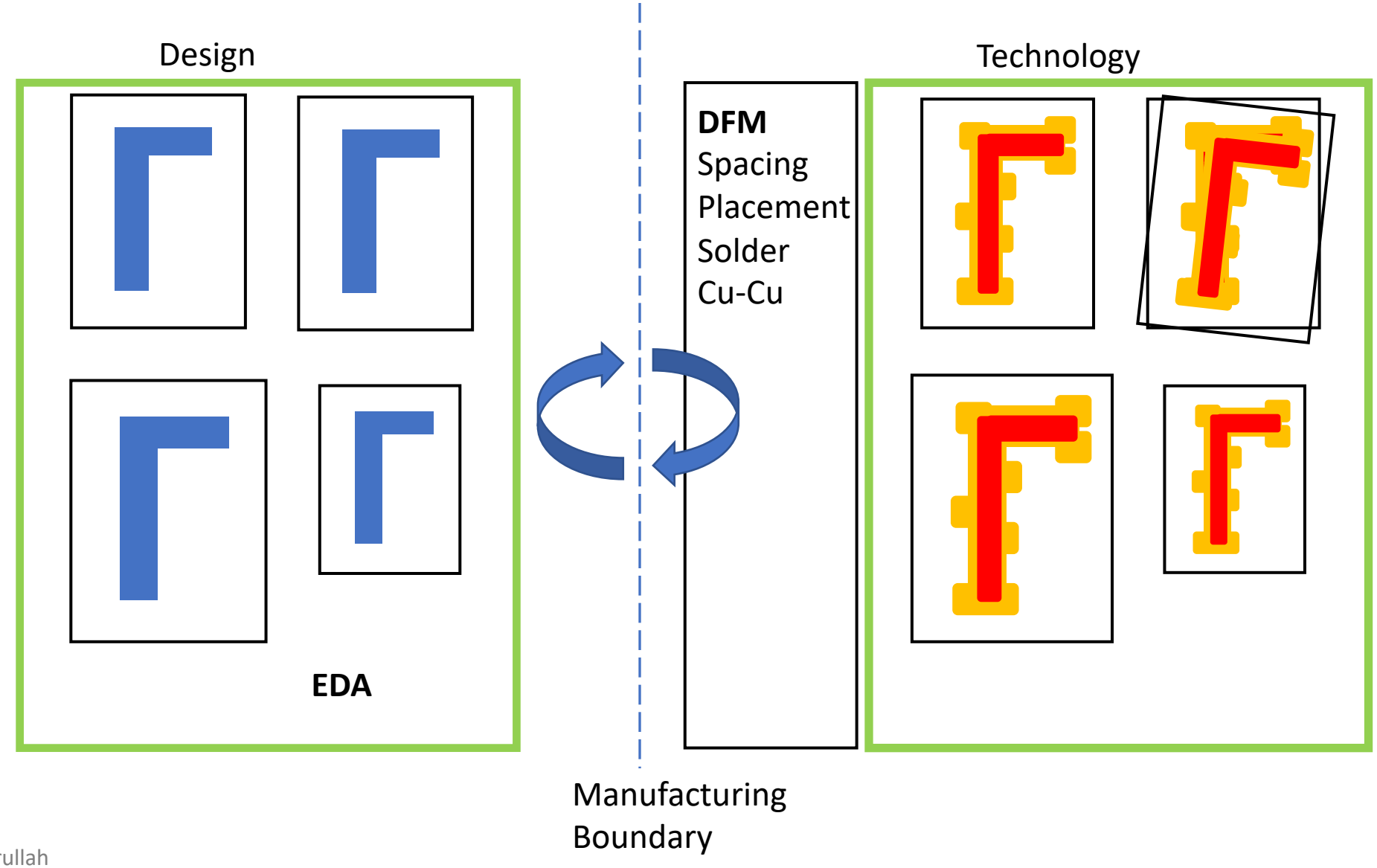
- Lib Cells
- Extraction Rules
- Metric Circuits
- Ring Oscillators
- Wire RC
- Variability



Chiplet-Technology Co-Optimization

Characterize Design Collaterals:

- Chiplets
- Extraction Rules
- Metric Circuits
- Ring Oscillators
- Wire RC
- Warpage
- Thermal
- Jmax
- Zo, S-param
- Alignment



Summary

1. Chiplets
   - Physical Goods. Testable. With Warranty.
   - Early-stage architecture across EE, ME, Packaging Eng, and Material Scientists is key.
   - MCM -> 2.5D -> Si Bridges -> Si Interposers -> Front End Fab Chiplet based 3D-ICs.
   - Chiplet Models are machine readable and different from Chip Data Sheets.

2. Design of Heterogeneous ICs
   - Early Power Estimation drives packaging technology choice.
   - Early Power Estimation helps with Thermal and Mechanical analyses and wise choices.
   - Clean power delivery requires thicker Cu layers and adequate decoupling.
   - Large and small signal D2D signaling requires capacitances reduction and smooth surfaces.

3. Operations and Test
   - System Level Test, System Level Test, System Level Test.
   - Yield is workable IFF design has no pair-wise bugs, cross talk, sensitivities.
   - Work out ELF in Chiplets and not after integration.

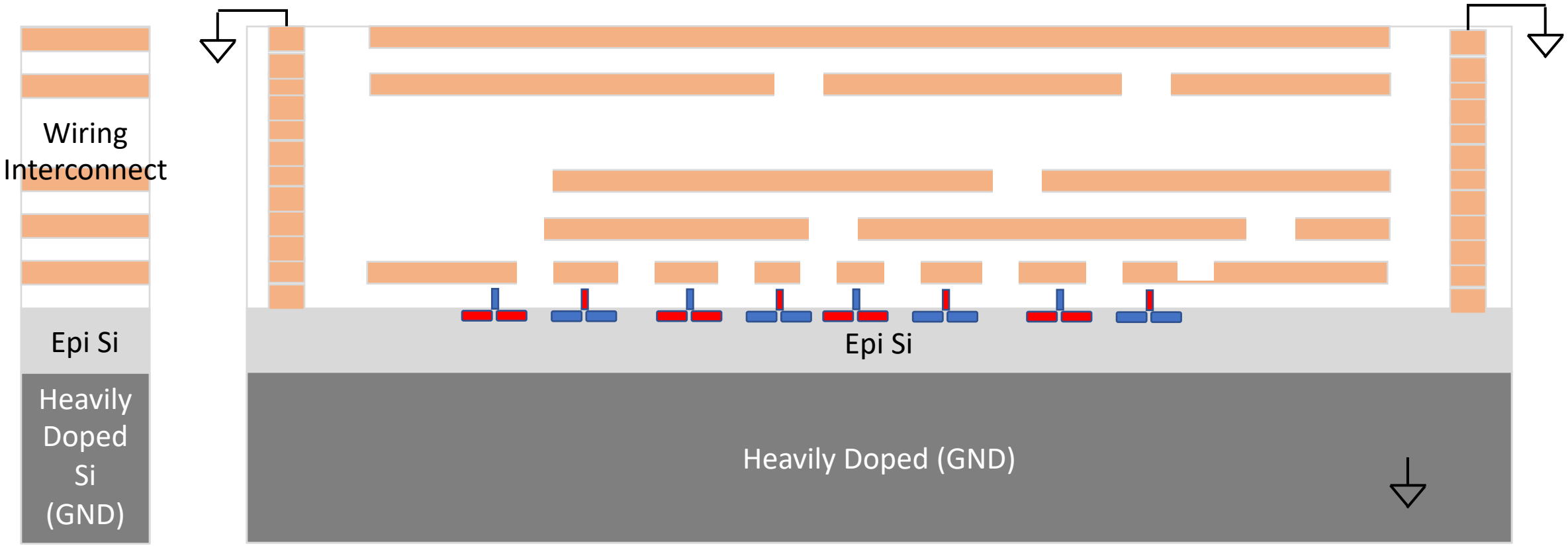
4. Technology Co-Optimization
   - New Areas for DTCO include interconnect RLC characterization and channel modeling
   - Power Delivery and Signal integrity
   - Rule Sets are needed for package performance for Mechanical, Thermal modeling

Thank You

Signaling

Backup

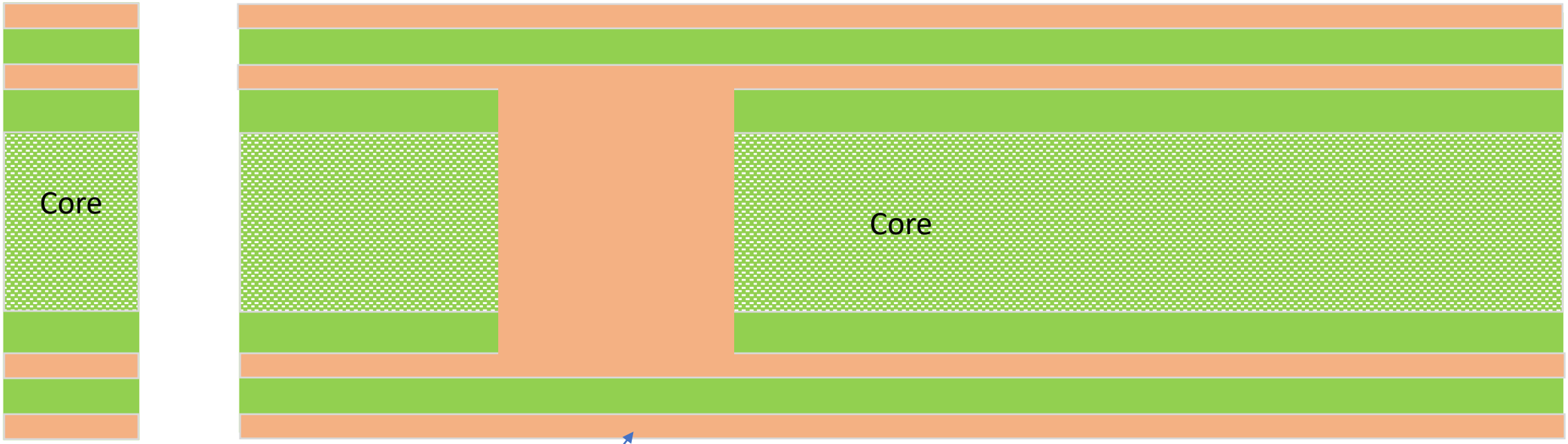
Signaling On Chip

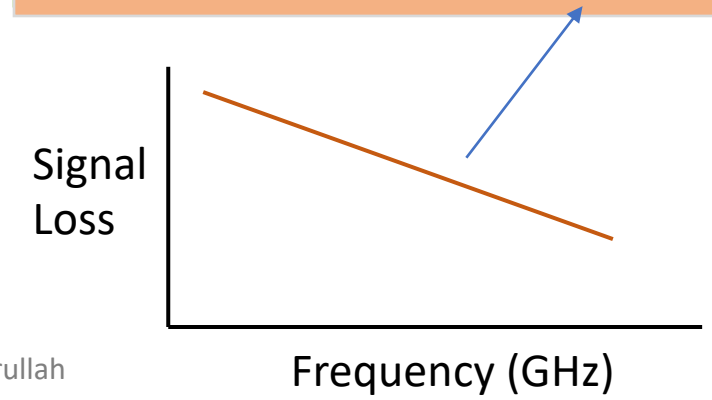


On Chip Signaling = Rail to Rail
IO Signaling = Low Swing, SerDes

C_wire/mm ~ 250 fF
E/bit/mm ~ 0.1 pJ

Signaling On Chiplet Substrates

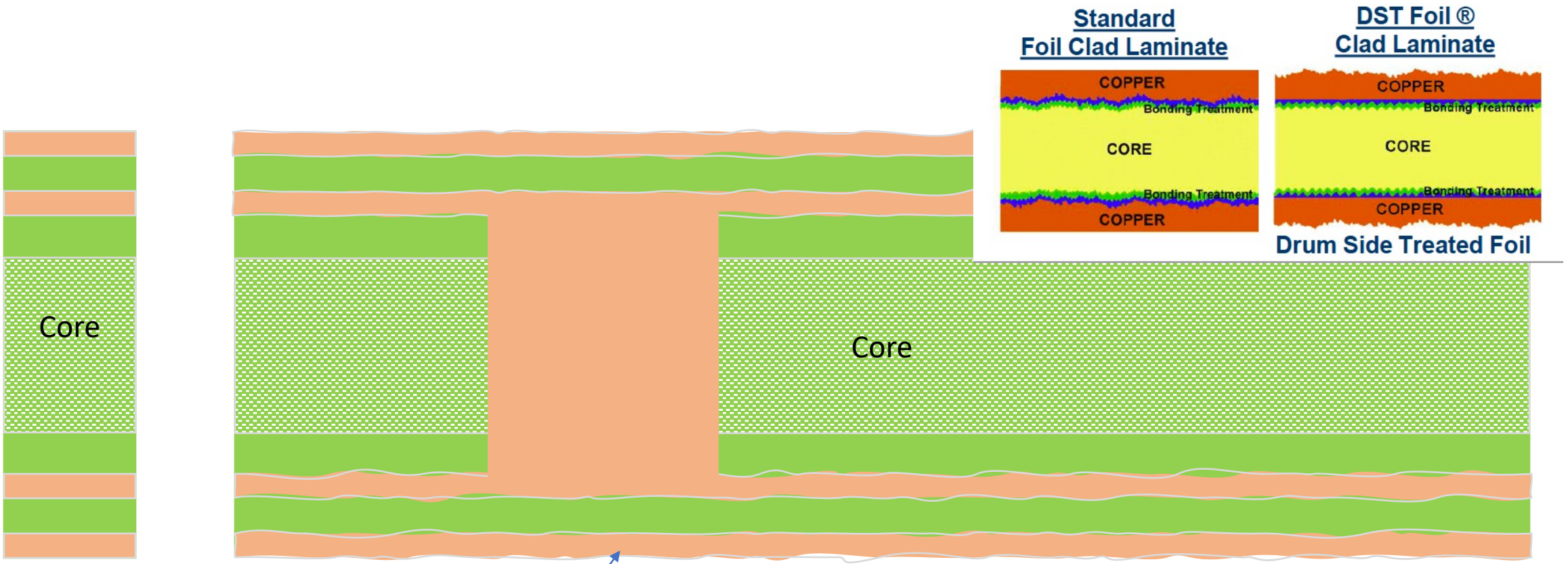


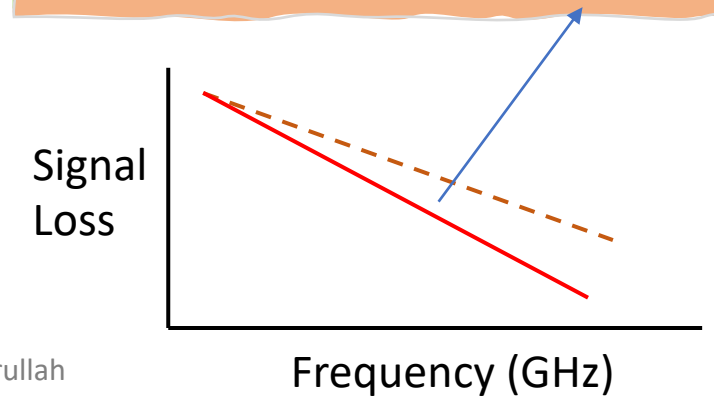


IO Signaling = Low Swing, SerDes
Side-band Signaling = Rail to Rail

C_wire/mm ~ 250 fF
E/bit/mm ~ 0.1 pJ

Signaling On Chiplet Substrates

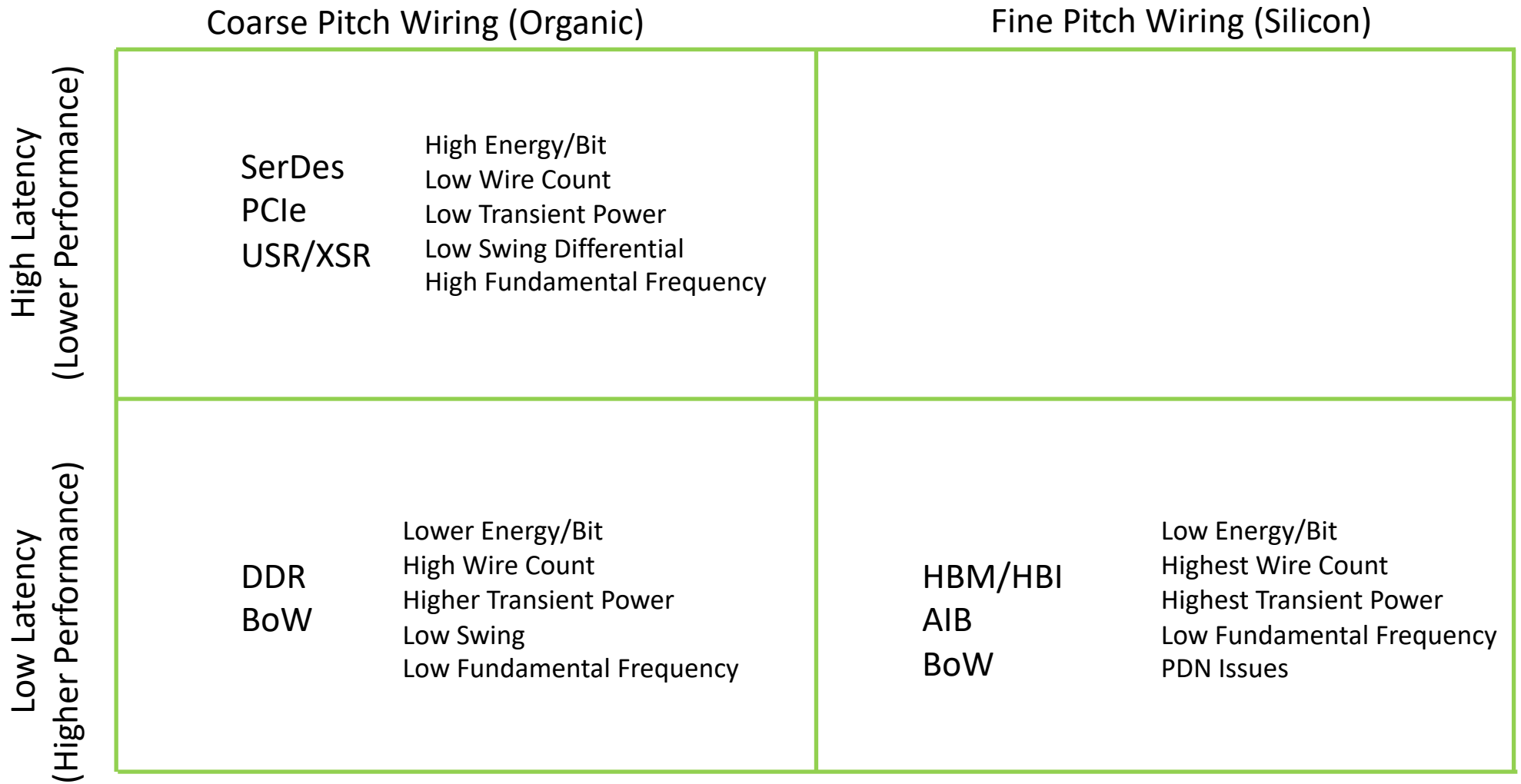




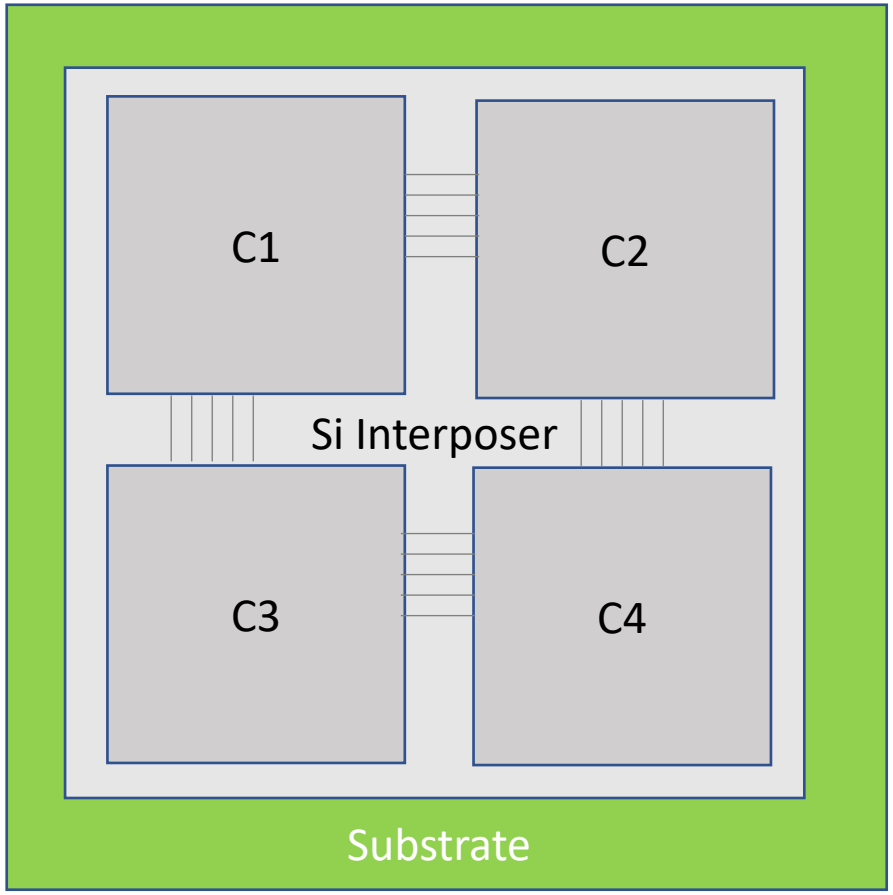
IO Signaling = Low Swing, SerDes
Side-band Signaling = Rail to Rail

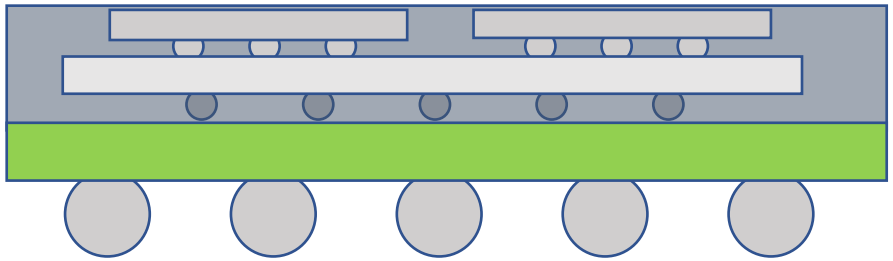
C_wire/mm ~ 250 fF
E/bit/mm ~ 0.1 pJ

Die-to-Die Signaling



Manufacturing and Testing





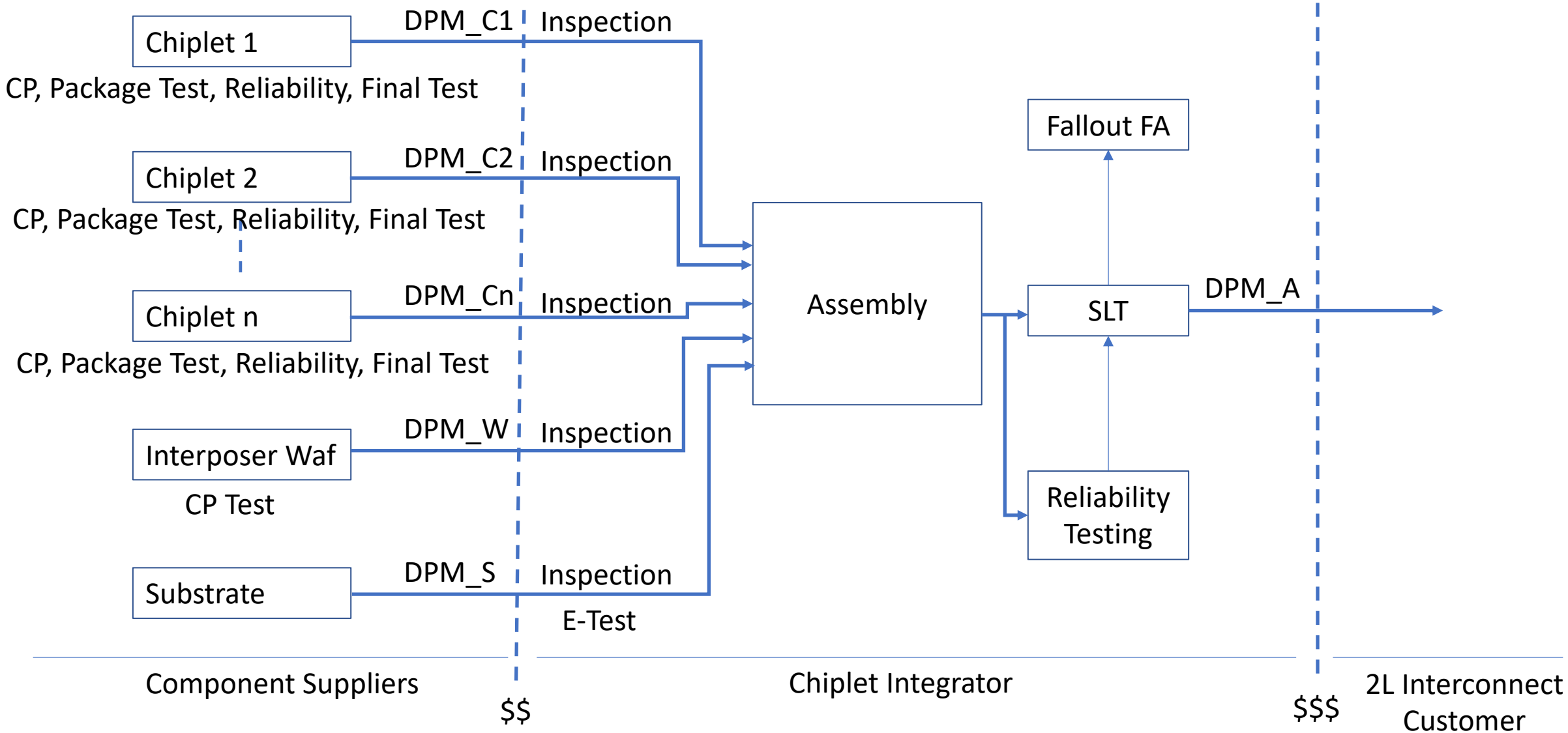
Testing for Heterogeneous Chips

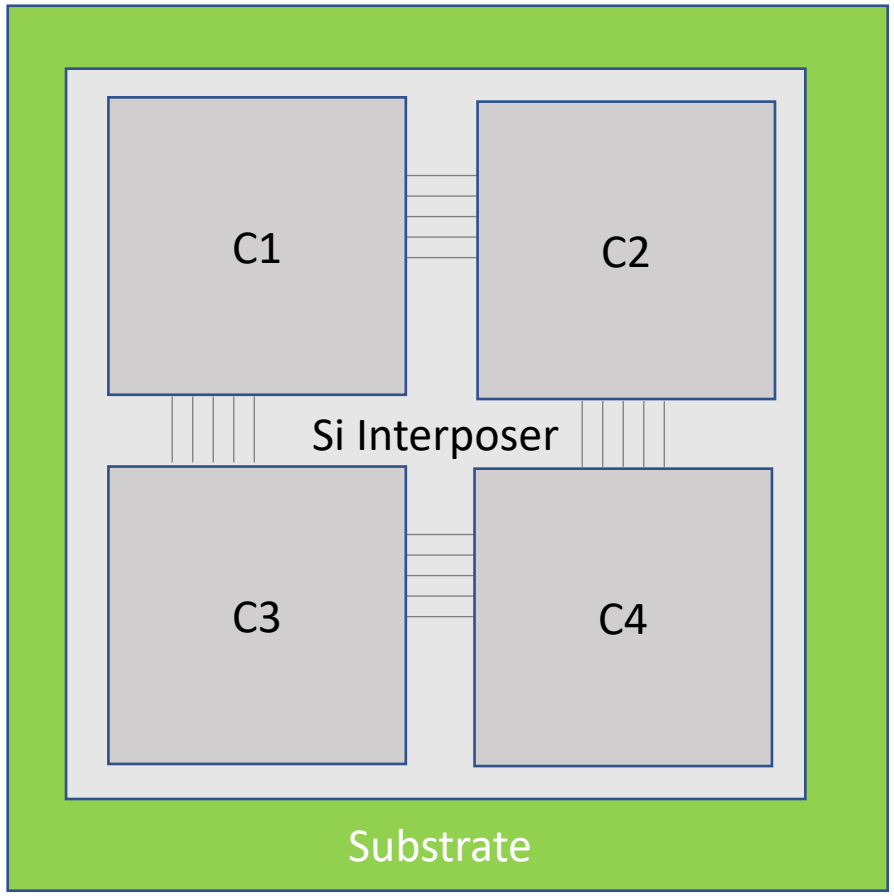
DFT & Verification:
- Need ESL (transaction level) and IBIS Models for all Chiplets
- Need Mechanical Models for all Chiplets for Thermal/Mech Simulations
- Simple JTAG in each Chiplet

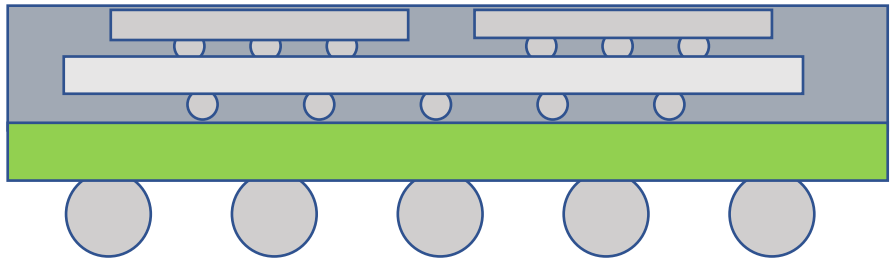
Incoming Material:
- Visual Inspection
- Quality of Chiplets to be guaranteed by the Vendor
- E-test for substrate
- CP test for Si Interposer

After Assembly:
- Inspection (e.g. x-rays)
- System level testing to verify assembly process (JTAG needed)
- Reliability testing

Chiplet Integration Ops Flow







Yield Estimation Example

Incoming DPMin Chiplet C1-C4= DPM_C < 100
Number of Chiplets = N = 4
Incoming DPM in Si Interposer= DRM_W <100

Failed Assemblies due to incoming DPM
= N x DPM_C+ DPM_W
= 4 x 100 + 100 = 500 (99.95%)

Control of Incoming DPM_C is the key for Yield.

Assembly Yield numbers can be awesome.

System Level Test is the key to control outgoing DPM For Heterogeneous Chips.