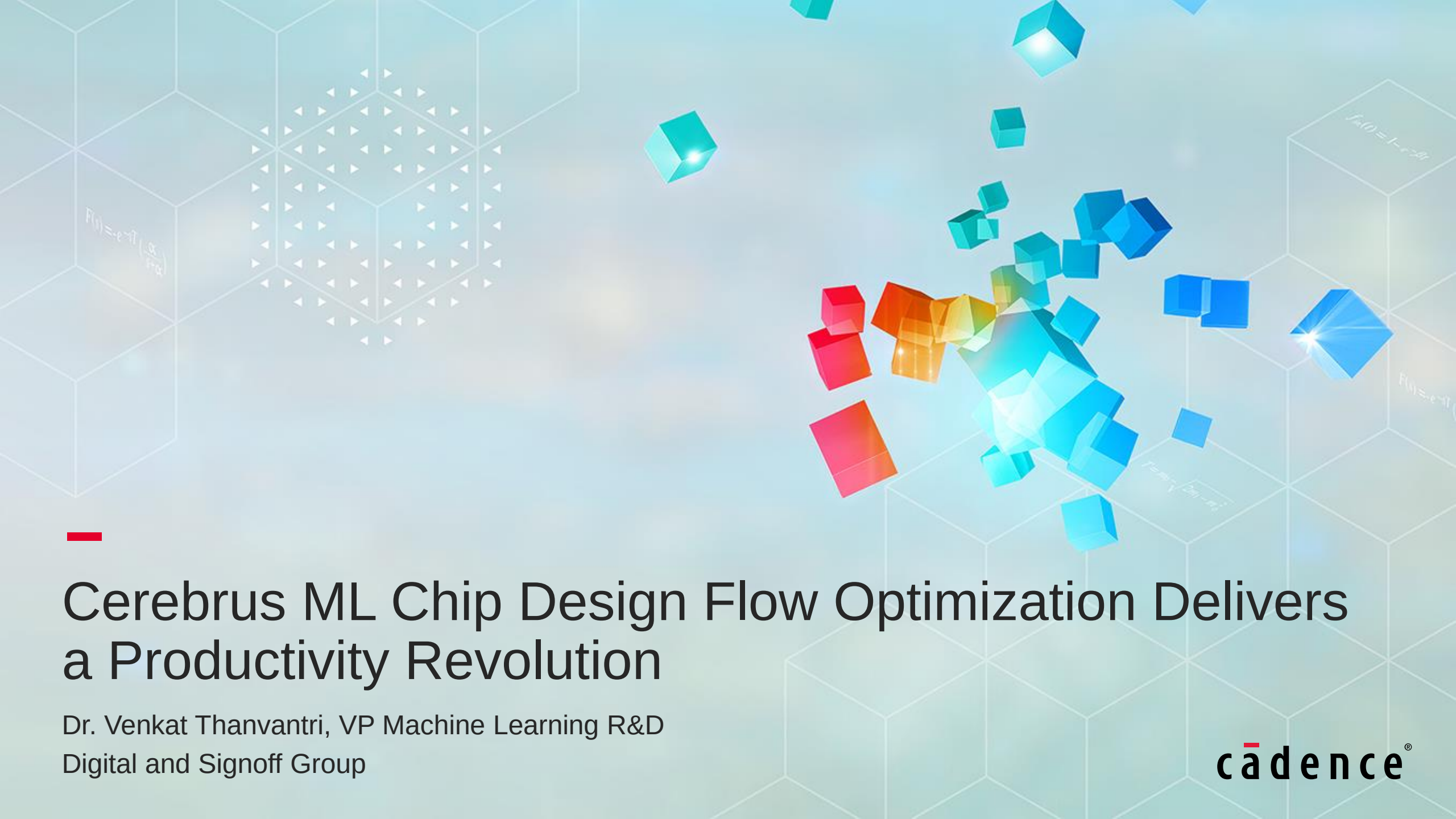


Cerebrus ML Chip Design Flow Optimization Delivers a Productivity Revolution

Dr. Venkat Thanvantri, VP Machine Learning R&D
Digital and Signoff Group

cadence®

Today's Chip Design Market Landscape

The semiconductor industry is experiencing a renaissance

- Strong growth in 5G, autonomous driving, hyperscale compute, and industrial IoT
- Underlying each of these trends is the application of artificial intelligence (AI) and machine learning (ML)

New applications and technological interdependencies are generating demand for even more compute, more functionality, faster data transmission speeds

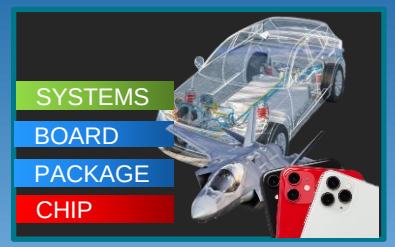
- Today's electronics have more chips in them with no end to this trend in sight

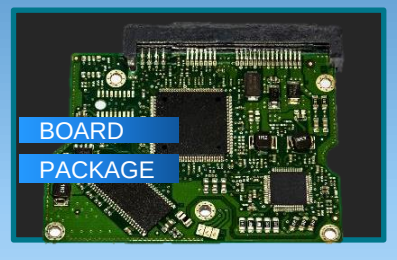
Next-generation chips must be produced faster and smarter

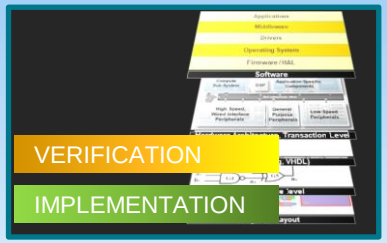
- Engineers are overloaded and need support to keep up with demand

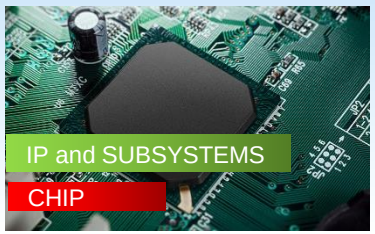
Targeting “High-Effort” Aspects of the Design Flows

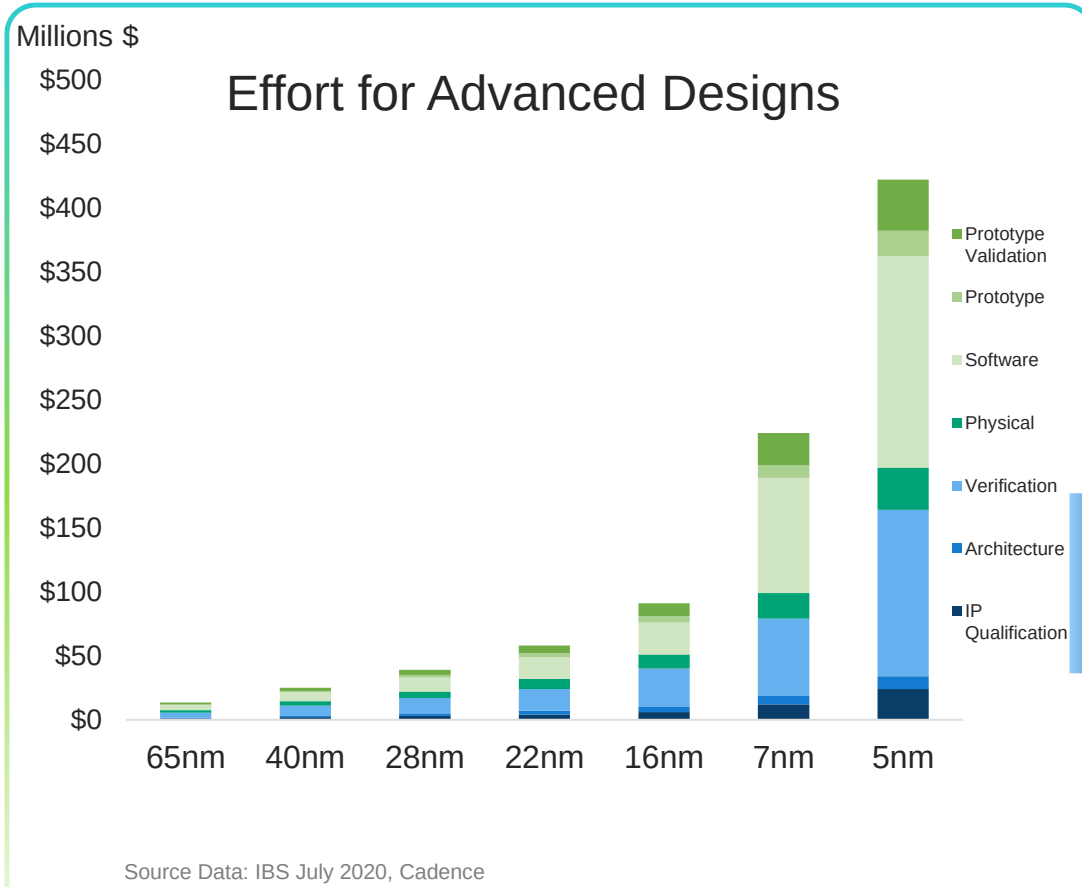
System Integration





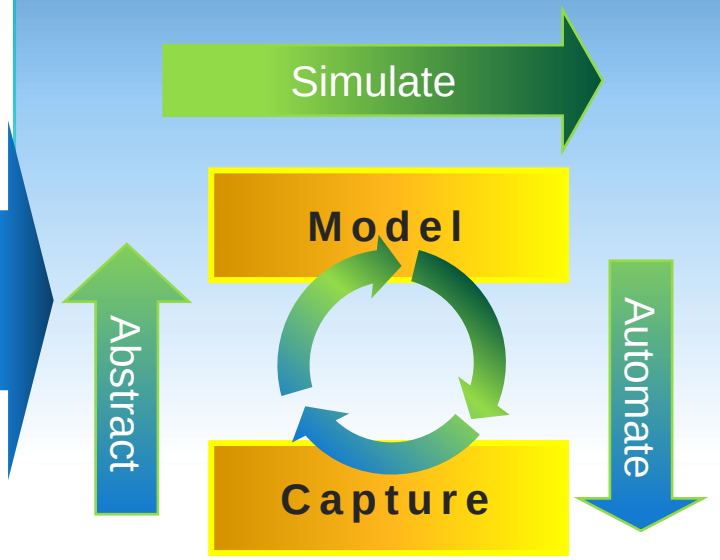






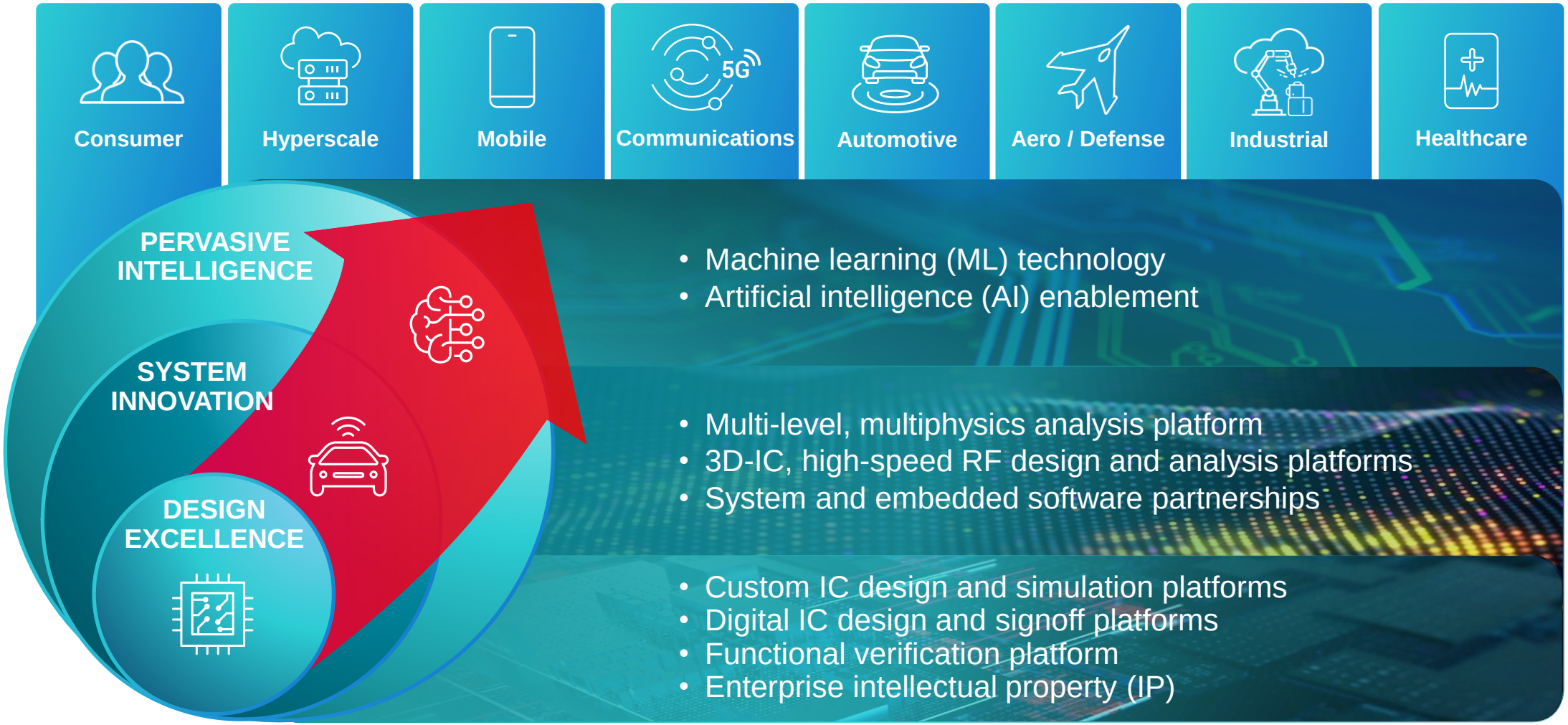
Source Data: IBS July 2020, Cadence

Analyze, Optimize



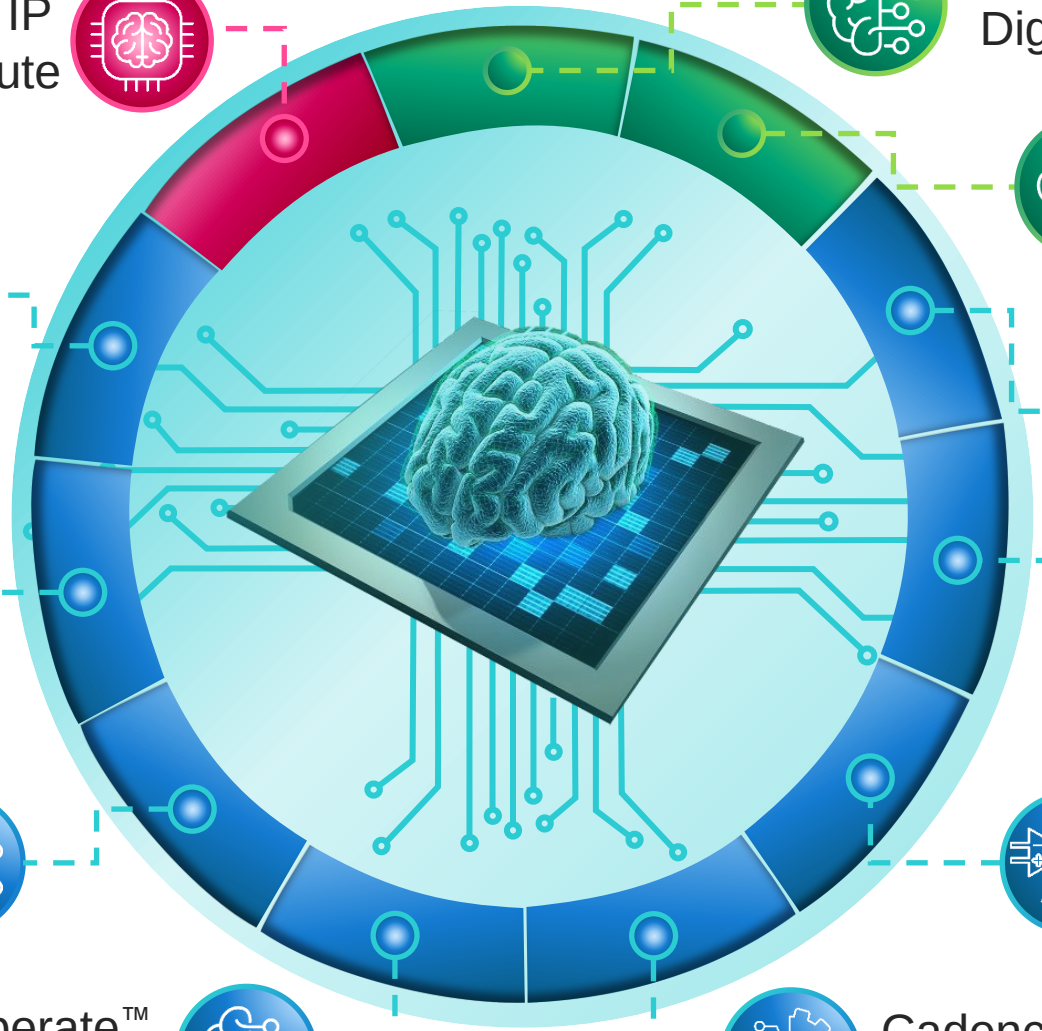
Cadence Intelligent System Design Strategy

Enabling end-to-end systems from devices to the cloud



Cloud Enabled — Partnerships with Ecosystem Leaders

Cadence AI/ML Technologies



Tensilica® AI IP
On-Device and Edge Compute

Cerebrus™
Digital Implementation Full Flow

Xcelium™ ML
Regression Simulation

Sigrity™
Signal Integrity

Innovus™
Digital Implementation

JasperGold®
Formal Verification

Allegro® X
PCB Layout

Spectre®
Monte Carlo Simulation

Virtuoso®
Custom and Analog Design

Liberate™
Library Characterization

Cadence® Design for Manufacturing (DFM) Technologies

Inside
Outside
Enablement

Machine Learning for Digital Implementation

Machine Learning Is Not New…

Machine Learning is the field of study that gives computers the ability to learn without being explicitly programmed."

Arthur Samuel, 1959

60 Years of Research

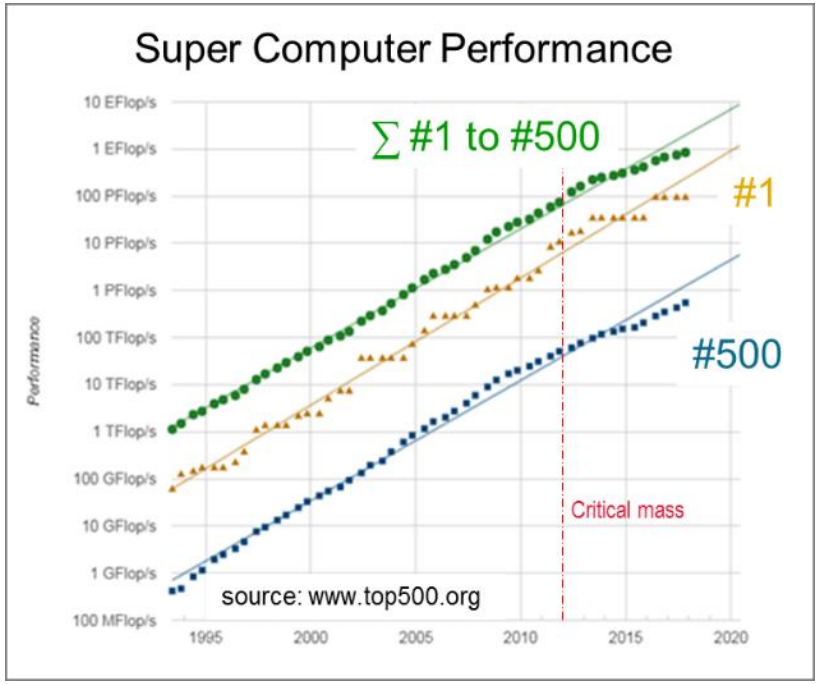
Artificial Intelligence

Neural Networks

Big Data

CNN

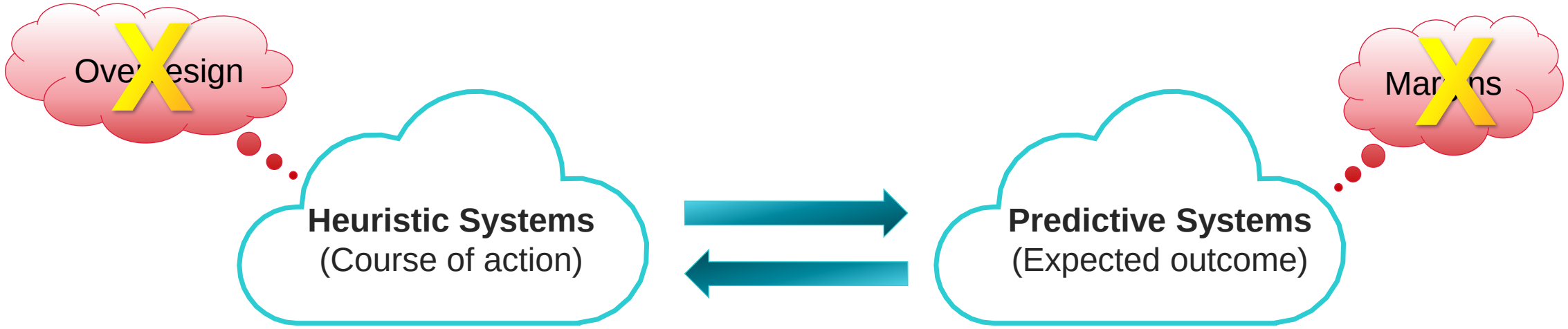
Deep Learning



High-Performance Cloud

Massive Storage Massively Parallel

Machine Learning Is a Good Fit for Digital Implementation



EDA is full of NP hard/NP complete problems

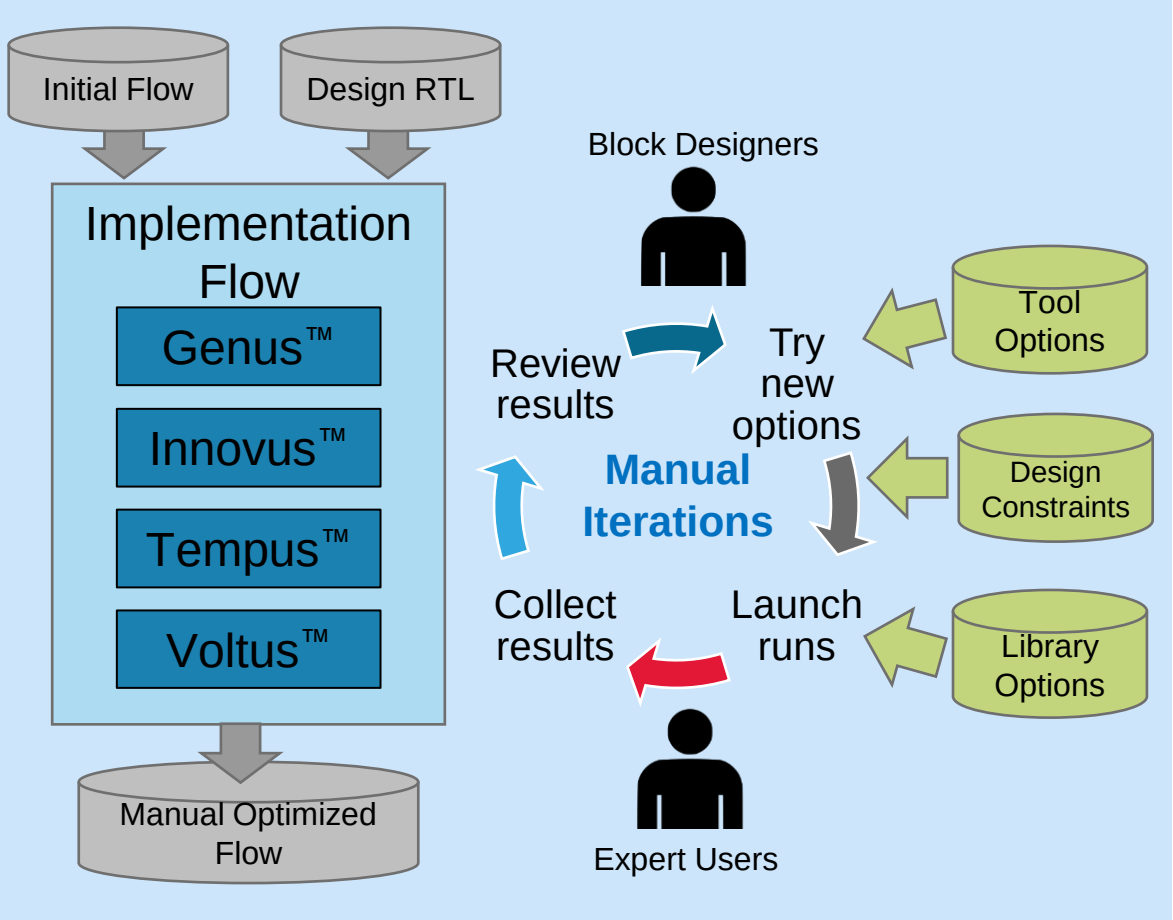
Non-trivial to solve quickly (ex: exponential time)

Overdesign and margins used

ML's robust, rapid pattern-matching framework can reduce overdesign and margin inefficiencies delivering improved PPA results

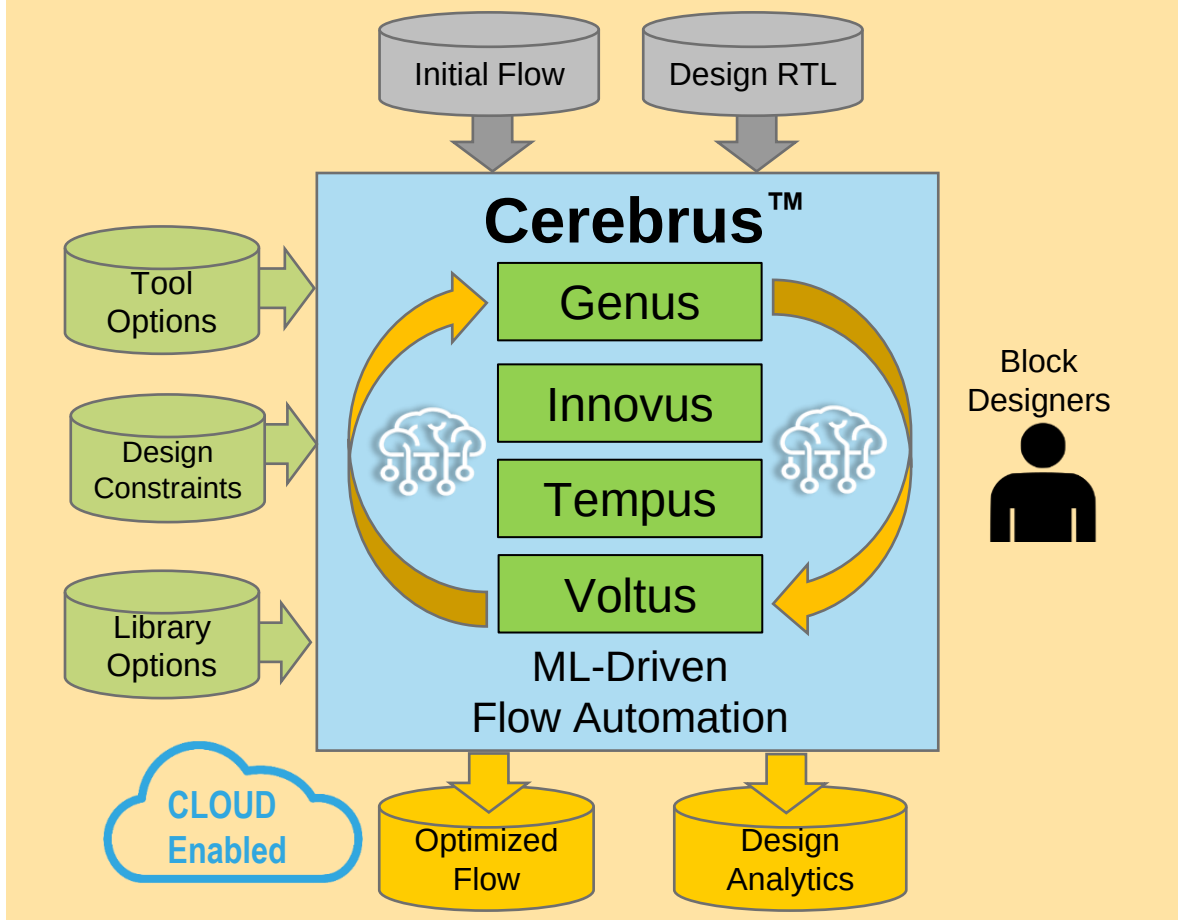
Cerebrus Intelligent Chip Explorer

Traditional Flow



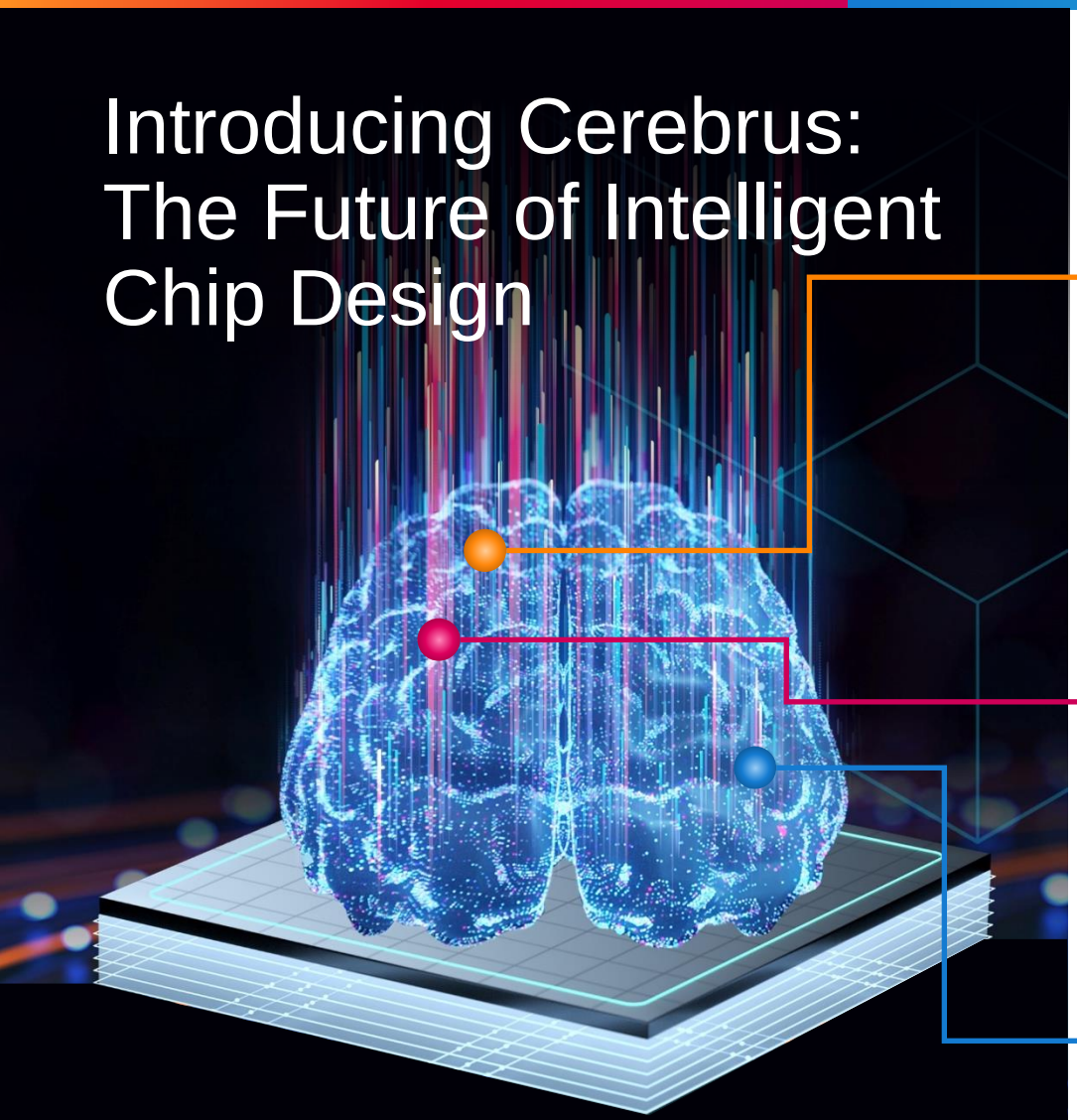
- High engineering effort
- Unpredictable schedules

Cerebrus ML Flow



- Improved designer productivity
- Better PPA
- Efficient compute usage

Introducing Cerebrus: The Future of Intelligent Chip Design



New machine learning (ML)-based tool that automates and scales digital chip design

Productivity and PPA Revolution

- Unique reinforcement ML
- Delivers up to 10X better productivity and 20% PPA improvements

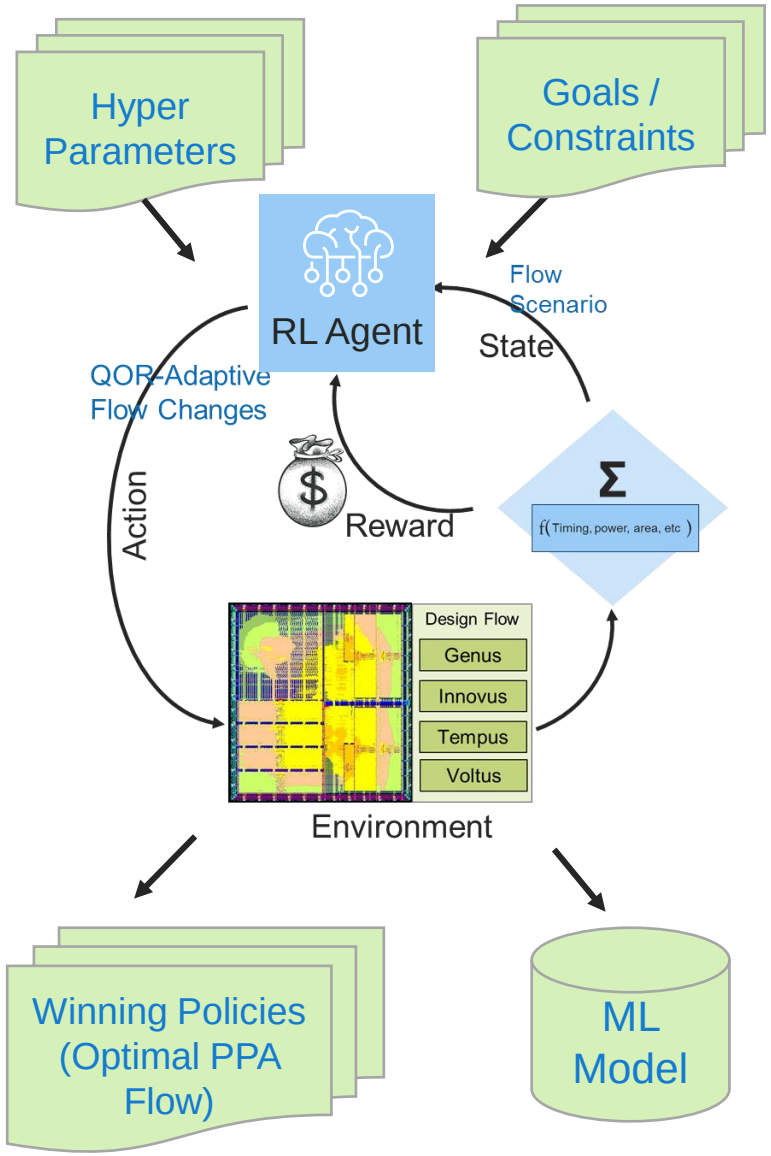
Automated RTL to GDS Full Flow Optimization

- Delivers better PPA more quickly
- Improves engineering team productivity

Scalable, Distributed Computing Solution

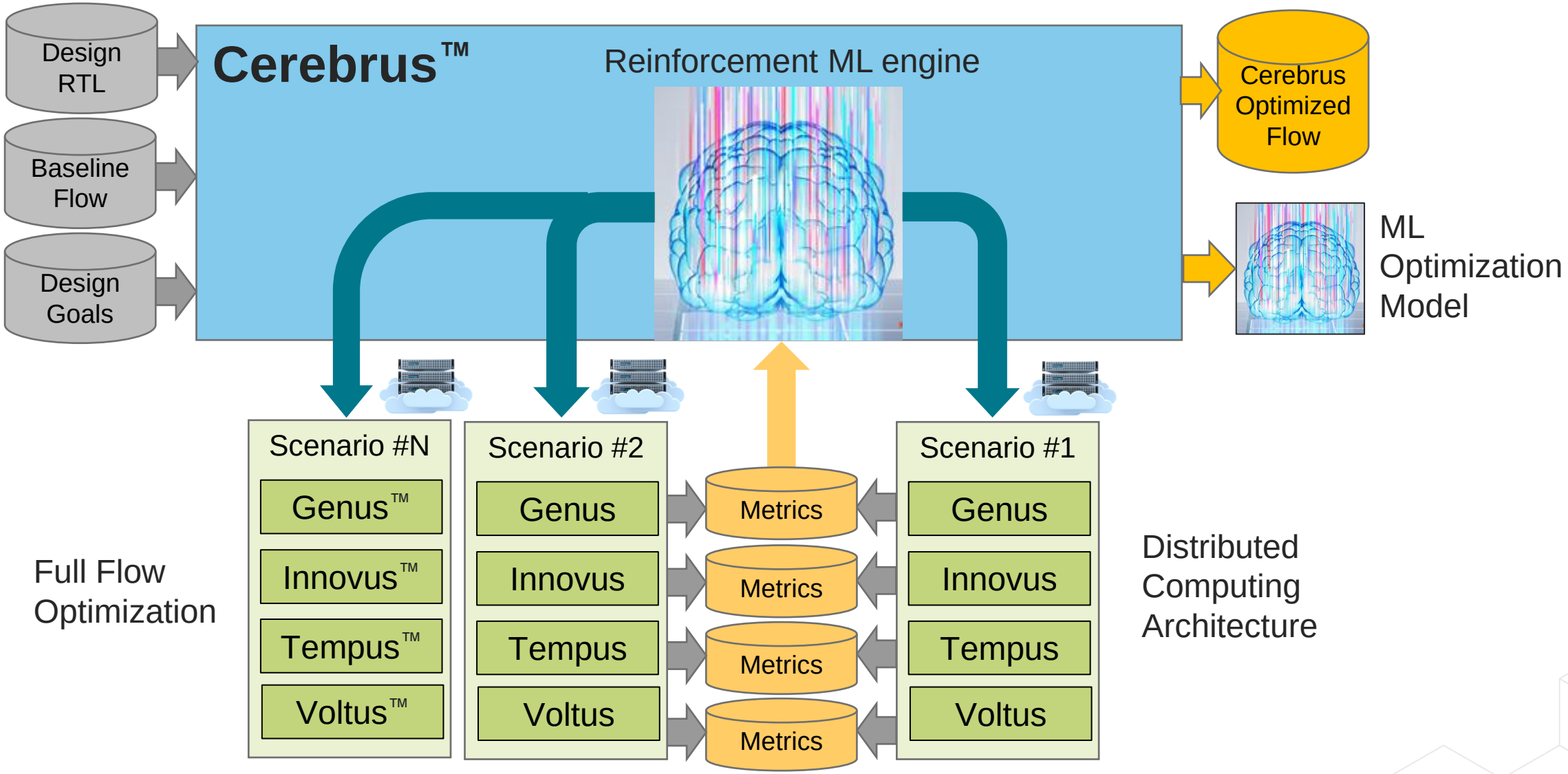
- On-premises or cloud computing resources
- Efficient, scalable solution as design size and complexity grow

Applying Reinforcement Learning Principles



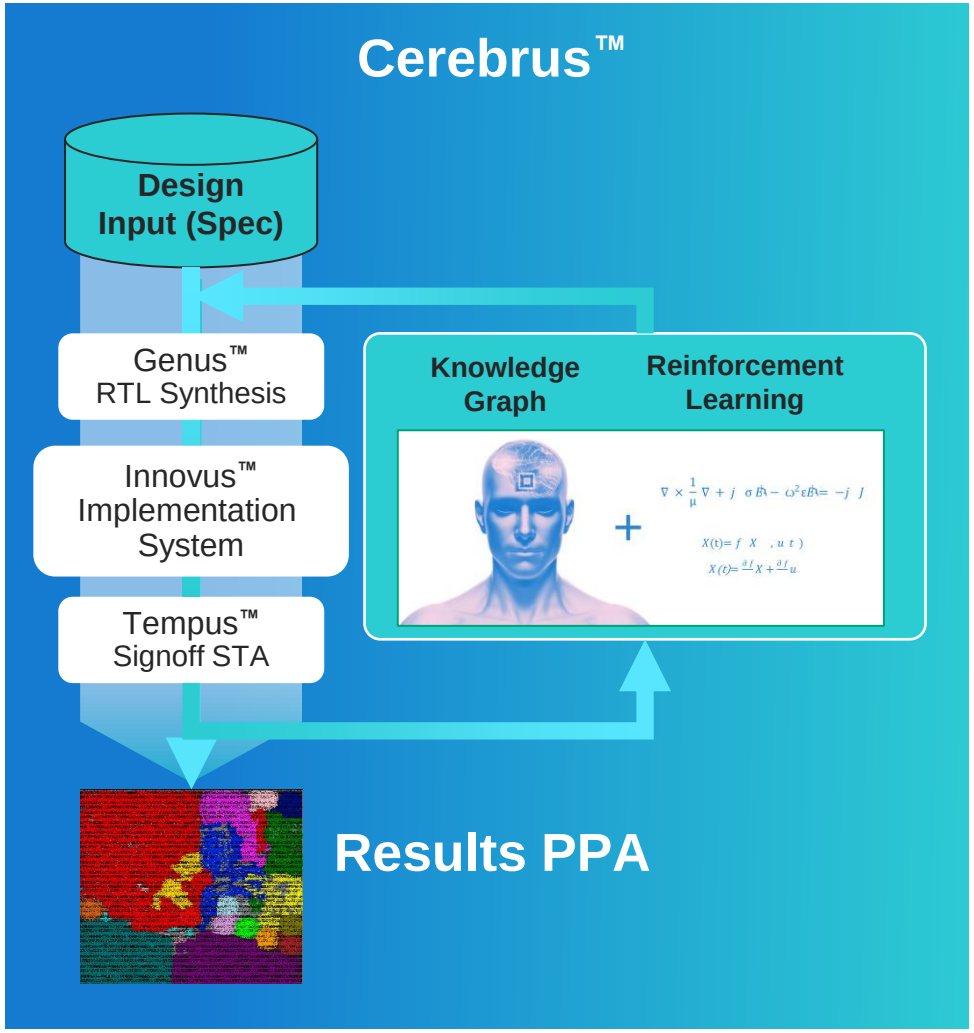
- Reinforcement Learning requires efficient exploration
- Scenario creation driven by probability of success
- Smart decision points (Early Stop / Reuse etc.)
- Resource management (CPU / Disk)

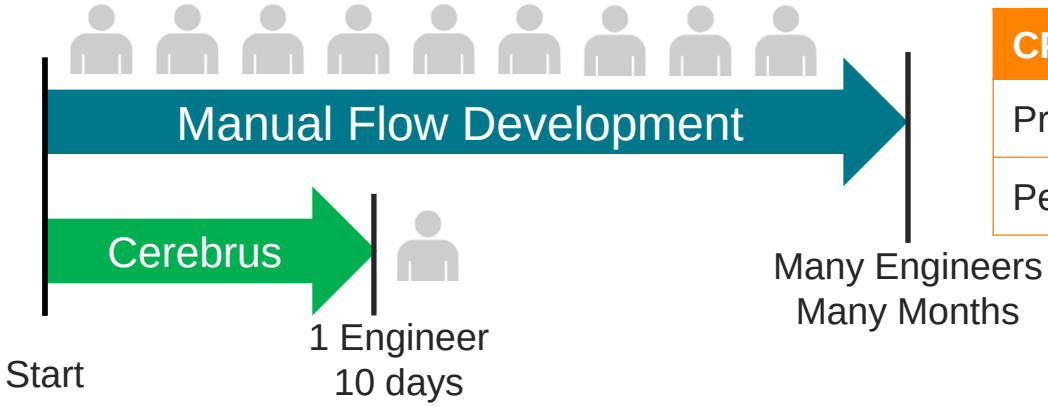
Cerebrus – Distributed Computing and ML Architecture



Cerebrus – ML for Better PPA and Full Flow Productivity

Smart ML flow optimization exploration improves designer efficiency





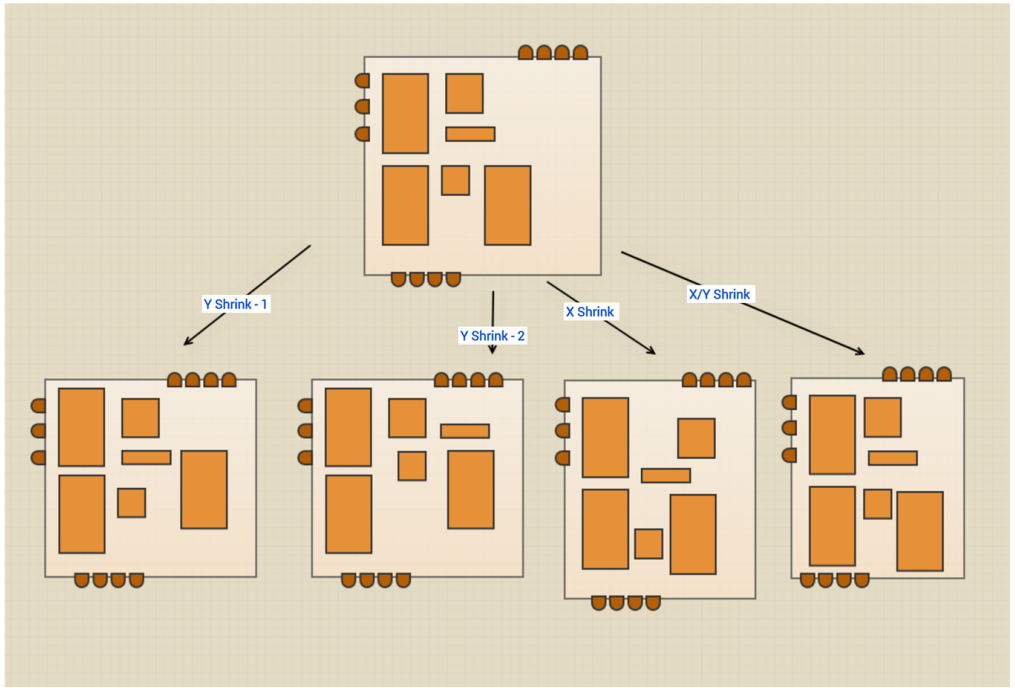
CPU	
Process	5nm
Performance	3.5 GHz

- Cerebrus automatically improved PPA of 5nm mobile CPU
- Cerebrus used 30 parallel jobs
- Within 10 days converged on improved flow

Cerebrus Improvements over Baseline

Parameter	Improvement	Percent
Performance	**420MHz**	**14%**
Leakage power	**26mW**	**7%**
Total power	**62mW**	**3%**
Density		**5%**

Cerebrus – Automated Floorplan Optimization



- Floorplan can be automatically resized in any direction
- Innovus™ mixed placer used to find optimal macro location in resized floorplan

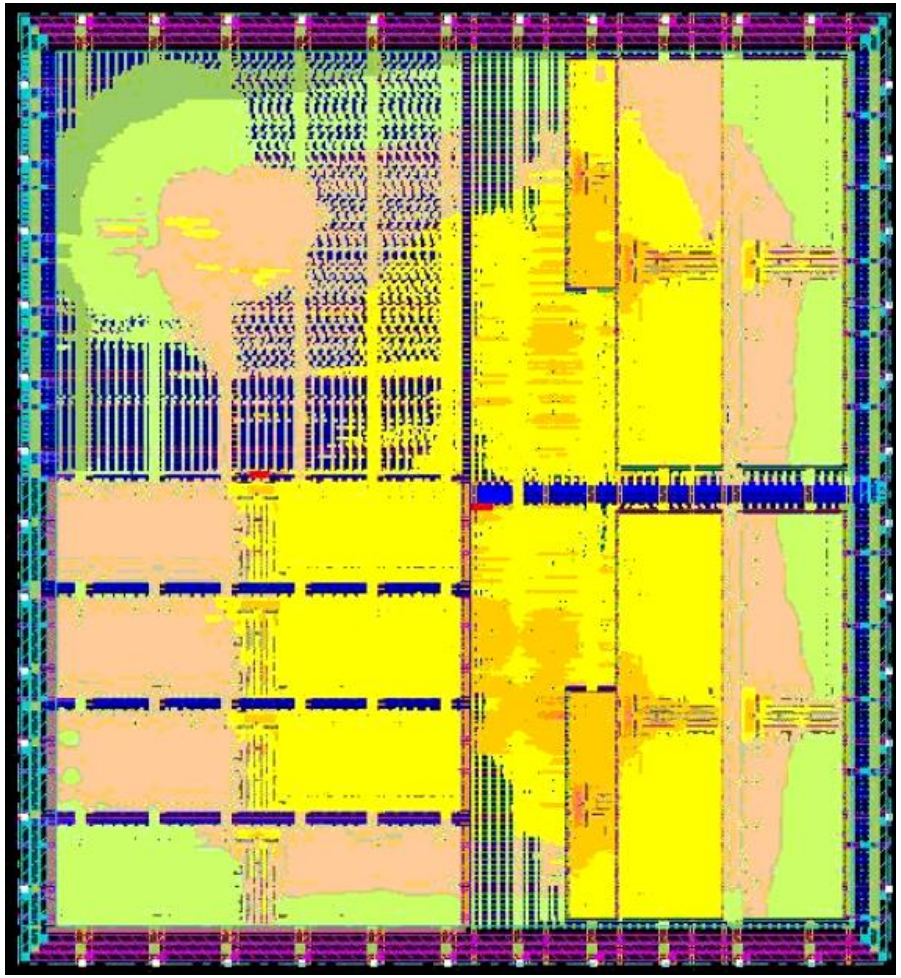
Design – CPU Core	
Process	12nm
Performance	2 GHz

- Customer wanted to achieve 2GHz on latest CPU implementation
- Cerebrus™ ran 50 flow experiments
  - Used Innovus mixed placer to improve floorplan
  - Other flow changes delivered better performance

Cerebrus Improvements over Baseline

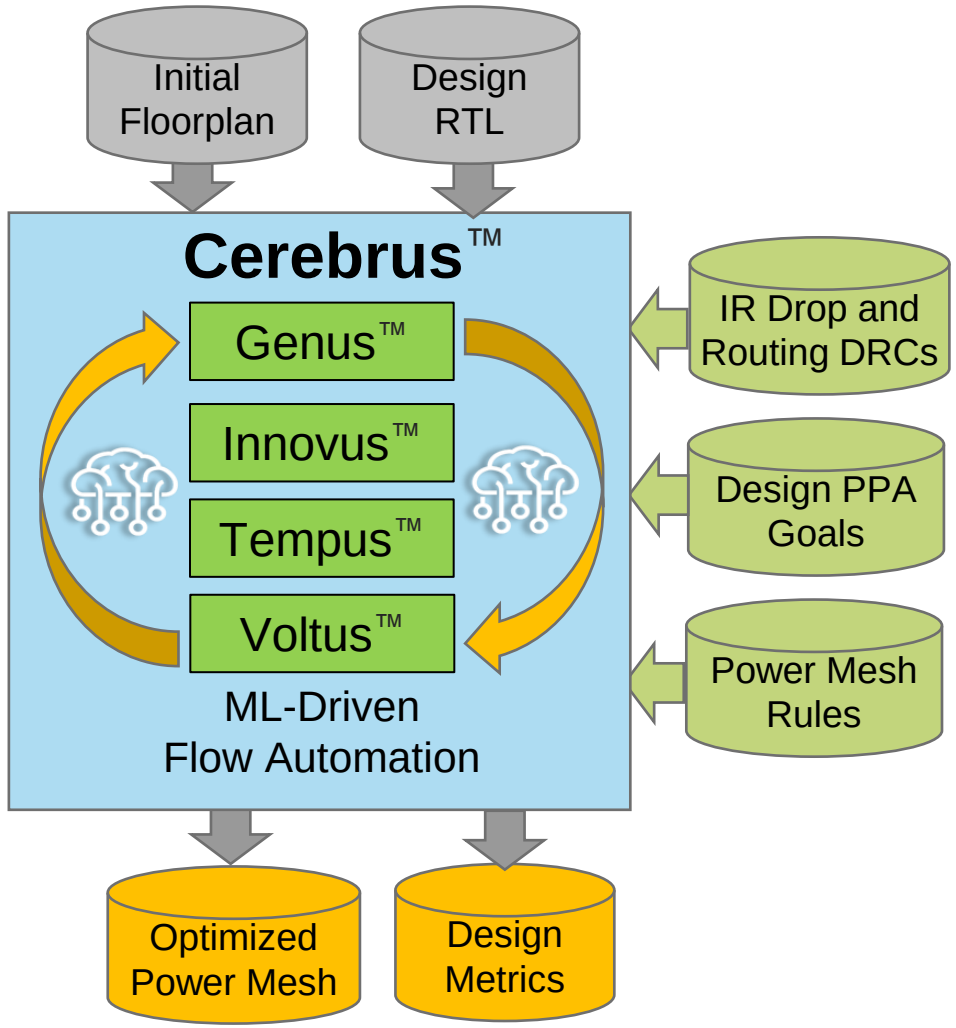
Parameter	Improvement
Performance	**+200MHz**
Total failing timing	**83%**
Leakage power	**17%**

Cerebrus – Power Mesh Optimization



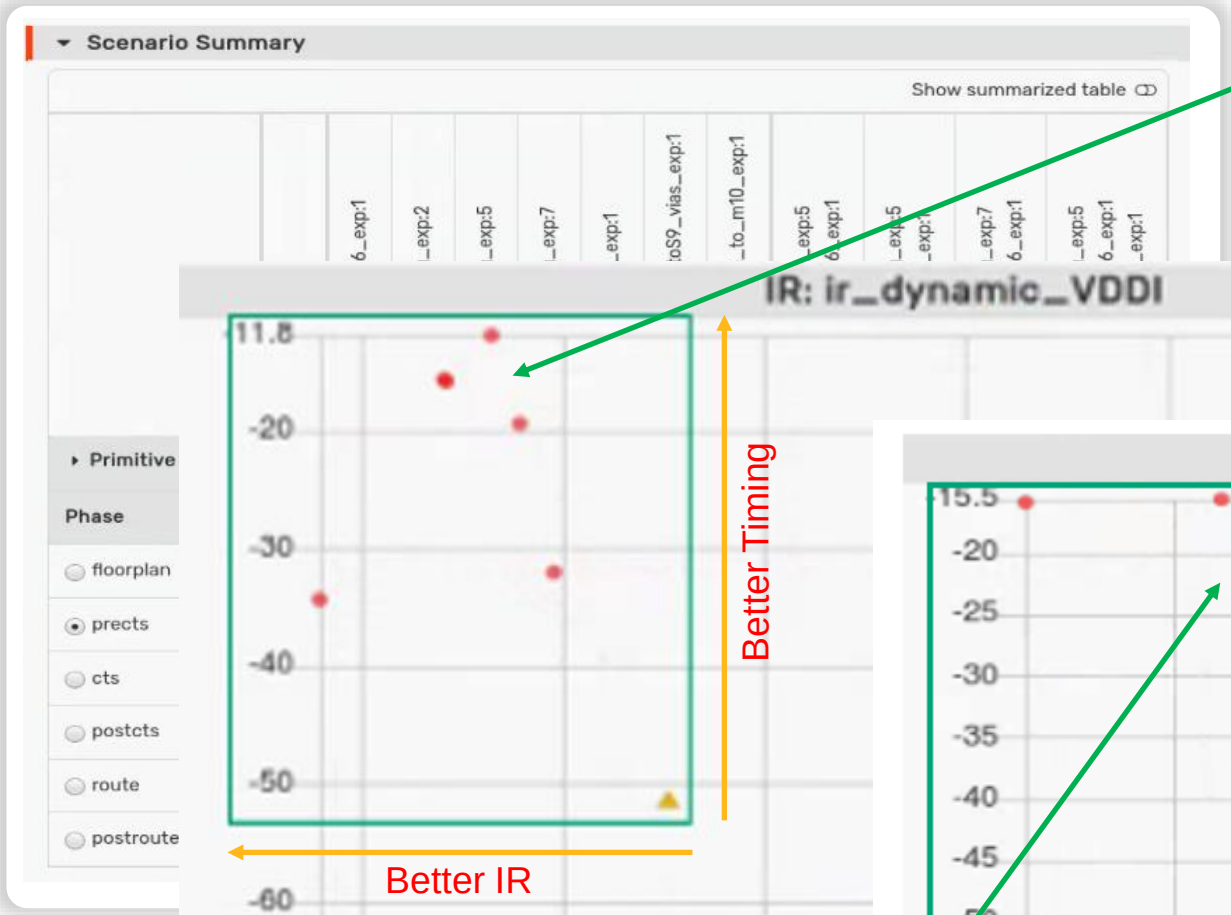
- Power mesh design is becoming critical for latest advanced-process nodes
  - Overdesign will compromise PPA results
  - Underdesign can generate many IR drop violations that require fixing
- Current power mesh design is a manual, iterative task
  - Requires a lot of effort impacting design schedule
  - Does not converge on optimal result
  - Must be done for each design independently
- Automation is needed to find optimal power mesh for each design

Cerebrus – ML Power Mesh Optimization



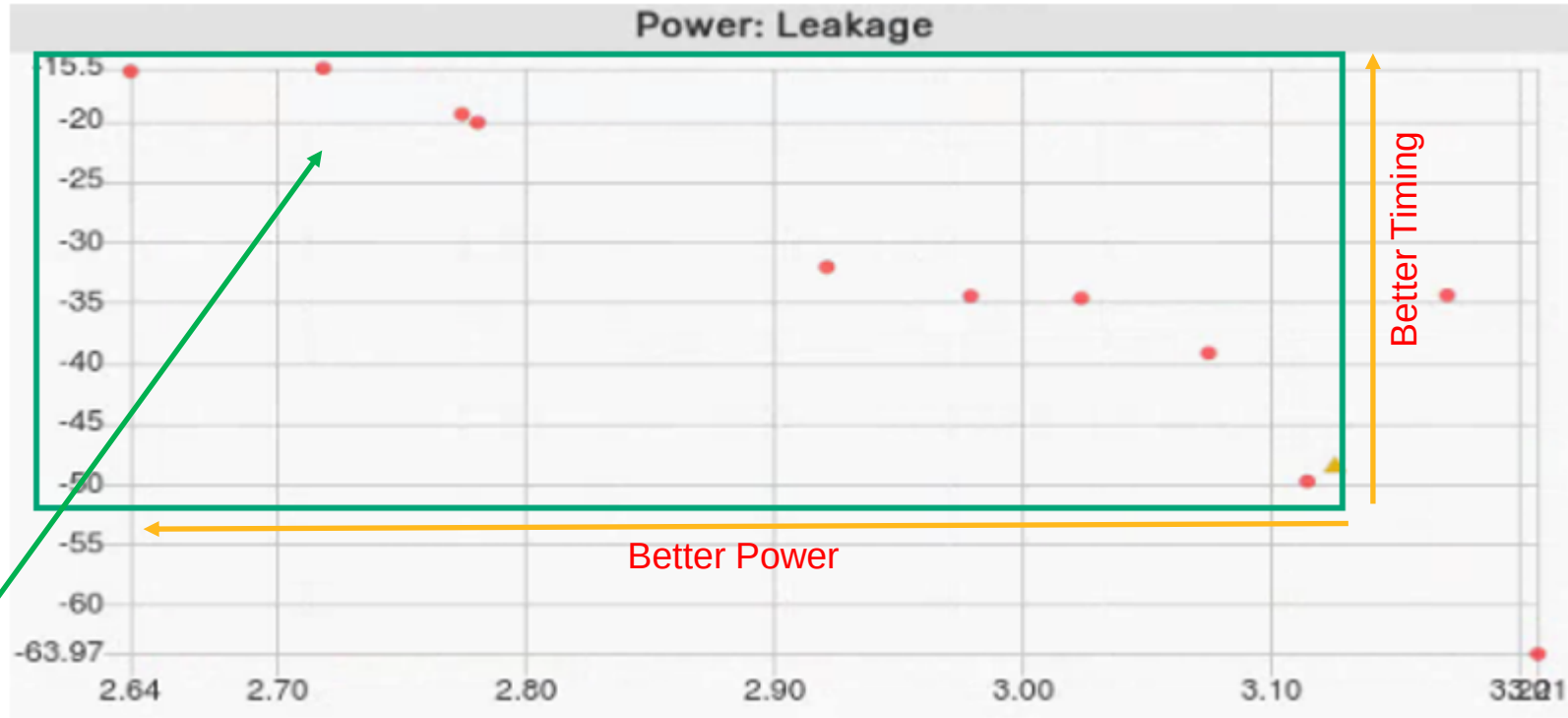
- Optimized power mesh must meet
  - Design IR drop limits
  - Routing convergence
- Design goals must also be optimized
  - Power
  - Performance
  - Area
- Automatically generate different power mesh combinations
  - Spacing changes
  - Full stripe connections
  - Via stacking
  - Via reduction

Cerebrus – Power Mesh Optimization Results



Better timing and IR drop

- Runs are automatically managed
- Only runs converging on goals are allowed to proceed



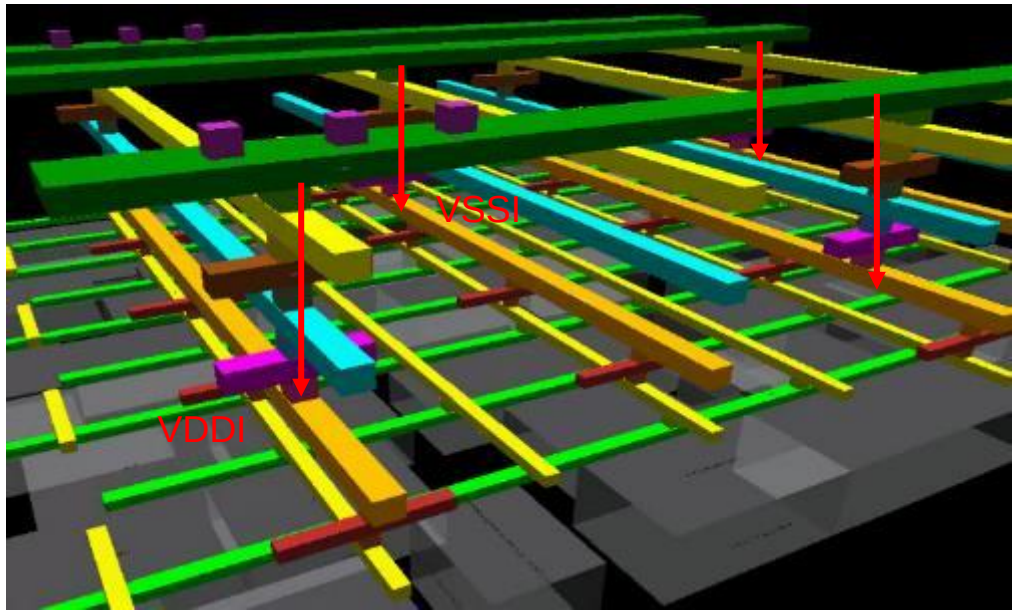
△ = Baseline result

● = Cerebrus™ result

Better timing and power

cadence

Cerebrus – Power Mesh Optimization Results



Completely automated solution

- Improved engineering productivity
  - No time consuming manual iterations
- Faster time to design tapeout
- Easily scalable to any number of designs

- Cerebrus™ optimization generated optimal power mesh improving design PPA
  - IR drop limits met
  - Routability maintained
- 4nm Block X
  - **67% improvement in timing**
  - Better power
- 4nm Block Y
  - **43% improvement in timing**
  - Improved power

Cerebrus – ML Capabilities Improved Flow, PPA, and Productivity

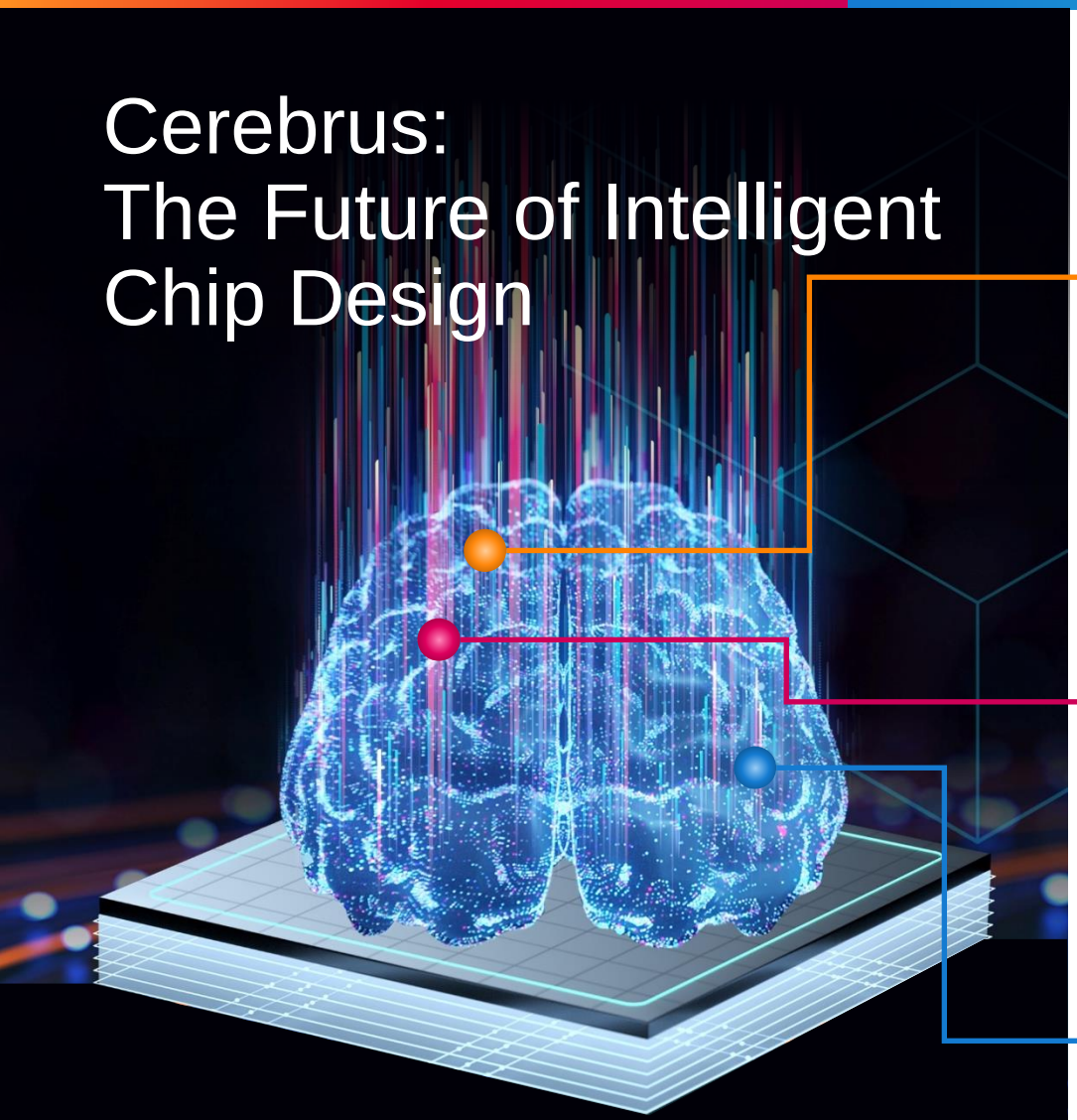
To efficiently maximize the performance of new products that use emerging process nodes, digital implementation flows used by our engineering team need to be continuously updated. Automated design flow optimization is critical for realizing product development at a much higher throughput. Cerebrus, with its innovative ML capabilities, and the Cadence RTL-to-signoff tools have provided automated flow optimization and floorplan exploration, improving design performance by more than 10%. Following this success, the new approach will be adopted in the development of our latest design projects.

Satoshi Shibatani,
Director, Digital Design Technology Department,
Shared R&D EDA Division, Renesas

As Samsung Foundry continues to deploy up-to-date process nodes, the efficiency of our Design Technology Co-Optimization (DTCO) program is very important, and we are always looking for innovative ways to exceed PPA in chip implementation. As part of our long-term partnership with Cadence, Samsung Foundry has used Cerebrus and the Cadence digital implementation flow on multiple applications. We've observed more than an 8% power reduction on some of our most critical blocks in just a few days versus many months of manual effort. In addition, we are using Cerebrus for automated floorplan power distribution network sizing, which has resulted in more than 50% better final design timing. Due to Cerebrus and the digital implementation flow delivering better PPA and significant productivity improvements, the solution has become a valuable addition to our DTCO program.

Sangyun Kim,
Vice President, Design Technology, Samsung Foundry

Cerebrus: The Future of Intelligent Chip Design



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Find more Cerebrus material at

www.cadence.com/go/cerebrus

- White paper
- Videos
- Product Information

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