SYNOPSYS®
Silicon to Software™

AI for EDA & EDA for AI Chip Designs

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Nov 4, 2021

AI for EDA

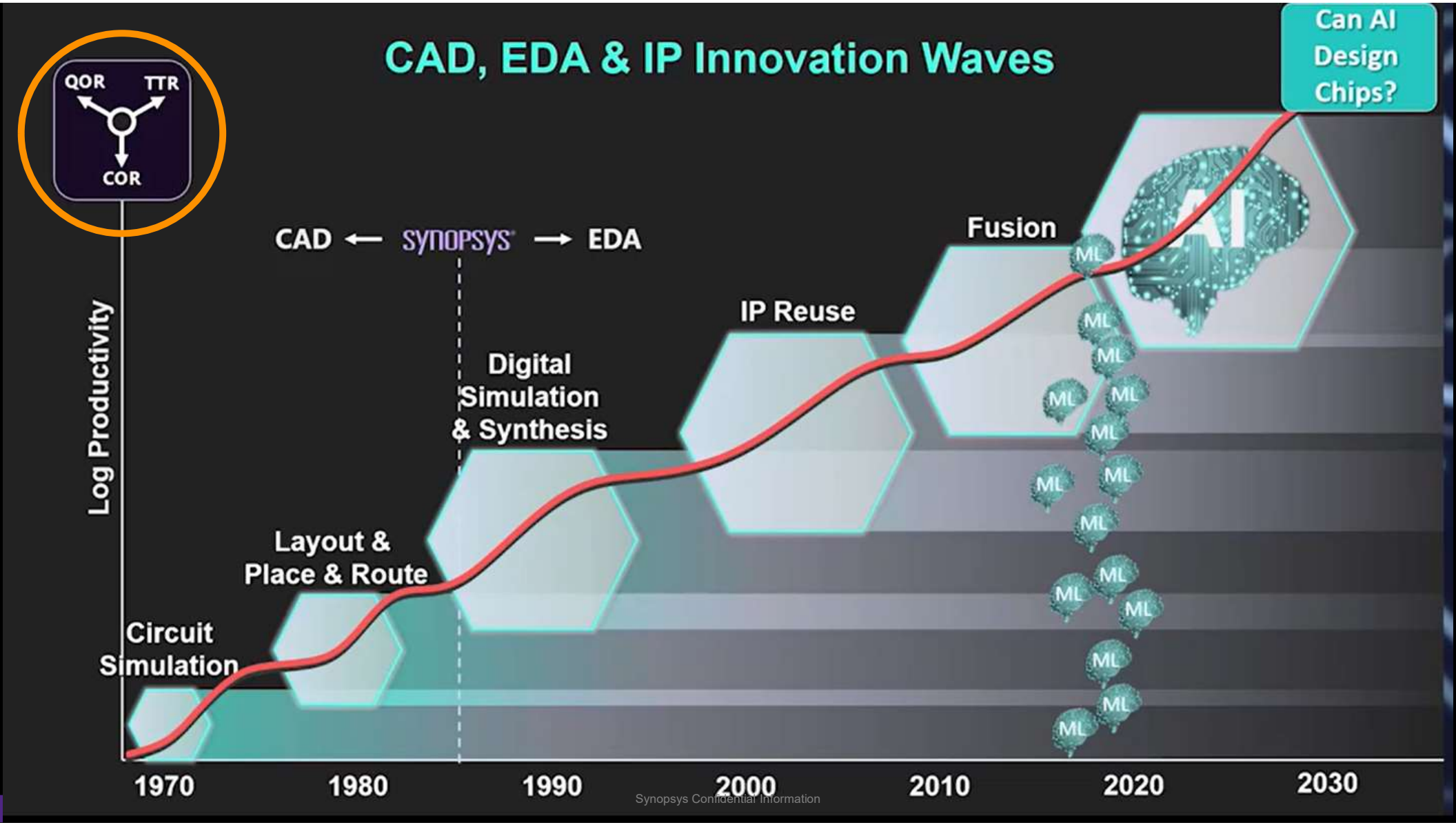
Using AI/ML to make EDA better

A tool better

AI/ML within a Tool

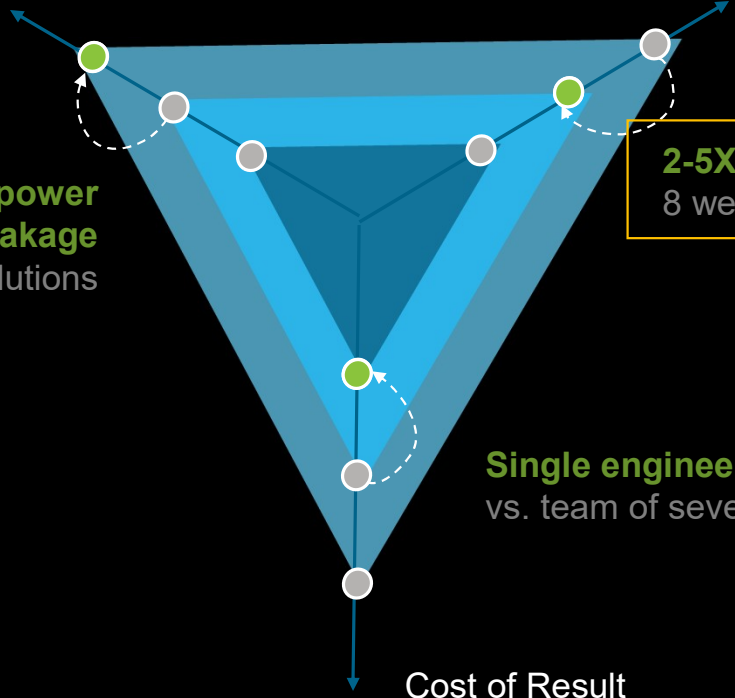
A flow better

AI/ML Around Tools



Strong Benefits of AI-Grade Productivity

Partner with a Leading US IDM



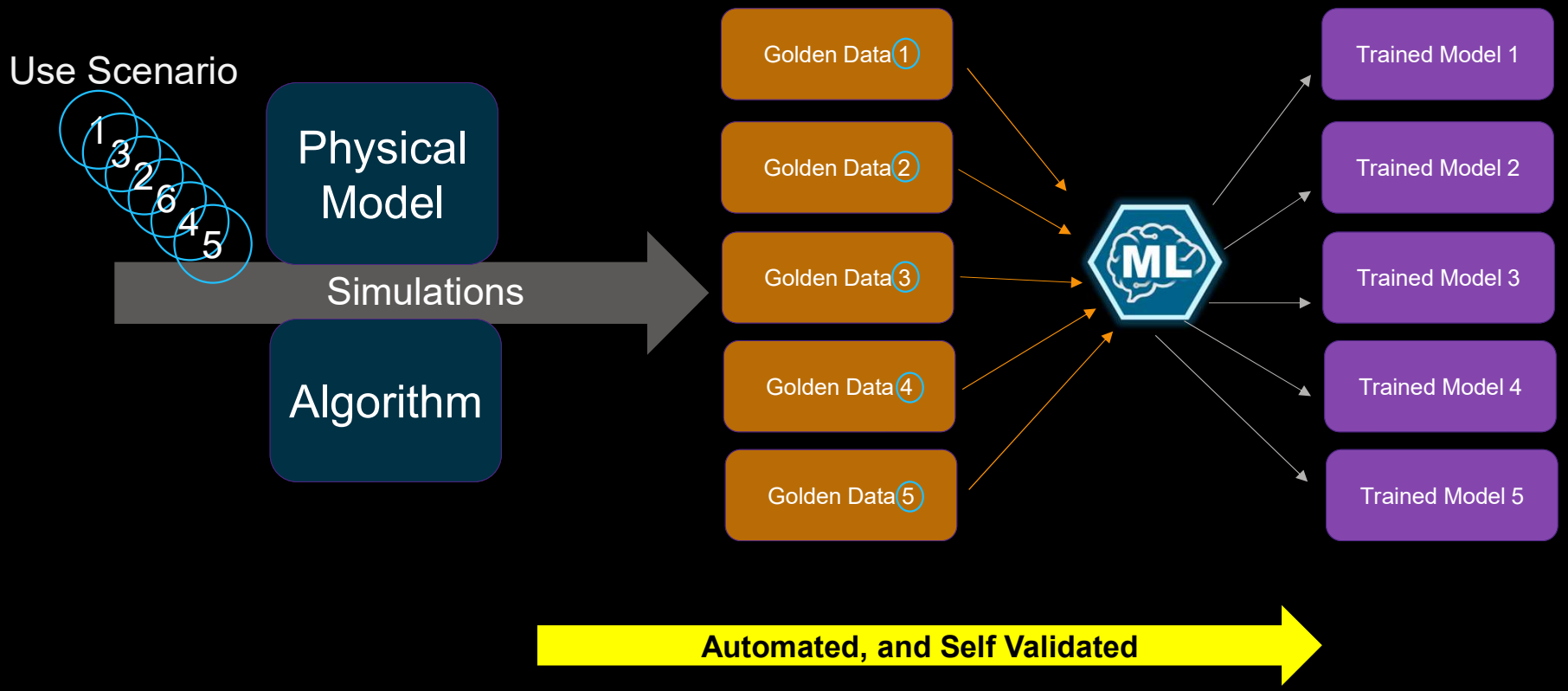
9% better total SoC power
30% better leakage
vs. manually-tuned solutions

2-5X faster convergence
8 weeks for 10 partitions

Single engineer
vs. team of several experts

- **More exploration, better PPA solutions**
- **Reduced schedules, faster product turnaround**
- **More products with current design teams**

ML is Great for TTR, Almost always !!!



Can/How ML Makes EDA Better?

AI/ML within a Tool

AI/ML Around Tools

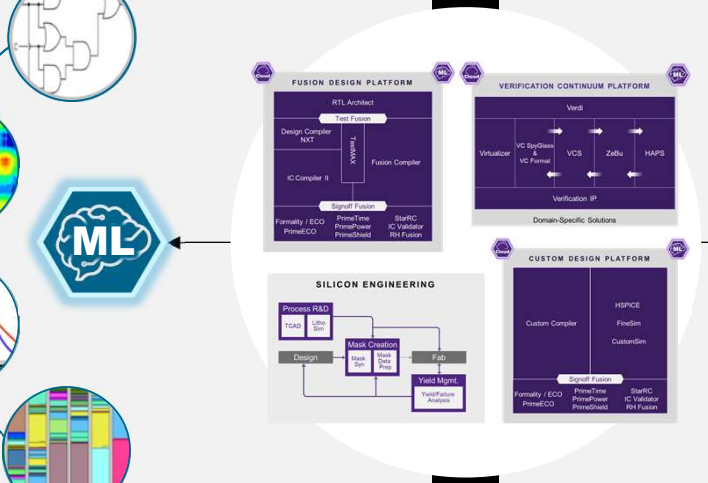
ML-Enhanced Tools

ML Optimizers
Power, timing, DRC

ML Predictors
Congestion, delay, IR-drop

ML Classifiers
DRC, criticality, yield

ML Schedulers
Memory, runtime



New AI-Driven Applications

Optimization AI Apps
Design Parameters

Debug AI Apps
Designer Assistance

Design AI Apps
Prescriptive Solutions

Quality AI Apps
Release, regression, triage

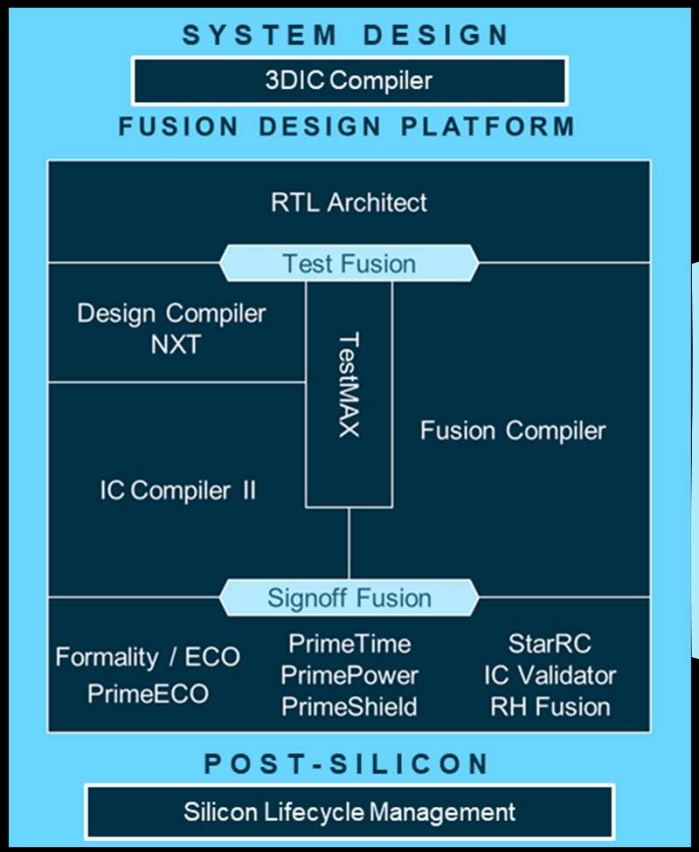
AI

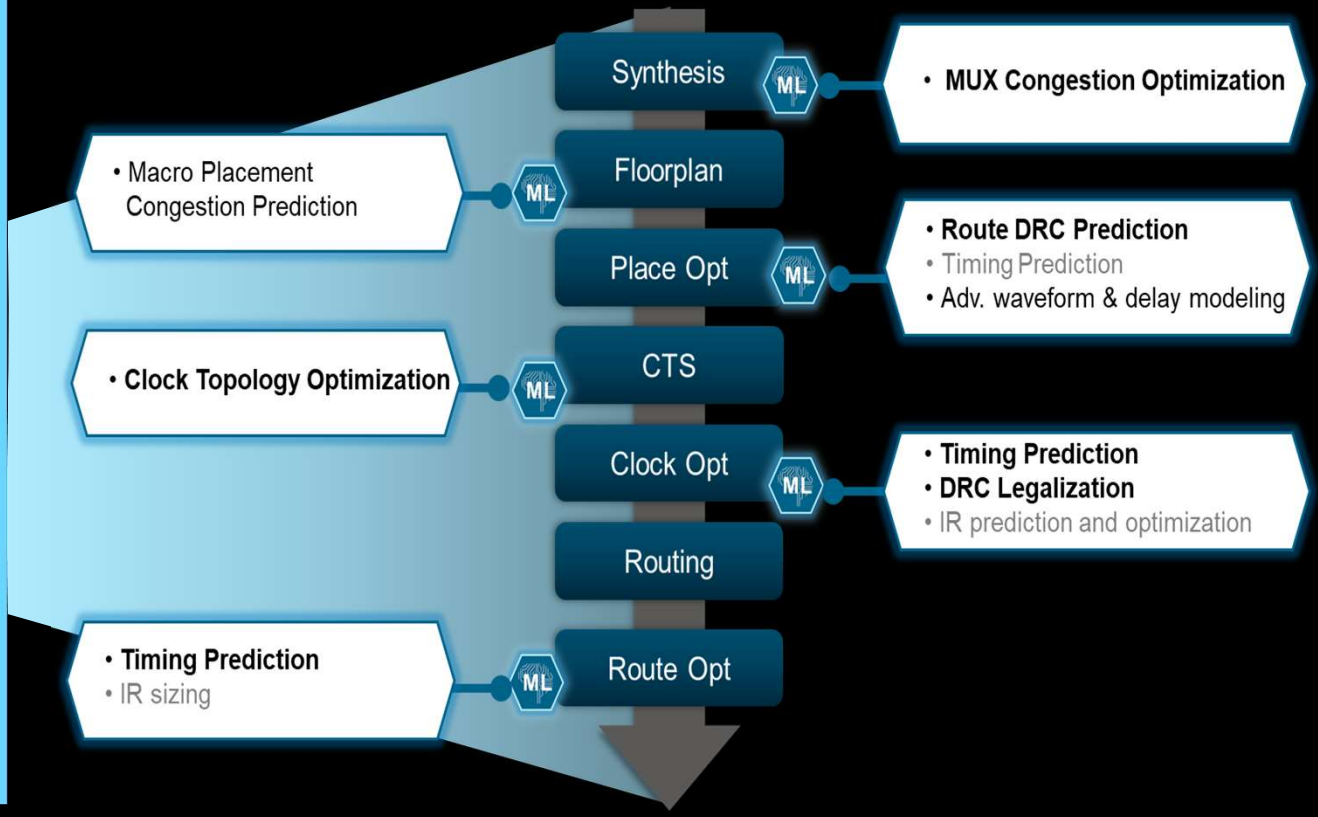
BETTER QOR, FASTER TTR

LEAP IN PRODUCTIVITY

ML-Driven Technologies Throughout **Implementation**

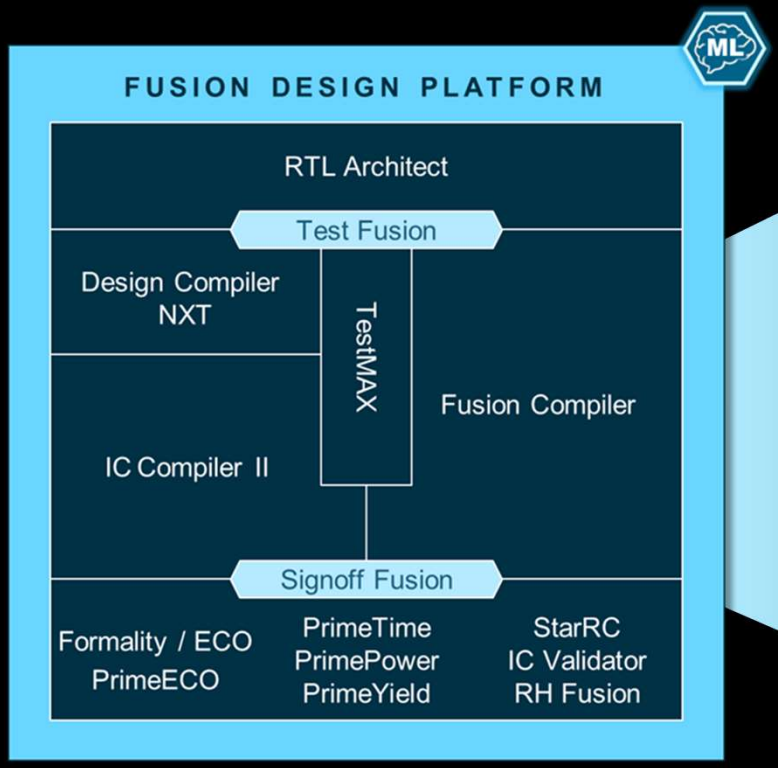
Improving PPA, Convergence and TTR

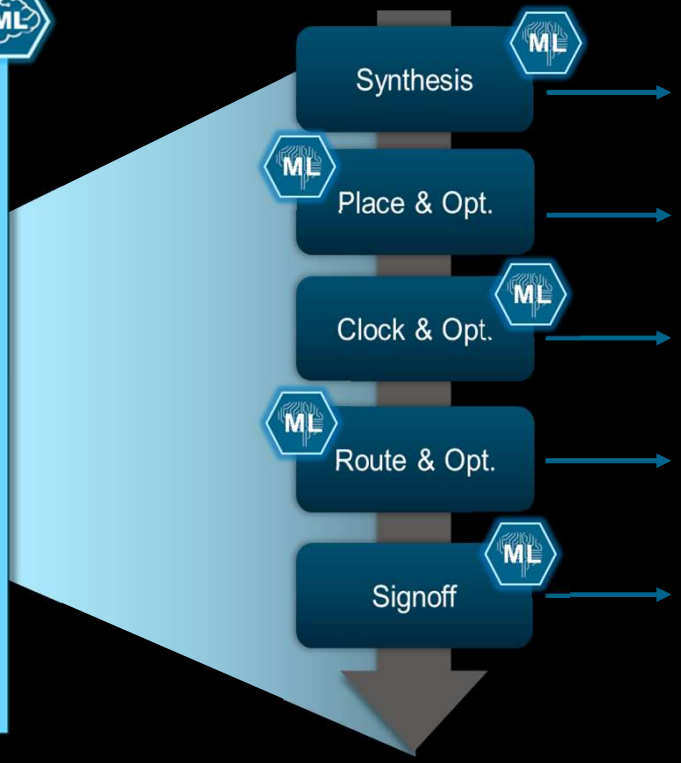




Machine-Learning Driven Digital Design and Signoff

"ML-e*verywhere*" delivering better PPA, predictable flow convergence and faster TTR

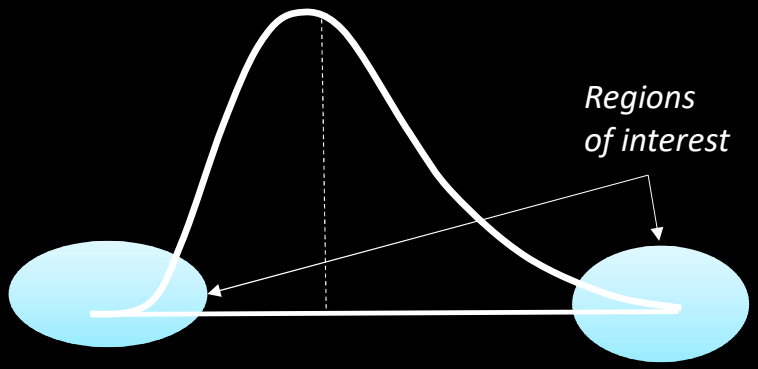




- Structural Congestion Prediction
- Macro Placement
- Advanced Waveform Prediction
- Timing (Delay) Prediction (pre-route)
- Timing (PBA) Prediction (post-route)
- Power ECO Recovery
- PBA Analysis Speedup
- Monte-Carlo Delay Prediction

Example in Analyzing ULV Variation Responses

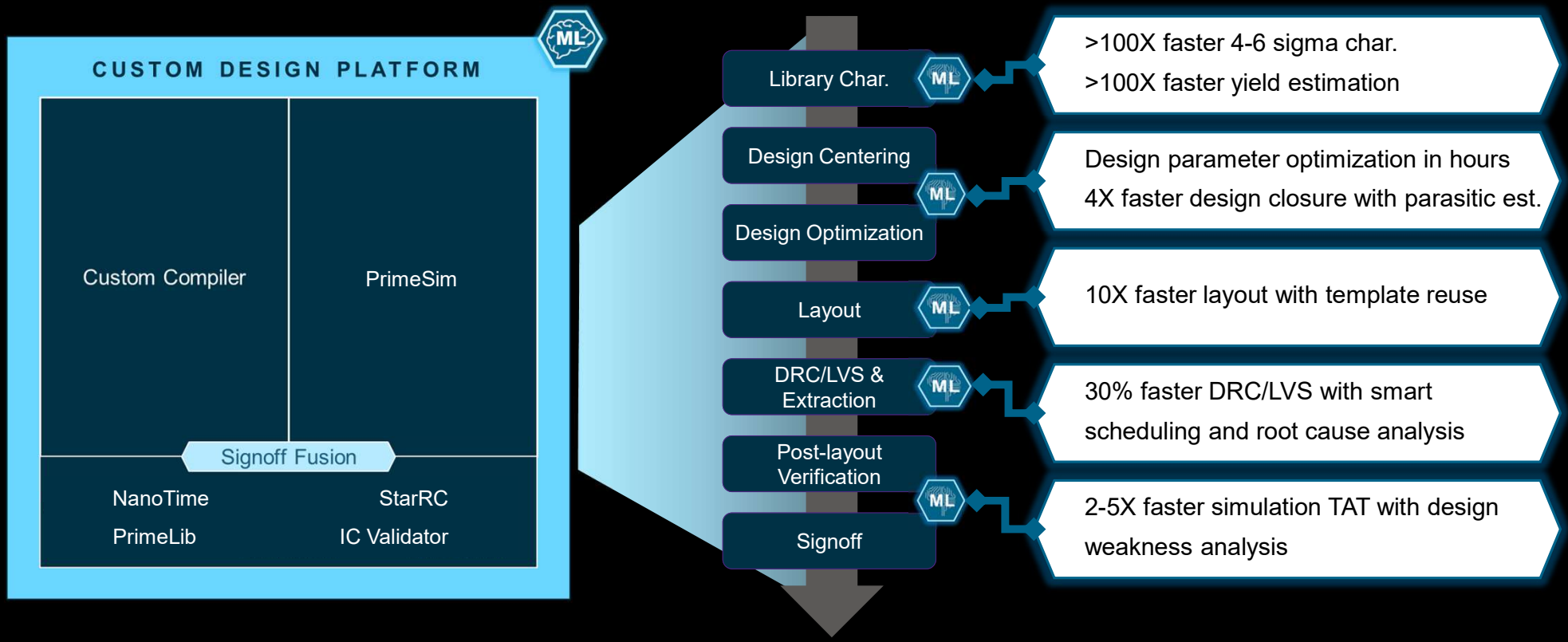
- Variation responses at ULV corners display skewed behavior
  - 3-sigma values of interest occur in the skewed/tail areas of the response



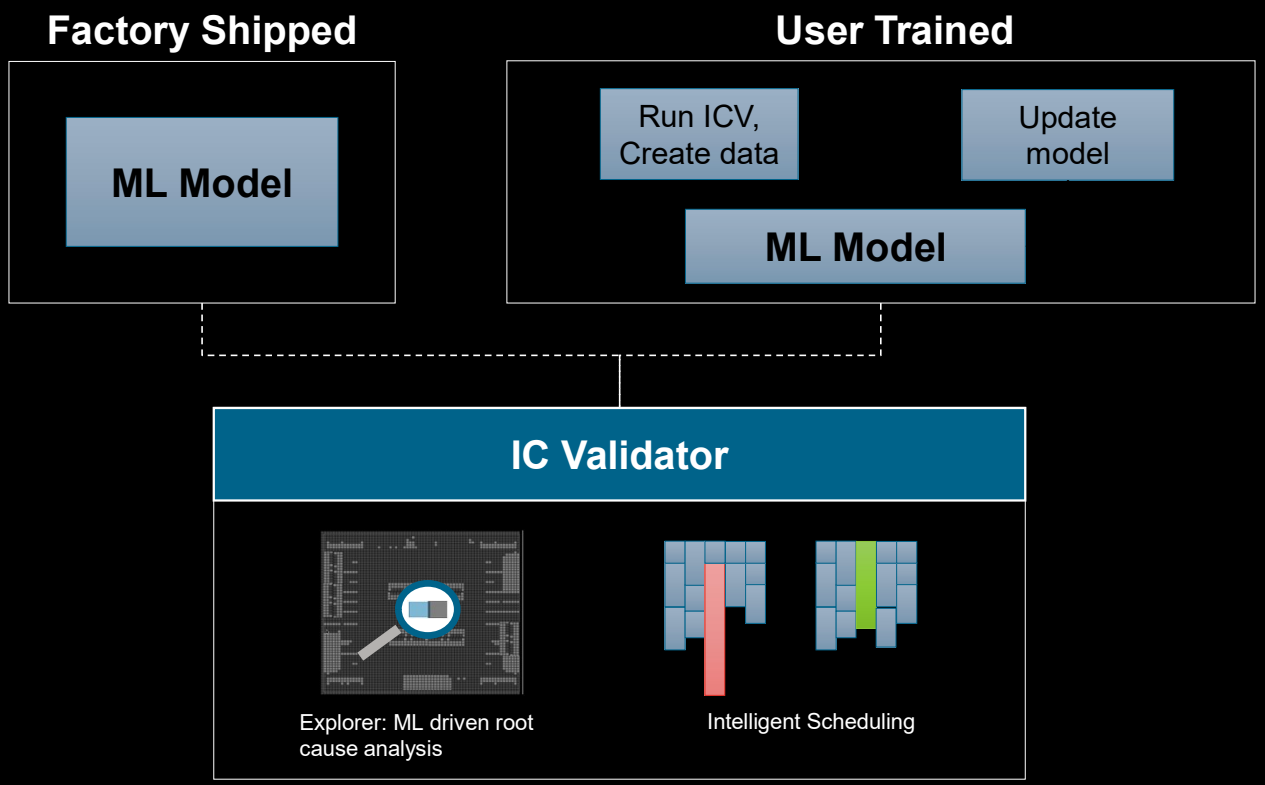
  - Simulation is required to accurately model these areas
  - Identification of these areas is crucial to managing performance and minimizing simulation effort
- ML provides a good approach to addressing this challenge

Machine Learning-Driven Custom Design

"ML-*everywhere*" enables higher design productivity and faster design-to-signoff TAT



DRC: User-site ML Model Training



- ML models shipped with IC Validator binary
- User can train the model using own data
- User site training available in 2021.06

Machine-Learning Driven Verification

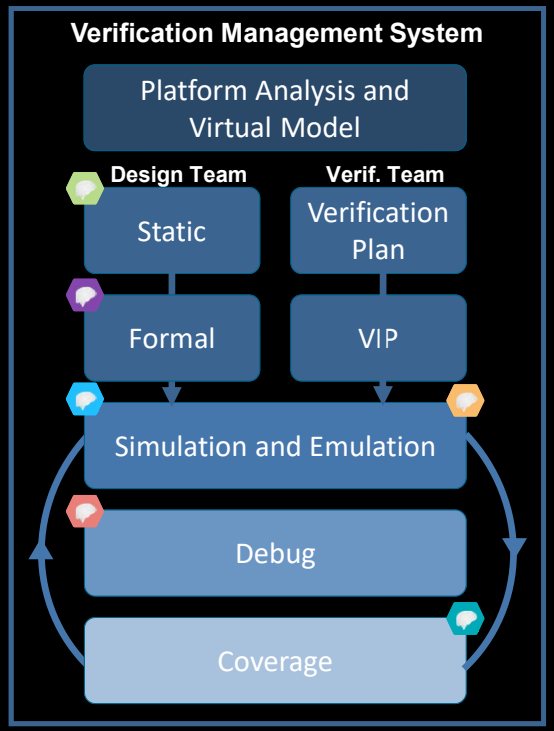
10X noise reduction with ML RCA

2X-5X runtime speedup with Regression Mode Accelerator

2X faster pre-checkin regression TAT with Intelligent Test Selection

1.3X-2X faster simulation runs with Dynamic Perf. Automation

2X-3X faster coverage convergence with Intelligent Coverage Opt.



1.25X faster FPGA compile

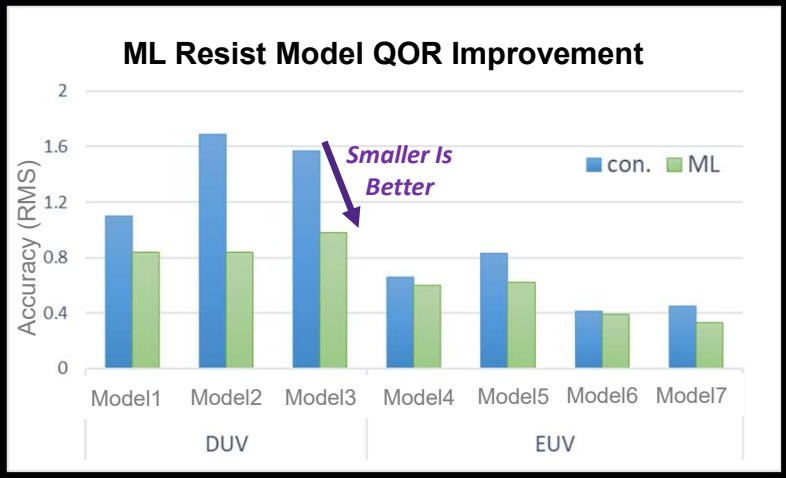
15% better timing QoR

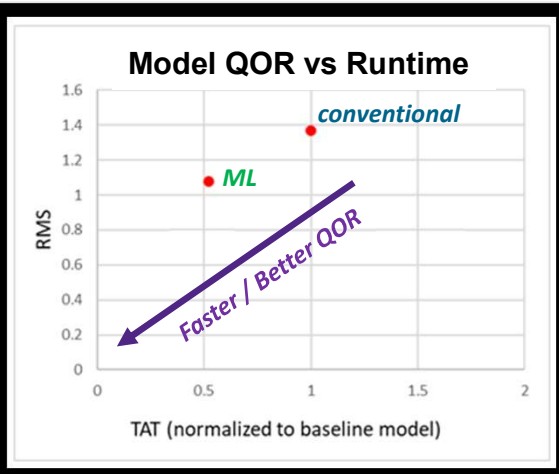
1.5X better compile resource usage

2X productive debug with Regr. Debug Automation

Proteus Machine Learning Models Offer Reduce QOR / TAT

- Machine learning OPC models provide better QOR than conventional models
  - Enables continued scaling
- ML resist models also provide faster turnaround time
  - Up to 2x runtime reduction
- Machine learning models validated by 4 major semiconductor fabs

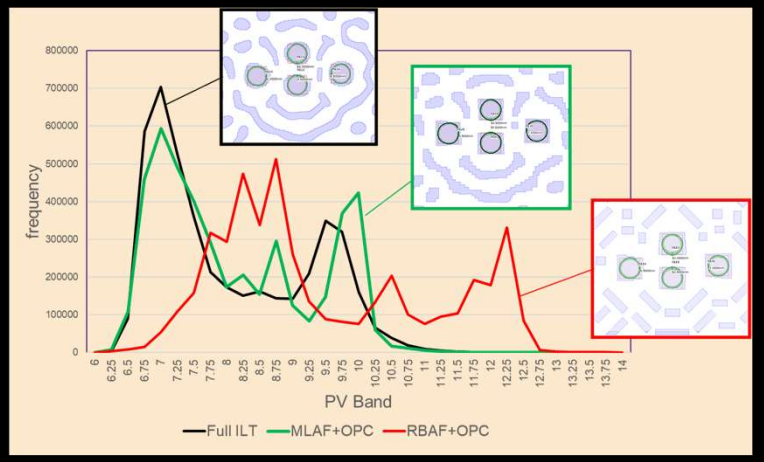




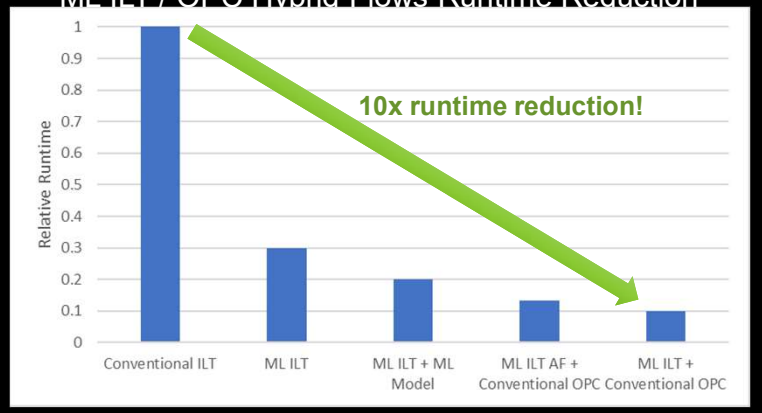
Machine Learning Correction Solutions Offer Improved QOR/TAT

- ML OPC and ILT correction with traditional models provides 2-3x runtime reduction compared to traditional OPC
  - ML models with ML correction provides an additional 2x runtime reduction with up to 2x improved QOR
- ML ILT for AF generation with traditional OPC provides full-ILT QOR but 5-10x faster than ILT
- ML ILT / OPC hybrid flows (Elastic OPC) offers ILT-like freeform correction but with OPC runtimes (10x faster)

ML ILT For AF Generation Provide ILT-Like Results

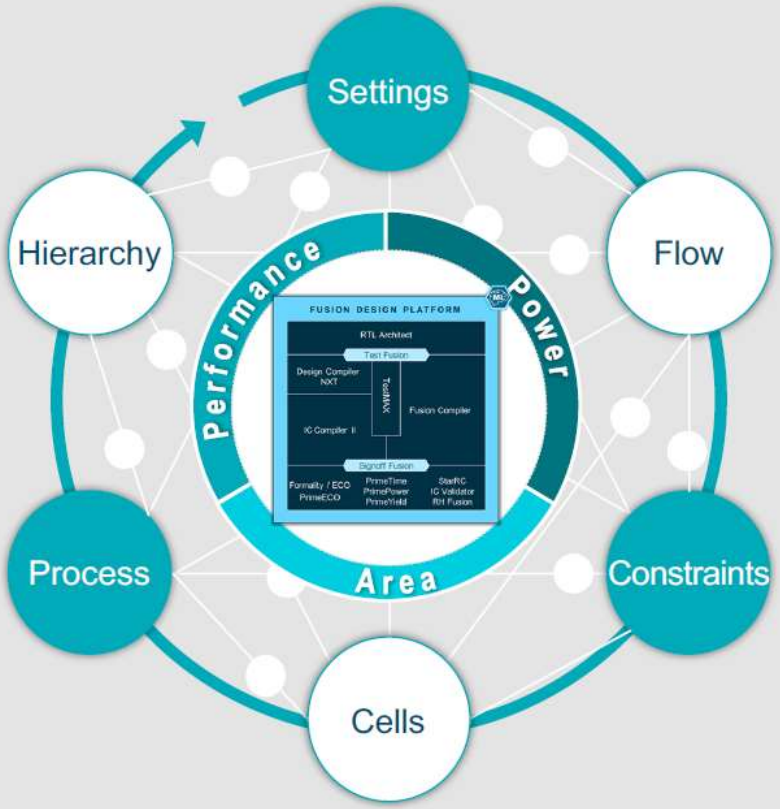


ML ILT / OPC Hybrid Flows Runtime Reduction



DSO.ai – AI-driven Design Space Optimization

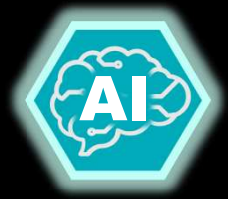
Industry's first AI application enables autonomous search for design targets



- Breakthrough reinforcement learning engine
  - Capable of exploring trillions of design recipes
- Multi-objective design space optimization
  - High-quality results from feasibility to closure
- Fully-integrated with Fusion Design Platform
  - Fast ramp-up through industry's richest technology foundation
- Cloud-ready for fast deployment
  - Supports on-prem, public, and hybrid clouds

DSO.ai: A Leap Forward In Design Productivity

Meeting design targets faster and with fewer resources across market verticals



x86 CPU Flow Optimization	**Arm Cortex-A55 CPU** Library Optimization	**Microcontroller** Library Optimization	**Custom AI Engine** Floorplan Optimization
fmax tns power **7% 5X 14%**	fmax tns pwr **5% 60X 10%**	fmax tns pwr **met 2X 28%**	area tns pwr **20% 4X 6%**
Met MHz/Watt from scratch in 3 weeks	Pushed MHz/Watt of optimized design in 4 days	Pushed leakage of optimized design in 2 weeks	Optimized floorplan for new Si process in 1 week
1 engineer	1 engineer	1 engineer	1 engineer
HPC	Mobile	Automotive	AI Accelerator

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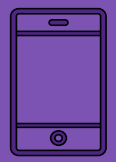
~~AI for~~ ~~EDA~~ ~~&~~ EDA for AI Chip Designs

DLA (Deep Learning Accelerators) is Everywhere

ICs Across All Markets to have AI Capabilities

MOBILE

All Premier Smartphones will integrate AI Processing Capabilities by 2021



DATA CENTER

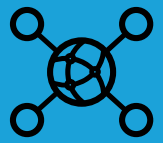
More than 50% of enterprises will deploy AI accelerators in their server infrastructure by 2022

AUTOMOTIVE

Volume production of autonomous vehicles will begin in 2023

IOT

More than 20% of IoT devices will have AI processing Capabilities by 2022



Strong Demand for AI Processing Hardware

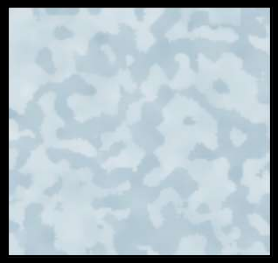
AI Market Projected To Grow to $36.8B by 2025

Artificial Intelligence Revenue, Top 10 Use Case, World Markets 2025 (M)

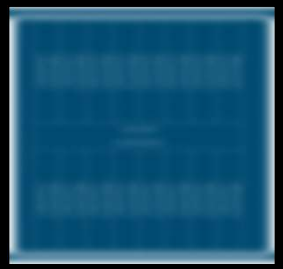
Source: Tractica

Chip Design: AI Accelerator Challenges

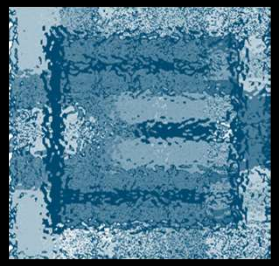
Synopsys is behind many AI Chips



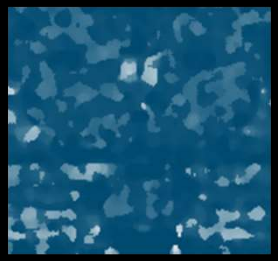
Leading GPU (NA)
5,000+ Cores
100+ TOPS Deep Learning



AI Accelerator (EU)
800+ mm^2
23+B transistors

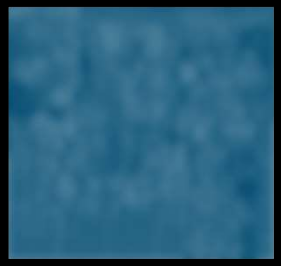


AI Accelerator (AP)
400+ mm^2
100+ TOPS Deep Learning



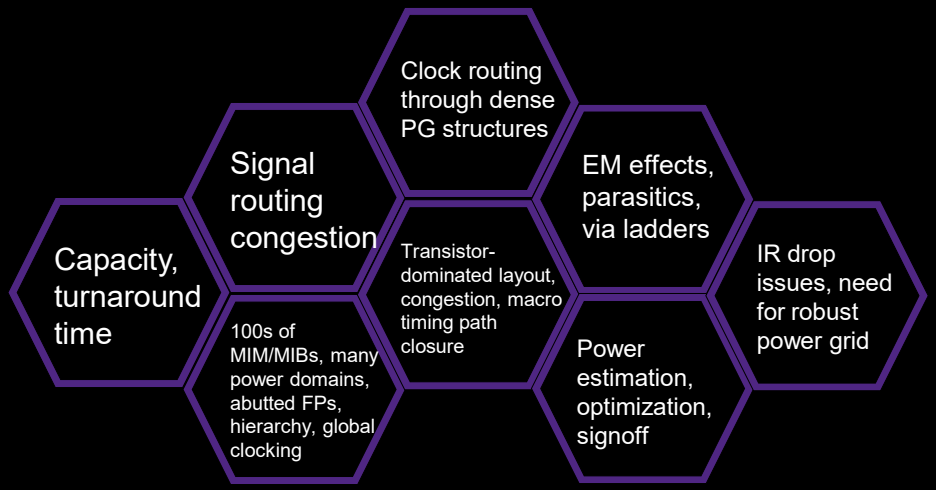
Latest Mobile AP (NA)
CNN Engine
7nm

Automotive SoC (AP)
Level 3/4 ADAS
300mW CNN Engine



Drone SoC (AP)
12nm AI IP Core
800MHz @ <3mm^2

Design Challenges

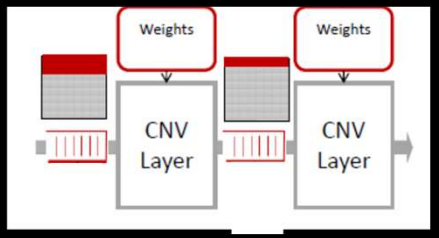


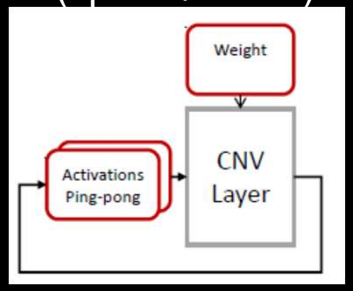
Synopsys's full-flow design platform for AI Accelerator

Broad Range of AI Accelerator Architectures

Range

CPU	GPU	FPGA	ASIC
Intel AMD ARM	NVIDIA AMD	Deephi Cambricon Teradeep Knupath	GoogleTPU Graphcore Wave Intel Nervana
Scalar processors with vector extensions	Vector-based SIMD with DL extensions	Customized micro-arch (temporal/dataflow)	Customized micro-arch (spatial/matrix)



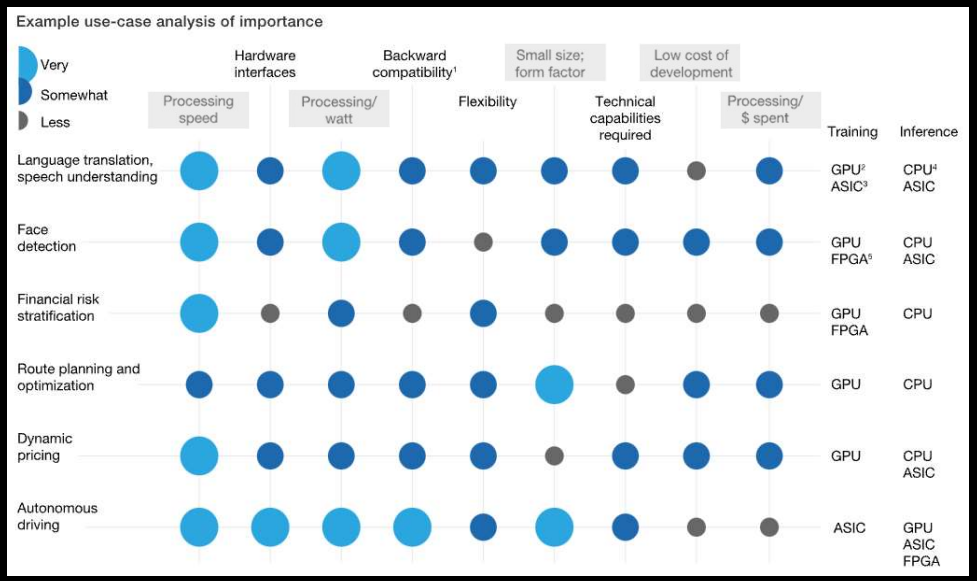


Ref: Architectures for Accelerating Deep Neural Networks, Xilinx, Hot Chips 2018

Various AI applications drive Dedicated Architecture in Hardware

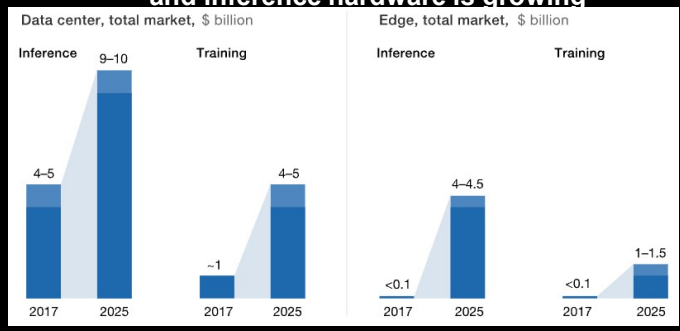
The need for exploring for better architecture for specific applications

The optimal compute architect will vary by use case



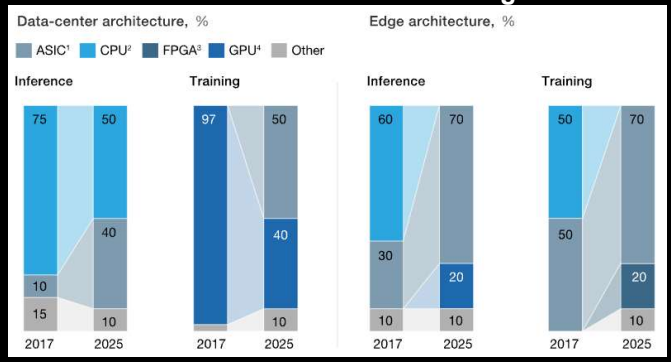
Source: McKinsey & Company

At both data centers and the edge, demand for training and inference hardware is growing



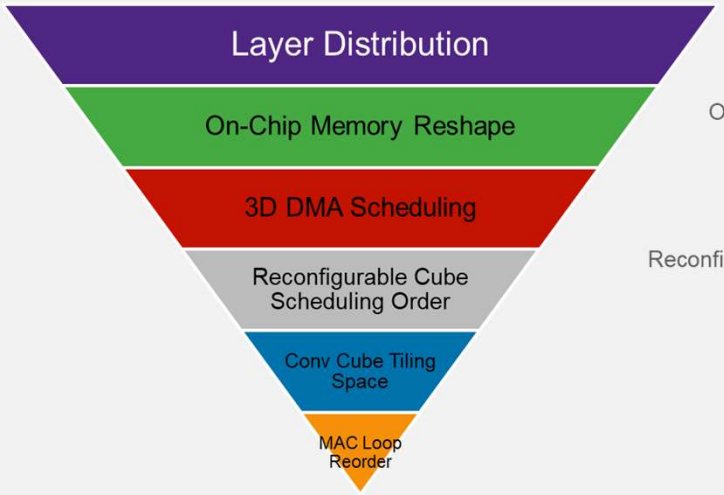
Source: McKinsey & Company

The preferred architectures for compute are shifting in data centers and the edge

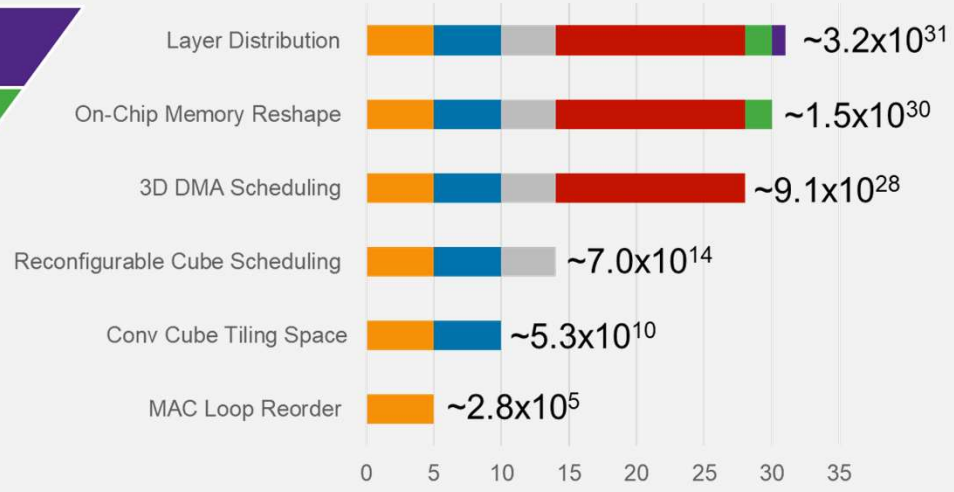


Source: McKinsey & Company

That’s how an application specific DLA architecture is defined



The actual DLA Design Exploration Space is HUGE



Challenges:

Long exploration time, can be months;

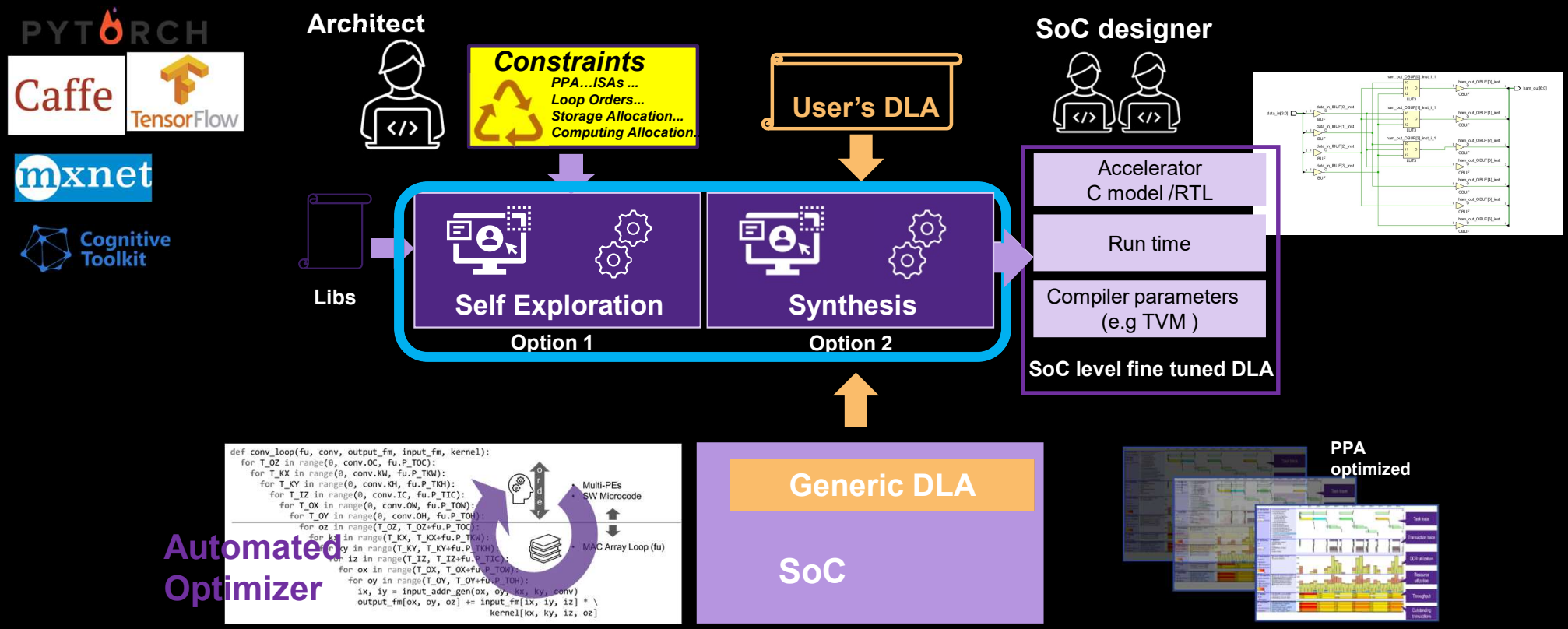
Limited exploration space;

Engineering load intensive;

High cost of human capital;

……

Should the architecting be automated?



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