



Using Machine Learning to Optimize Semiconductor Test

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Agenda

- 1 Overview of Machine Learning (ML)
- 2 Background to ML and Test
- 3 Introduction to Opens-Shorts Testing
- 4 Data Analysis Classification and Clustering
- 5 Optimizing Semiconductor Test with ML
- 6 Next Steps – Conclusion

What is Machine Learning (ML)?

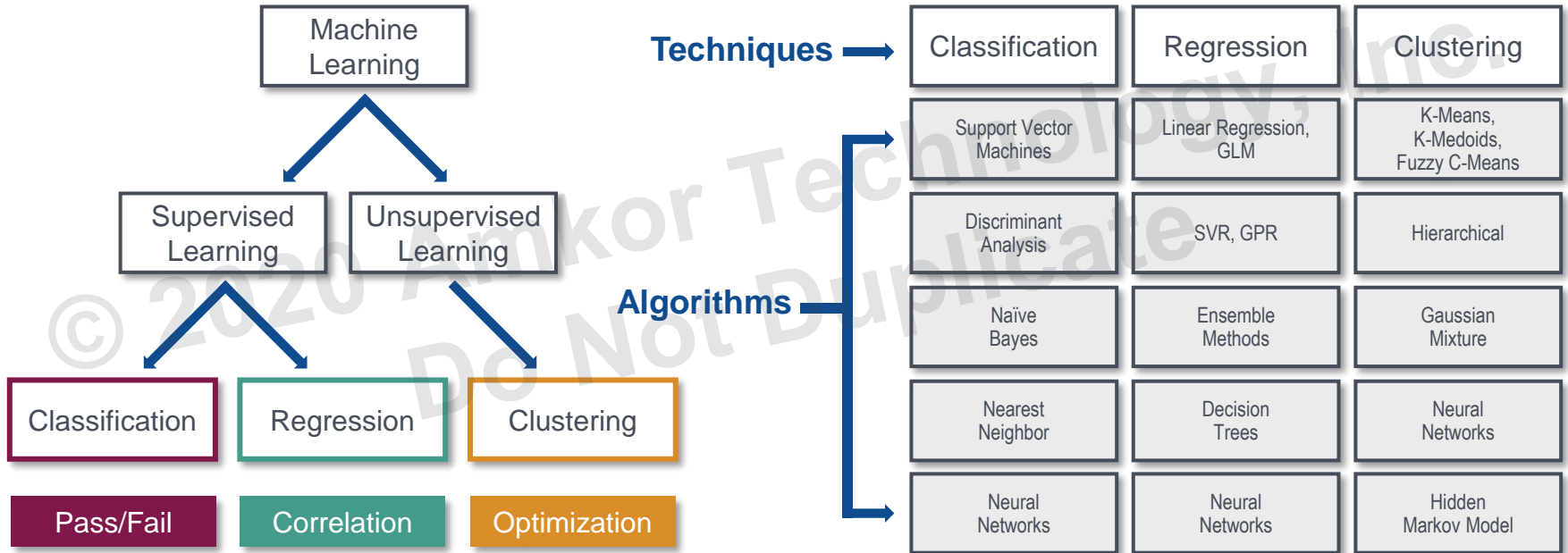
- ▶ Tom Mitchell
 - ▷ Ex-chair Machine Learning Department at Carnegie Mellon University
 - ▷ A computer program is said to learn from experience “E” with respect to some task “T” and some performance measure “P”, if its performance on “T”, as measured by “P”, improves with experience E
 - » $P\{T[E(m)]\}$
where m = number of samples
- ▶ ML in simple terms “More data makes predictions!”

Image Source: [Andrew Ng – Machine Learning Course](#)



Machine Learning

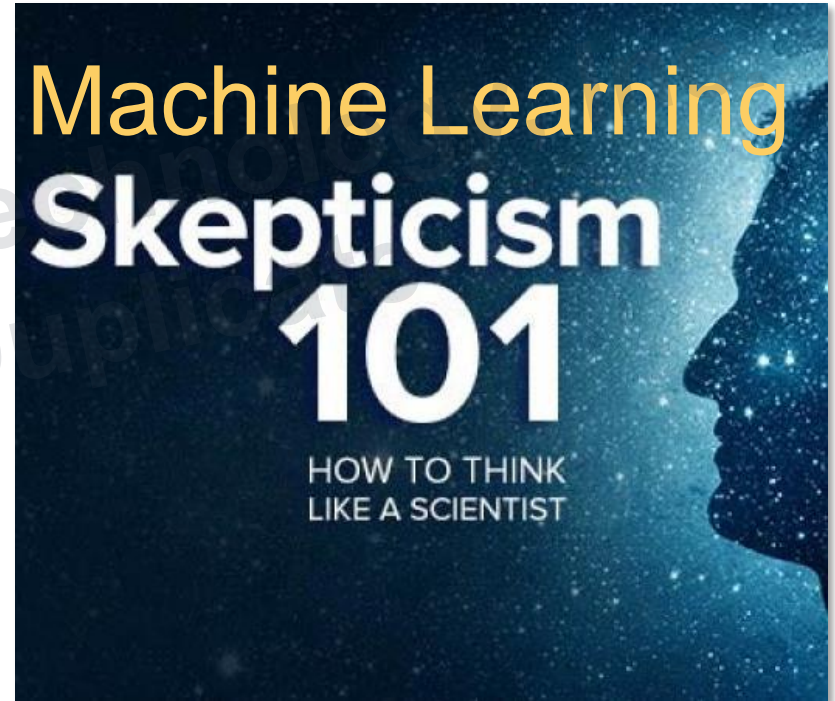
Machine Learning Techniques



Source: [Mathworks.com](https://www.mathworks.com)

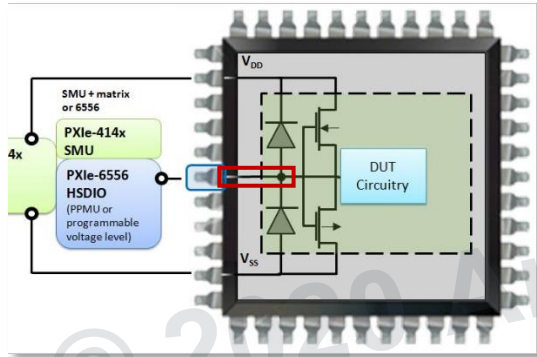
Background of ML and Semiconductor Test

- ▶ Test engineer skepticism
 - ▷ Is ML in test yet another conspiracy by “big data” companies, creating a new market to sell more products?
 - ▷ Really? Can machine learning (ML) improve semiconductor test?
 - ▷ What about product quality?
 - ▷ Who will teach the machine? ML is a new field I did not study this
 - ▷ Will I still have a job?
- ▶ Using the simple opens-shorts test, try to debunk the myth that ML has no place in semiconductor test



Source: [TheGreatCourses.com](https://www.thegreatcourses.com/courses/how-to-think-like-a-scientist/). "How to Think Like a Scientist"

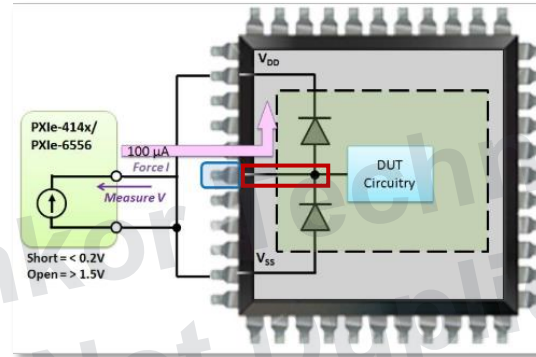
Semiconductor Testing 101 “Opens/Shorts” Test



Source: Ni.com

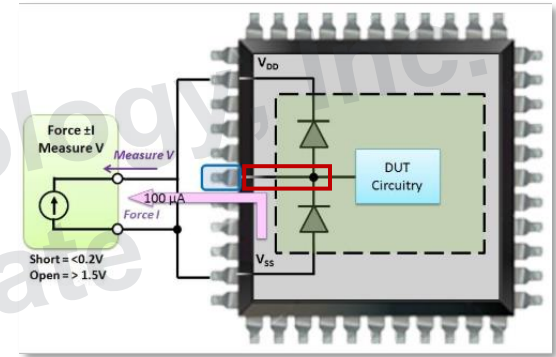
Purpose

- ▶ Verify the external pin is connected to the die
- ▶ Verify that the pin is not shorted to another



Uses ESD Diode to VDD

- ▶ Force current and measure voltage



Uses ESD Diode to VSS

- ▶ Sink current 100 uA and measure voltage. Voltage clamp set at 2V

The Device Under Test (DUT)

- ▶ DUT pin map
- ▶ Pins grouped by colors
 - ▷ Grey
 - » Power & ground
 - ▷ Green, blue, purple
 - » Input/Output

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	NC	NC	TRNG_3	TUDD	TRNG_2	TRNG_2	VSS	TRNG_3	TRNG_3	TRNG_3	A5	A5	A5	A5
B	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	NC	TRNG_3	TRNG_3	TUDD	TRNG_2	TRNG_2	VSS	TRNG_3	TRNG_3	D5	VD03.3	VD03.3	VD03.3	VD03.3
C	TRNG_3	TRNG_3	DVSS	TRNG_3	NC	TRNG_3	TRNG_3	DVSS	DVDD	DVDD	DVDD	TRNG_3	TRNG_3	TRNG_3	TRNG_3	D5	A9	A7	A2	VD03.3
D	TVSS	TVSS	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	DVDD	DVDD	DVDD	DVDD	TRNG_3	TRNG_3	TRNG_3	VSS	D8	A8	VD03.3	VD03.3	VD03.3
E	TRNG_2	TRNG_2	TRNG_3	NC	RVSS	TRNG_3	TRNG_3	DVDD	DVDD	DVDD	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	D4	A6	A4	VD03.3	MEC
F	TRNG_2	TRNG_2	TRNG_3	TRNG_3	RVSS	TRNG_3	TRNG_3	DVDD	DVDD	DVDD	VSS	DVSS	TRNG_3	VSS	RD05	D3	D2	VD03.3	VD03.3	MD0
G	TUDD	TUDD	TUDD	VSS	VSS	RVSS	VSS	TRNG_3	TRNG_3	DVSS	DVSS	VSS	JTAG_2	JTAG_2	MD03.3	VD03.3	D6	DDVP	REF_DVDD	VSS
H	RVA	TRNG_3	DVSS	TRNG_3	VSS	VSS	VSS	VSS	VSS	VSS	RVSS	RVSS	RVSS	JTAG_2	RVA	LS	NC	RVD	RVD	VSS
J	DVSS	TRNG_3	TRNG_3	DVDD	TRNG_3	VSS	VSS	VSS	VSS	VSS	TRNG_3	TRNG_3	TRNG_3	TRNG_3	VSS	VD01.8	JTAG_2	RVD	RVD	VSS
K	TRNG_3	TRNG_3	VSS	TRNG_3	VSS	VSS	VSS	VSS	TRNG_3	TRNG_3	NC	NC	TRNG_3	TRNG_3	TRNG_3	TRNG_3	JTAG_2	RVA	RVA	RVA
L	RVSS	TRNG_3	TRNG_3	VSS	VSS	VSS	VSS	VSS	TRNG_3	JTAG_2	JTAG_2	TRNG_3	JTAG_2	RVA	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3
M	TRNG_3	RVSS	RVA	TRNG_3	VSS	VSS	VSS	TRNG_3	TRNG_3	TRNG_3	TRNG_3	VSS	VD01.8	TRNG_3	TRNG_3	VSS	VD01.8	TRNG_3	TRNG_3	TRNG_3
N	TRNG_3	RVSS	TRNG_3	TRNG_3	DVSS	DVSS	RVA	DVSS	TRNG_3	TRNG_3	TRNG_3	VSS	TRNG_3	VD01.8	VD01.8	VD01.8	VD01.8	VSS	TRNG_3	TRNG_3
P	TRNG_3	TRNG_3	TRNG_3	TRNG_3	DVSS	TRNG_3	TRNG_3	DVSS	TRNG_3	TRNG_3	TRNG_3	VSS	VSS	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3
R	TRNG_3	TRNG_3	TRNG_3	TRNG_3	DVSS	DVSS	TRNG_3	TRNG_3	TRNG_3	TRNG_3	RVA	RVA	RVA	RVA	RVA	RVA	RVA	RVA	RVA	RVA
T	TRNG_3	TRNG_3	DVSS	DVSS	DVSS	TRNG_3	RVA	TRNG_3	TRNG_3	RVA	RVA	RVA	RVA	VD01.8	RVA	RVA	RVA	RVA	RVA	RVA
U	TRNG_3	TRNG_3	NC	TRNG_3	DVSS	DVSS	TRNG_3	TRNG_3	DVSS	DVSS	RVA	RVA	VSS	TRNG_3	VSS	RVA	RVA	RVA	RVA	RVA
V	TRNG_3	TUDD	NC	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	DVSS	RVA	RVA	RVA	RVA	RVA	RVA	RVA	RVA
W	TRNG_3	TUDD	TRNG_3	TRNG_3	RVA	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TUDD	RVA	RVA	RVA	VD01.8	RVA	RVA	RVA	RVA	RVA	RVA
Y	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	VSS	TRNG_3	TRNG_3	TUDD	RVA	VSS	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3	TRNG_3

Source: [MaximIntegrated.com](https://www.maximintegrated.com)

Test Method – I/O Pins

- ▶ Example: Testing pin A2
 - ▷ All other pins are grounded
 - ▷ V clamp = 2V
 - ▷ I force = 100 uA
 - ▷ Measure voltage on the pin
- ▶ Fail condition
 - ▷ Pins shorted
 - » Measured voltage: $0.2 < V$
 - ▷ Pin is open
 - » Measured voltage: $V > 1.5$

Device Under Test

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	TEST1	TEST2	TEST3	TEST4	TEST5	NC	NC	TEST9	TEST10	TEST11	TEST12	VSS	TEST14	TEST15	TEST16	D1	A5	A6	A1
B	DVSS	DVSS	TEST1	TEST2	TEST3	DVDD	NC	TEST7	TEST8	TEST10	TEST11	TEST12	VSS	TEST14	D6	VDD3.3	VDD3.3	A3	VDD3.3	VDD3.3
C	TEST1	TEST2	DVSS	TEST4	NC	TEST5	TEST6	TEST7	DVDD	DVDD	TEST11	TEST12	TEST13	TEST14	D7	A8	A7	A2	VDD3.3	REF_CLK
D	VSS	DVSS	TEST1	TEST2	TEST3	NC	TEST5	DVDD	DVDD	DVDD	DVDD	TEST11	TEST12	TEST13	VSS	D5	A8	VDD3.3	VDD3.3	VDD3.3
E	TEST1	TEST2	TEST3	NC	VSS	TEST5	MODEC	DVDD	DVDD	DVDD	TEST11	TEST12	TEST13	TEST14	B1	D4	A6	A4	VDD3.3	MISC
F	TEST1	TEST2	TEST3	TEST4	VSS	TEST5	RVD0	DVDD	DVDD	DVDD	VSS	DVSS	TEST13	VSS	RDD0	D3	D2	VDD3.3	VDD3.3	MISO
G	TEST1	TEST2	TEST3	VSS	VSS	VSS	VSS	TEST7	TEST8	DVSS	DVSS	VSS	TEST13	TEST14	MODEC	VDD3.3	D0	GPIO	REF_CLK	VSS
H	TEST1	TEST2	DVSS	TEST4	VSS	VSS	VSS	VSS	VSS	VSS	TEST10	VSS	VSS	TEST13	TEST14	TEST15	NC	A0	TEST19	VSS
J	DVSS	TEST1	TEST2	DVDD	TEST5	VSS	VSS	VSS	VSS	TEST10	VSS	TEST11	TEST12	TEST13	VSS	VDD1.8	TEST16	A0	TEST19	VSS
K	TEST1	TEST2	VSS	TEST4	VSS	VSS	VSS	VSS	TEST10	TEST11	NC	NC	TEST13	TEST14	TEST15	TEST16	TEST17	TEST18	TEST19	TEST20
L	VSS	TEST1	TEST2	VSS	VSS	VSS	VSS	VSS	TEST10	TEST11	TEST12	TEST13	TEST14	TEST15	TEST16	TEST17	TEST18	TEST19	TEST20	TEST21
M	TEST1	VSS	TEST3	TEST4	VSS	VSS	VSS	TEST7	TEST8	TEST9	TEST10	VSS	VDD1.8	TEST14	TEST15	VSS	VDD1.8	TEST19	TEST20	TEST21
N	TEST1	VSS	TEST3	TEST4	DVSS	DVSS	TEST7	DVSS	TEST9	TEST10	TEST11	VSS	TEST13	VDD1.8	VDD1.8	VDD1.8	VDD1.8	VSS	TEST20	TEST21
P	RVD0	TEST1	TEST2	TEST3	DVSS	TEST5	TEST6	DVSS	TEST9	TEST10	TEST11	VSS	VSS	TEST13	TEST14	TEST15	TEST16	TEST17	TEST18	TEST19
R	TEST1	TEST2	TEST3	TEST4	DVSS	DVSS	TEST7	RVD0	TEST9	TEST10	VSS	VSS	TEST13	TEST14	TEST15	TEST16	TEST17	TEST18	TEST19	TEST20
T	TEST1	VSS	DVSS	DVSS	DVSS	DVSS	TEST7	VSS	TEST9	VSS	TEST11	TEST12	TEST13	TEST14	TEST15	TEST16	TEST17	TEST18	TEST19	TEST20
U	TEST1	VSS	NC	TEST4	DVSS	DVSS	TEST6	TEST7	DVSS	DVSS	TEST11	TEST12	VSS	TEST14	VSS	TEST16	TEST17	TEST18	TEST19	TEST20
V	TEST1	TEST2	NC	TEST4	TEST5	TEST6	TEST7	TEST8	TEST9	DVSS	TEST11	TEST12	TEST13	VSS	TEST15	TEST16	TEST17	TEST18	TEST19	TEST20
W	TEST1	TEST2	TEST3	TEST4	TEST5	TEST6	TEST7	TEST8	TEST9	TEST10	TEST11	TEST12	TEST13	VDD1.8	TEST15	TEST16	TEST17	TEST18	TEST19	TEST20
Y	TEST1	TEST2	TEST3	TEST4	TEST5	TEST6	VSS	TEST8	TEST9	TEST10	TEST11	VSS	TEST13	TEST14	TEST15	TEST16	TEST17	TEST18	TEST19	TEST20

Source: [MaximIntegrated.com](https://www.maximintegrated.com)

Power and Ground

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	TVSS	TVSS	TVSS	TVSS	TVSS	NC	NC	TVSS	VDD	TVSS	TVSS	TVSS	TVSS	TVSS	VSS	D1	A8	A2	A1
B	DVSS	DVSS	TVSS	TVSS	TVSS	DVDD	NC	TVSS	VDD	TVSS	TVSS	TVSS	TVSS	TVSS	D8	VDD3.3	VDD3.3	A3	VDD3.3	VDD3.3
C	TVSS	TVSS	DVSS	TVSS	TVSS	TVSS	TVSS	TVSS	DVDD	DVDD	DVDD	DVDD	TVSS	TVSS	D7	A9	A7	A2	VDD3.3	REF_DCA
D	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	DVDD	DVDD	DVDD	DVDD	DVDD	TVSS	TVSS	TVSS	VSS	D8	A8	VDD3.3	VDD3.3	VDD3.3
E	TVSS	TVSS	TVSS	NC	RVS	RTP	MODEC	DVDD	DVDD	DVDD	TVSS	TVSS	TVSS	TVSS	REF	D4	A6	A4	VDD3.3	MD
F	TVSS	TVSS	TVSS	TVSS	RVS	TVSS	VDD	DVDD	DVDD	DVDD	VSS	DVSS	TVSS	VSS	REF	D3	D2	VDD3.3	VDD3.3	MD
G	VDD	VDD	TVSS	VSS	VSS	RVS	VSS	TVSS	TVSS	DVSS	DVSS	VSS	TVSS	TVSS	MODEC	VDD3.3	D5	D6	REF	REF
H	TVSS	VSS	DVSS	TVSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RVS	RVS	TVSS	REF	D5	NC	REF	REF
J	DVSS	TVSS	TVSS	DVDD	TVSS	VSS	VSS	VSS	VSS	TVSS	RVS	TVSS	TVSS	RVS	VSS	VDD1.8	TVSS	REF	REF	VSS
K	TVSS	TVSS	VSS	TVSS	VSS	VSS	VSS	VSS	TVSS	TVSS	NC	NC	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
L	RVS	TVSS	TVSS	VSS	VSS	VSS	VSS	VSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
M	TVSS	RVS	TVSS	TVSS	VSS	VSS	VSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
N	RTP	RVS	TVSS	TVSS	DVSS	DVSS	TVSS	DVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
P	TVSS	TVSS	TVSS	TVSS	DVSS	TVSS	TVSS	DVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
R	TVSS	TVSS	TVSS	TVSS	DVSS	DVSS	TVSS	TVSS	TVSS	TVSS	RVS	VSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
T	TVSS	TVSS	DVSS	DVSS	DVSS	DVSS	TVSS	RVS	RTP	RVS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
U	TVSS	TVSS	NC	TVSS	DVSS	DVSS	TVSS	TVSS	DVSS	DVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
V	TVSS	VDD	NC	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	DVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
W	TVSS	VDD	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	VDD	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS
Y	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	VDD	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS

Source: [MaximIntegrated.com](https://www.maximintegrated.com)

▶ Connectivity to VDD

- ▷ VDD 3.3
- ▷ VDD 1.2
- ▷ VDD 1.8

- ▷ DVDD
- ▷ TVDD

▶ Connectivity to VSS

- ▷ VSS
- ▷ TVSS
- ▷ DVSS

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Test Method – Power & Ground

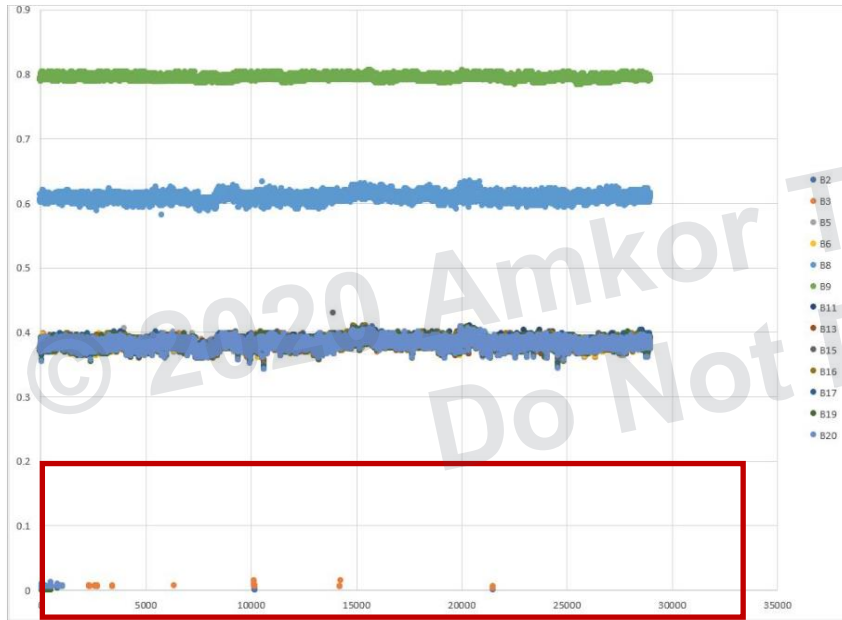
- ▶ Example: Testing pin A1 (Vss)
 - ▷ All other pins are open
 - ▷ Next Vss pin forms the return path
 - ▷ I force = 100 mA, clamp 0.5V
 - ▷ Measure voltage on the pin
 - ▷ Repeat for all pins in the group
 - ▷ 4W test (ideal)

- ▶ Fail condition
 - ▷ Pin is open
 - » Measured voltage: $V > 0.1V$

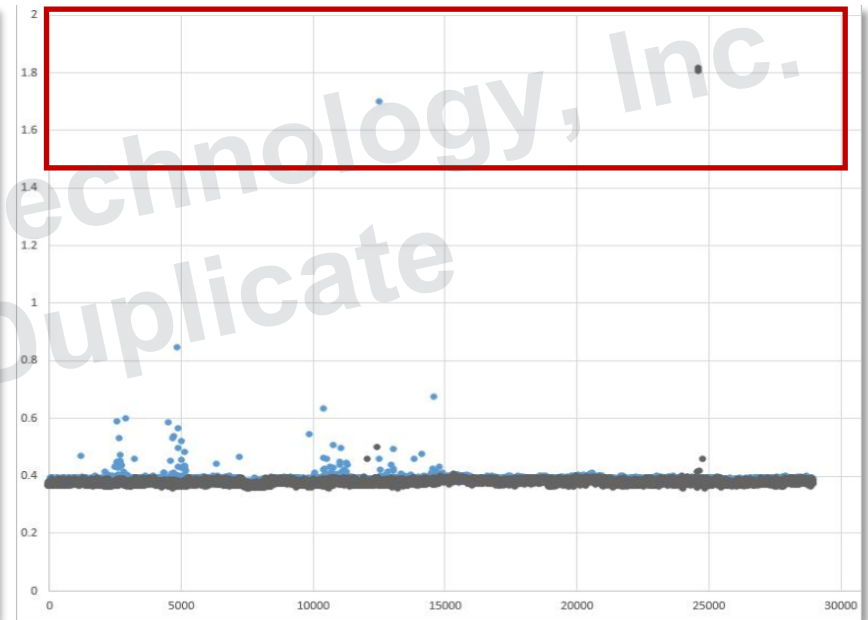
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	TPIN3	TPIN3	TPIN3A	TPIN3	TPIN3A	NC	NC	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
B	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	NC	NC	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
C	TPIN3	TPIN3	DVSS	TPIN3	NC	TPIN3	TPIN3	TPIN3	DVSS	DVSS	DVSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
D	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	TVSS	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD
E	TPIN3	TPIN3	TPIN3	NC	RVIN	TPIN3	TPIN3	DVDD	DVDD	DVDD	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
F	TPIN3	TPIN3	TPIN3	TPIN3	RVIN	TPIN3	RVIN	DVDD	DVDD	DVDD	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
G	TVDD	TVDD	TVDD	VSS	VSS	RVIN	VSS	TPIN3	TPIN3	DVSS	DVSS	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
H	RVIN	TPIN3	DVSS	TPIN3	VSS	VSS	VSS	VSS	VSS	VSS	RVIN	RVIN	RVIN	RVIN	RVIN	RVIN	RVIN	RVIN	RVIN	RVIN
J	DVSS	TPIN3	TPIN3	DVDD	TPIN3	VSS	VSS	VSS	VSS	TPIN3	RVIN	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
K	TPIN3	RVIN	VSS	RVIN	VSS	VSS	VSS	VSS	TPIN3	TPIN3	NC	NC	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
L	RVIN	TPIN3	RVIN	VSS	VSS	VSS	VSS	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
M	TPIN3	RVIN	RVIN	TPIN3	VSS	VSS	VSS	TPIN3	TPIN3	TPIN3	TPIN3	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
N	TPIN3	RVIN	TPIN3	TPIN3	DVSS	DVSS	RVIN	DVSS	TPIN3	TPIN3	TPIN3	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
P	RVIN	TPIN3	TPIN3	TPIN3	DVSS	TPIN3	TPIN3	DVSS	TPIN3	TPIN3	TPIN3	VSS	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
R	TPIN3	TPIN3	TPIN3	TPIN3	DVSS	DVSS	TPIN3	RVIN	TPIN3	RVIN	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
T	TPIN3	TVSS	DVSS	DVSS	DVSS	DVSS	TPIN3	RVIN	TPIN3	RVIN	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
U	TPIN3	TVSS	NC	TPIN3	DVSS	DVSS	TPIN3	DVSS	DVSS	DVSS	TPIN3	TPIN3	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
V	TPIN3	TVDD	NC	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	DVSS	TPIN3	TPIN3	TPIN3	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
W	TPIN3	TVDD	TPIN3	TPIN3	RVIN	RVIN	TVSS	TPIN3	TPIN3	TPIN3	DVDD	TPIN3	TPIN3	TPIN3	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3
Y	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TVSS	TPIN3	TPIN3	TPIN3	DVDD	TPIN3	VSS	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3	TPIN3

Source: [MaximIntegrated.com](https://www.maximintegrated.com)

Classification (Pass/Fail) Training Using ML

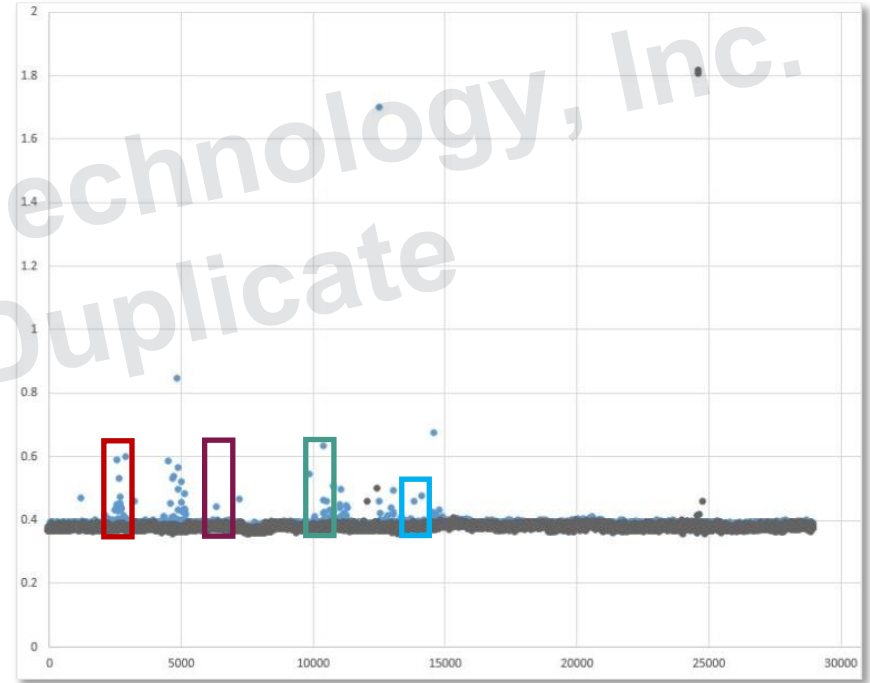
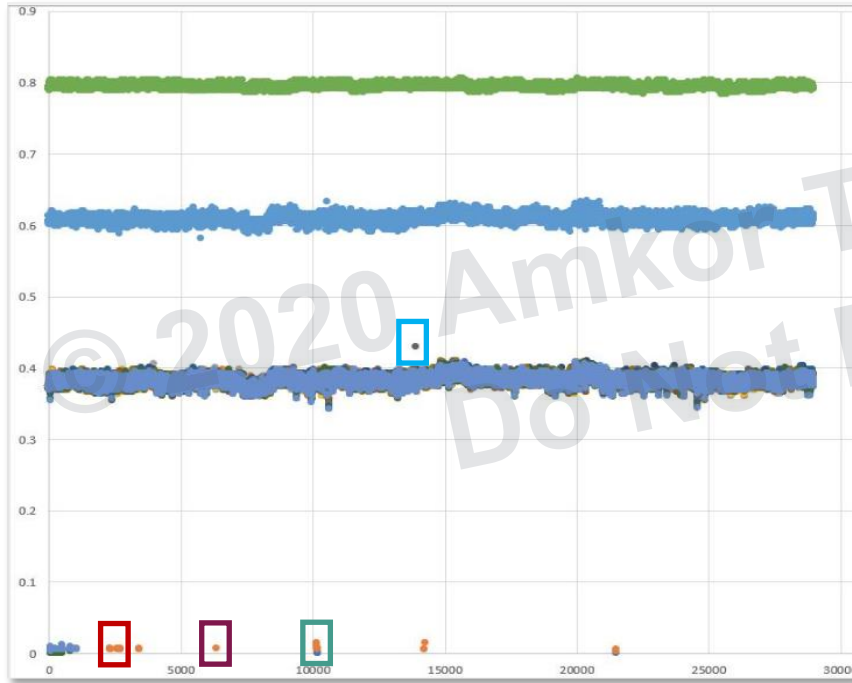


Pins failing with shorts $< 0.2V$

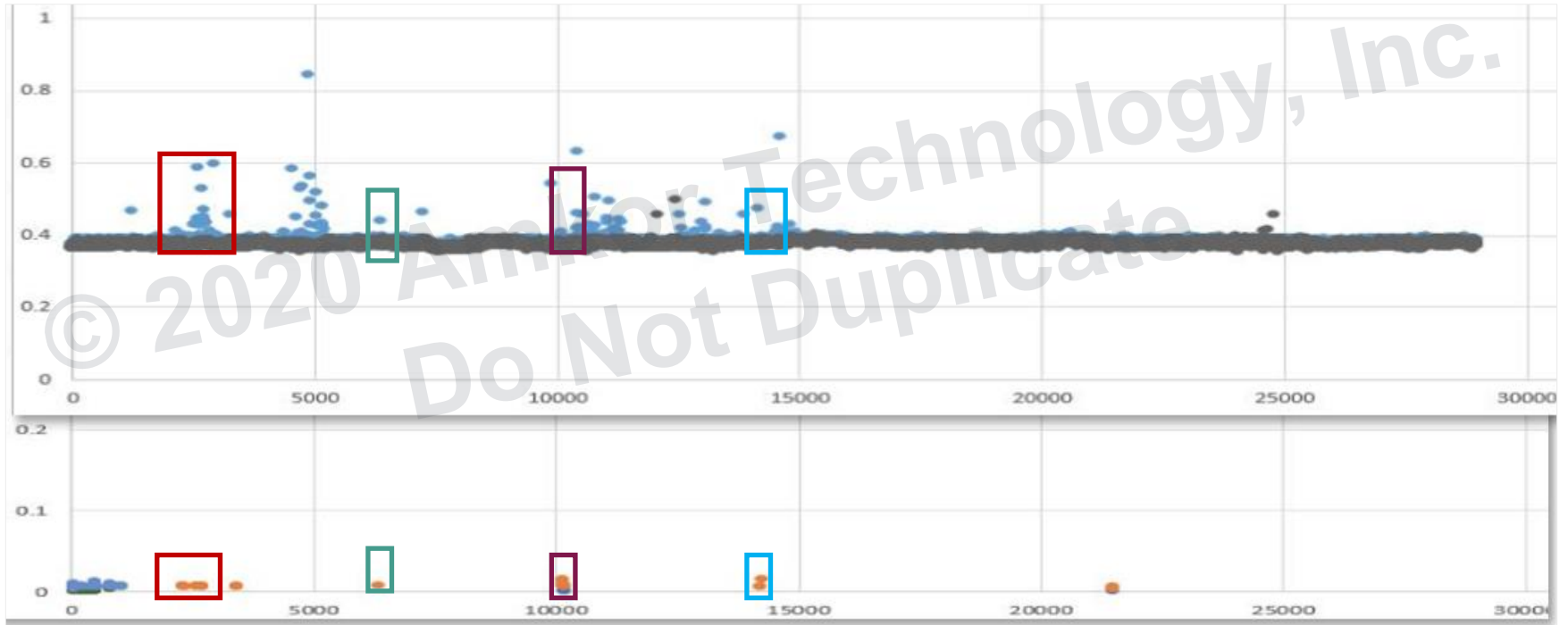


Pins failing with opens $> 1.5V$

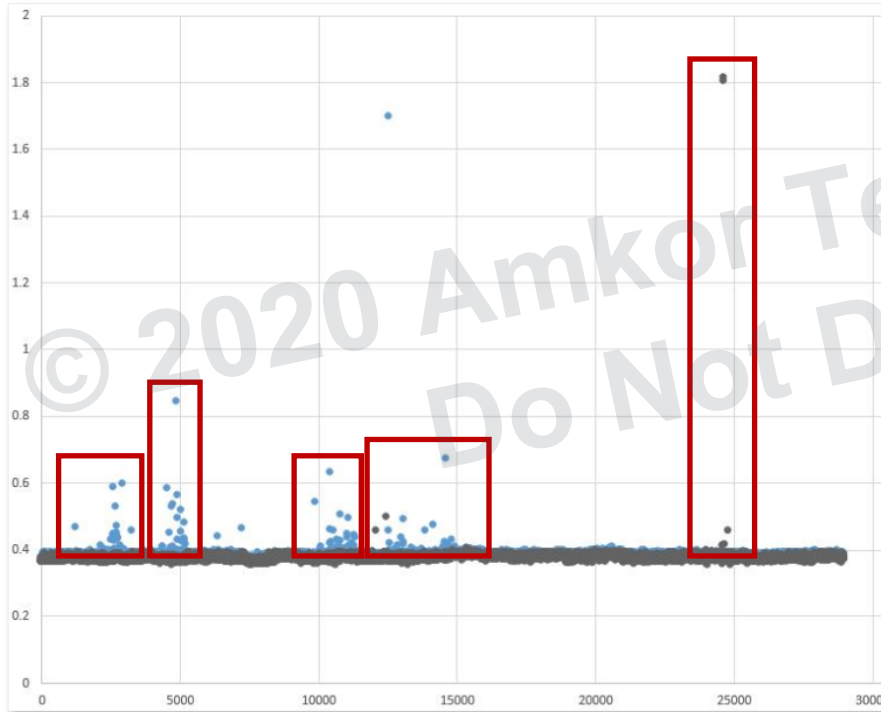
Clustering (Correlation)



Overlaying the Two Graphs



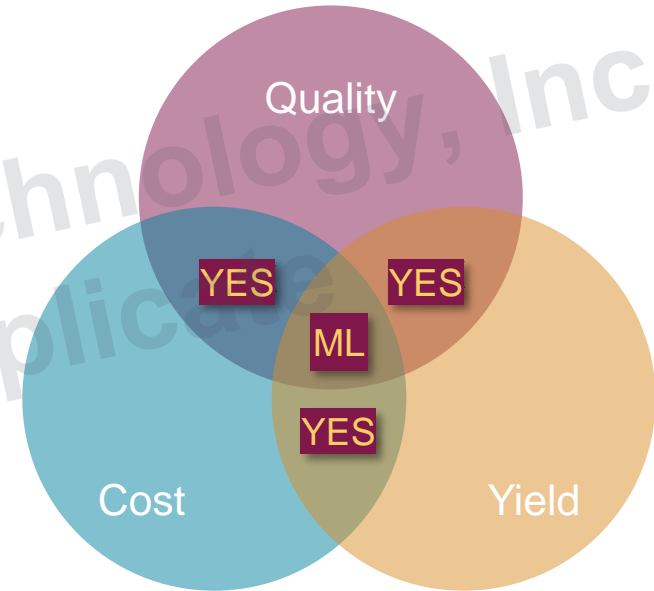
Clustering (Optimization)



- ▶ Opens >1.5V
- ▶ Cluster signature
- ▶ Conclusions

Optimizing Semiconductor Test

- ▶ Reduce the cost of test
 - ▷ Man, machine life, multi-site
 - ▷ Test early & targeted test
- ▶ Improve yield
 - ▷ Socket cleaning
 - ▷ Pogo replacements
- ▶ Improve quality
 - ▷ Fail is truly a fail
 - ▷ Pass is truly a pass



ML = Machine Learning
Mission Possible

ML to Reduce the Cost of Test

- ▶ Analyzing test data
 - ▷ Appropriate “man-to-machine” ratio
 - ▷ Test socket maintenance cycles
 - ▷ Tester calibration cycles
- ▶ Adaptive test
 - ▷ Change test sequence
 - ▷ Predictive failure
 - ▷ Fail early



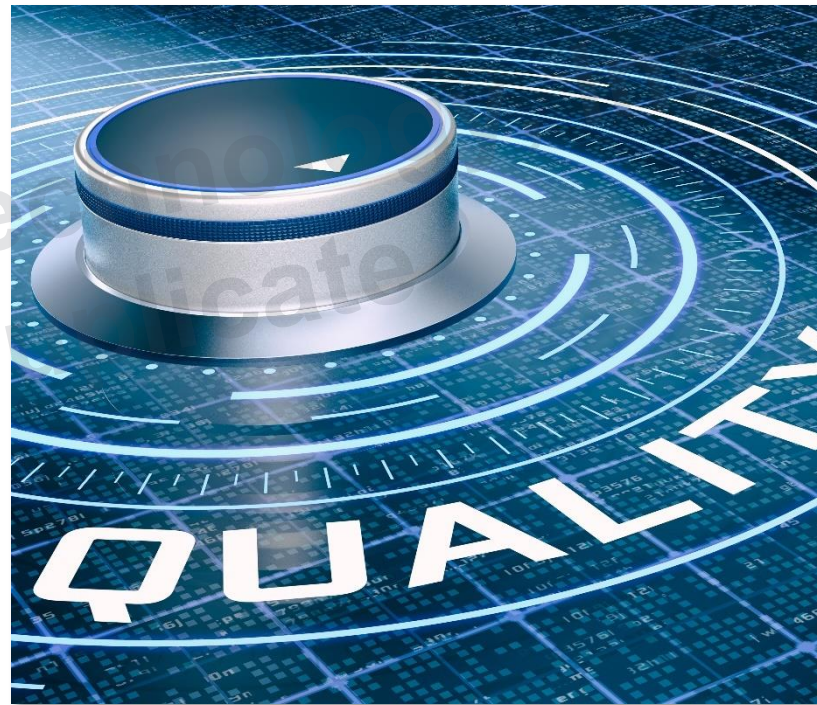
ML to Improve Yield

- ▶ Get rid of false fails
 - ▷ Test socket maintenance cycles
 - ▷ Tester calibration cycles
 - ▷ Predict pass/fails with higher accuracy
- ▶ Adaptive test with down binning
 - ▷ Adapt tests with different inputs and limits



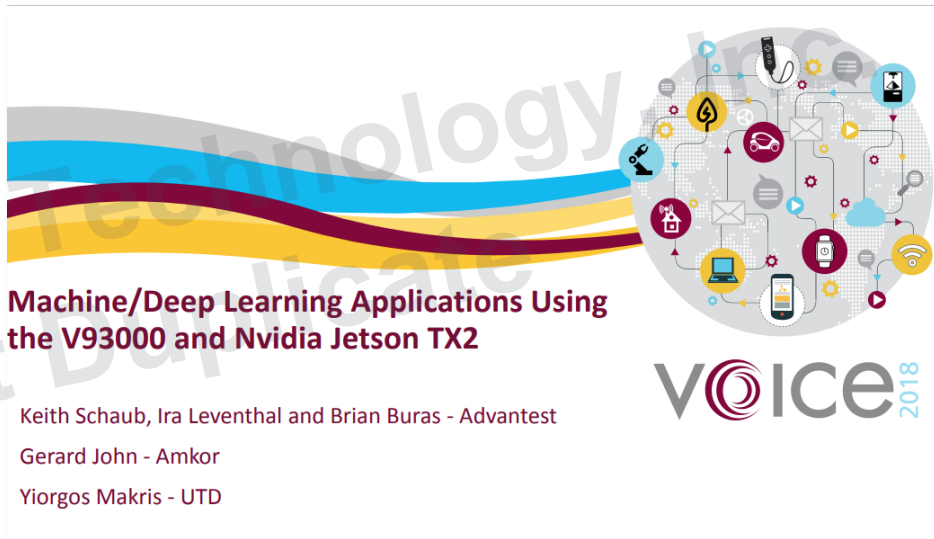
ML to Improve Quality

- ▶ Part average testing
 - ▷ Catch the “flakey” parts
- ▶ Shift left testing
 - ▷ Test early and test hard
 - ▷ Unit-level traceability
 - » Implement 2D bar codes
 - » Lot number
 - » Wafer number
 - » Die X-Y, substrate ID
 - » Material information
 - UF, TIM, lid attach
 - » Test information
 - Tester, prober, handler, site #



Next Steps

- ▶ Machine learning in test
 - ▷ Best introduced by tester companies
 - ▷ Integration with handlers
- ▶ Addressing the test engineer skepticism
 - ▷ ML is **not** a conspiracy
 - ▷ Who will train the machine?
 - ▷ Will I still have a job?
- ▶ Prior art



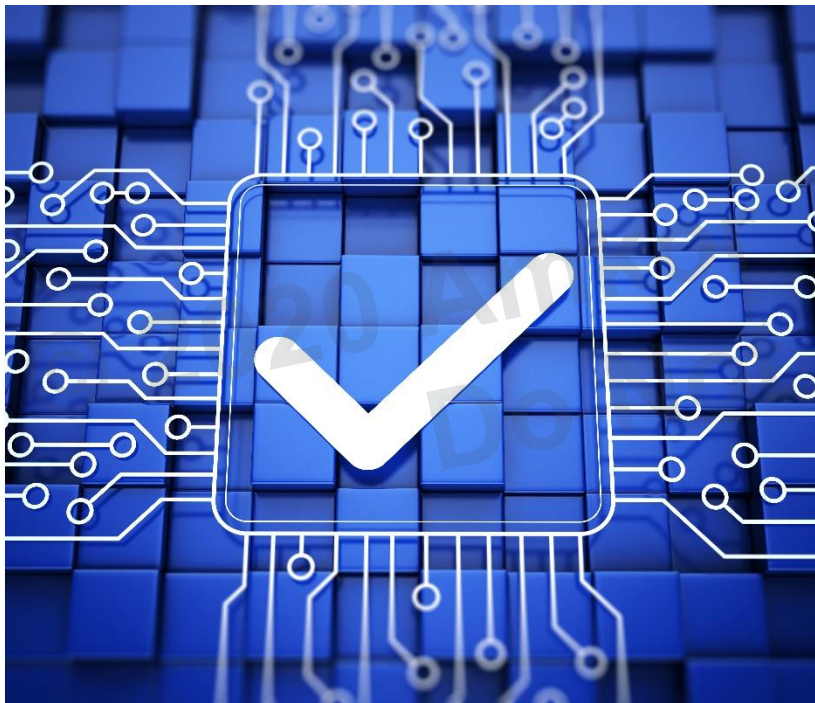
Machine/Deep Learning Applications Using the V93000 and Nvidia Jetson TX2

Keith Schaub, Ira Leventhal and Brian Buras - Advantest
Gerard John - Amkor
Yiorgos Makris - UTD

VOICE 2018

Source: Amkor.com

Conclusion



- ▶ Machine learning algorithms help
 - ▷ Optimize test cost
 - ▷ Improve quality
 - ▷ Improve yield
- ▶ Its introduction brings a paradigm shift to test engineering



Thank You

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