Using Machine Learning to Optimize Semiconductor Test

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Agenda

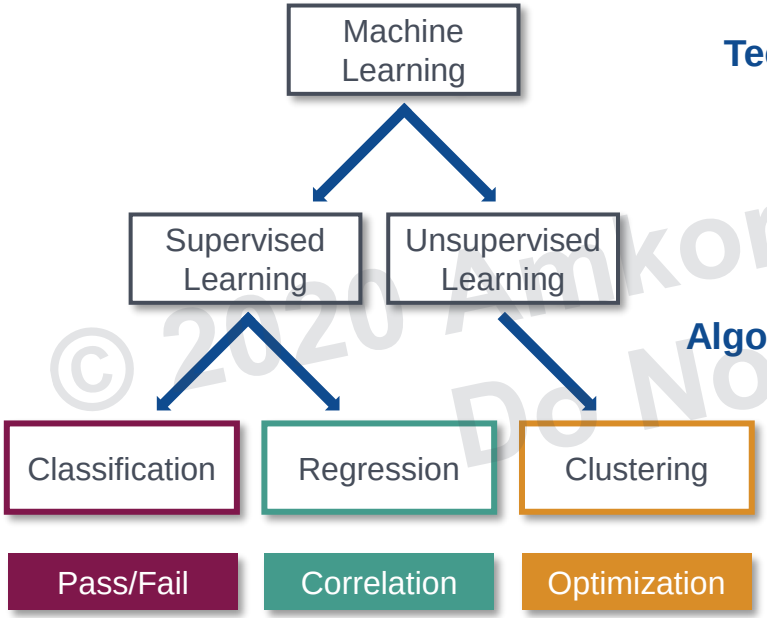
1. Overview of Machine Learning (ML)
2. Background to ML and Test
3. Introduction to Opens-Shorts Testing
4. Data Analysis Classification and Clustering
5. Optimizing Semiconductor Test with ML
6. Next Steps – Conclusion

What is Machine Learning (ML)?

- Tom Mitchell
  - Ex-chair Machine Learning Department at Carnegie Mellon University
  - A computer program is said to learn from experience “E” with respect to some task “T” and some performance measure “P”, if its performance on “T”, as measured by “P”, improves with experience E
    - P{T[E(m)]}
      where m = number of samples
- ML in simple terms “More data makes predictions!”

Image Source: Andrew Ng – Machine Learning Course

Machine Learning Techniques

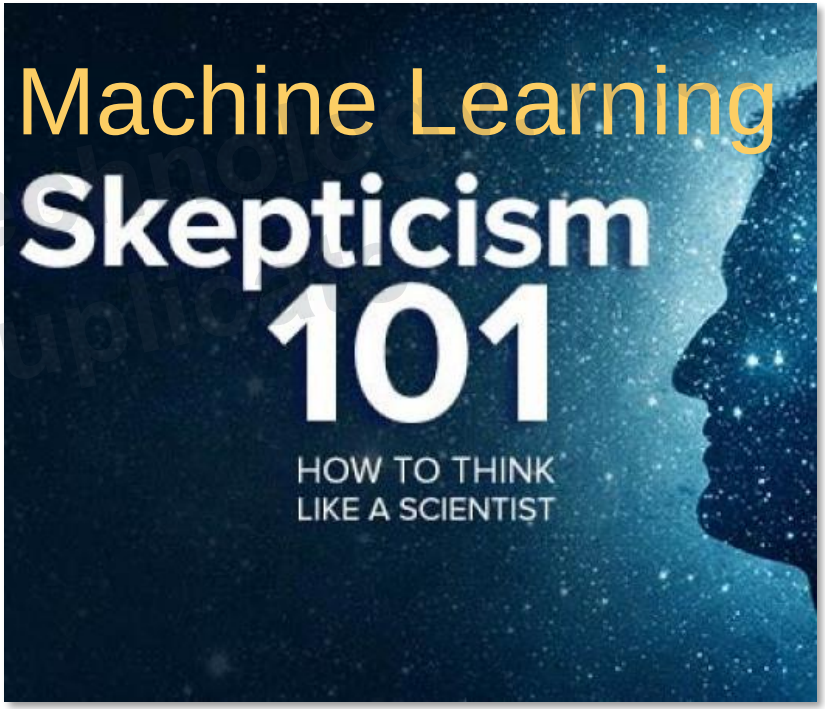


Techniques →	Classification	Regression	Clustering
Algorithms →	Support Vector Machines	Linear Regression, GLM	K-Means, K-Medoids, Fuzzy C-Means
	Discriminant Analysis	SVR, GPR	Hierarchical
	Naïve Bayes	Ensemble Methods	Gaussian Mixture
	Nearest Neighbor	Decision Trees	Neural Networks
	Neural Networks	Neural Networks	Hidden Markov Model

Source: Mathworks.com

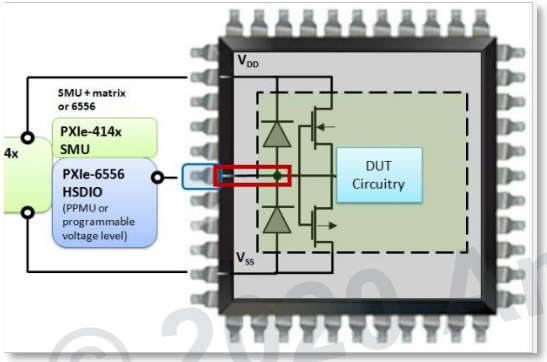
Background of ML and Semiconductor Test

- Test engineer skepticism
  - Is ML in test yet another conspiracy by “big data” companies, creating a new market to sell more products?
  - Really? Can machine learning (ML) improve semiconductor test?
  - What about product quality?
  - Who will teach the machine? ML is a new field I did not study this
  - Will I still have a job?
- Using the simple opens-shorts test, try to debunk the myth that ML has no place in semiconductor test



Source: TheGreatCourses.com. “How to Think Like a Scientist”

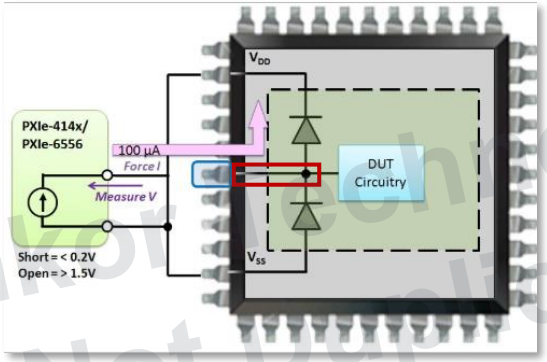
Semiconductor Testing 101 “Opens/Shorts” Test



Source: Ni.com

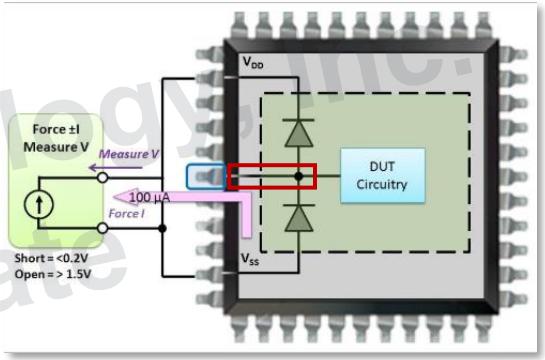
Purpose

- Verify the external pin is connected to the die
- Verify that the pin is not shorted to another



Uses ESD Diode to V_{DD}

- Force current and measure voltage

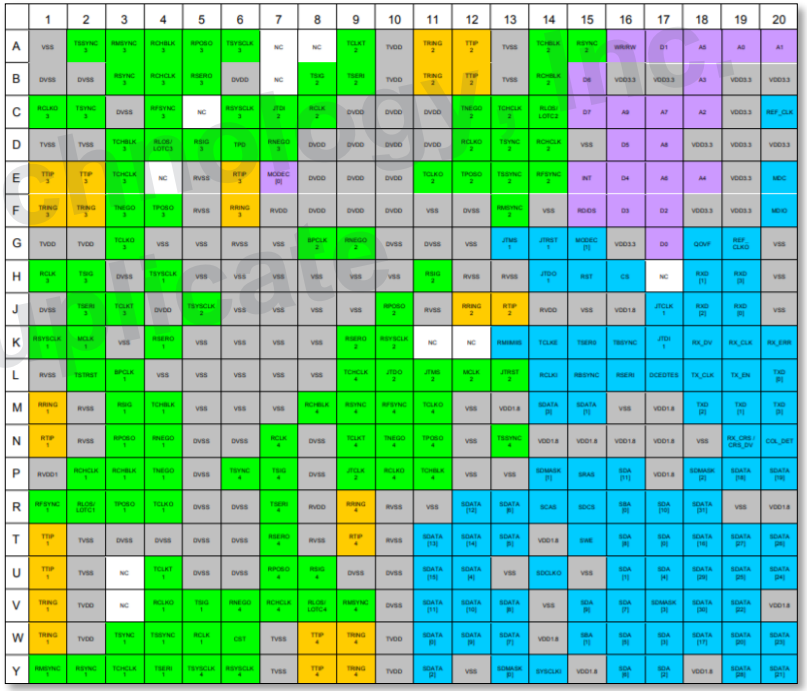


Uses ESD Diode to Vss

- Sink current 100 uA and measure voltage. Voltage clamp set at 2V

The Device Under Test (DUT)

- DUT pin map
- Pins grouped by colors
  - Grey
    - Power & ground
  - Green, blue, purple
    - Input/Output

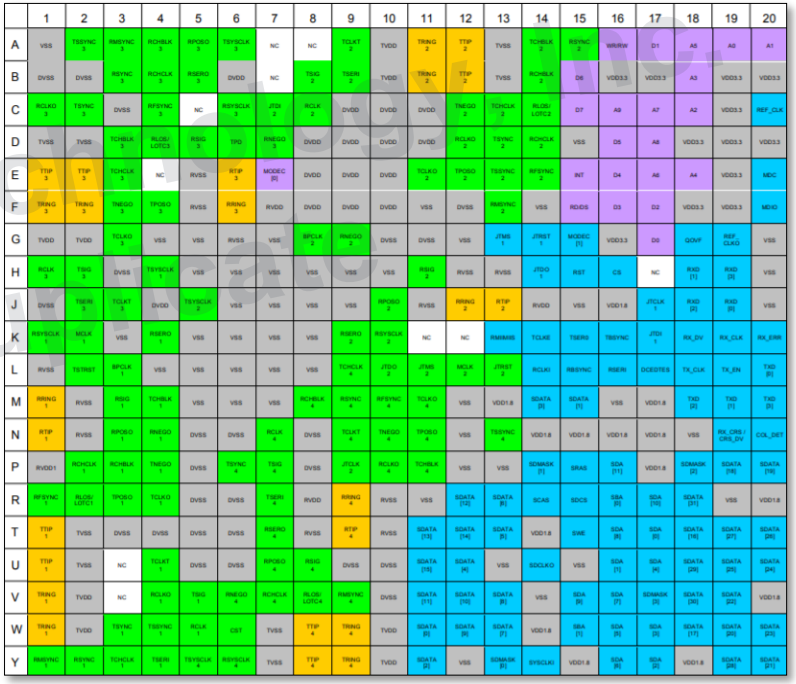


Source: MaximIntegrated.com

Test Method – I/O Pins

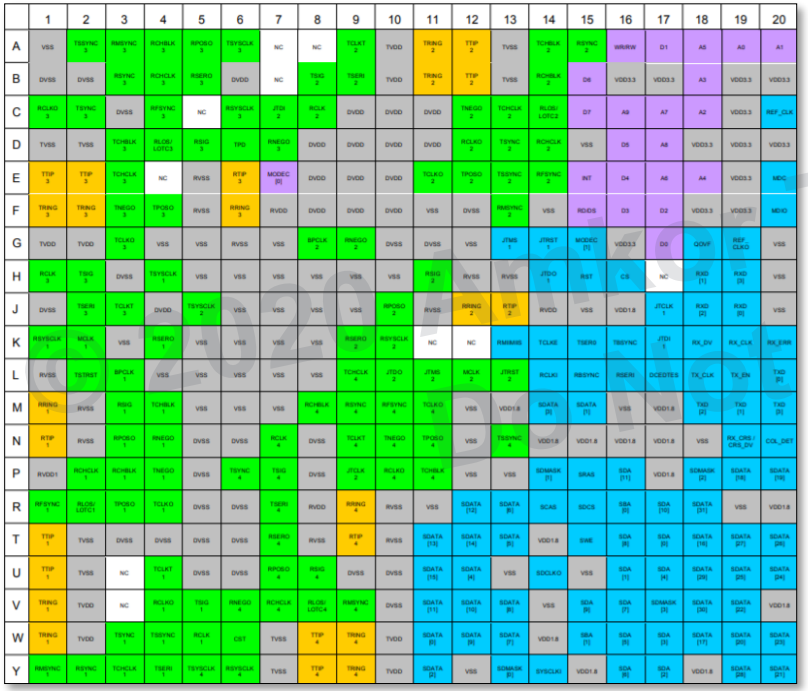
- Example: Testing pin A2
  - All other pins are grounded
  - V clamp = 2V
  - I force = 100 uA
  - Measure voltage on the pin
- Fail condition
  - Pins shorted
    - Measured voltage: 0.2 < V
  - Pin is open
    - Measured voltage: V > 1.5

Device Under Test



Source: MaximIntegrated.com

Power and Ground

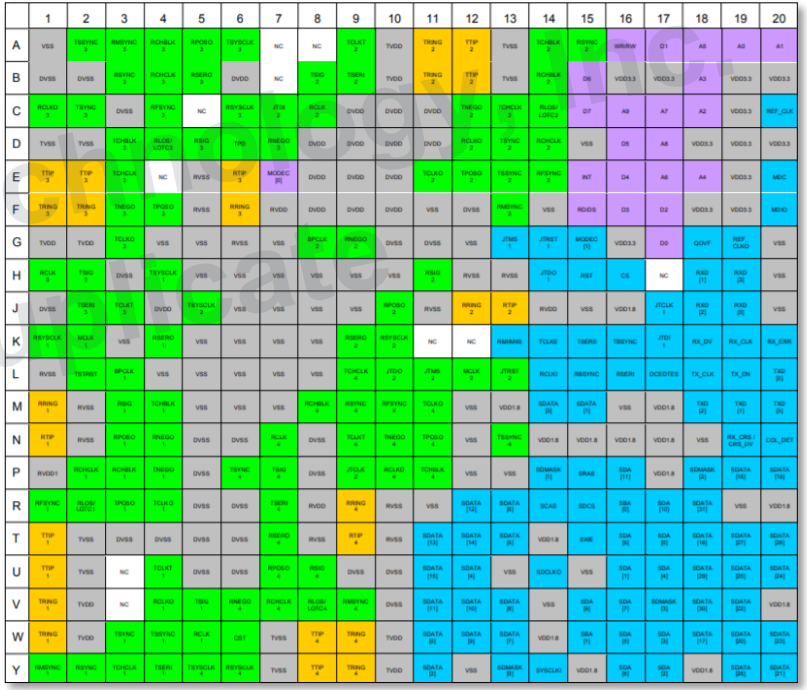


Source: MaximIntegrated.com

- Connectivity to VDD
  - VDD 3.3
  - VDD 1.2
  - VDD 1.8
  - DVDD
  - TVDD
- Connectivity to VSS
  - VSS
  - TVSS
  - DVSS

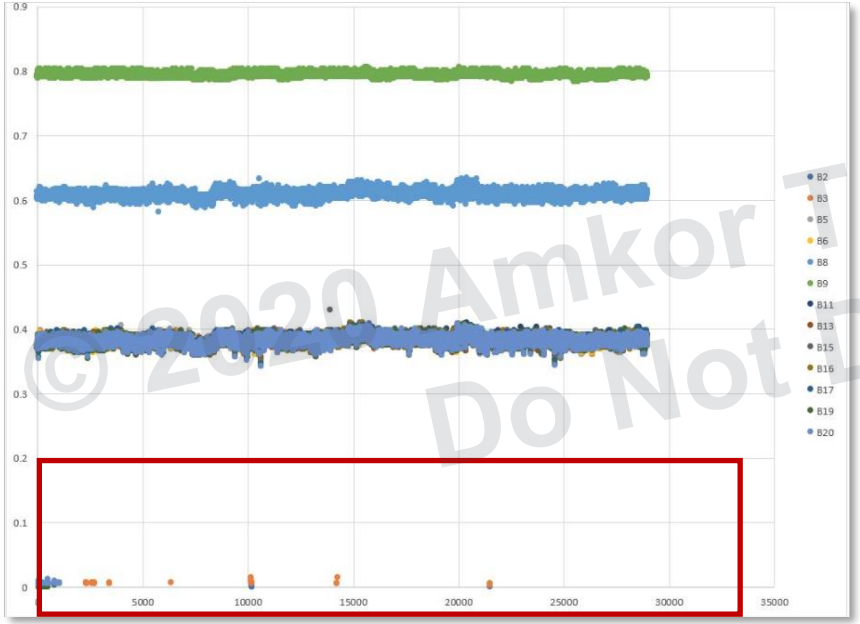
Test Method – Power & Ground

- Example: Testing pin A1 (Vss)
  - All other pins are open
  - Next Vss pin forms the return path
  - I force = 100 mA, clamp 0.5V
  - Measure voltage on the pin
  - Repeat for all pins in the group
  - 4W test (ideal)
- Fail condition
  - Pin is open
    - Measured voltage: V > 0.1V

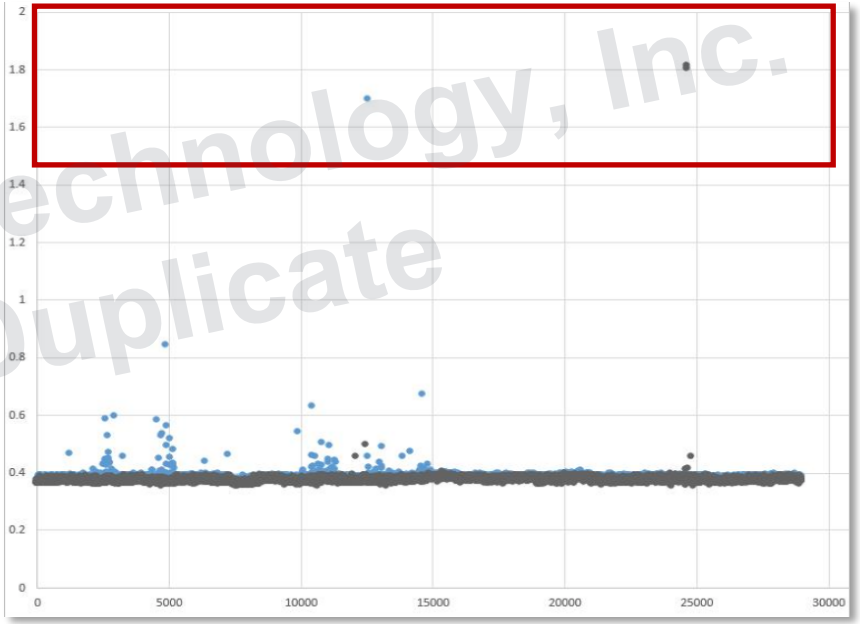


Source: MaximIntegrated.com

Classification (Pass/Fail) Training Using ML

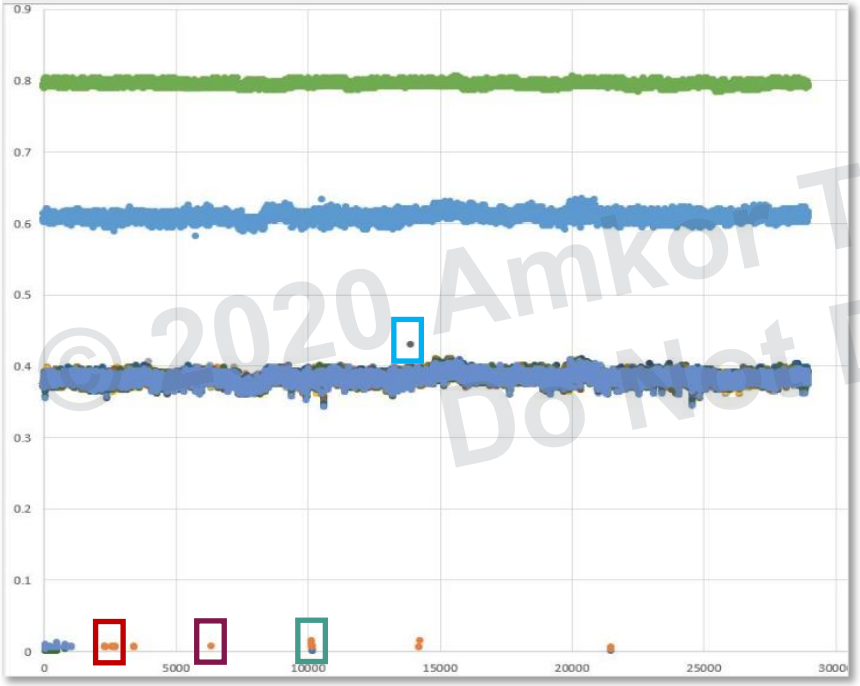


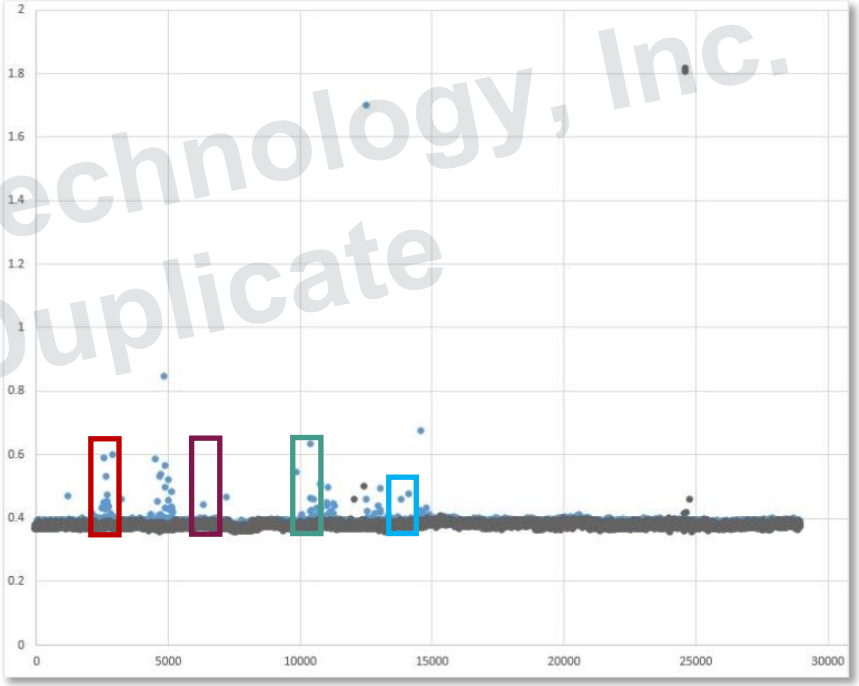
Pins failing with shorts <0.2V



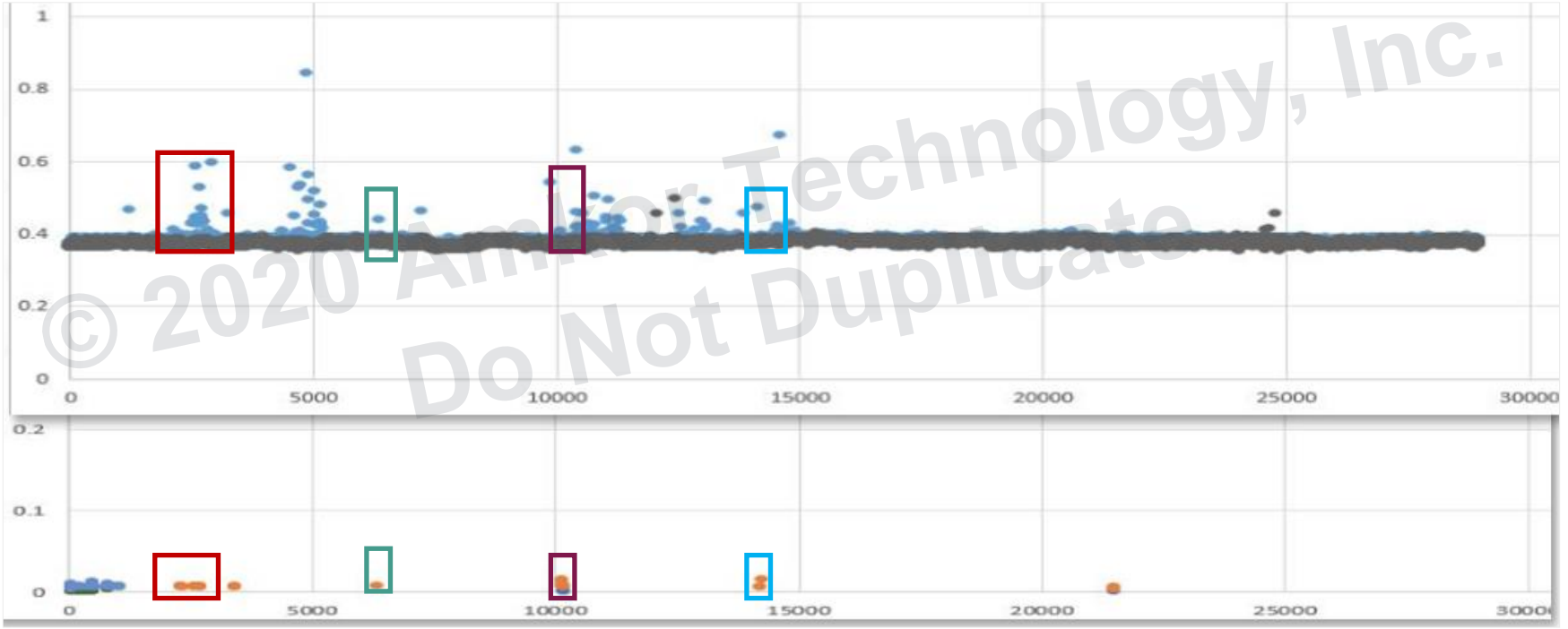
Pins failing with opens >1.5V

Clustering (Correlation)

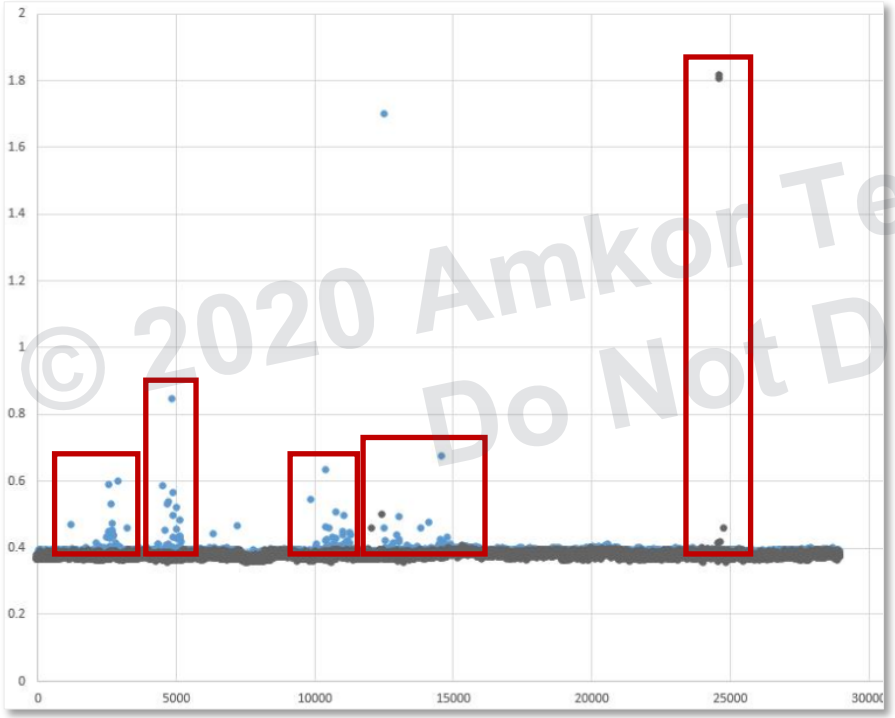




Overlaying the Two Graphs



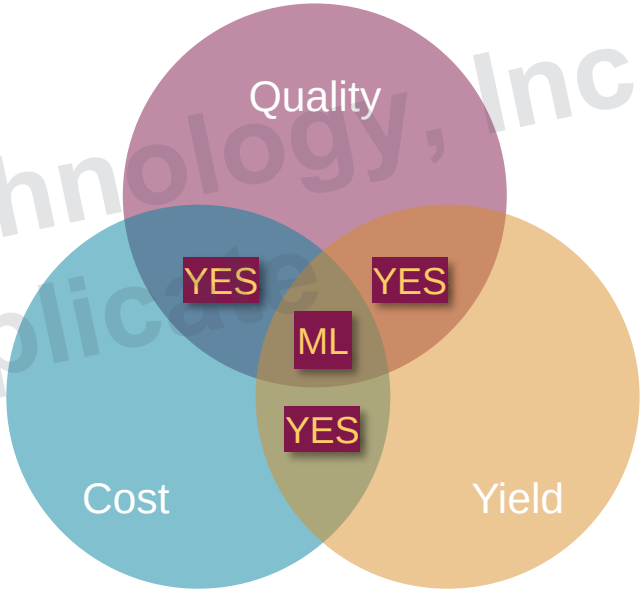
Clustering (Optimization)



- Opens >1.5V
- Cluster signature
- Conclusions

Optimizing Semiconductor Test

- Reduce the cost of test
  - Man, machine life, multi-site
  - Test early & targeted test
- Improve yield
  - Socket cleaning
  - Pogo replacements
- Improve quality
  - Fail is truly a fail
  - Pass is truly a pass



ML = Machine Learning
Mission Possible

ML to Reduce the Cost of Test

- Analyzing test data
  - Appropriate “man-to-machine” ratio
  - Test socket maintenance cycles
  - Tester calibration cycles
- Adaptive test
  - Change test sequence
  - Predictive failure
  - Fail early

ML to Improve Yield

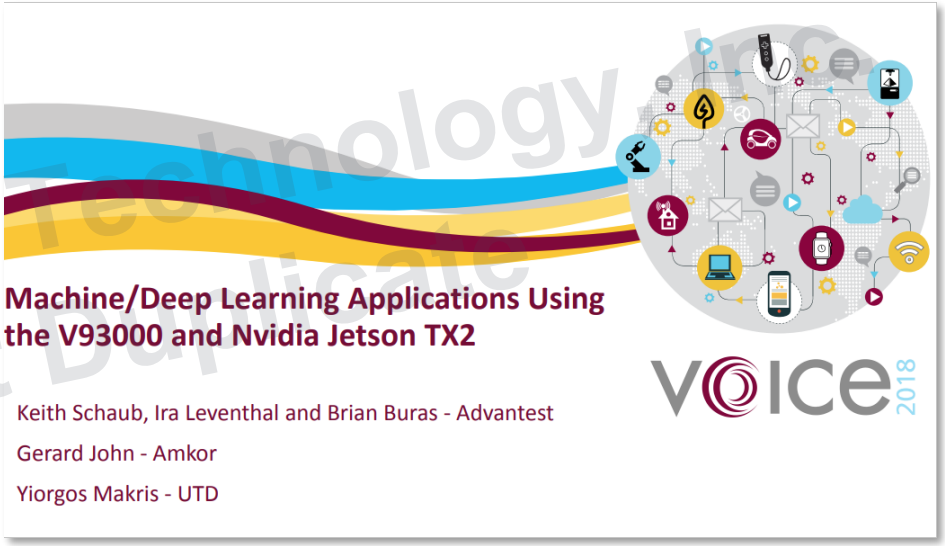
- Get rid of false fails
  - Test socket maintenance cycles
  - Tester calibration cycles
  - Predict pass/fails with higher accuracy
- Adaptive test with down binning
  - Adapt tests with different inputs and limits

ML to Improve Quality

- Part average testing
  - Catch the “flakey” parts
- Shift left testing
  - Test early and test hard
  - Unit-level traceability
    - Implement 2D bar codes
    - Lot number
    - Wafer number
    - Die X-Y, substrate ID
    - Material information
      - UF, TIM, lid attach
    - Test information
      - Tester, prober, handler, site #

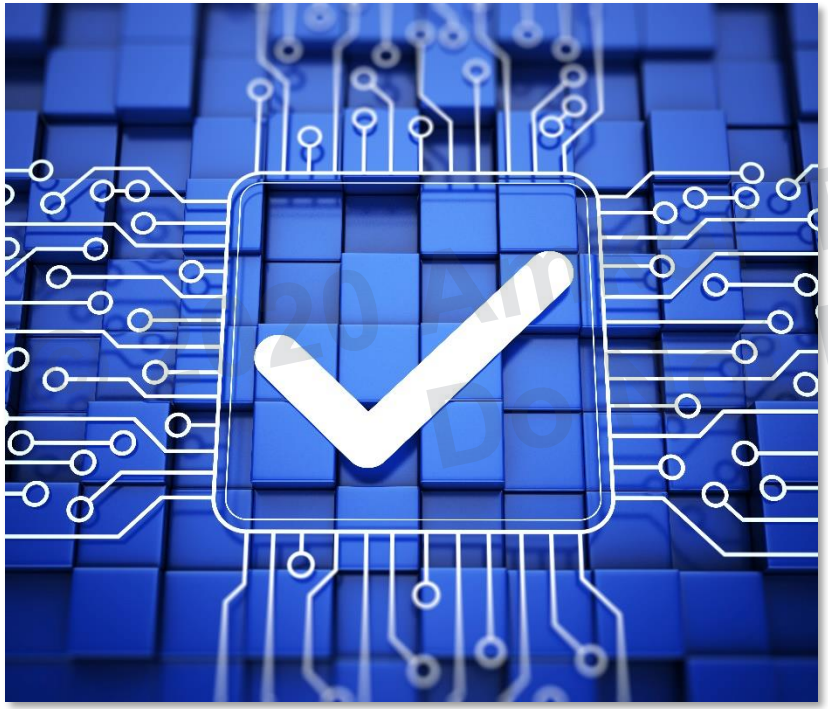
Next Steps

- Machine learning in test
  - Best introduced by tester companies
  - Integration with handlers
- Addressing the test engineer skepticism
  - ML is **not** a conspiracy
  - Who will train the machine?
  - Will I still have a job?
- Prior art



Source: Amkor.com

Conclusion



- Machine learning algorithms help
  - Optimize test cost
  - Improve quality
  - Improve yield
- Its introduction brings a paradigm shift to test engineering

Thank You

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