What does it take to photonize silicon?

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Computation and communication

Cerebras Wafer Scale Engine

Cerebras WSE
1.2 Trillion Transistors
46,225 mm² Silicon

Largest GPU
21.1 Billion Transistors
815 mm² Silicon

A half century lesson:

Electronics is best for data **computation** and photonics is best for data **transmission**!

Moore’s Law

SEMICONDUCTOR TECHNOLOGY EVOLVES

DRIVEN BY CHANGING APPLICATION LANDSCAPE

Invention of point-contact transistor 1947

Invention of IC 1958

Invention of diode laser 1962

Concept of data transmission in optical fiber 1965

Intel 4004 1971

Mobile phone 1973

Transistor Scaling Principle 1974

Concept of WDM 1978

Flash Memory 1984

Invention of EDFA 1987

Pentium CPU 1995

FinFET 1999

3G 2002

Amazon Web Service 2002

iPhone 2007

4G 2009

GPU (21B Transistors) 2017

7nm FinFET 2018

5nm CMOS 2020

2050 and beyond

Data center, cloud computing

Transistor Radio | Mini-Computer | PC / Internet | Mobile | AI / 5G

Connectivity challenges in data centers

Modern Highly-Interconnected Data Center

SERVERS
10G SFP+
25G SFP28
10G SFPwire AOC
25G SFPwire AOC

TOR/LEAF SWITCHES
40G QSFP+
4x10G QSFP+
100G QSFP28
4x25G QSFP28
10G SFP+
25G SFP28
10G SFPwire AOC
25G SFPwire AOC
4x10G Breakout AOC
4x25G Breakout AOC

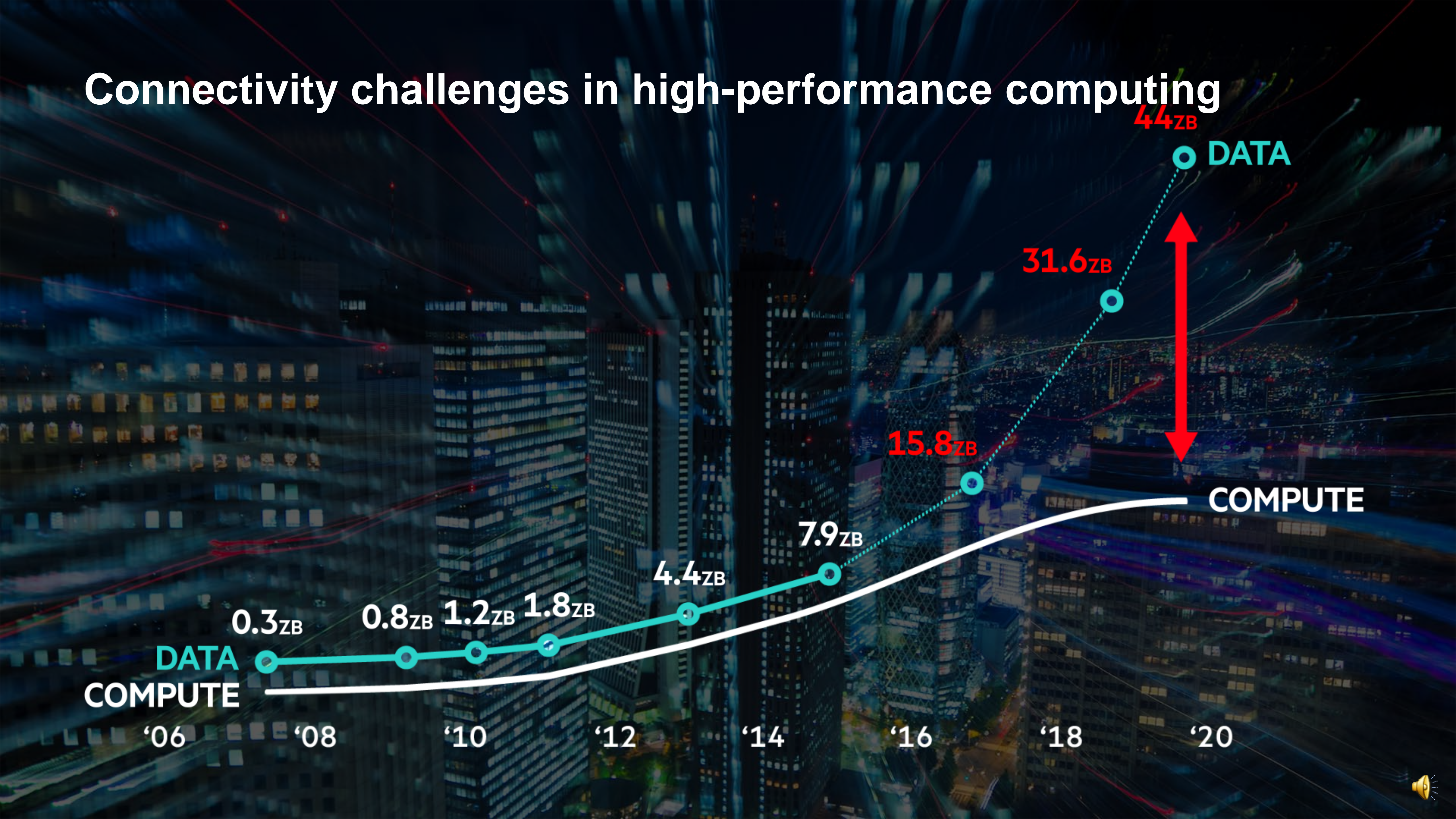
ROUTERS
100G CFP4
100G CFP2
100G CFP
100G CFP2-ACO

WAN

CORE/SPINE SWITCHES
40G QSFP+
100G QSFP28
40G/100G Quadwire AOC
100G CXP
100G C.wire AOC
120G/300G BOA

Source: elvast, microsoft

Connectivity challenges in high-performance computing



Two different technological worlds

Silicon

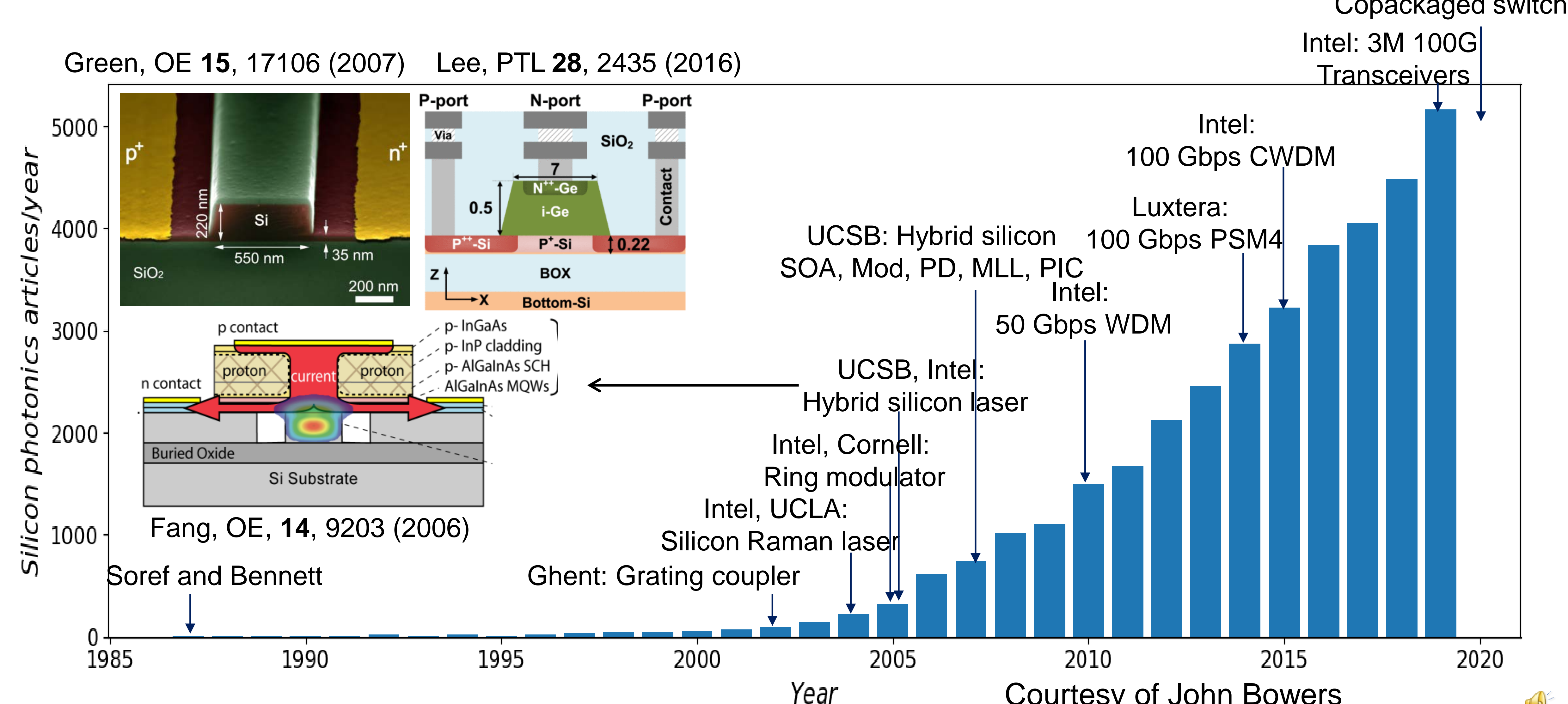
Compound semiconductors

- Microelectronic integration: device size, wafer scale, manufacture technique
- Photonic integration: material, functionality, fabrication compatibility

Conventional expensive III-V photonics

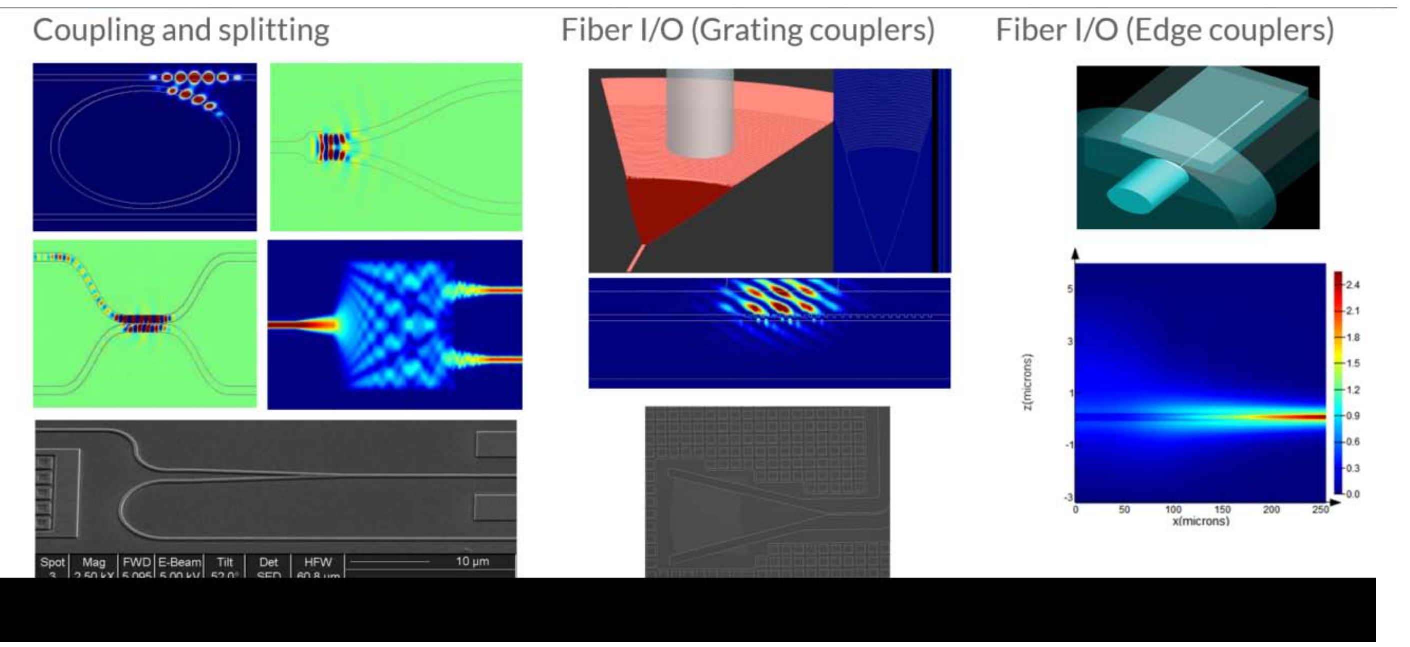
Large-scale silicon-based photonics

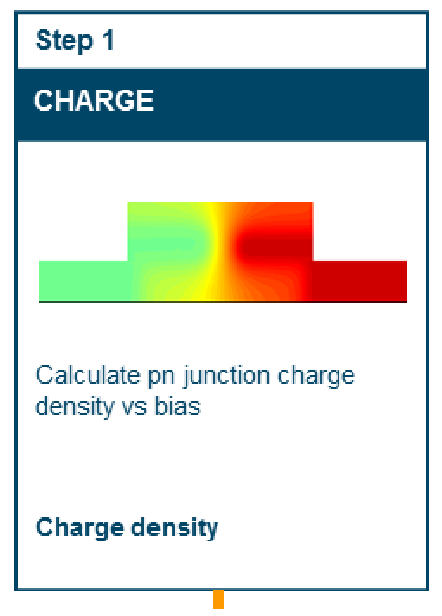
Silicon photonics: a short history

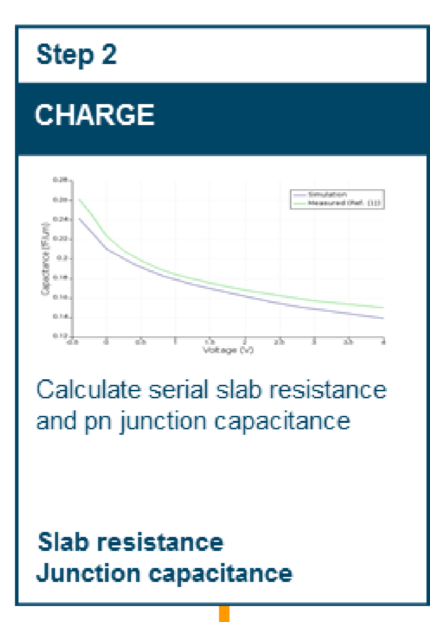


Photonize silicon

Phase I: component design





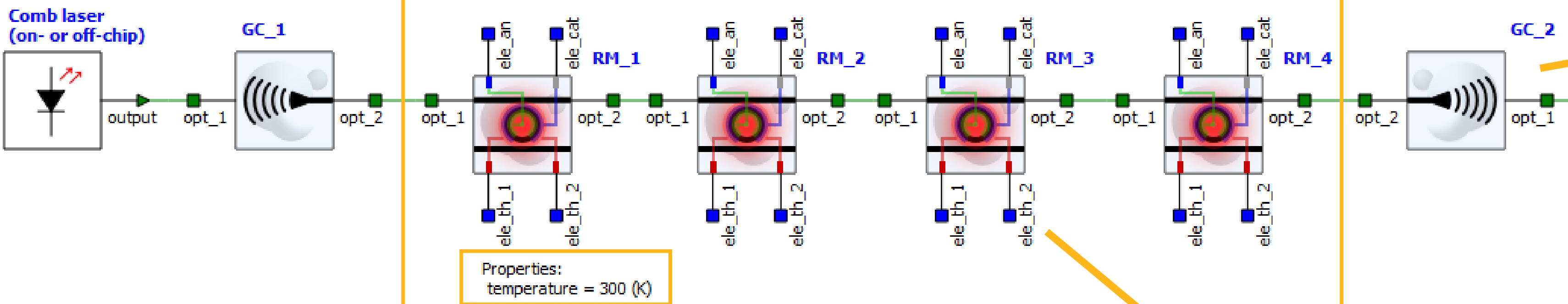


– High accuracy in material parameters and multi-physics models
  – Coherent integration of electromagnetics, electro-optic effect (e.g., plasma dispersion effect) and RF, etc.
  – Critical temperature-dependence included

Courtesy: James Pond (Lumerical/Ansys)

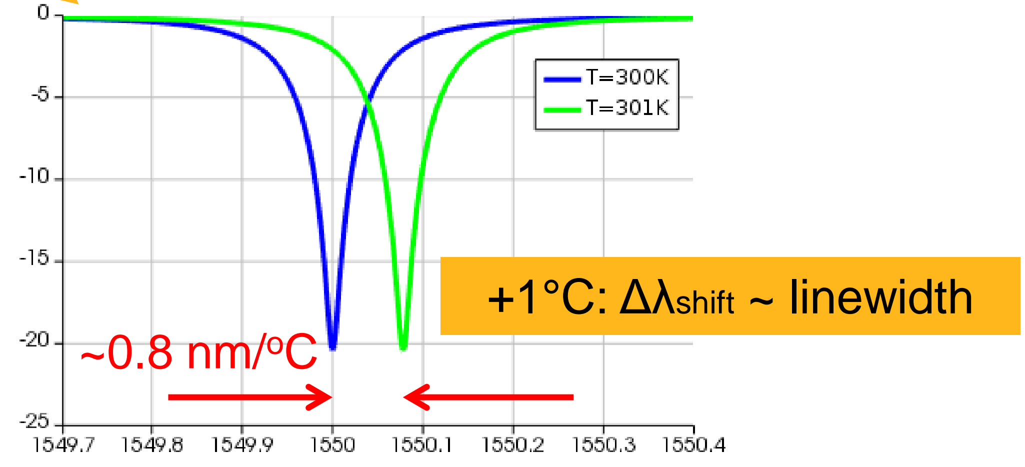
Phase I: photonic circuit design

- WDM (wavelength division multiplexing) optical interconnects



Rings

- Provide energy-efficient data modulation and WDM function
- Very sensitive to temperature (and manufacturing variations*)
- Often require active tuning (thermo-optic , electro-optic effect)



Ref : HPE/Lumerical at TSMC OIP 2020

Thermal Simulation for 3DIC Silicon Photonics System

RHSC/Totem for Digital IC and EIC on heat generation
RHSC-ET for PIC Package: heat generation, dissipation, and thermal couplings of chips and optical components

Convection and radiation to ambient air

EIC

Laser

Digital IC

Fiber array

PIC "Interposer"

BGA substrate

Conduction dissipation to PCB

Heat generation in chips and optical components

Conduction in solids

Convection in air and radiation in space

Full 3DIC thermal simulation

Temperature map in the Si Interposer layer

Update local temperature of each photonic device

Run photonic circuit simulation

Courtesy of Norman Chang (Ansys)

https://www.3dincites.com/2014/01/lessons-learned-trenches-3d-ic-manufacturing-sensor-applications/

Silicon photonic foundry players

Region	Si_3N_4	Si + Ge modulators and PDs	Si+Ge modulators and PDs + Integrated Lasers
North America	Honeywell	2021 → AIM photonics, GLOBAL FOUNDRIES, Tower Semiconductor, bridg Bridging the Innovation Development Gap → 2021	intel
Europe	LIGENTEC, LioniX	2021 → imec, cea leti → 2021	
Asia		tsmc, SMIC, SITRI, A*STAR, AMICRA microtechnologies, CompoundTek → 2021	

Photonize silicon

Phase II: CMOS foundry fabrication

– 65 nm toolset sufficient for most silicon photonics components

– Dimension control is very critical

1.5 μm

Building blocks of silicon photonic systems

Source: CEA Leti

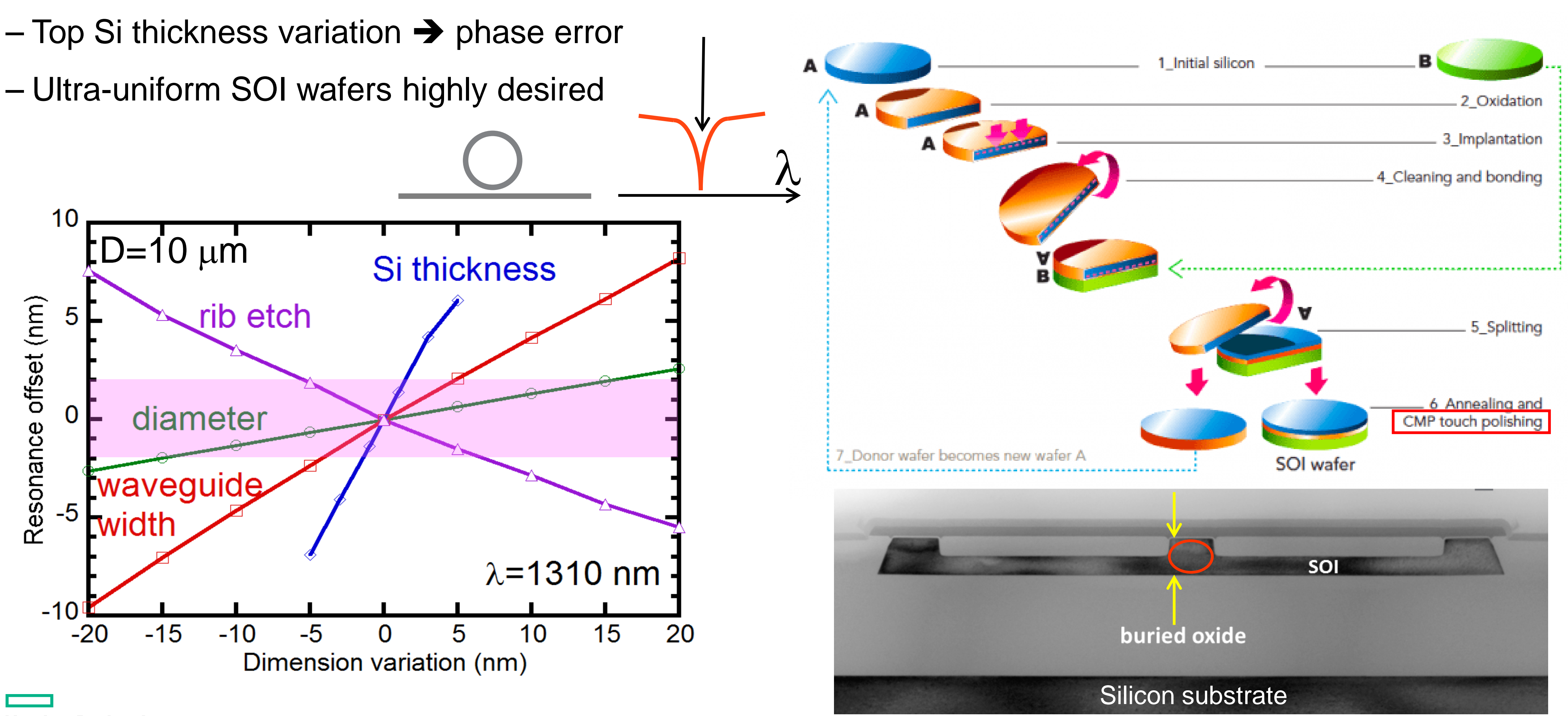
Streshinsky, OPN **24**, 32 (2013)

Photonize silicon

Phase II: SOI wafer

– Top Si thickness variation ➔ phase error

– Ultra-uniform SOI wafers highly desired



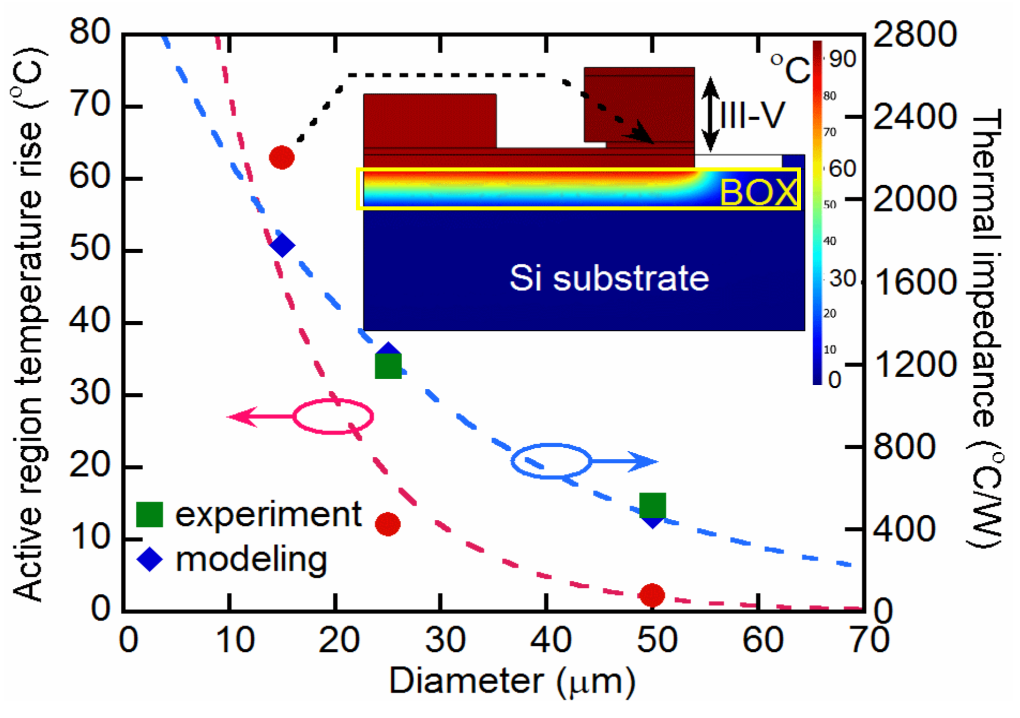
Hewlett Packard Enterprise

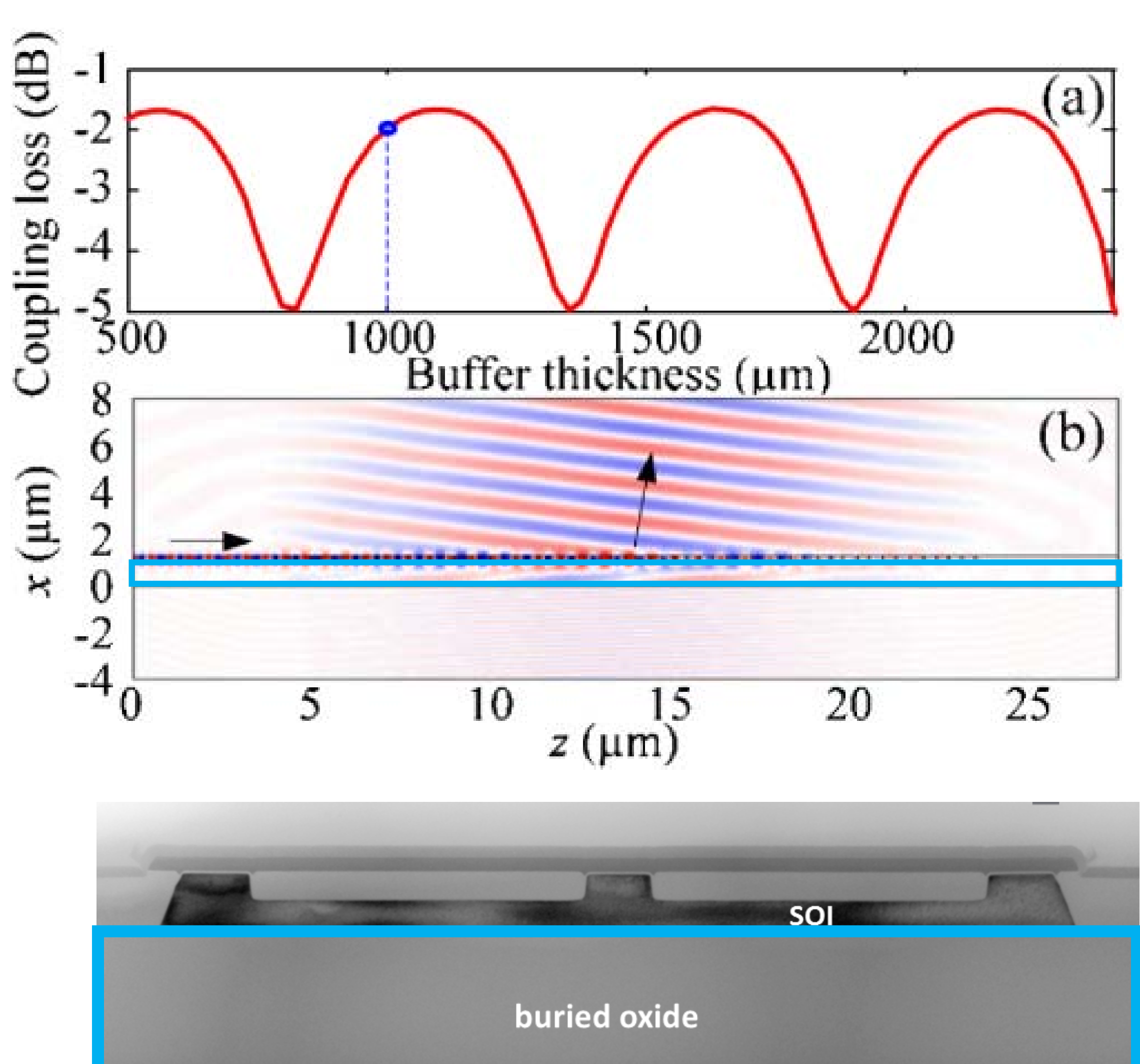
Source: SOITEC, chipworks

Photonize silicon

Phase II: SOI wafer

- BOX thickness matters
  - Optical impact to grating coupler, …
  - Thermal impact to thermal tuning and heat dissipation





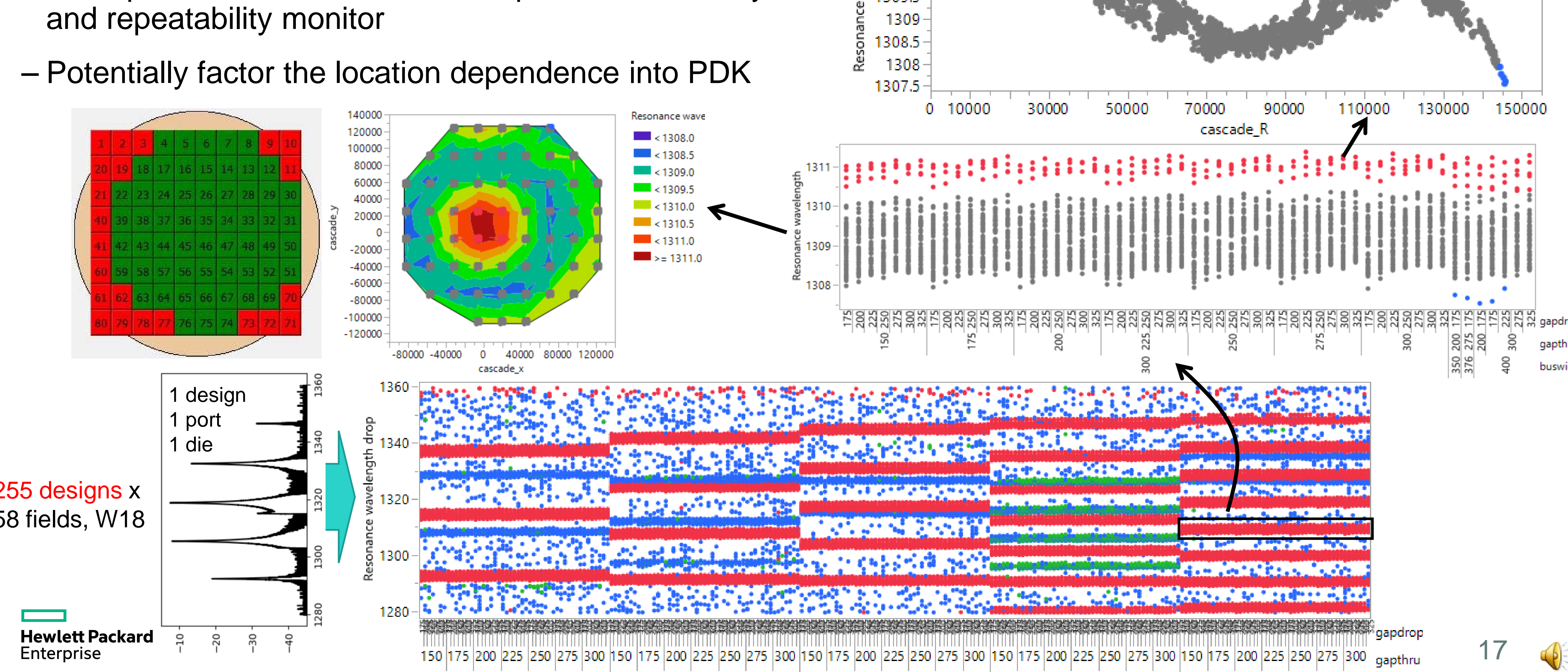
Source: chipworks
Ding, OL **38**, 2732 (2013)

Photonize silicon

Phase III: wafer-level testing/screening

– Use optical resonance devices as process uniformity and repeatability monitor

– Potentially factor the location dependence into PDK



Silicon photonics PDK development

Silicon Photonics DRM

Hewlett Packard Enterprise
PDK

Hewlett Packard Enterprise
SVRF Deck

Design of Experiment

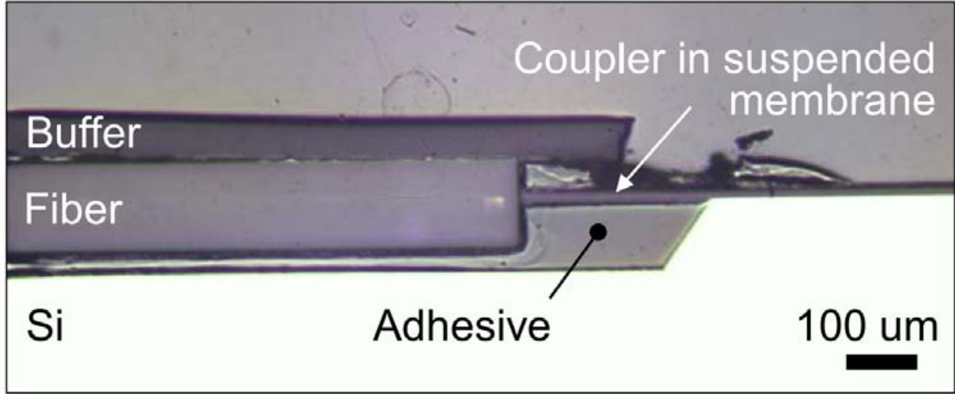
Silicon Photonics Foundry

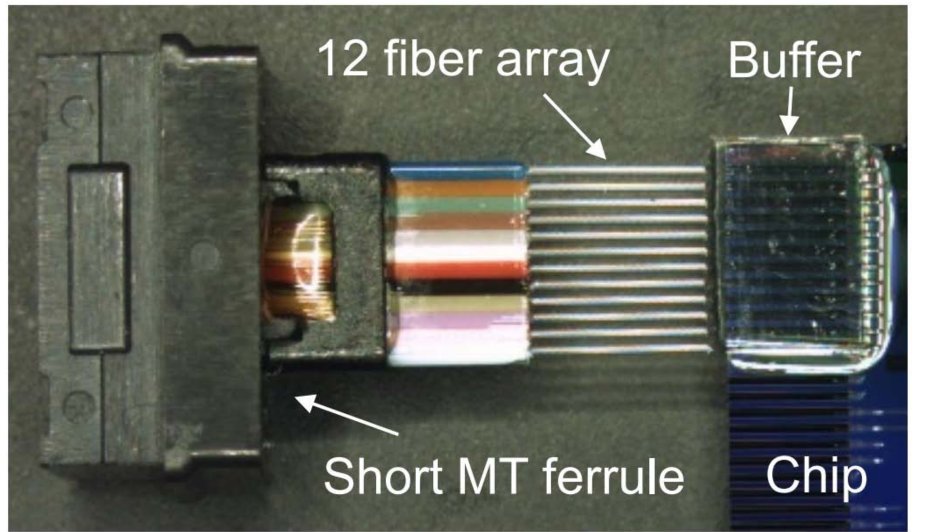
Automated Wafer Level Test

Photonize silicon

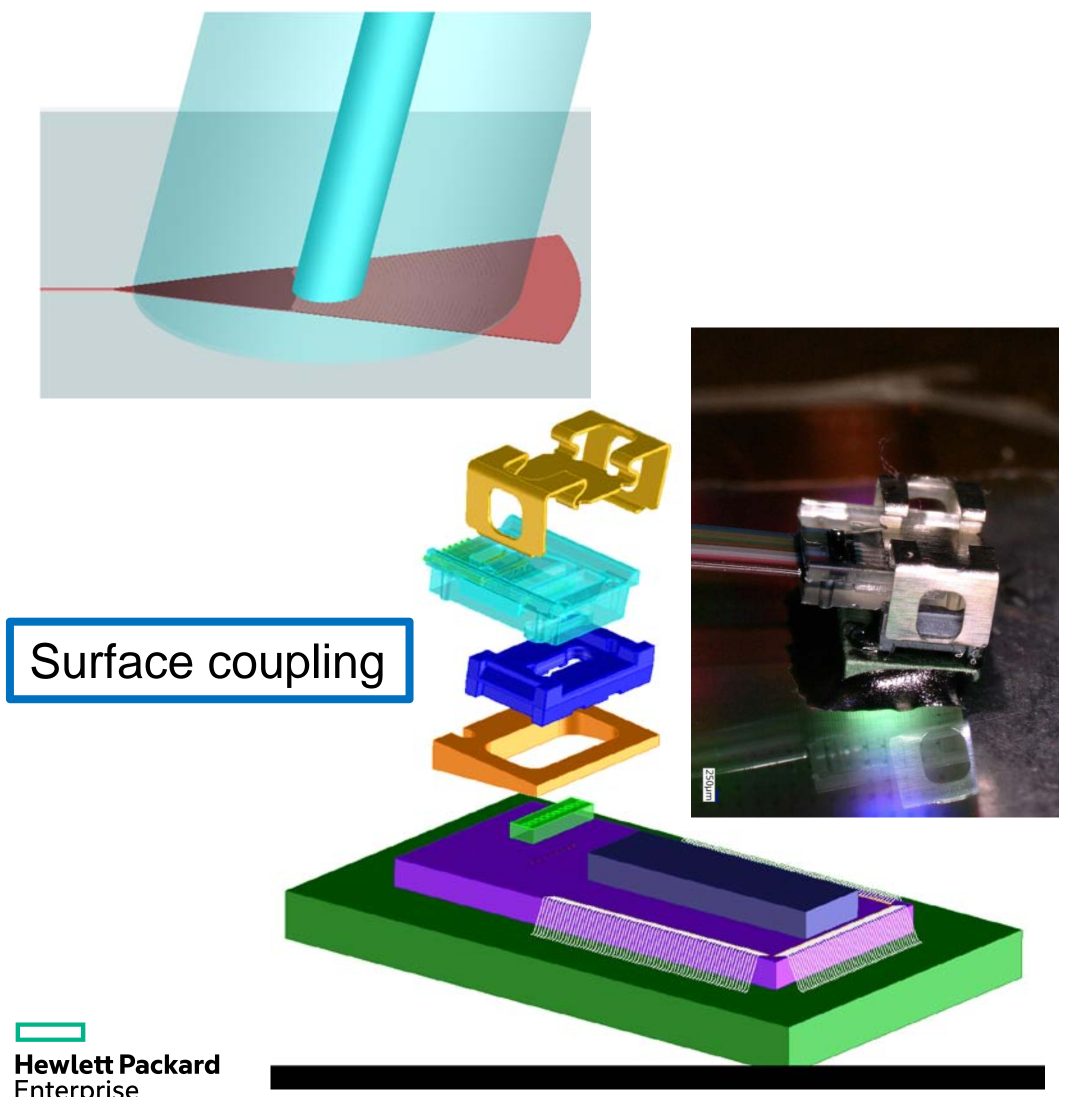
Phase III: Packaging – fiber attachment

In-plane coupling





Surface coupling



Source: IBM

Photonize silicon

Phase III: Packaging – electronics-optics integration

Heat Sink
ASIC
SOI SiPh Interposer
TSV (low/high speed signals, power)
Organic Substrate
Grating coupler

Through-silicon-vias
DRAM
Nano-FPGA
Reconfigurable nanophotonic network
L3 caches
Inter-core nanphotonic networks
FinFET based many-core processrs

2D integration

- Simple, mature
- Limited bandwidth, Low density

2.5D integration

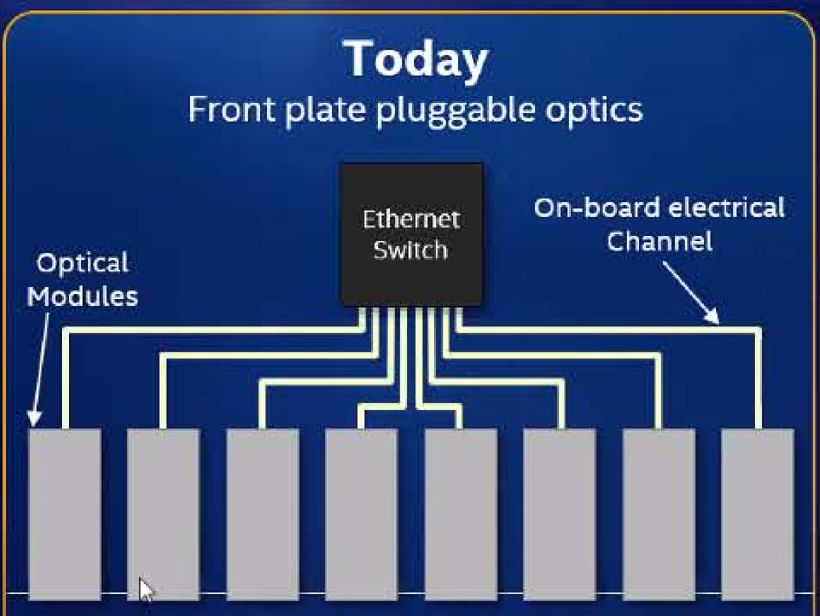
- High speed, low power consumption, flexible
- Fabrication, thermal management

3D integration

- Largest bandwidth, smallest footprint, largest density
- Thermal management, system design, reliability

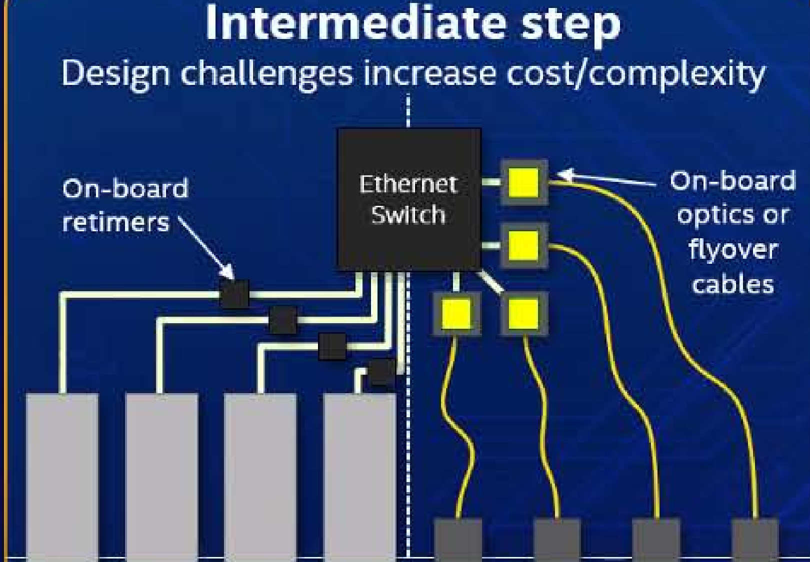
The Path to Photonics Integration

Today
Front plate pluggable optics



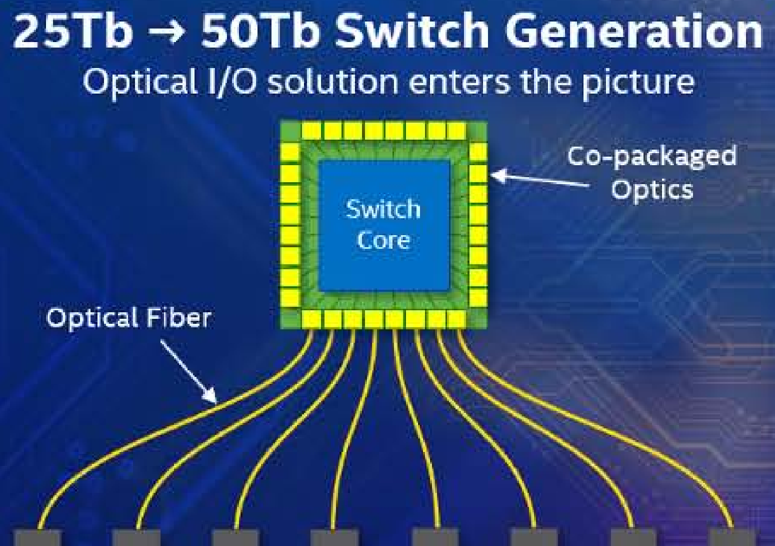
- 25G integrated SerDes
  - High-power I/O to drive copper traces and cables
- Optical links between switches (SFP/QSFP modules)

Intermediate step
Design challenges increase cost/complexity



- 50G – 100G integrated SerDes
  - On-board re-timers or flyover cables may be needed for 100G
  - Increases cost, complexity
- On-board optics being introduced
  - Bandwidth density improves

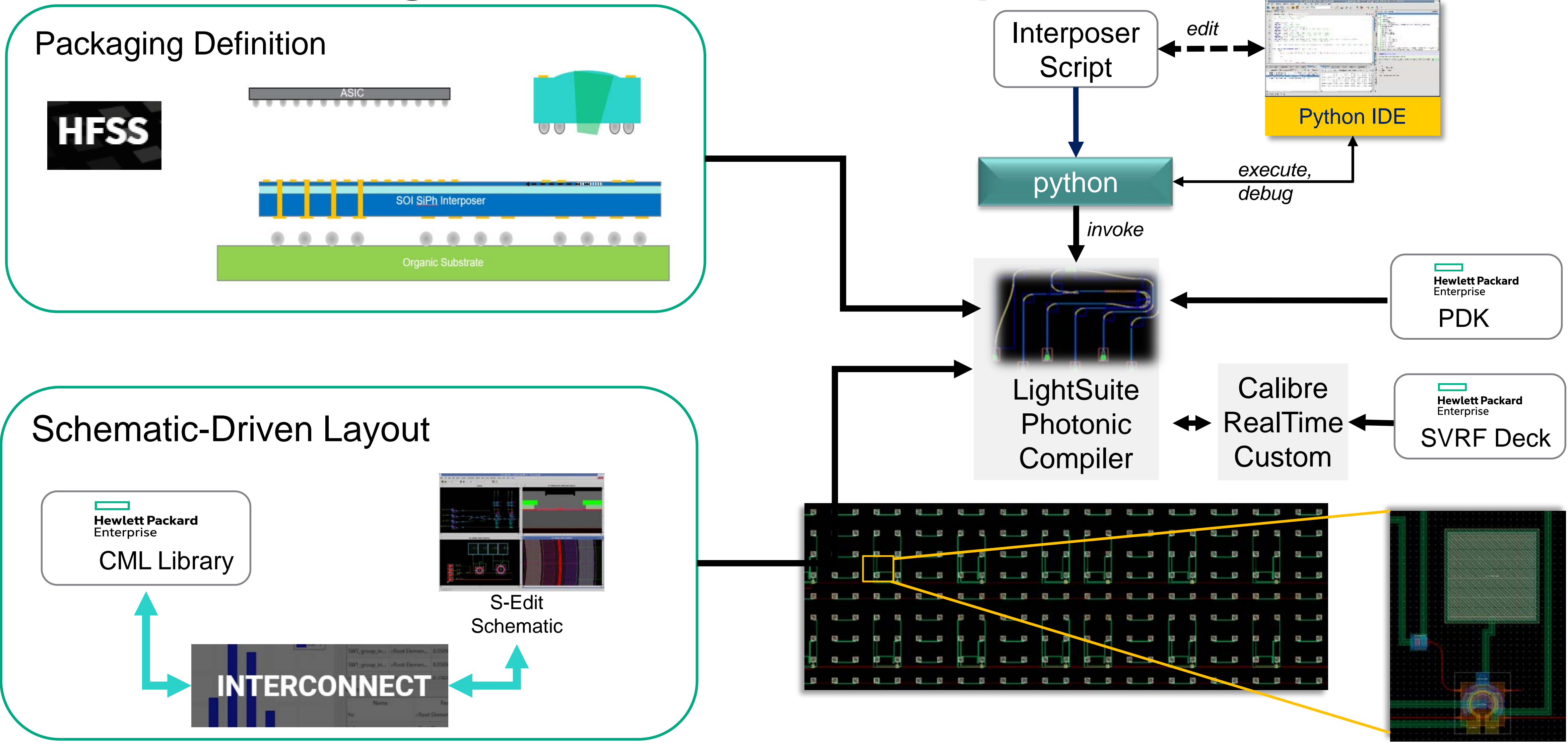
25Tb → 50Tb Switch Generation
Optical I/O solution enters the picture



- Co-packaged "optical I/O"
  - Photonics-optimized SerDes
- Break copper constraints
- Significant power reduction
- Innovation in photonics, packaging, and manufacturing technology

Source: Intel

Automated design flow and Electronics-photonics co-simulation

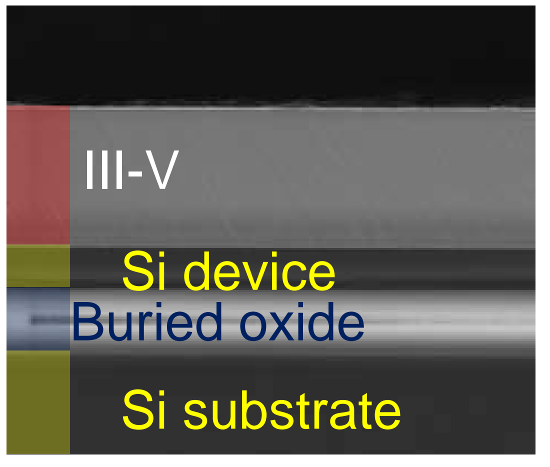


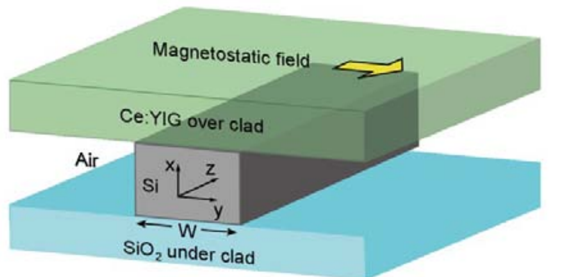
Courtesy of Ashkan Seyedi

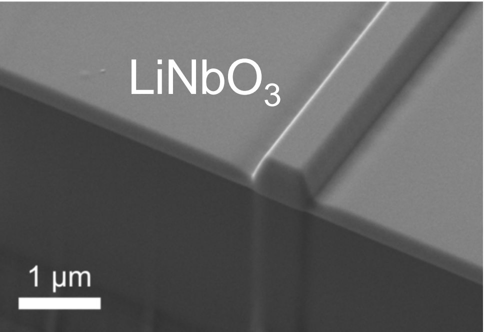
Heterogeneous photonic integration on silicon

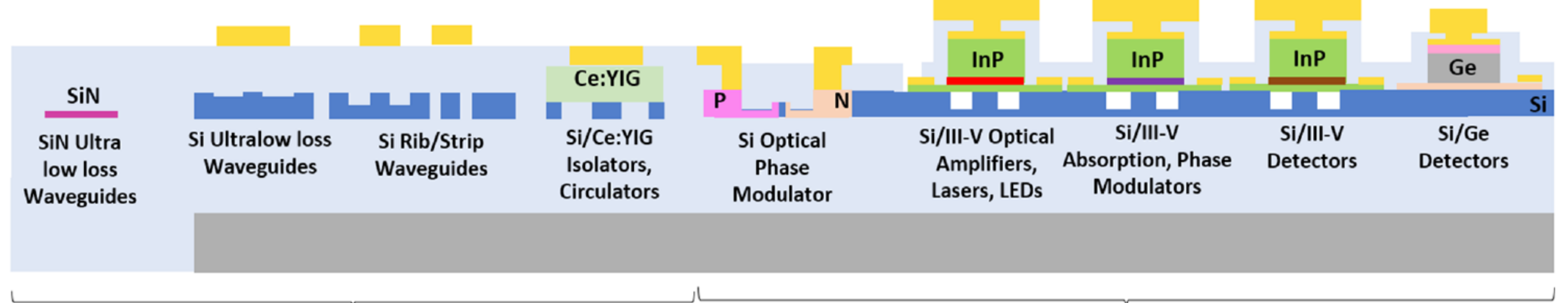
Wafer bonding or heteroepitaxy

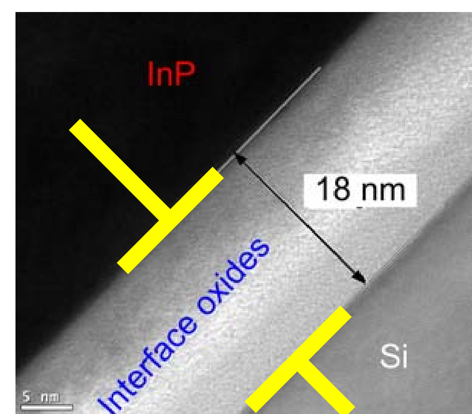
- Enablement of missing functionalities on silicon
  - IIIV-on-Si: optical gain, strong nonlinearity
- Enhancement of weak functionality on silicon
  - LiNbO3-on-Si: high-speed modulation, strong nonlinearity
- Innovative new structure realization
  - Heterogeneous MOS capacitor











https://ong.ethz.ch/

Tran, APL Photon. **4**, 111101 (2019)

Mizumoto, SPIE, 89880C (2014)

Silicon photonic market forecast

(Source: Silicon Photonics 2020 report, Yole Développement, 2020)

Datacenter transceivers
Long haul transceivers
Optical interconnects
Automotive LiDAR
Immunoassay tests
Fiber-optic gyroscope
5G transceivers

2019
$480M

$364M
$117M

CAGR2019-2025 40%

2025
$3.9B

$3.6B
$18M
$20M
$22M
$44M
$61M
$186M

YOLE Développement

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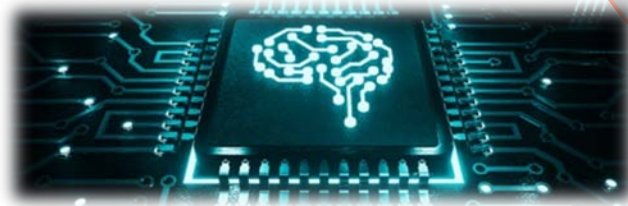
Applications



Information technology

- Telecom, 5G
- Datacenter, HPC, AI
- Optical computation
- Quantum optics

Optical metrology

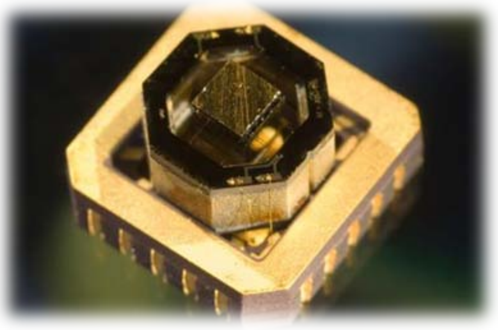
- Optical clock
- Navigation
- Spectroscopy

Silicon Photonics

1000X reduction in scale, cost and power consumption

Sensing

- LIDAR
- Gyro
- Imaging



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