Unleash Innovation

Package-Level Heterogeneous Integration – Trends and Challenges

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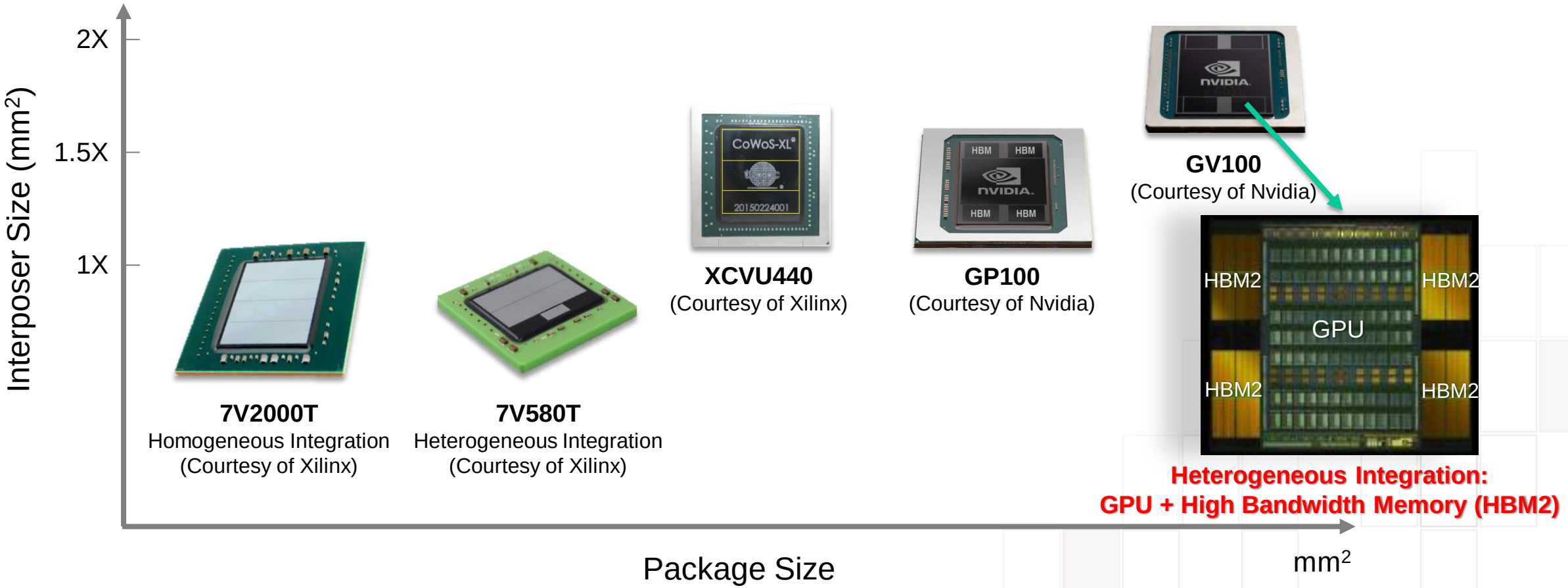
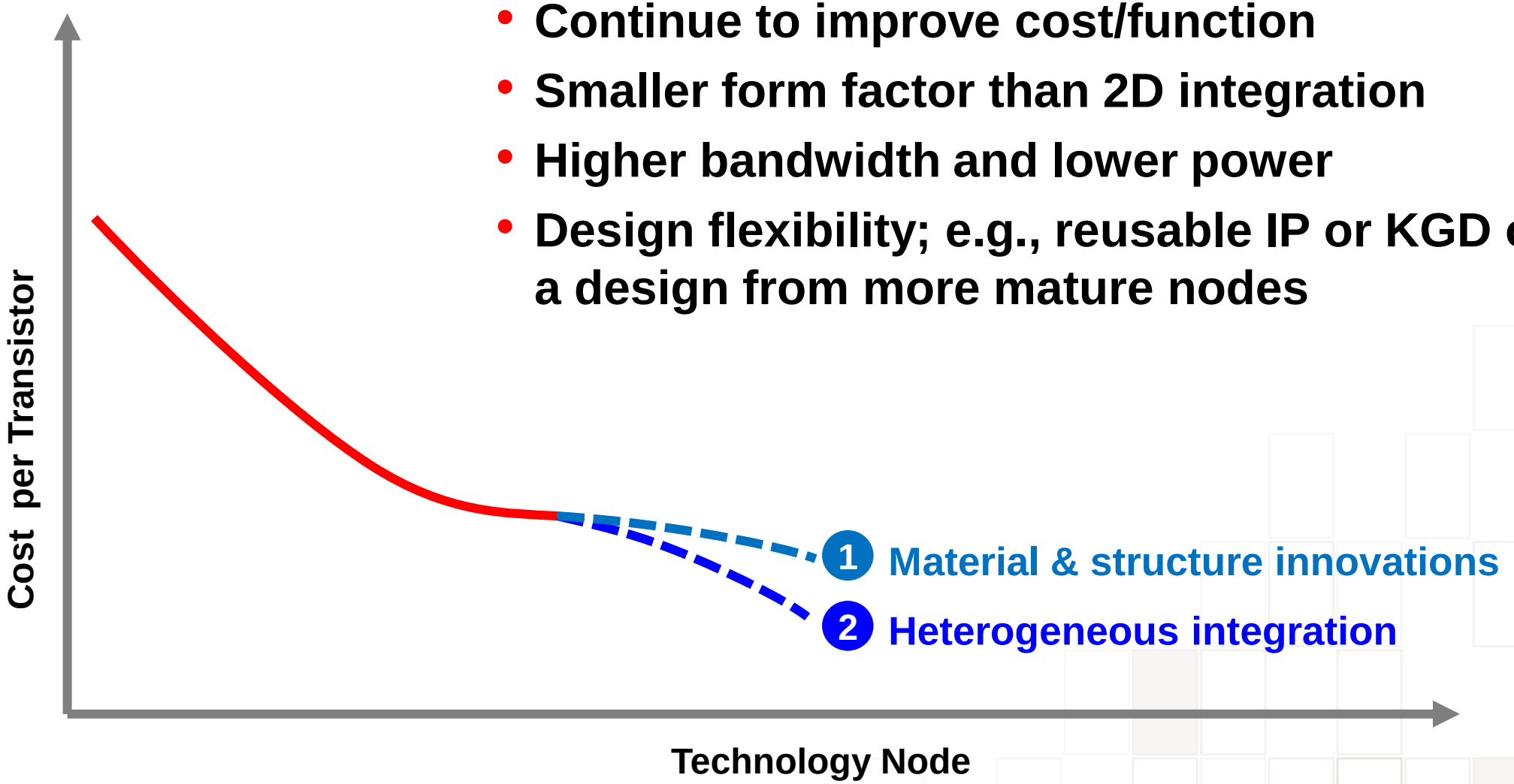
TSMC Technology Inc., North America

Heterogeneous Integration Is Gaining Momentum



Moore's Law Continues with Heterogeneous Integration

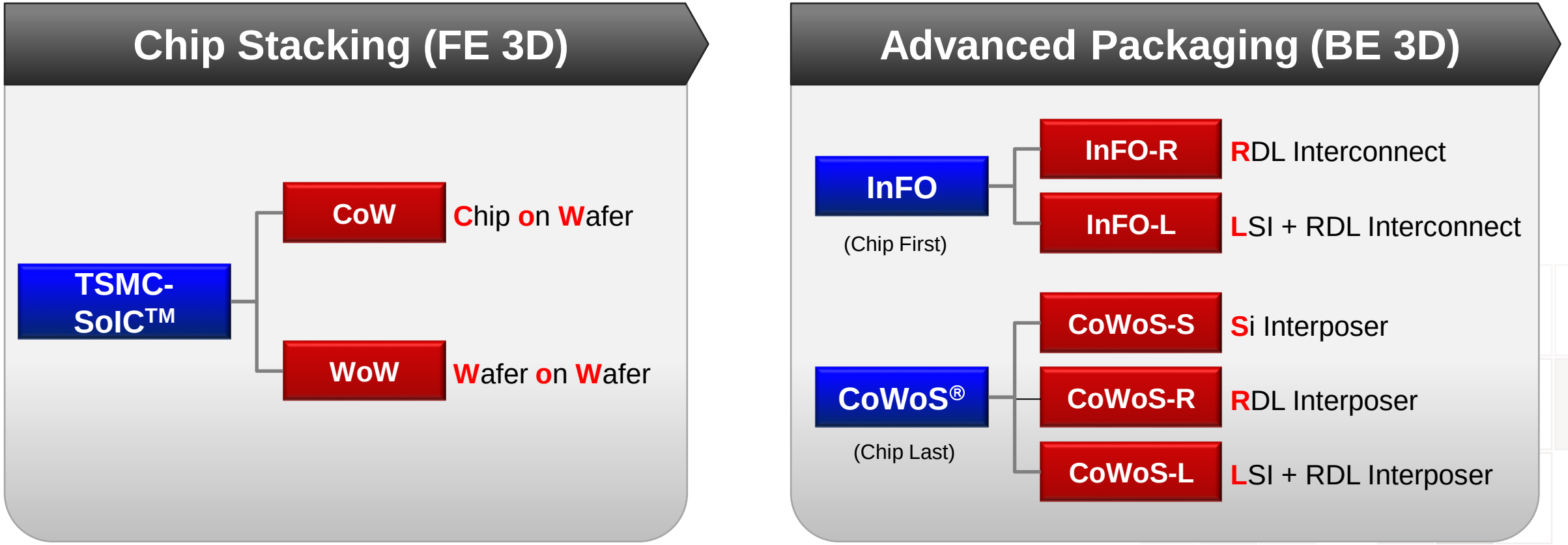
- Continue to improve cost/function
- Smaller form factor than 2D integration
- Higher bandwidth and lower power
- Design flexibility; e.g., reusable IP or KGD of a design from more mature nodes



Outline

- Introduction
- Heterogeneous Integration Technology Trends
- Design Challenges
- System/Technology Co-optimization Needs
- Summary

TSMC 3DFabric™

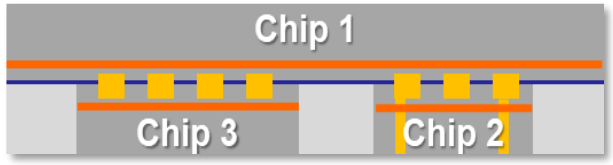


SoIC: System on Integrated Chips

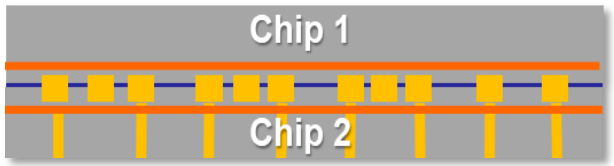
InFO: Integrated Fan-Out
CoWoS: Chip on Wafer on Substrate
RDL: Redistribution Layer
LSI: Local Si Interconnect

Wafer-Level Heterogeneous Integration Technologies

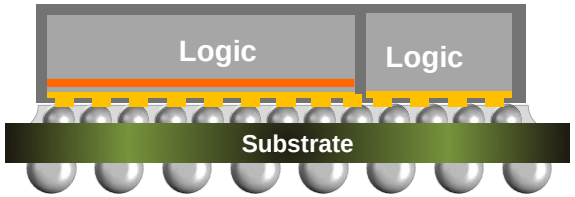
- **Frontend 3D Technologies**
  - CoW: Chip-on-Wafer



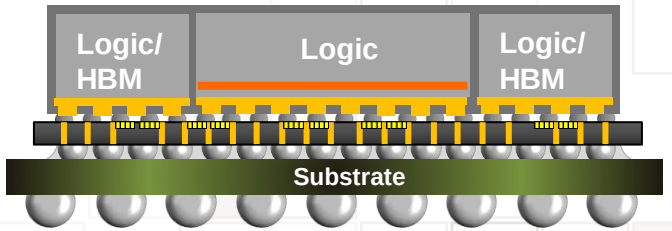
  - WoW: Wafer-on-Wafer



- **Backend Packaging Technologies**
  - InFO: Integrated Fan-Out



  - CoWoS®: Chip-on-Wafer-on-Substrate

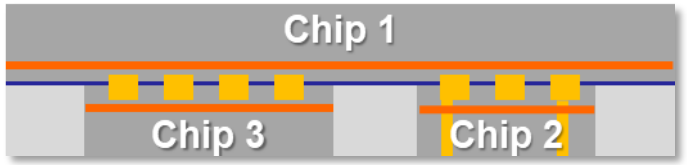


Combinations of 3D IC System Integration Technologies

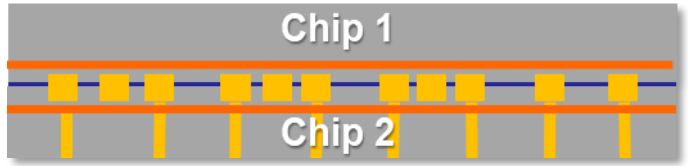
Unleash Innovation

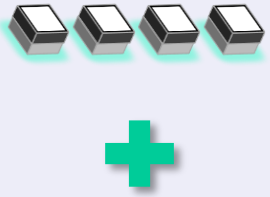
Logic Die Form

CoW



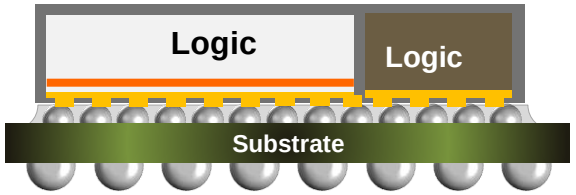
WoW



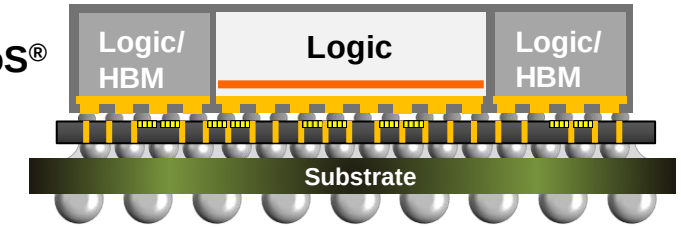


Packaging Choice

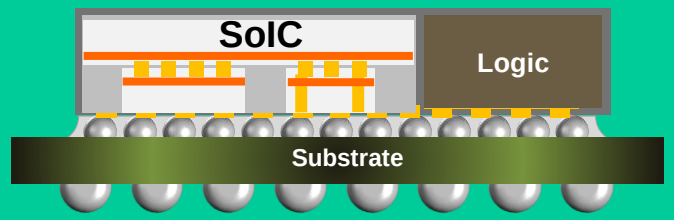
InFO

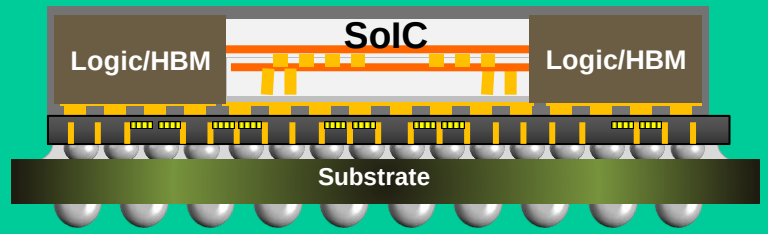


CoWoS®

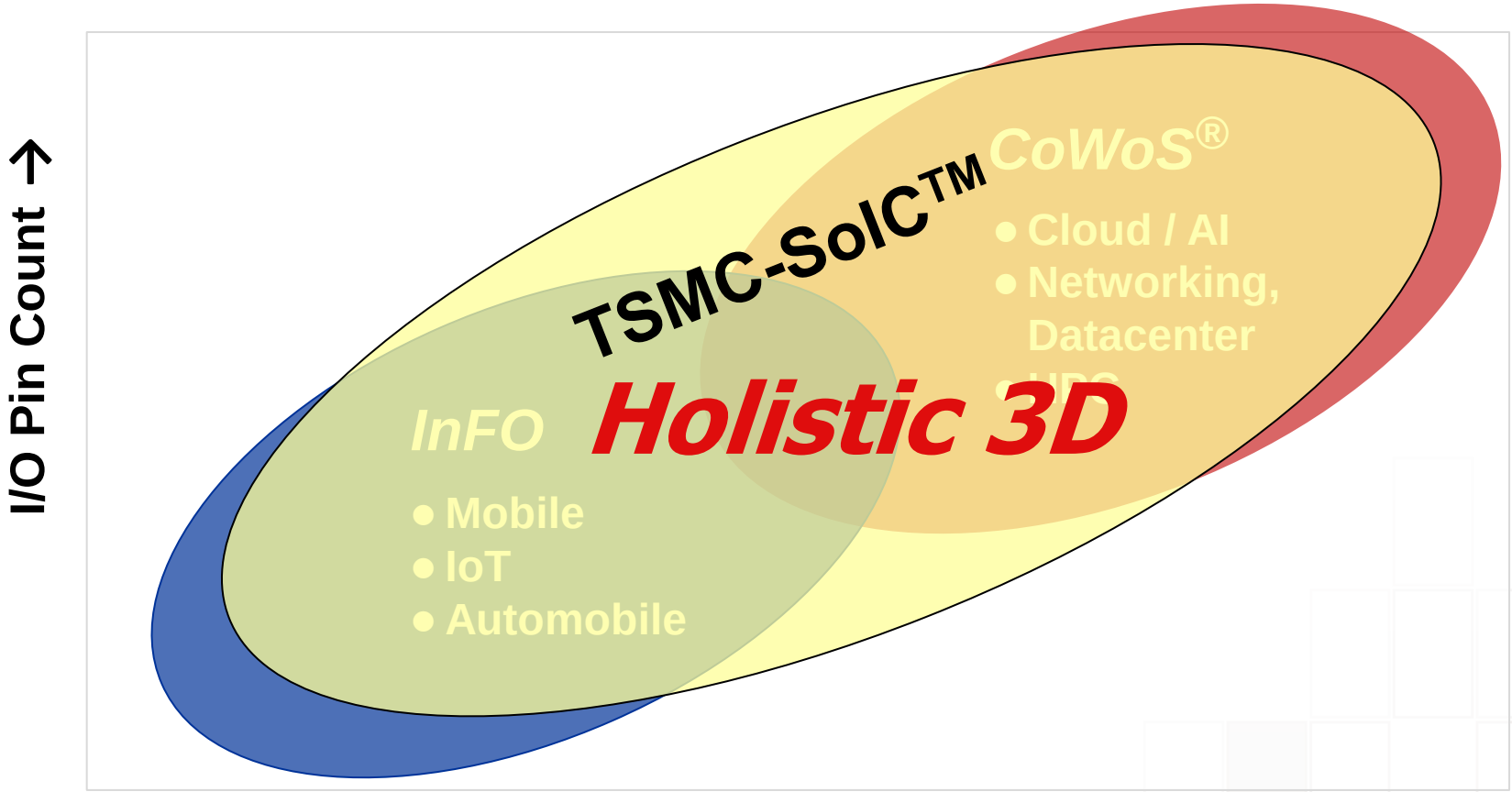


3D IC Packaging Technology with Silicon Integration Flexibility



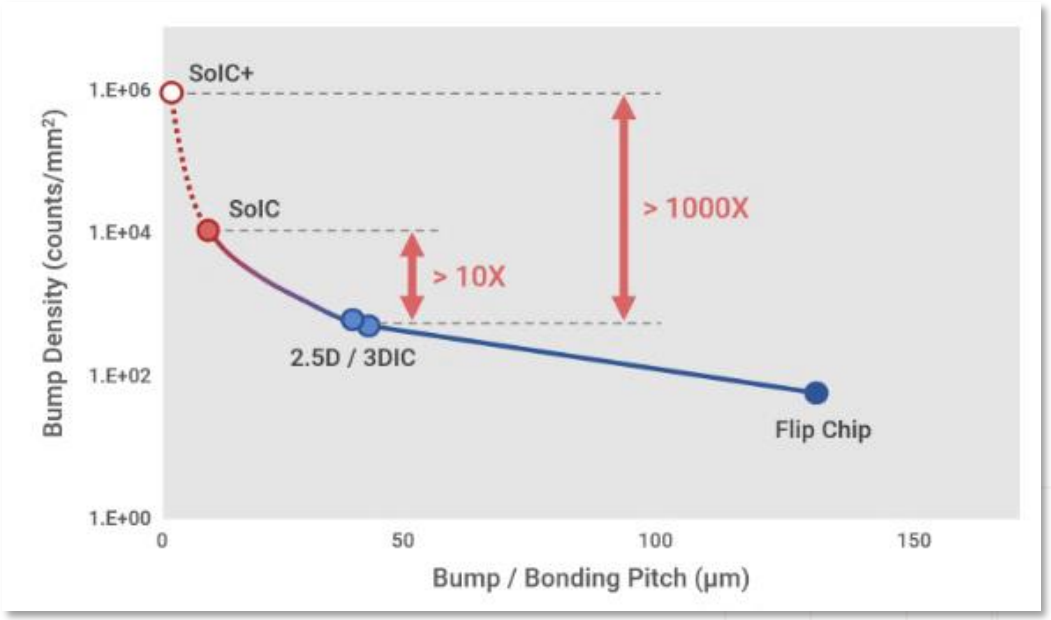


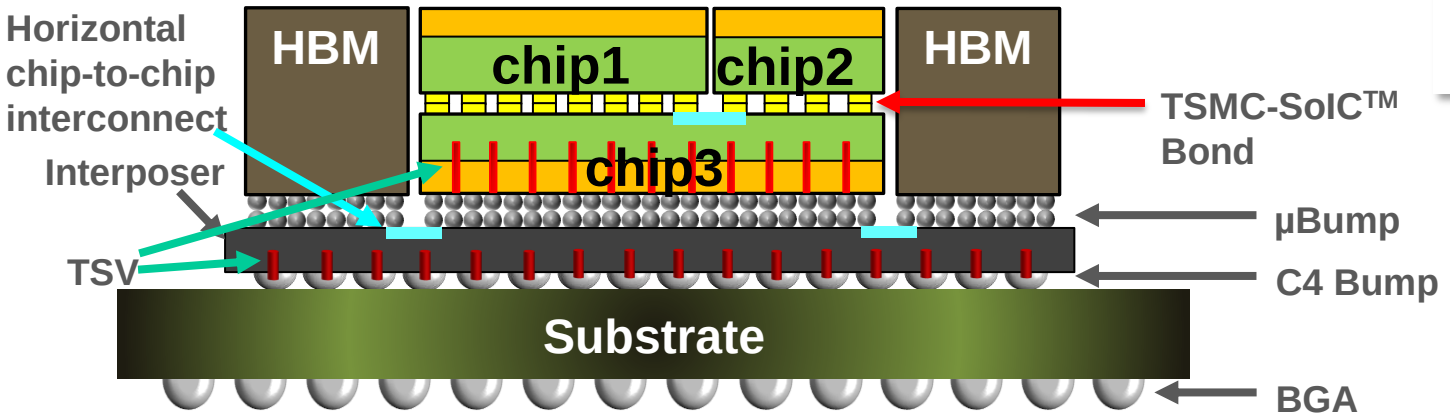
TSMC 3DFabric™ – A Holistic 3D Integration Platform



Advanced Packaging Technology Trends

- Smaller bump/bond pitch
- Larger package size
- 3D integration





Outline

- Introduction
- Heterogeneous Integration Technology Trends
- Design Challenges
- System/Technology Co-optimization Needs
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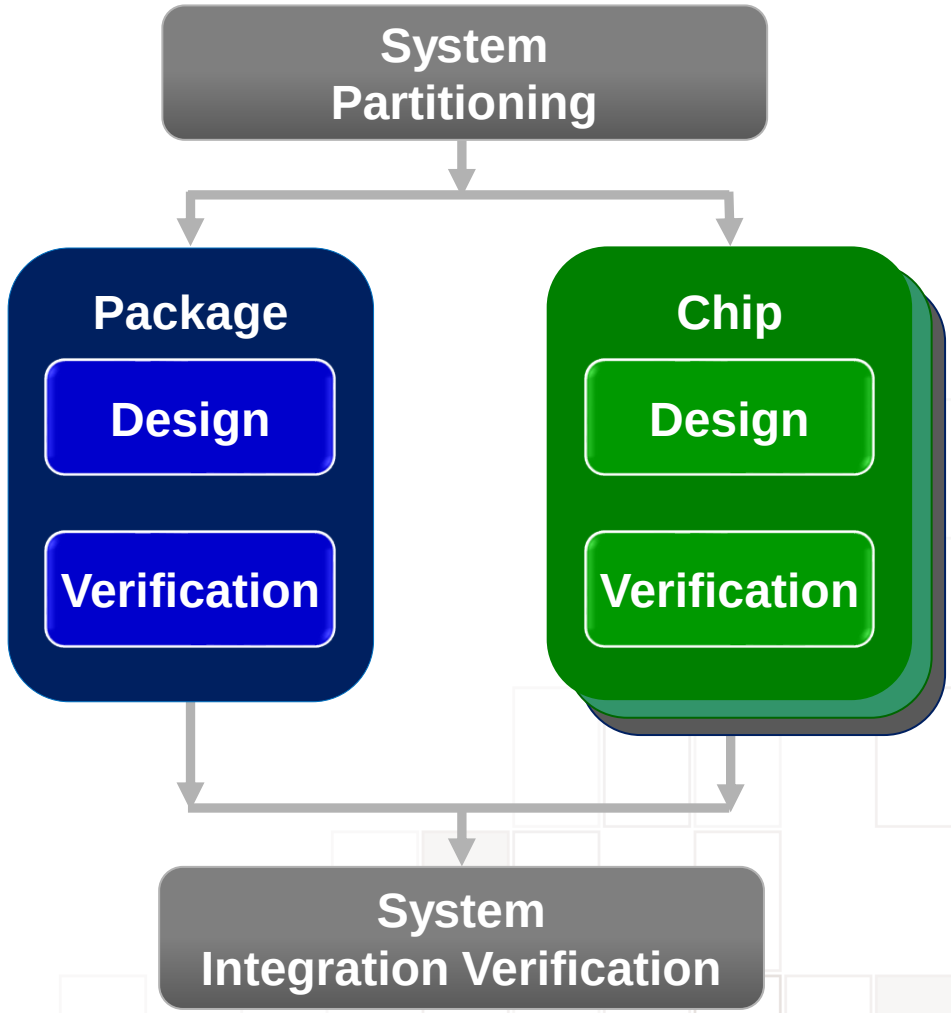
System Dis-integration and Chiplet Integration Design and Verification

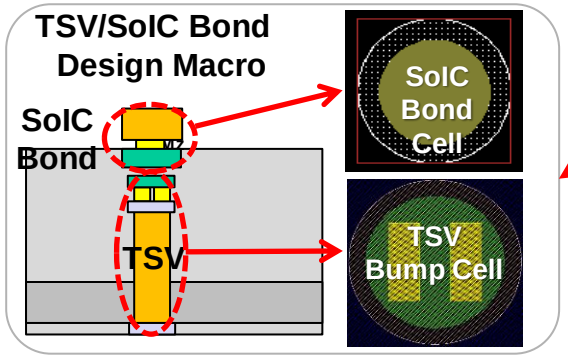
A hierarchical approach

- System partitioning
  - Functions and timing/power budgets
- Package floorplan
  - Chip locations
- Chip implementation
  - Pin/bumps locations constraints
- Package-chip interface
  - Logical
  - Physical
  - Electrical
  - Test
- Full integration verification

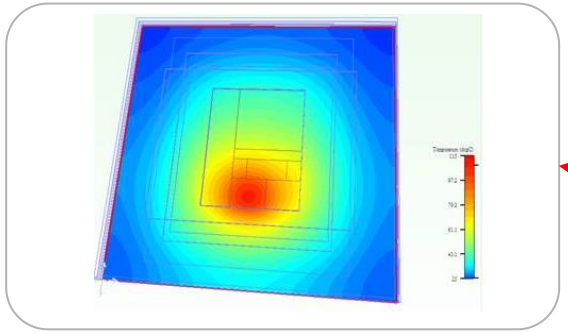


TSMC-SoIC™ Design Challenges

- Design macros



- Heterogeneous technology timing closure
- Thermal



Import Macro Lib

TSVs/TDVs/
SoIC Bonds Placement

APR

DRC/LVS/RCX/STA

SI/PI/IR/EM

Thermal

System
Partitioning

Package

Design

Verification

Chip

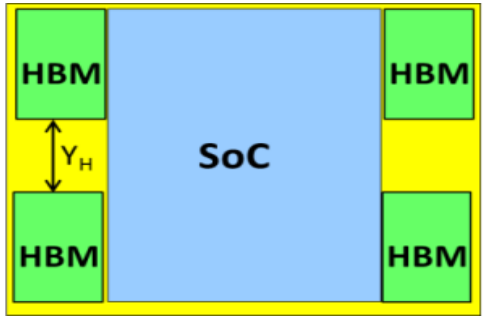
Design

Verification

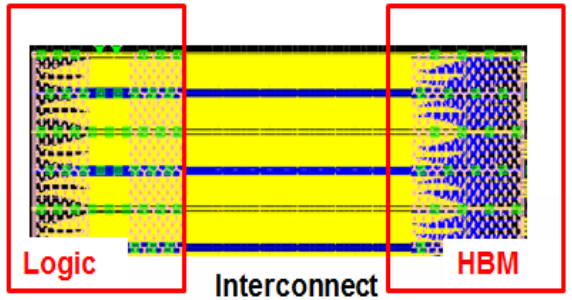
System
Integration Verification

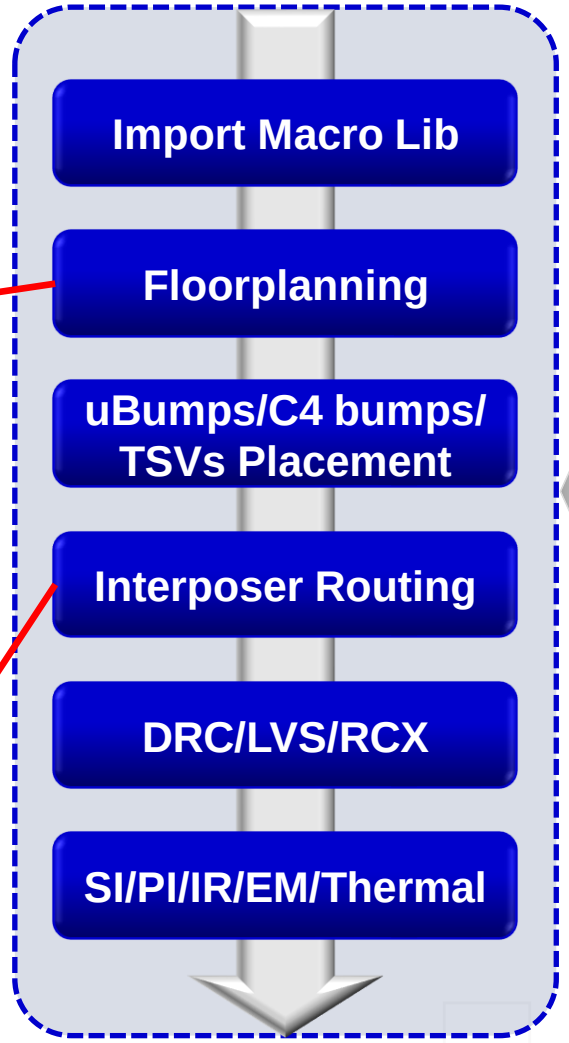
CoWoS® Package Design Challenges

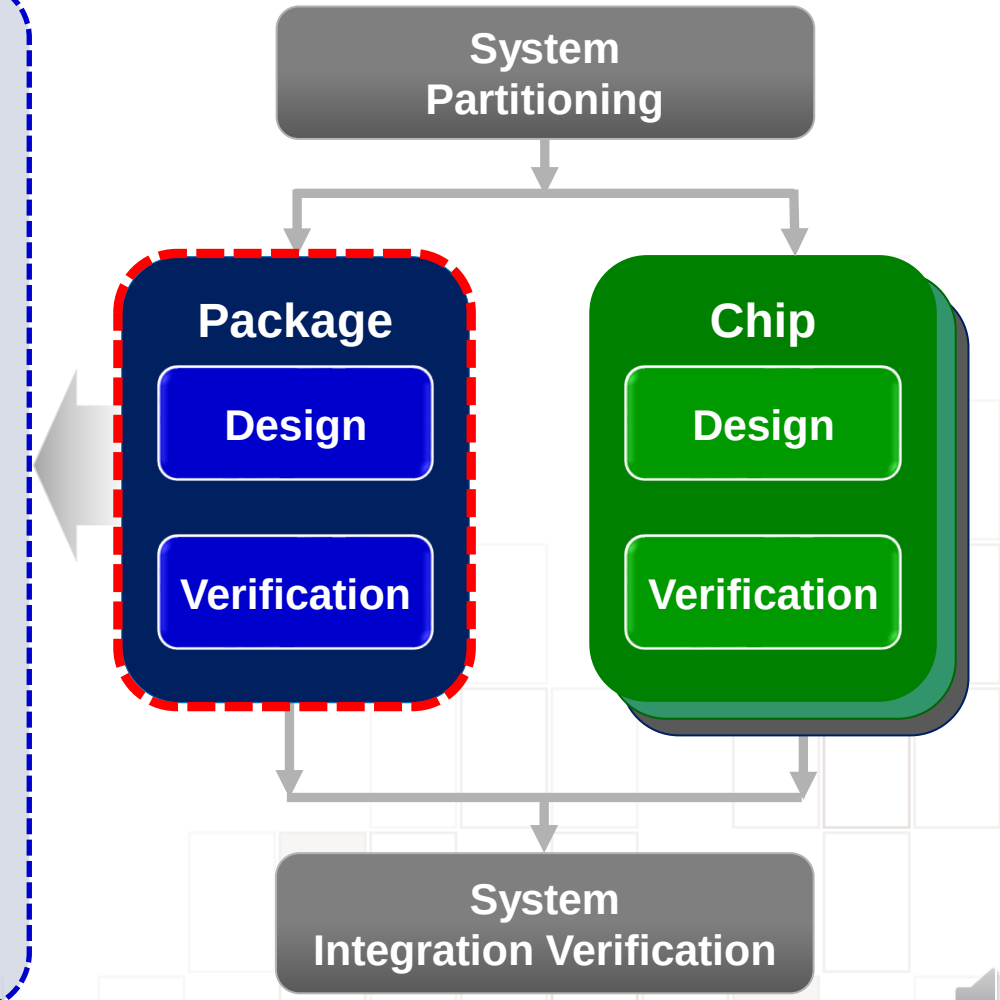
- **Warpage**
  - **Warpage-aware floorplan**



- **High bus bandwidth density**
  - **Impedance-matched routing**
  - **Shielding**

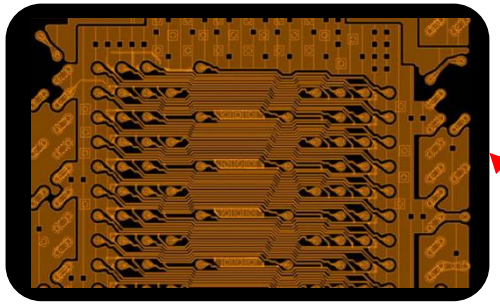




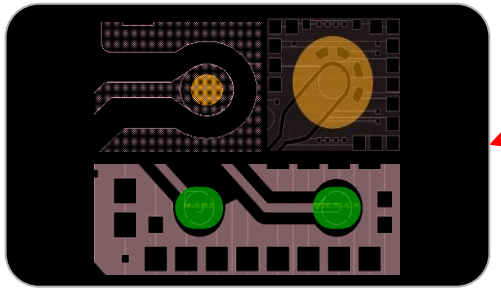


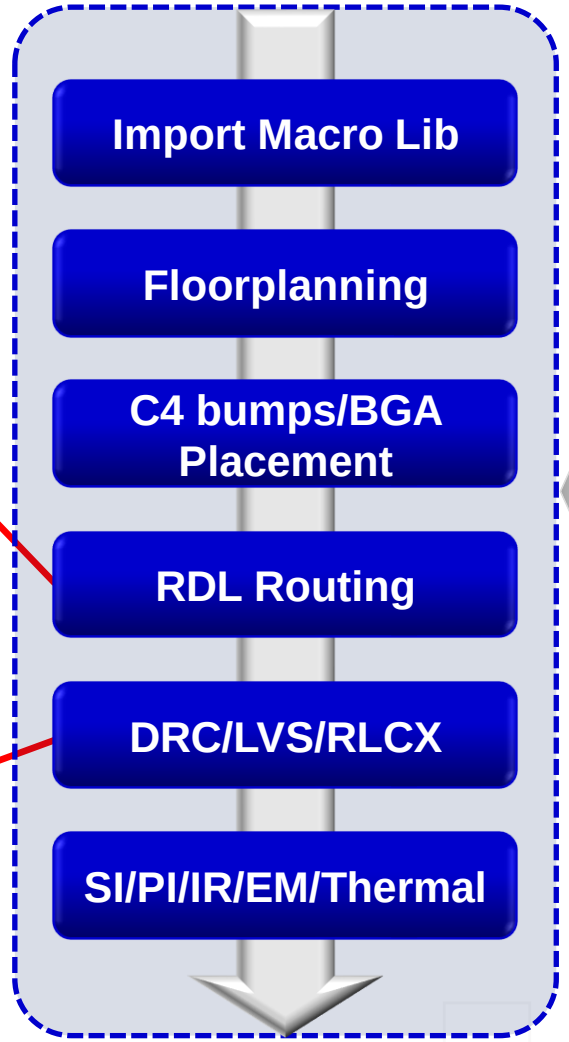
InFO Package Design Challenges

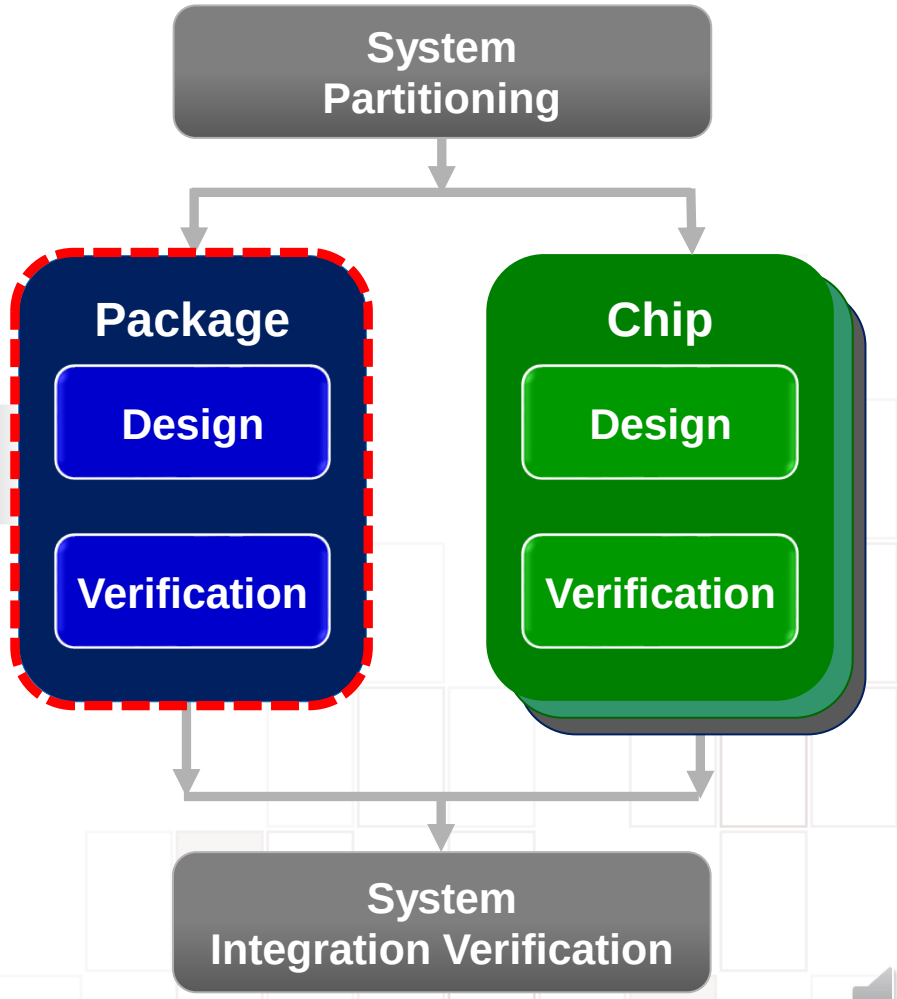
- Unique shapes create challenges for
  - Layout and routing



  - DRC/LVS/RLC Extraction

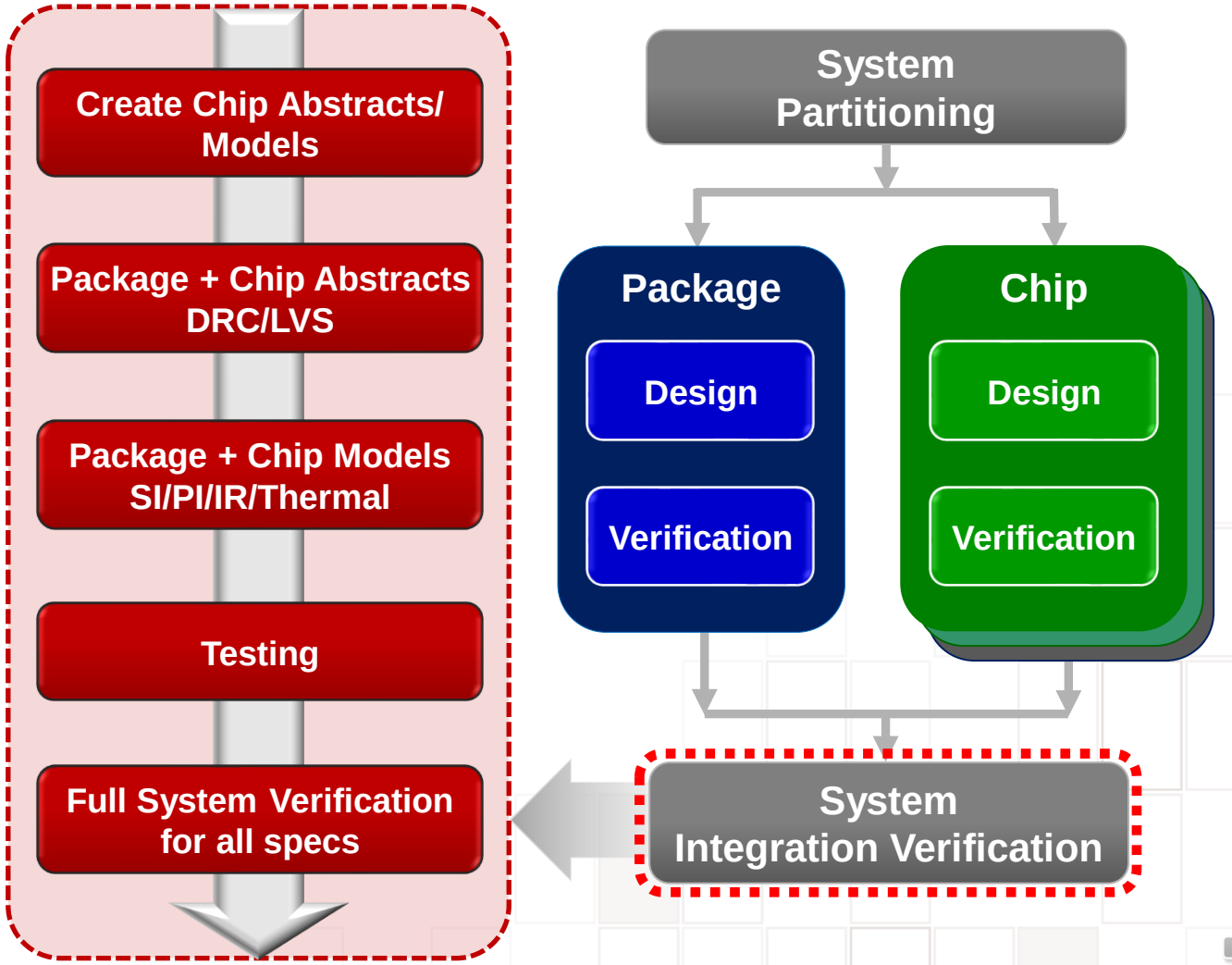






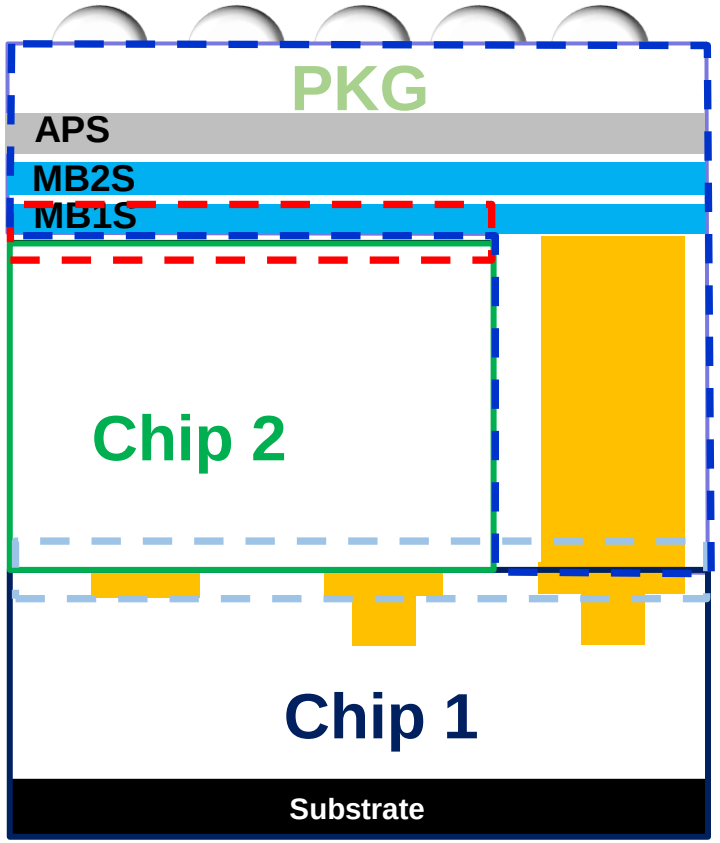
Package-Chip Integration Verification Challenges

- Tools capacity and run time
  - Hierarchical flow
  - Chip abstracts/models creation
- Interface verification
  - Electrical
  - Physical
  - Logical
  - Testing
  - 3D Vertical stacking blocks 2D chip probe pads



Comprehensive Interface Connectivity Check

- A SoIC example

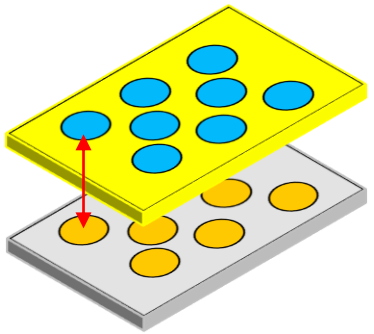


: PKG Connectivity Check

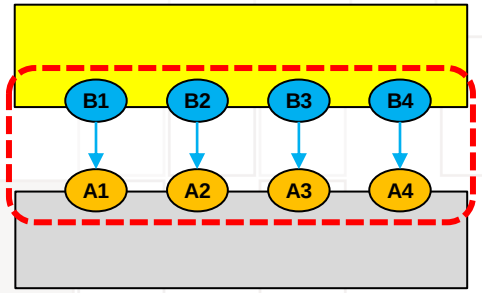
: Chip2 and PKG Connectivity Check

: Chip1, Chip2 and PKG Connectivity Check

Alignment

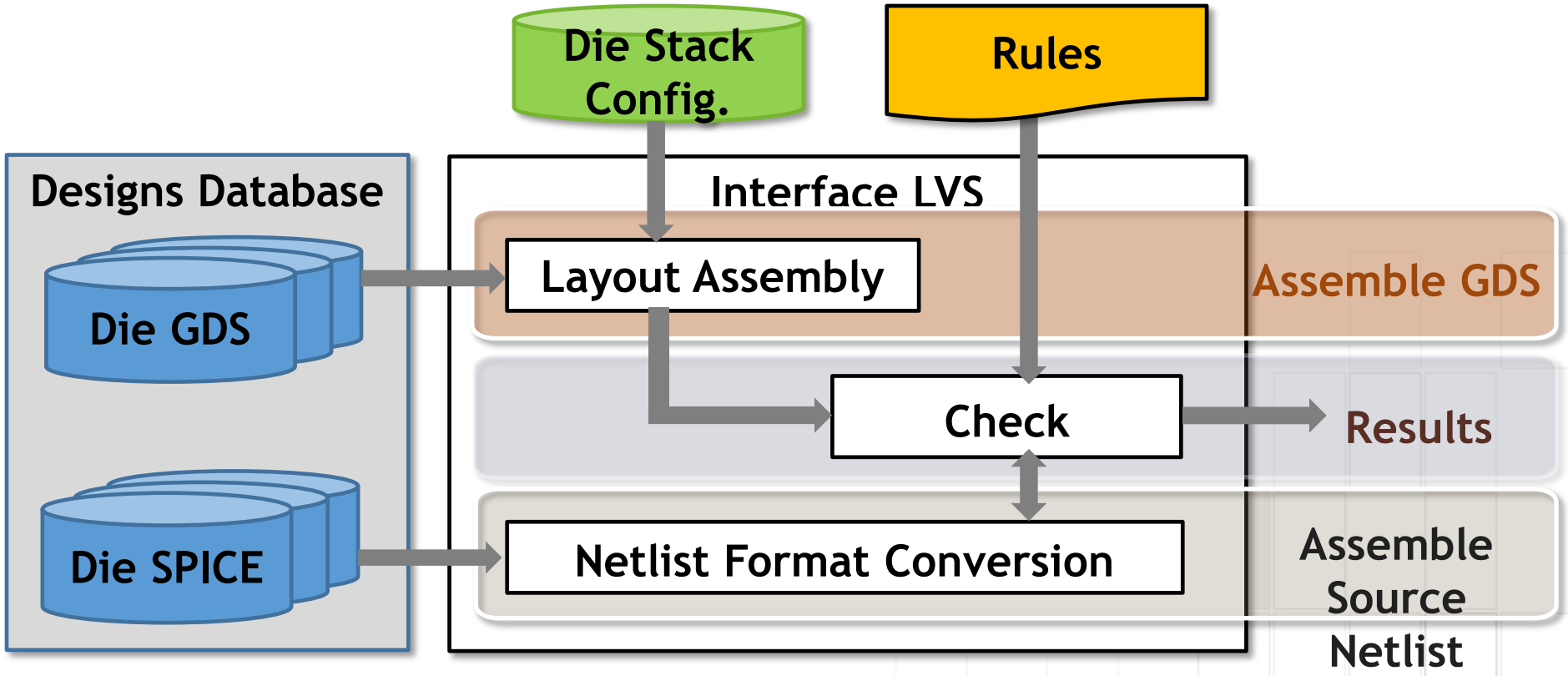


Connectivity



Coping with Hybrid Design Databases

- Different dies may come from different technologies and are represented in different design databases
- Hybrid design databases need to be merged for DRC/LVS/RC analyses



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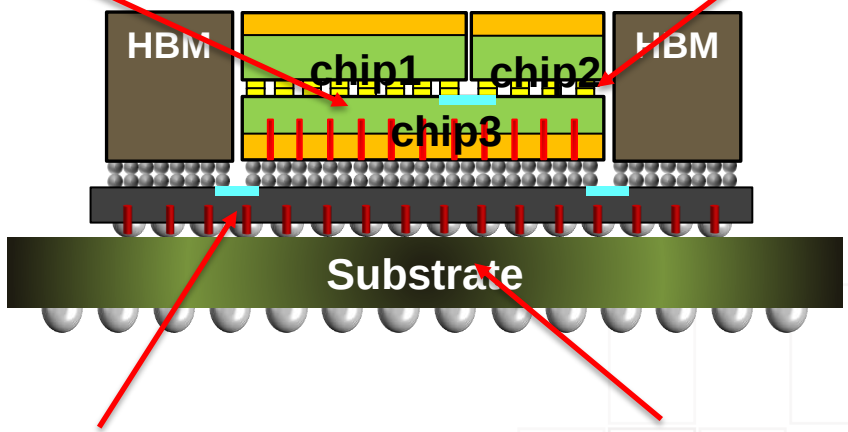
System/Technology Co-Optimization

- **Objectives**
  - Cost, performance, power, area, yield, form factor
- **Co-Optimization examples**
  - Chip-to-chip link speed
    - I/O drivers, ESD, routing patterns
  - Power Delivery Network
    - Decoupling cap, voltage regulators, power TSVs

Thermal analysis
Thermal optimization
Thermal-aware floorplan

Vertical connections:
I/O, ESD, STA, DFT



Horizontal connections:
Crosstalk prevention layout
Interconnect SI/PI analysis
I/O, ESD, STA, DFT

PDN analysis and design
Stack IR/EM analysis
IPD/SHDMIM/DECAP effect
Chip power modeling

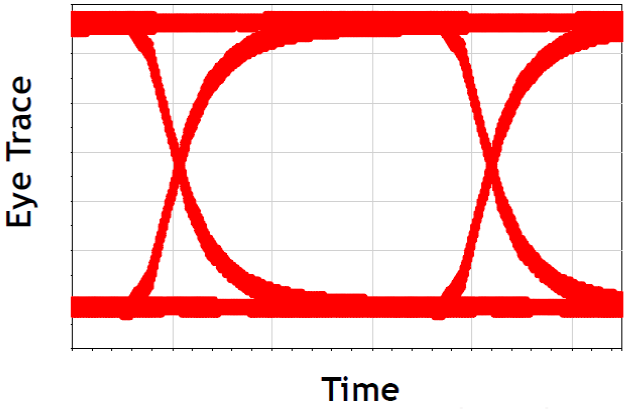
Package Die-to-Die Interconnect Parameters

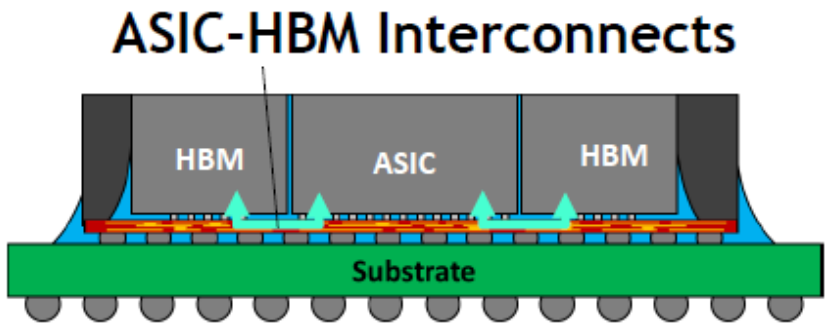
- Different package interconnects have different RC loading
- Different dies have different PVT variations
- ➢ Need to optimize I/O circuits for power, performance, and area for each packaging technology

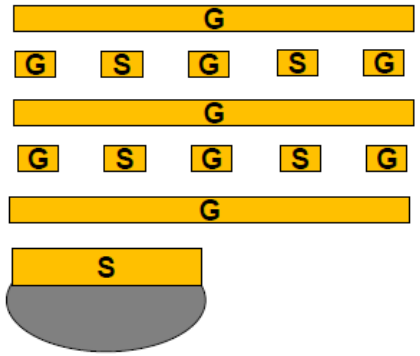
	MCM	CoWoS®	InFO	TSMC-SoIC™
I/O Circuits	GPIO	HBM PHY, LIPINCON™	LIPINCON™	Lite I/O
Bump/Bond Pitch	130 µm	40 µm	40 µm	< 10 µm
Trace Length	10 ~ 20 mm	0.5 ~ 10 mm	1 mm	0.01 mm
Channel Insertion Loss	High	Medium	Medium	Low
Power Efficiency	Low	Medium	Medium	High

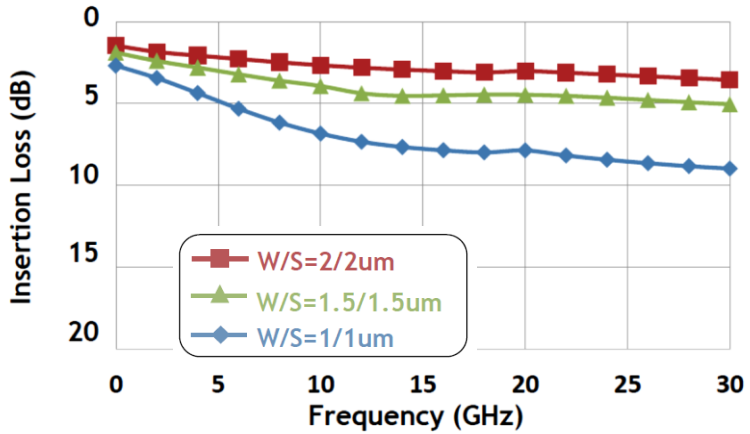
Interface Interconnect Design Optimization

- **High data rate bus design requires optimization on**
  - **Shielding pattern**
  - **Routing width/spacing**
  - **Number of routing layers**



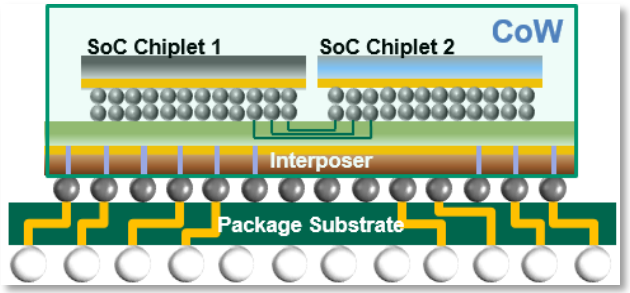


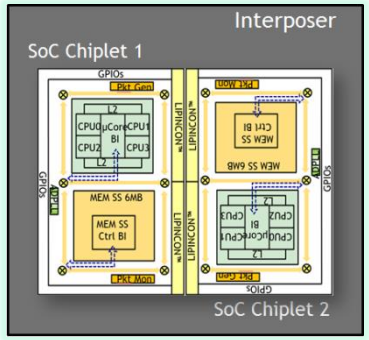


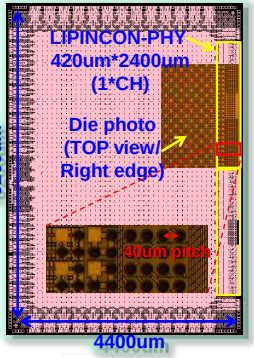


High Speed Interface I/O Design Optimization

- **Design goals**
  - High speed
  - Low energy
  - PVT variation tolerant







A CoWoS® Example

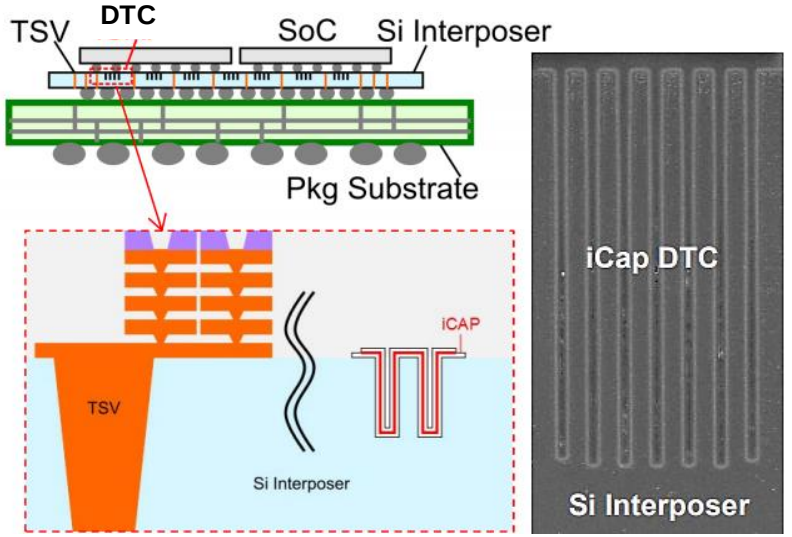
- 7nm 4GHz Arm® A72 based CoWoS® chiplet design for HPC Application
- LIPINCON™ for inter-chiplet PHY
  - Bandwidth: 320 GB/s
  - Data rate: 8 Gbps
  - Power efficiency: 0.56pJ/bit
  - Bandwidth density: 1.6 Tb/s/mm²
  - 0.3V low swing I/O

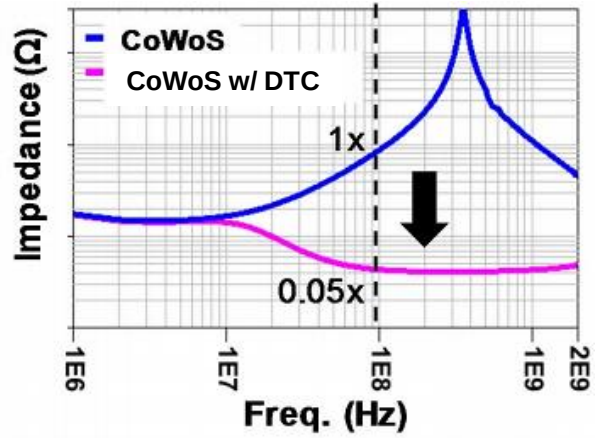
Comparison	IEEE JSSC 4/2020	ISSCC'18	ISSCC'17	Hot Chip'16
Company	TSMC	AMD	Intel	TSMC
Technology	7nm FinFET	14nm FinFET	14nm FinFET	16nm FinFET
Vsw (V)	0.3	low-swing	-	0.3
Bus Width	320	256	-	256
Channel	CoWoS 500µm	MCM -	EMIB 1mm	InFO 550µm
Die-to-Die Bump Pitch (µm)	40	>100	55	40
Data Rate (Gbit/s/pin)	8	5.3	2	2.8
IO Power Eff. (pJ/bit)	0.073	-	-	0.062
PHY Power Eff. (pJ/bit)	0.56	2	1.2	0.42
Bandwidth Density (Tbit/s/mm²)	1.6	-	1.5	0.3

Source: M. Lin, et al., p. C28, Symposium on VLSI Circuits, 2019

Si-Interposer Deep Trench Capacitor (DTC)

- **Key benefits**
  - Lower PDN impedance
  - Reduced voltage droop
  - More efficient than MIM cap
- **High-K deep trench capacitors**
  - 340 nF/mm^2
  - Low leakage current
    - < 1 fA/μm^2 @ 105C
  - Long TDDB lifetime
    - 1000 years @ 1.35V

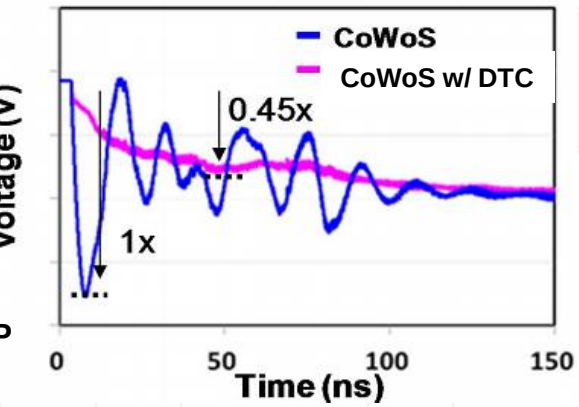




Power delivery network impedance

	CoWoS	CoWoS w/ DTC
PDN |Z| @100MHz	1x	0.05x
Voltage droop	1x	0.45x

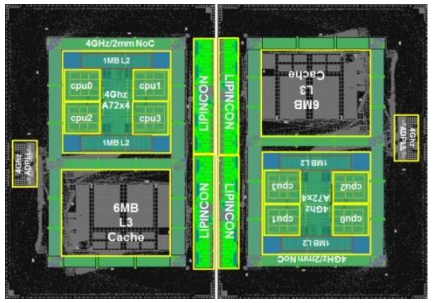
Compare CoWoS Technology with and without iCAP

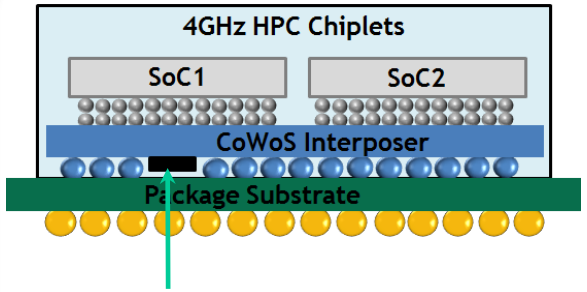


System level voltage droop

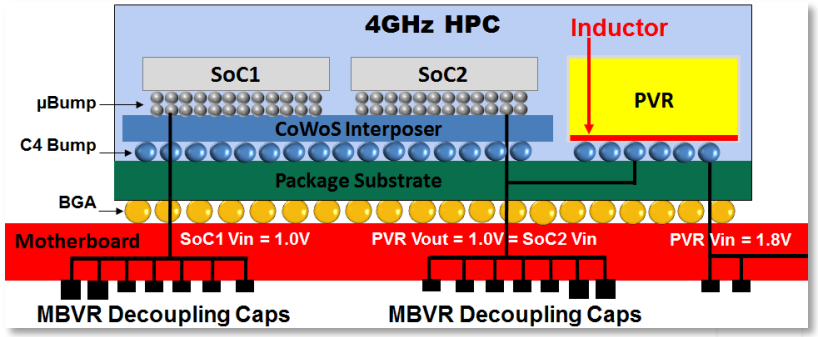
Source: S. Y Hou, et al., p. 462, IEDM 2019

System-In-Package Optimization by IPD Capacitors and in-Package Voltage Regulator with On-Die Inductors



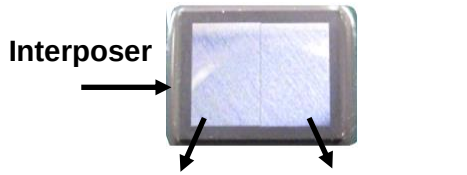


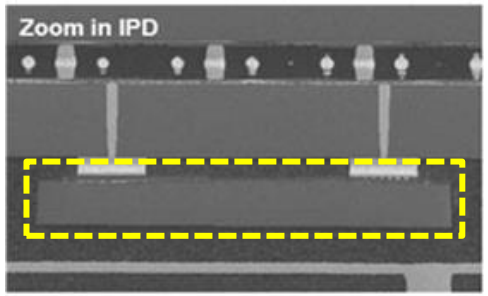
IPD under Si-Interposer

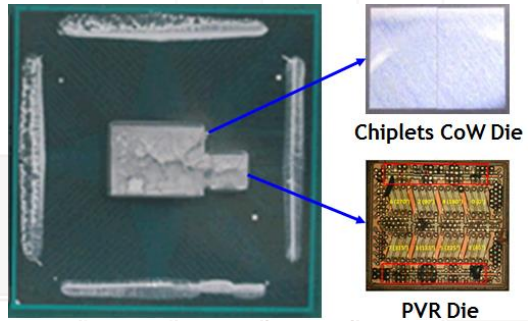


- 7nm 4GHz CoWoS dual-chiplets using LIPINCON™ PHY for cross-chiplet interface
- IPD Caps under Si-Interposer
- In-Package VR (PVR) with low-loss on-die Inductor

N7 HPC Chiplets CoW





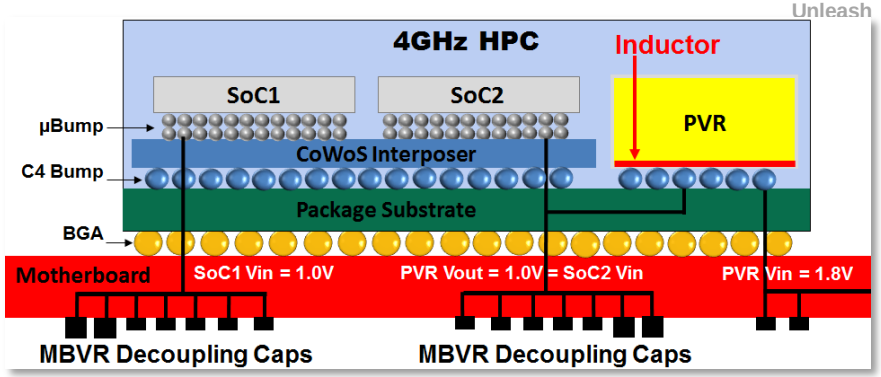


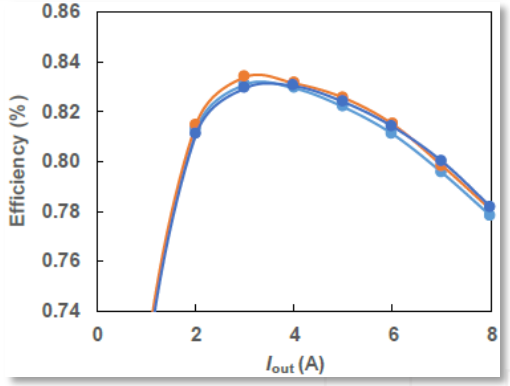
In-Package Voltage Regulators

- In-Package Voltage Regulators (PVRs)
  - Save system board areas
  - Reduce system power loss due to PCB traces on the motherboard

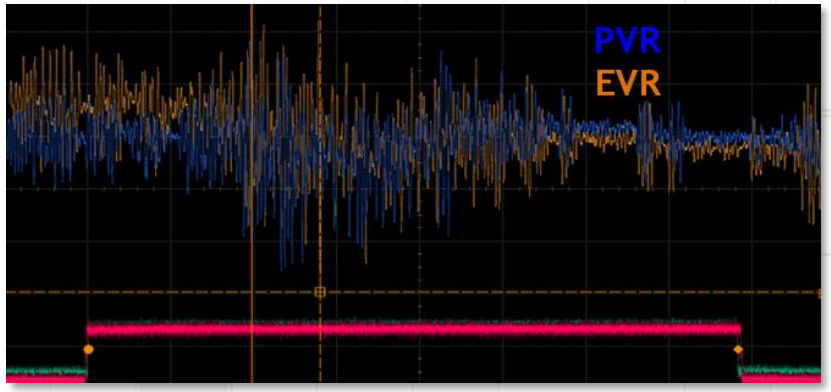
➢ A PVR example

  - 4GHz dual HPC chiplets on Si-interposer with both CoW and PVR die on substrate
  - PVR regulates SoC2 and external VR (EVR) regulates SoC1
  - Both deliver 4GHz performance at 1V and correlate well running Dhrystone at 4GHz
  - PVR peak efficiency for target Vout at 1.0V is 83–84%



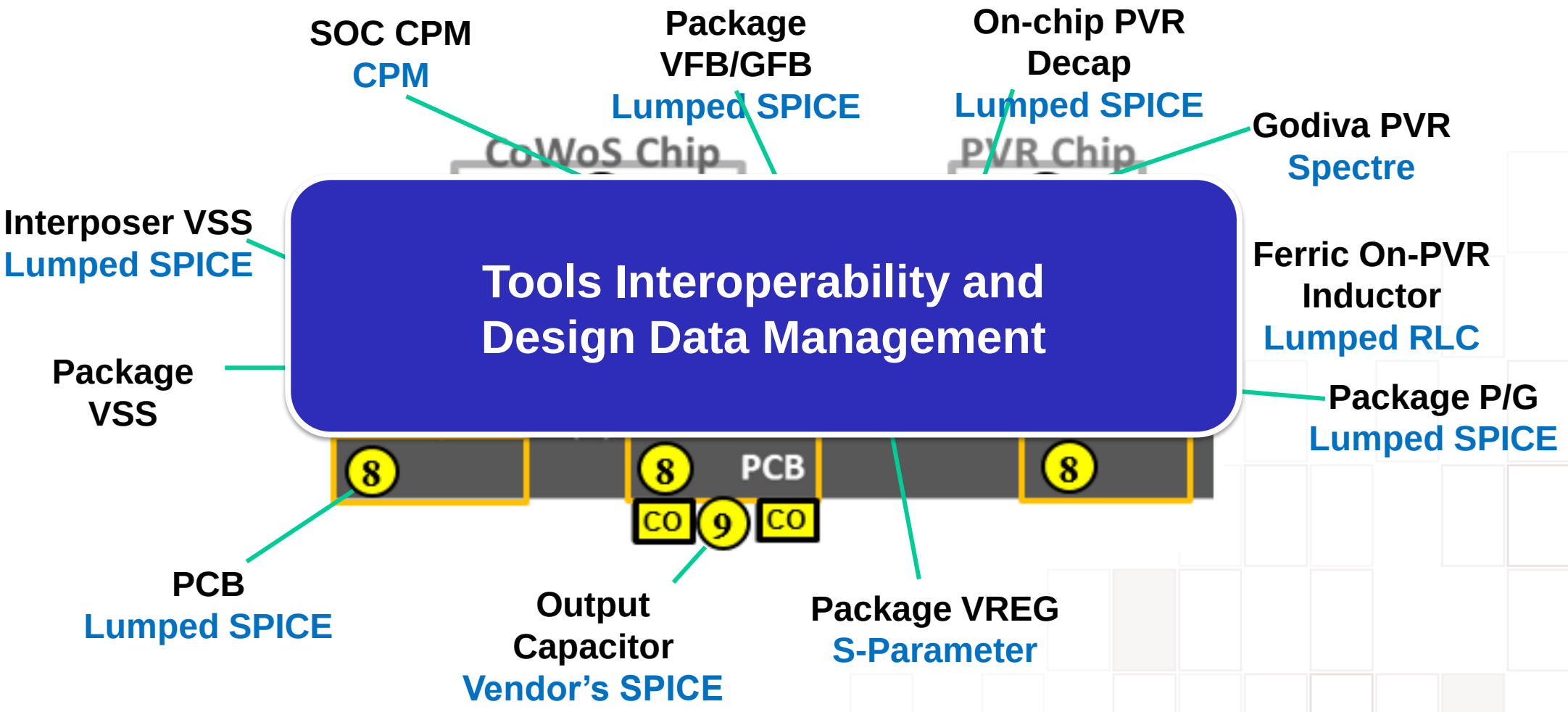


Measured PVR efficiency vs. *I*out at *V*in = 1.7V, *V*out = 1.0V, and *f*sw = 120MHz



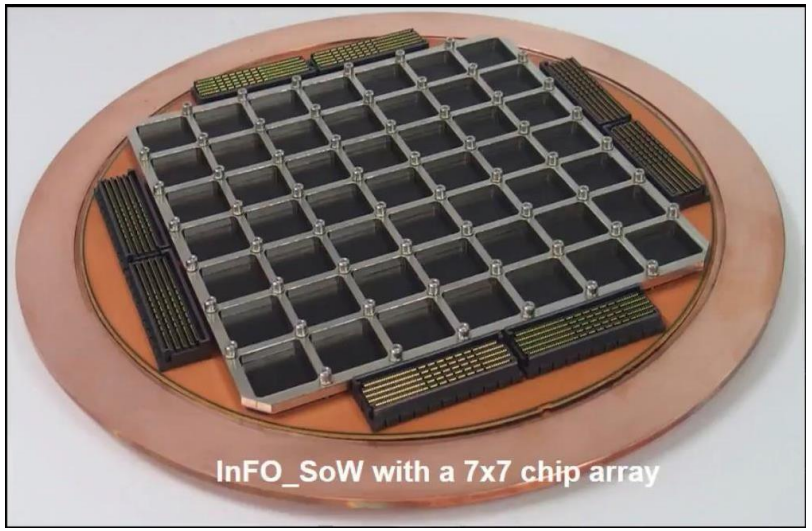
Source: A. Roth, et al., JFS5.5, Symposium on VLSI Circuits, 2020

System-Level PDN Modeling and Analysis Challenge

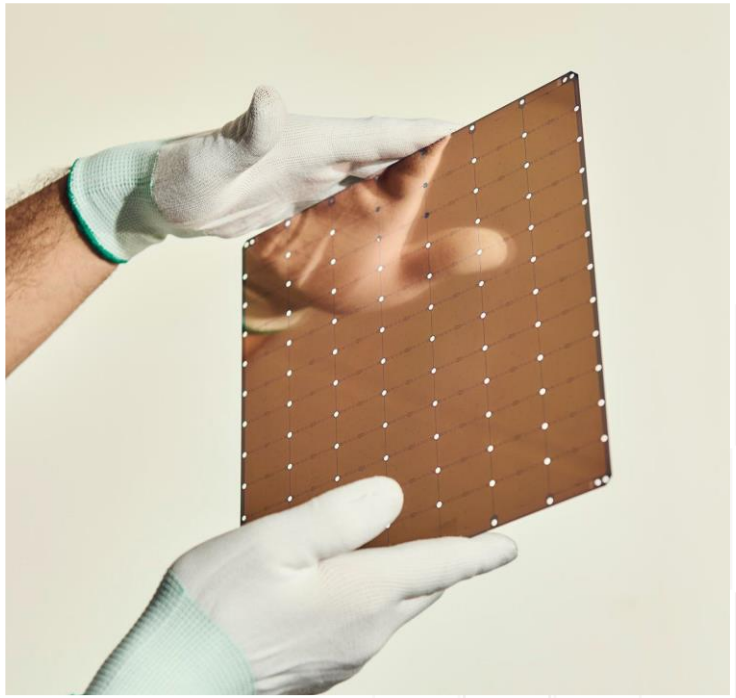


System on Wafer Verification Challenge

- **EDA tools scalability**
  - **Capacity and run time**



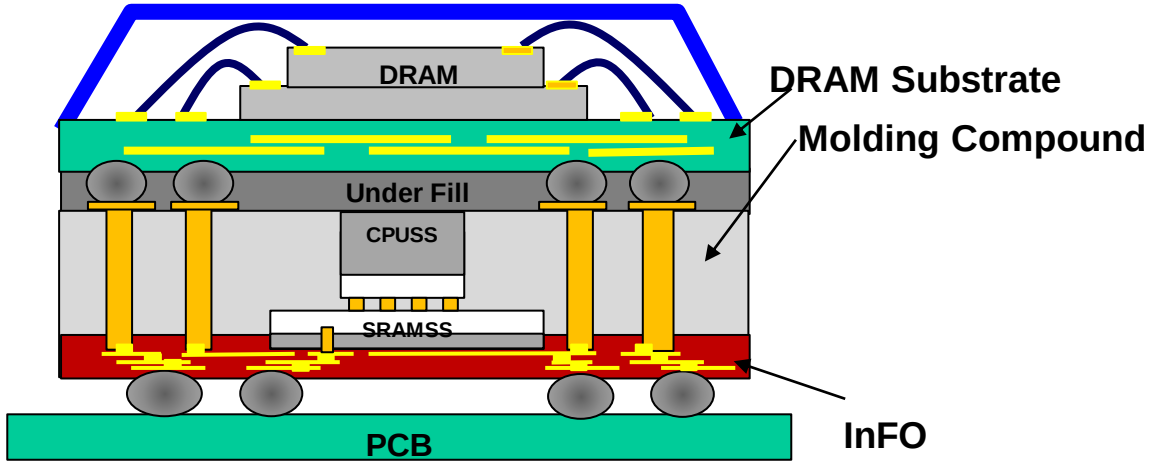
S. R. Chun, et al., ECTC, 2020.

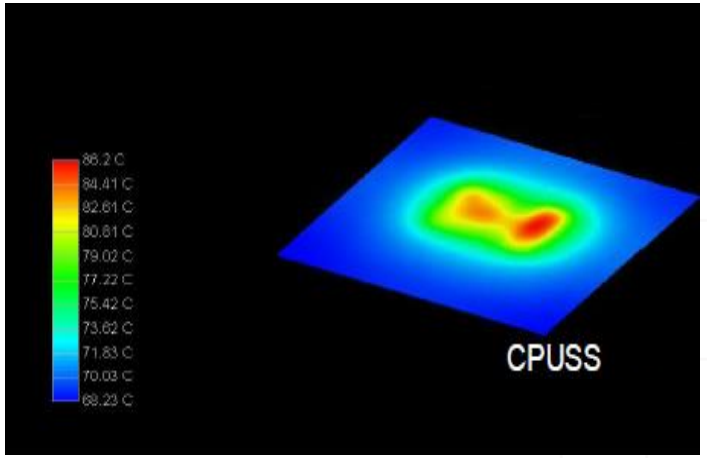


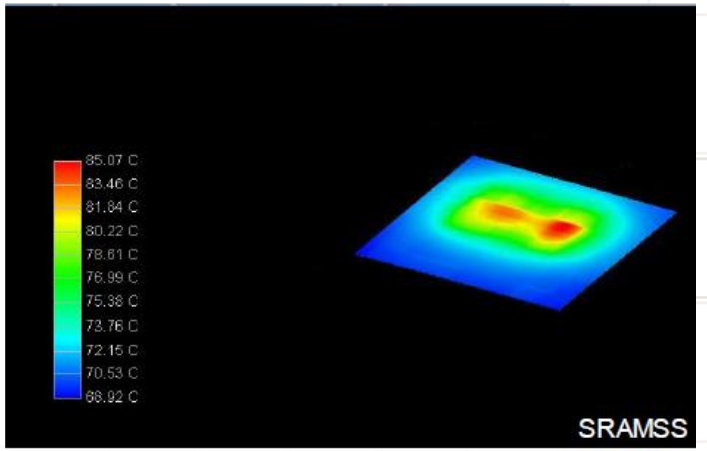
Cerebras Wafer Scale Engine,
S. Lie, Hot Chips, 2020.

Thermal Design Challenge

- **System-Technology co-optimization is needed**
  - **Package: form factors, architectures, materials**
  - **Stacked dies: 3D floorplan, die thickness, DVFS**
  - **Electric-Thermal co-simulation**







Summary

- Moore's law continues with heterogeneous integration technologies
- Technology trends
  - Increasing package size
  - Decreasing bump/bond pitch
- Many system/technology co-optimization opportunities exist to reduce cost and improve performance, power, area, and yield
- Design technology platforms have been streamlined and are more productive. Still better integration/interoperability between tools is needed.

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Unleash Innovation

Thank You