# Circuit Reliability Mitigation Techniques & EDA Requirements

**EDPS 2019**


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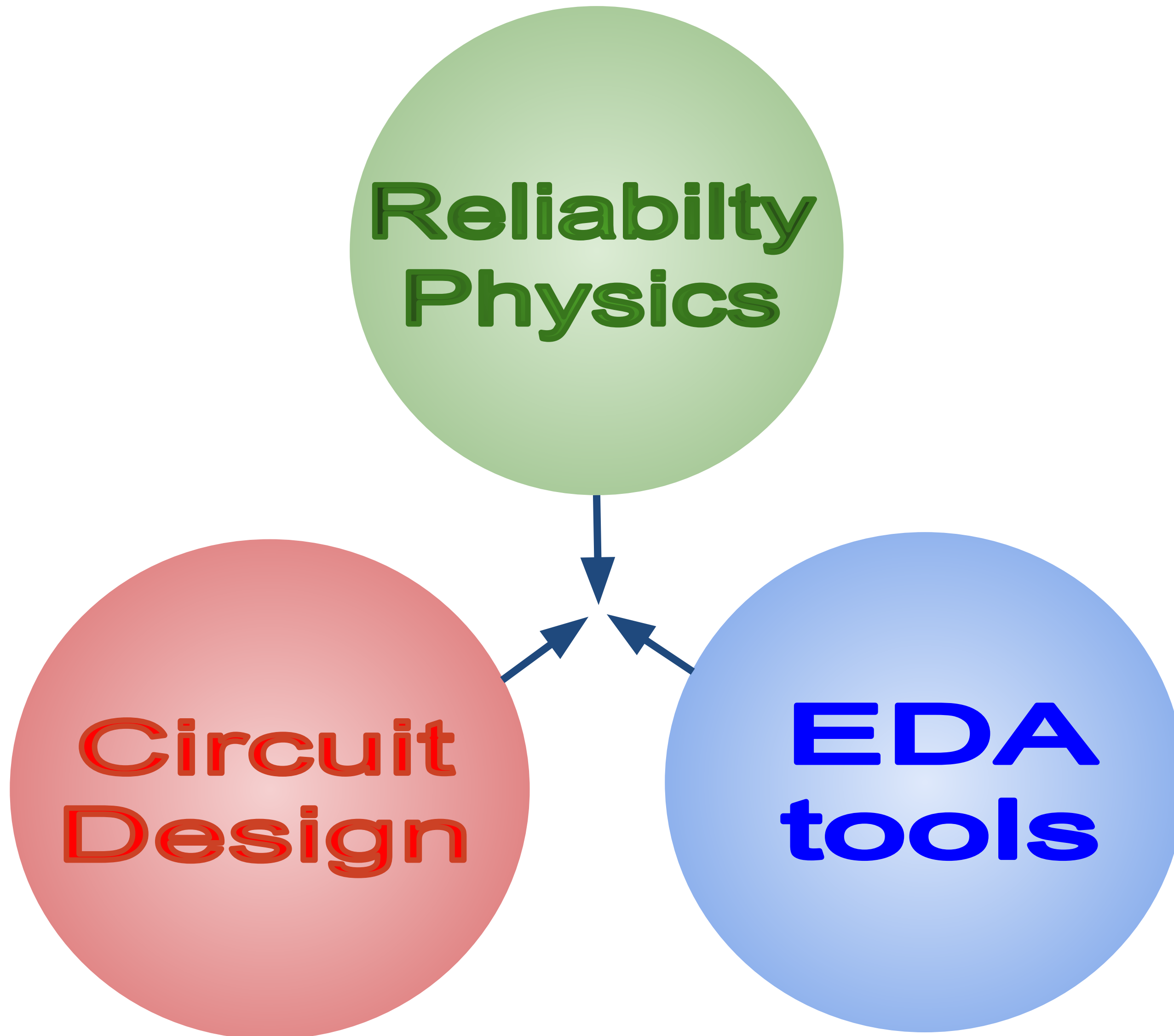
# Purpose



# Outline

- Introduction
- Main Reliability Degradation Mechanisms
  - Voltage, Temperature, Activity dependencies
- Impact on Circuits and Products
  - Reliability Circuit Analysis & optimization
  - Aging monitors
  - Adaptive techniques
  - HTOL Best practices
- EDA requirements
- Conclusions

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# Introduction

- Accurate Circuit Reliability analysis is a must
  - Reduce design margins and time to market
  - Maximize product performance and reliability.
- Reliability specifications are typically based on DC measurements and certain Voltage, Temp
- Reliability analysis is very challenging due Voltage, Temperature and workload activity variations over the lifetime of the product
- Need very close cooperation amongst Reliability Physics, Circuit and EDA Experts

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# Main Reliability Degradation Mechanisms

- **NBTI** Negative Bias Temperature Instability
- **PBTI** Positive Bias Temperature Instability
- **RTN** Random Telegraphic noise
- **HCI** Hot Carrier Injection
- **TDDB** Time Dependent Dielectric Breakdown
- **EM** Electromigration
- **SER** Soft Error Rate

# Failure Mechanisms main Characteristics

- **NBTI** Vt increase, mobility decrease, PMOS -> speed degradation
- **PBTI** Vt increase, mobility decrease, NMOS -> speed degradation
- **RTN** Increases Vmin in SRAMs -> power impact
- **HCI** Hot Carrier Injection -> mobility decrease, NMOS-> speed degradation
- **TDDB** Gate oxide leakage-> affects functionality and can cause stuck at failures
- **EM** Can cause metal opens -> functionality failures
- **SER** Can cause wrong data storage

# Reliability Mechanism Dependencies

| | parameter | Temperature | Voltage | Recovery |
|---|---|---|---|---|
| **NBTI** | \|VTH\| | exp(-Ea/kT) | exp((VGS-VTH)/Tox) | partial |
| **PBTI** | \|VTH\| | exp(-Ea/kT) | exp((VGS-VTH)/Tox) | partial |
| **RTN** | \|VTH\| | exp(-Ea/kT) | exp((VGS-VTH)/Tox) | partial |
| **HCI** | Idlin | weak | exp(VDS) for Id>0 | no |
| **TDDB** | MTTF (T63.2%) | exp(-Ea/kT) | exp(\|VGS\|) | no |
| **EM** | MTTF (T50%) | exp(-Ea/kT) | ~V | partial |
| **SER** | SER | ~T | ~1/V | yes |

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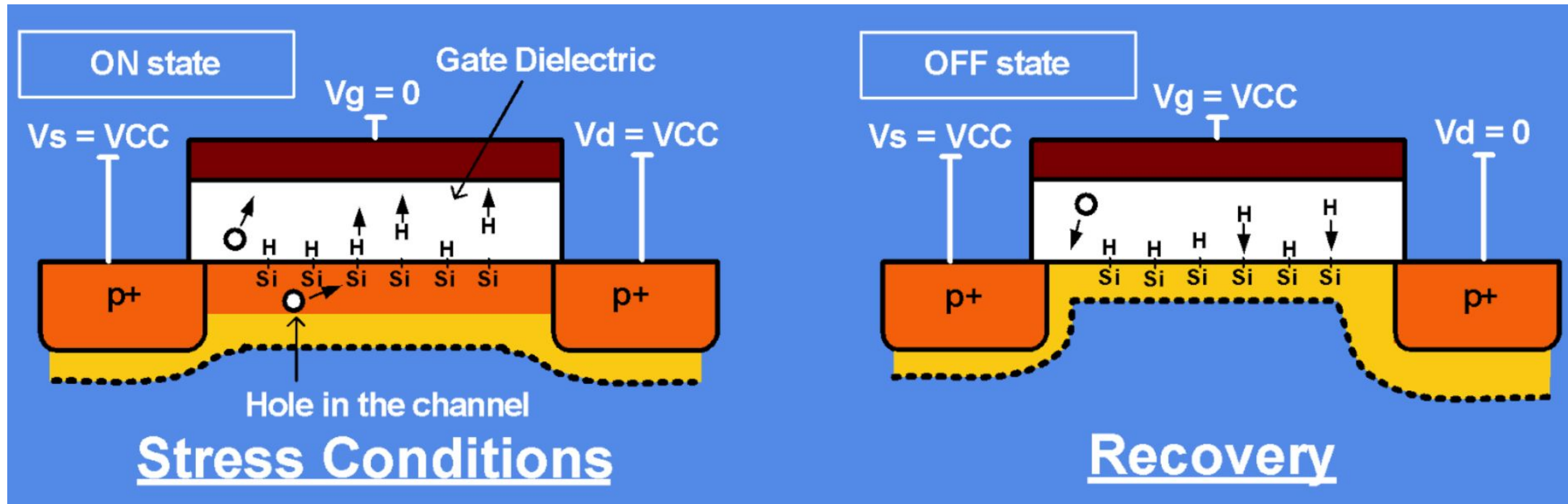
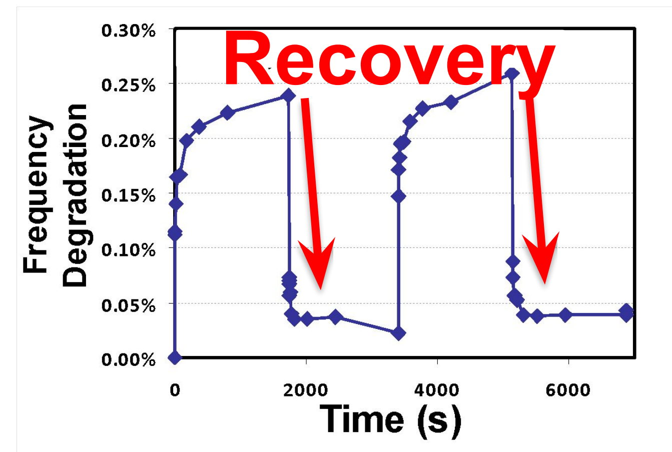
# Introduction to NBTI

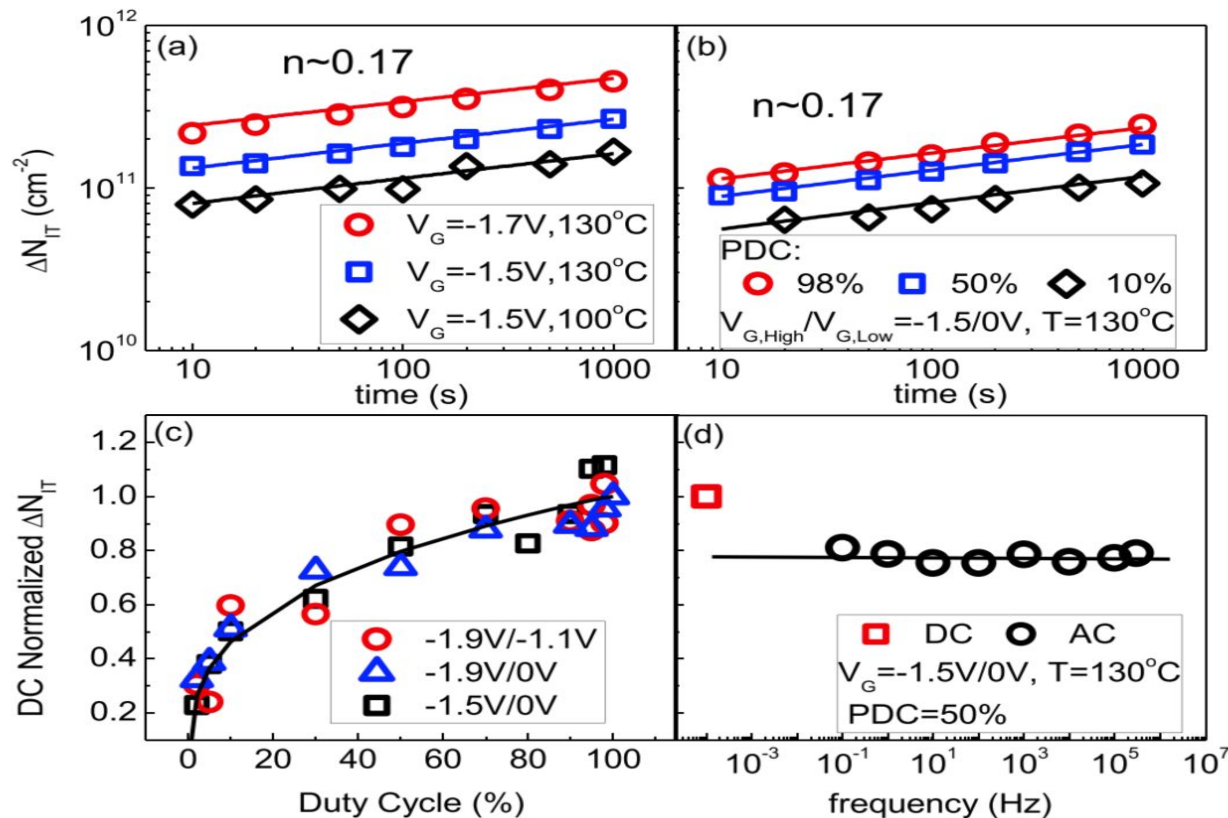



Keane, et al., VLSI Symp. 2009




- Channel holes interact with Si-H bonds at interface to create traps
- Increase in |Vth|
  - ~20-30% increase in 10 years
- Partial recovery occurs when PMOS is turned off

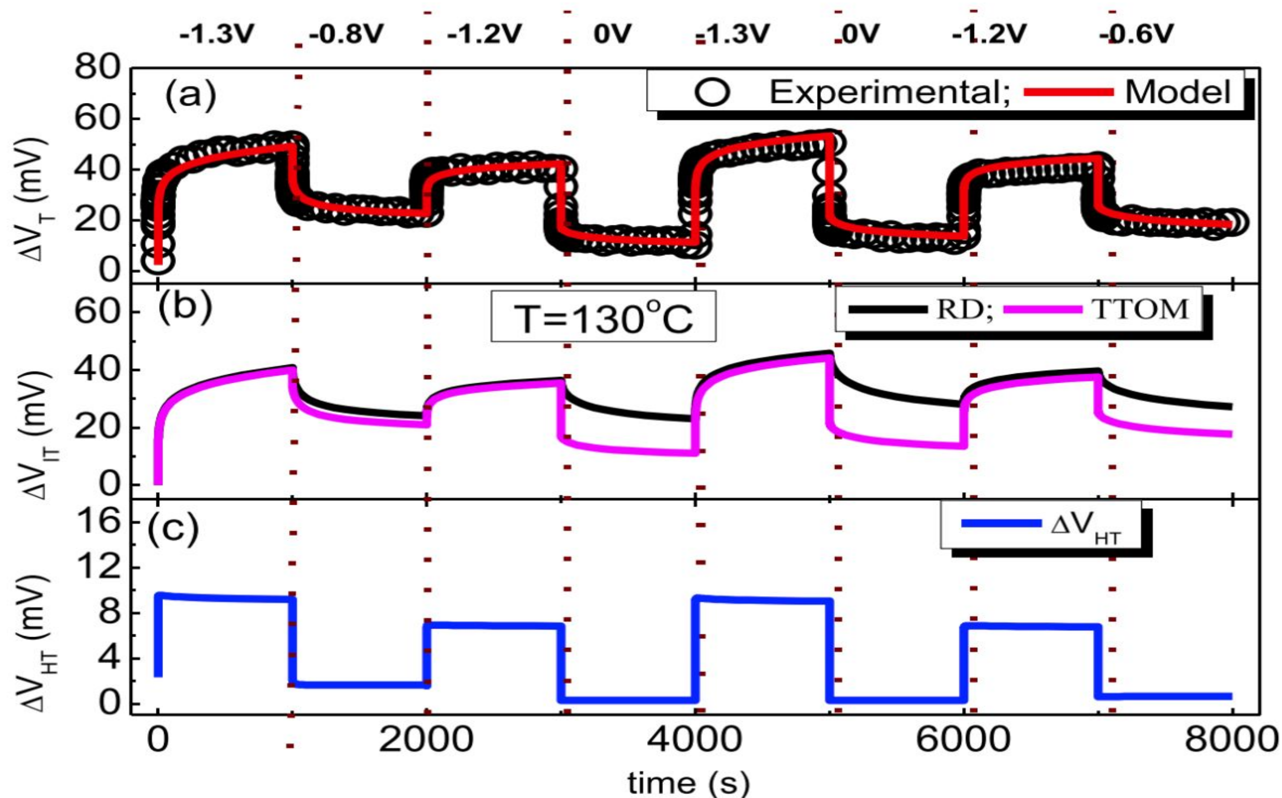
# NBTI, PBTI - Stress & Recovery




RD model prediction of DCIV data for (a) dc stress, (b) ac stress with different PDCs, (c) PDC dependence, and (d) frequency independence.

Parihar et al, Trans Electron Devices, March 2016

# NBTI, PBTI - Stress & Recovery

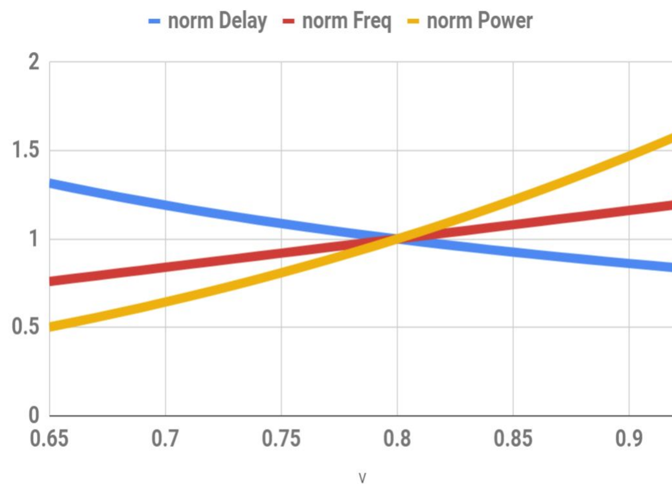



(a) Experimental (symbols) and model prediction (lines) of $\Delta V_T$ time evolution with constant stress time and varying $V_{\text{G-STR}}$. (b) $V_{\text{IT}}$ from the RD and TTOM enabled RD. (c) $V_{\text{HT}}$ time evolution.

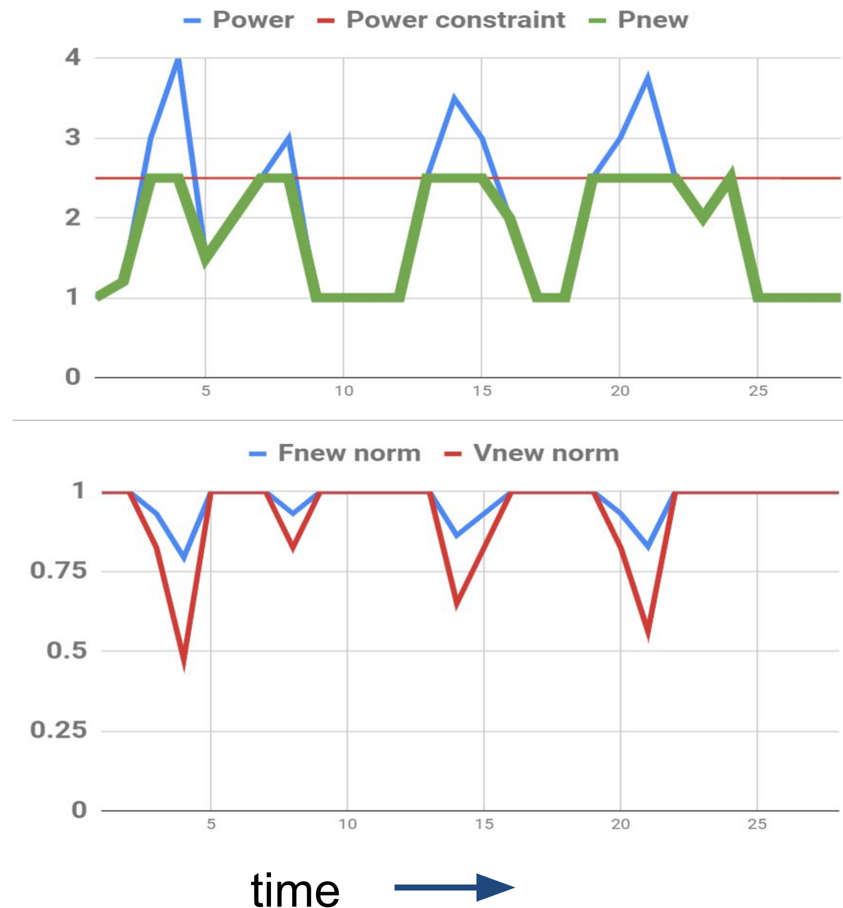
Parihar et al, Trans Electron Devices, March 2016

# NBTI, PBTI and DVFS

- Continuous Voltage, Frequency change

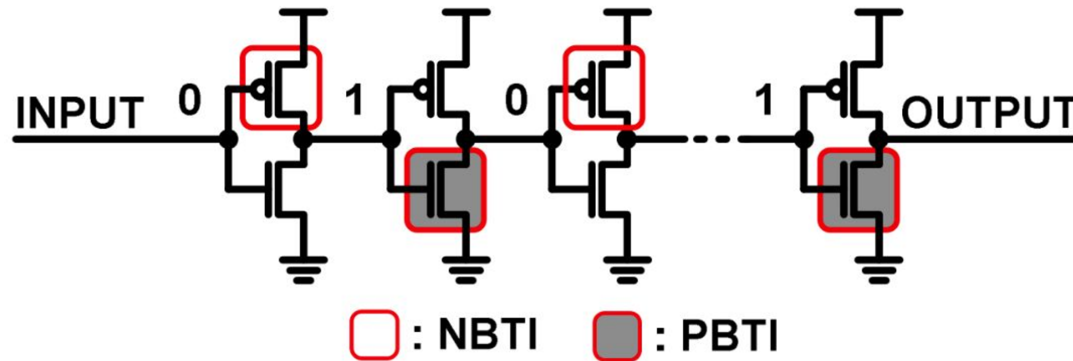


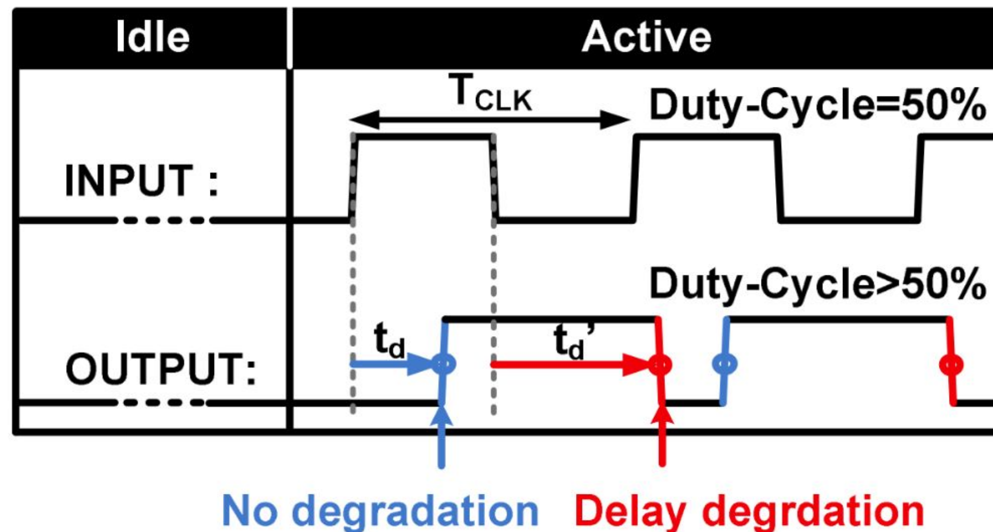

PBTI stress conditions vary substantially over time




time →

# NBTI, PBTI - Asymmetric Stress




Wang et al, IRPS 2013

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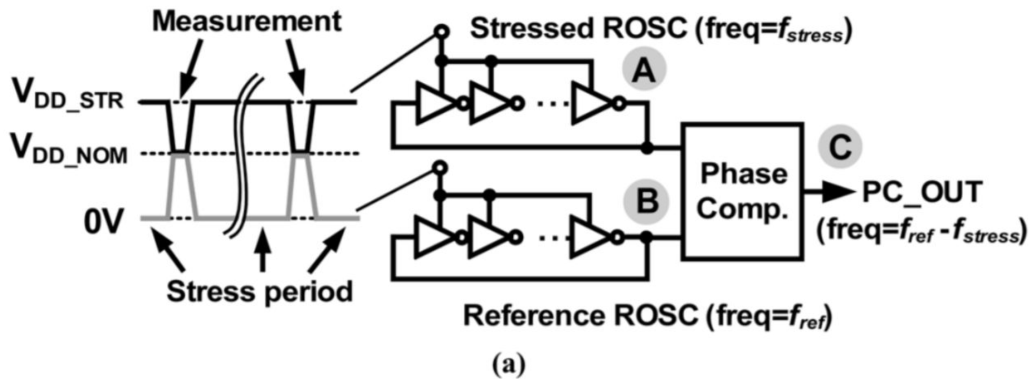
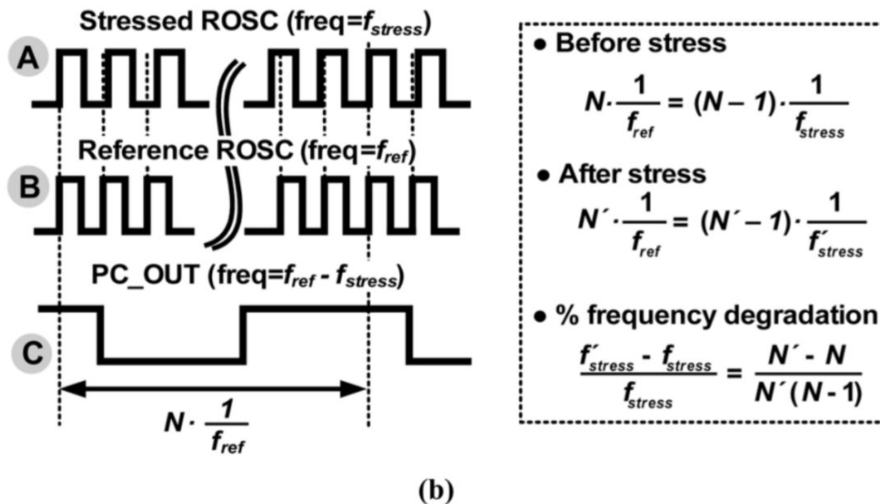
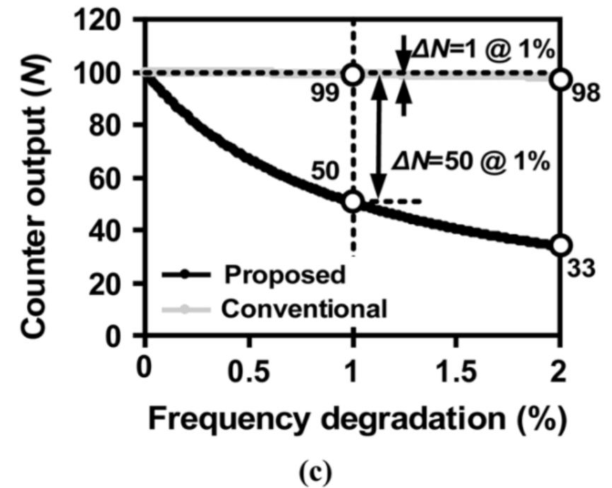
# High Sensitivity NBTI Monitor



(a)



(b)

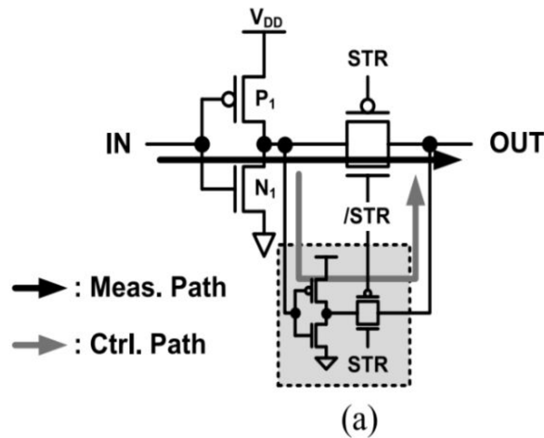


(c)

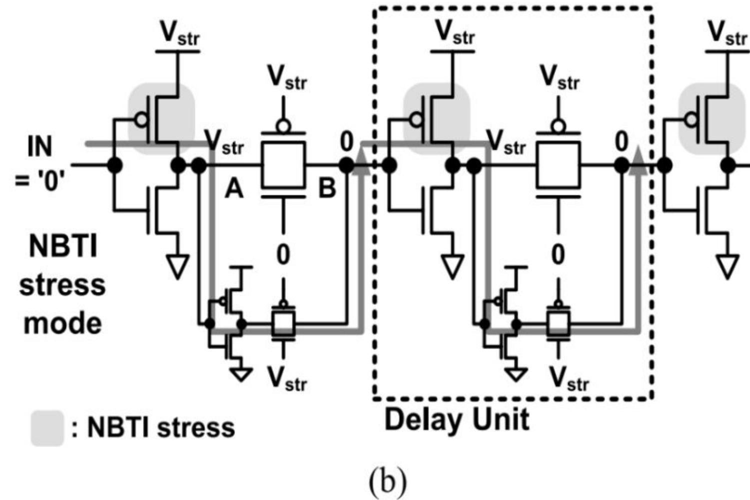
The proposed technique provides 50x higher sensing resolution for detecting 1% frequency degradation compared to conventional simple ring oscillator technique

Kim et al , JSSC, APRIL 2008

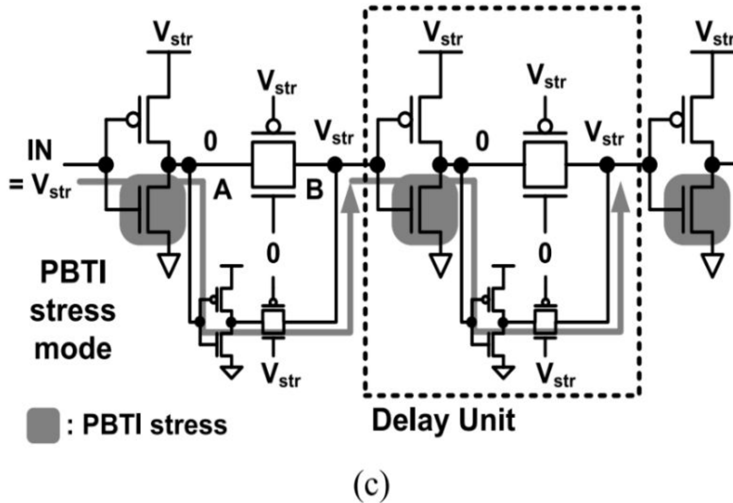
# Separate NBTI, PBTI monitor



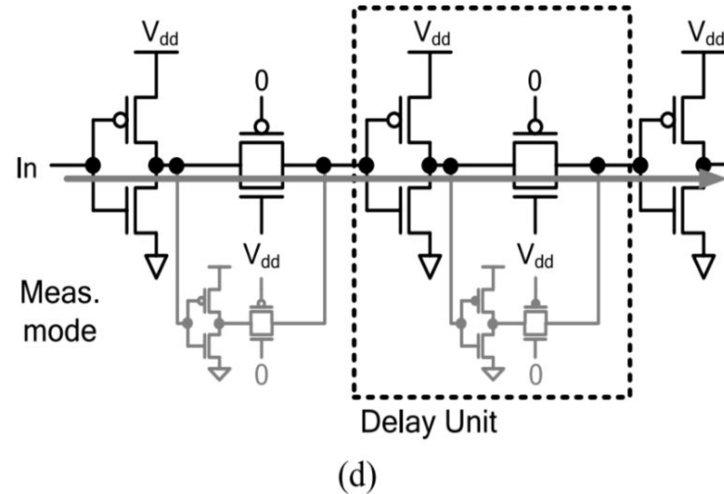
(a)



(b)



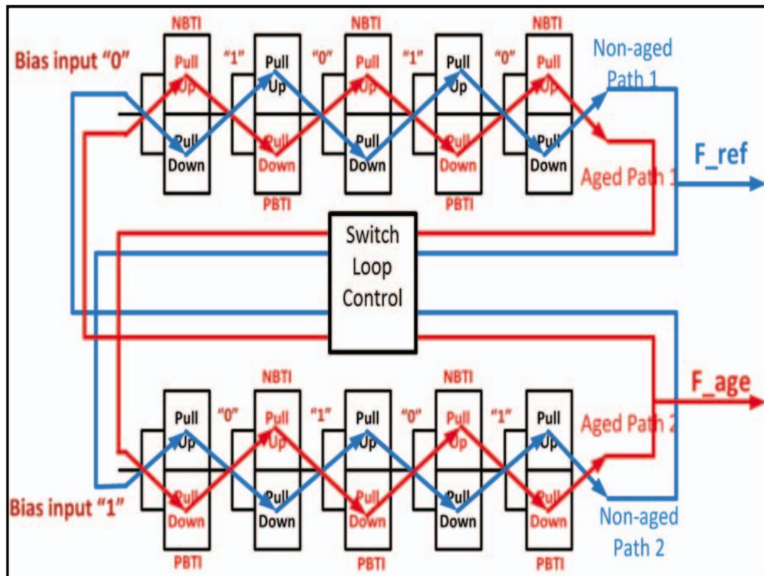
(c)



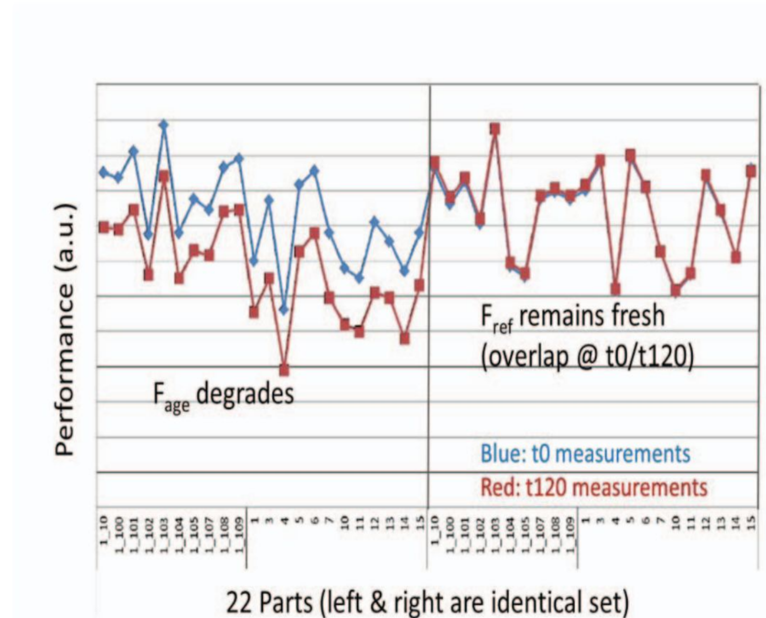
(d)

Kim et al, Trans VLSI, 2015

# In Situ NBTI, PBTI Monitor



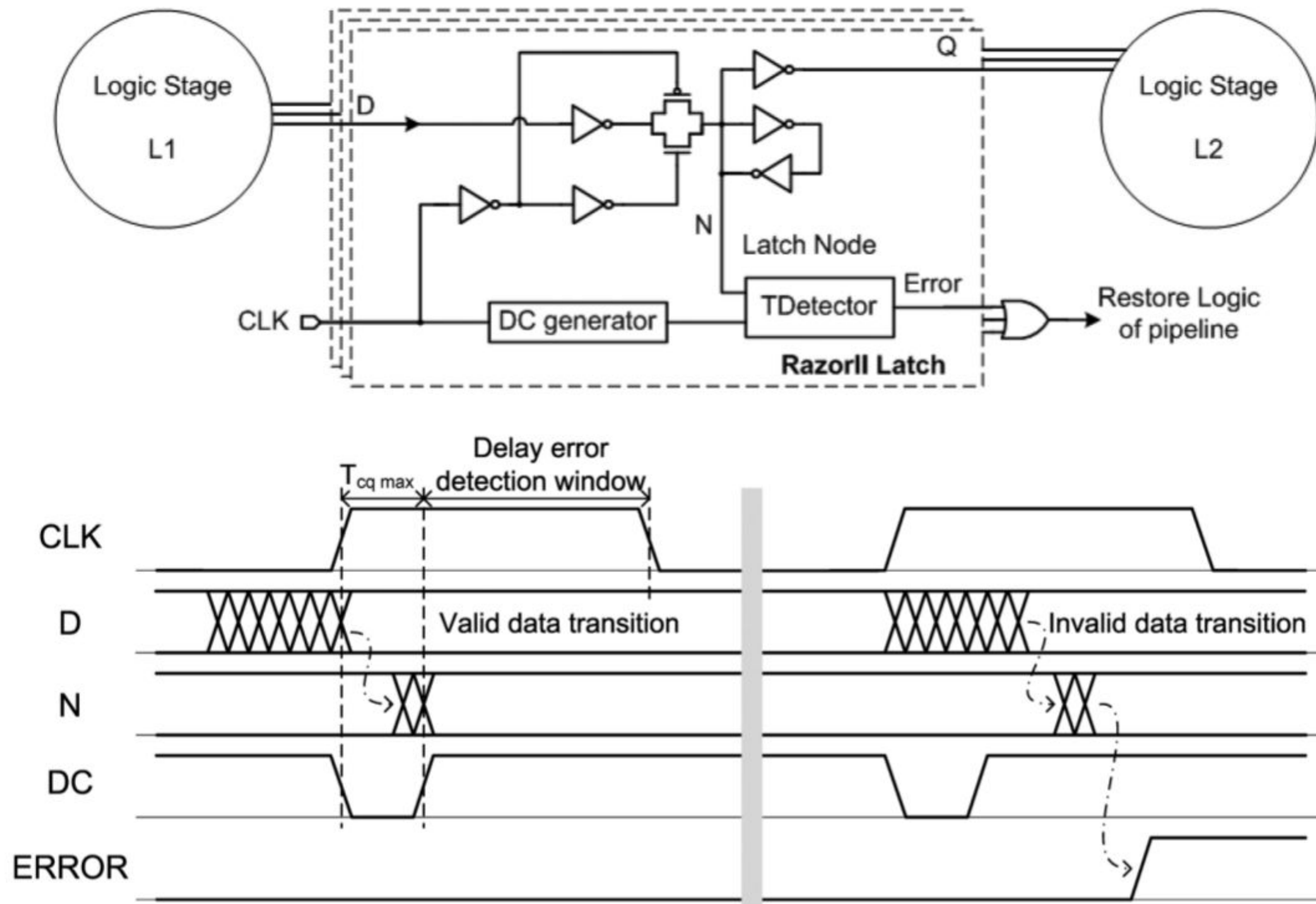

An on-chip aging sensor design utilizes two identical aging paths and a loop control logic. Aged (under DC conditions) and non-stressed devices can be looped into two ROs, respectively. The frequency delta between aging output $F_{age}$ and reference output $F_{ref}$ monitors in-situ on-chip aging.




HTOL results validate the sensor function designed in 20nm node. $F_{age}$ degrades with enhanced aging sensitivity and $F_{ref}$ shows no change after 120 hours. The delta is used to calculate voltage compensation in AVS close loop.

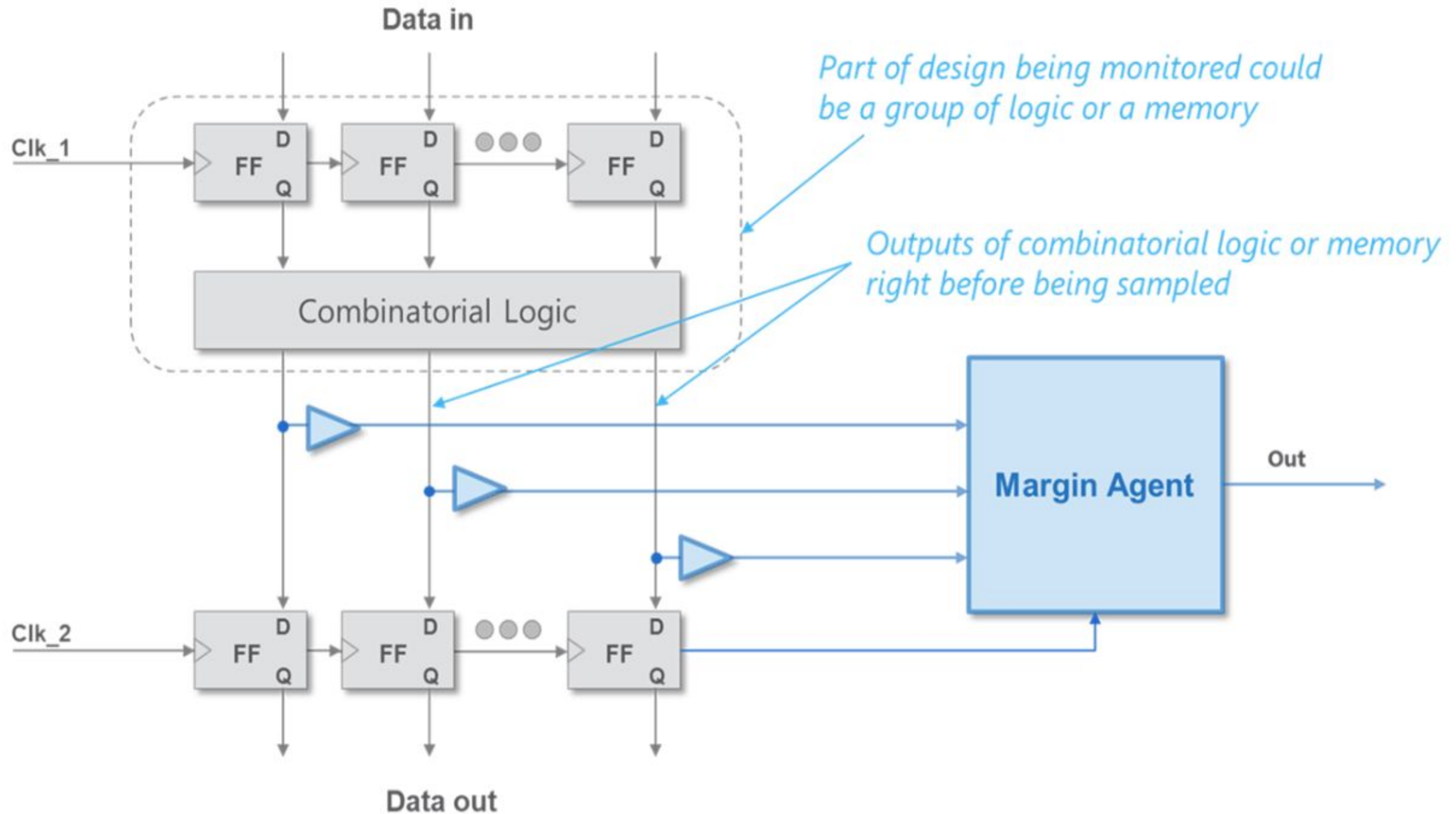
Kufluoglou et al, IRPS2017

# Razor II -Timing Margin Check



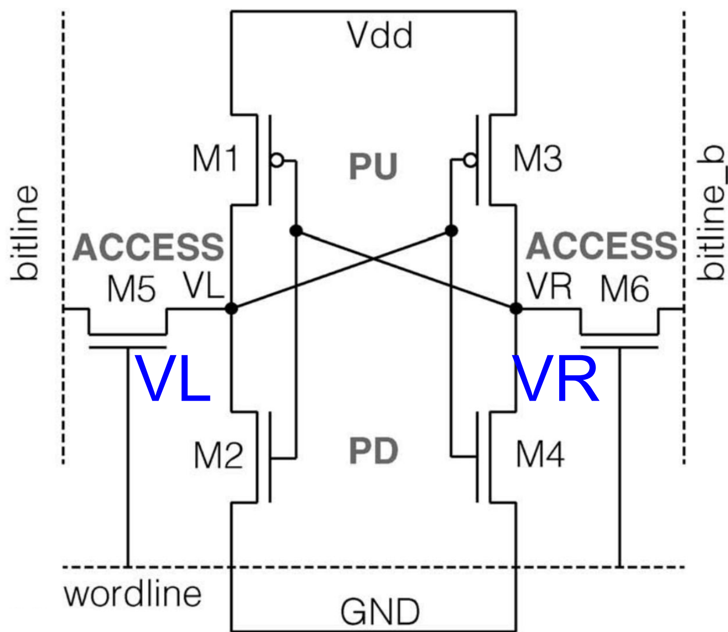

Das, et al, JSSC 2009

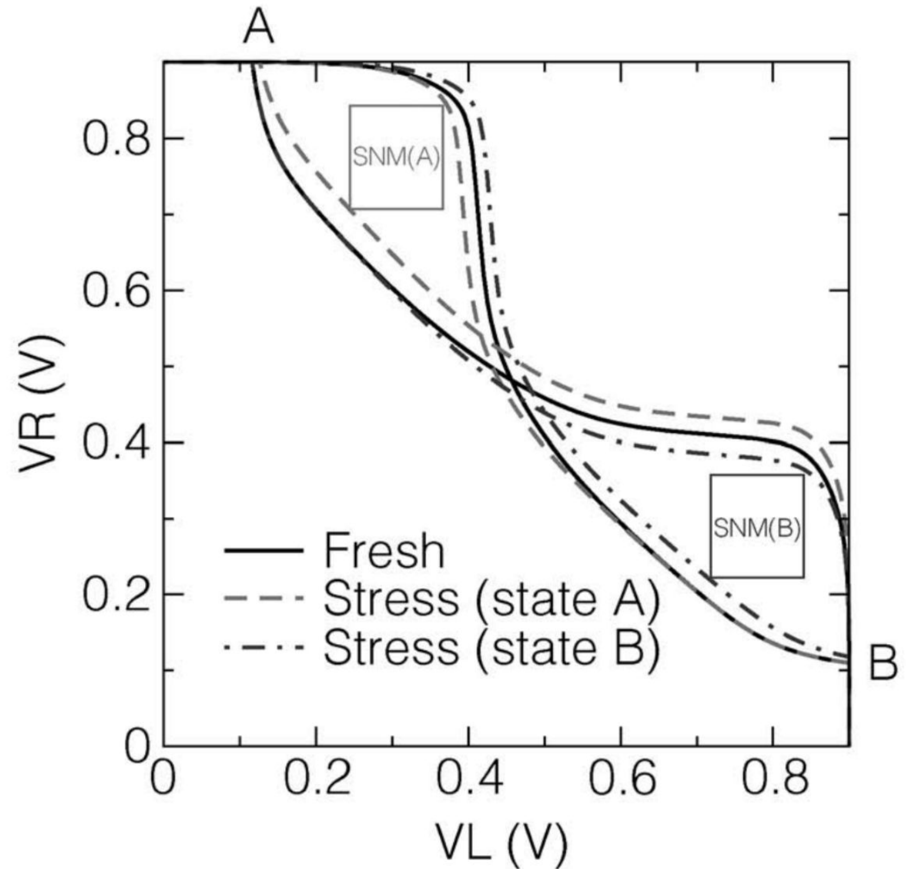
# Aging Monitors as IP




Landman et al, IRPS 2019

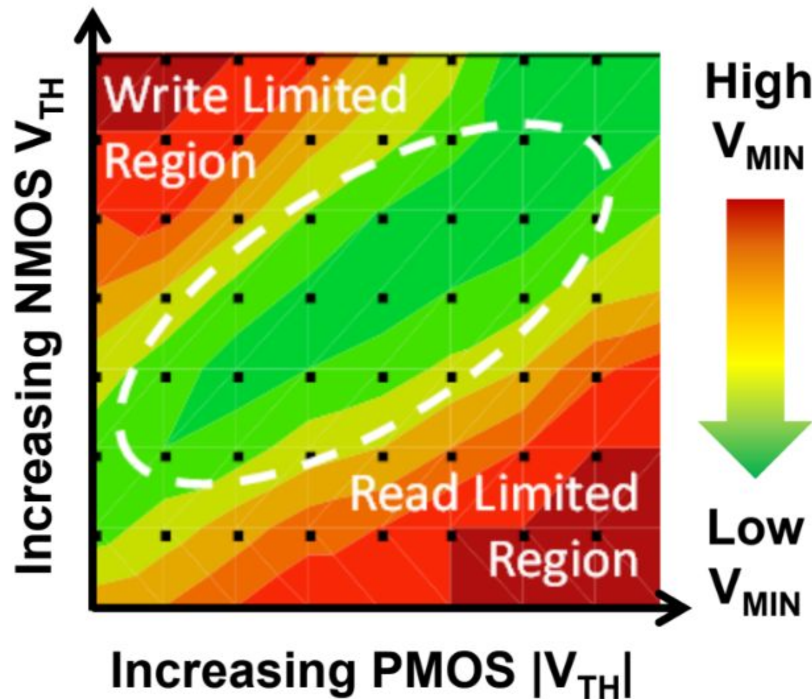
# NBTI, PBTI Impact on SNM

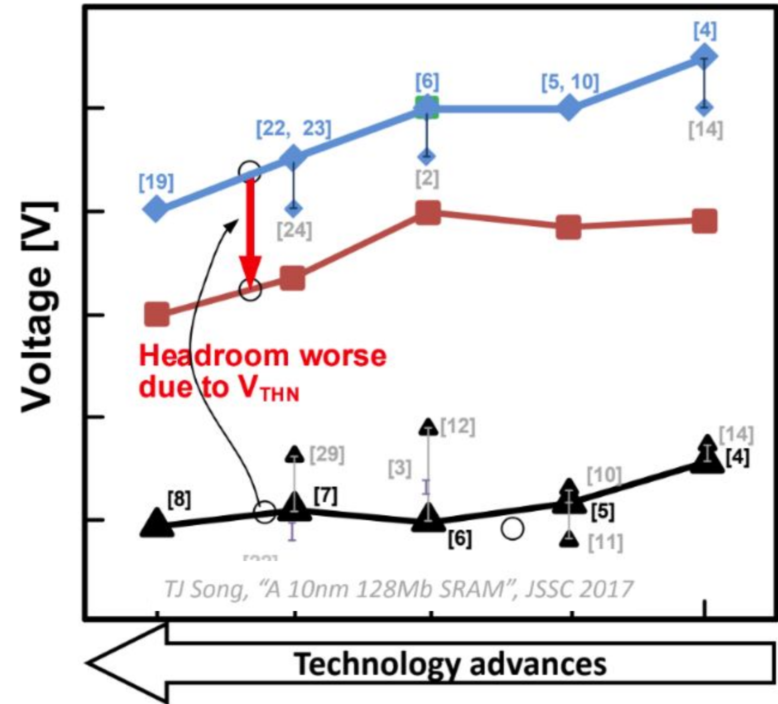



Wand et al, IEEE Design & Test 2013

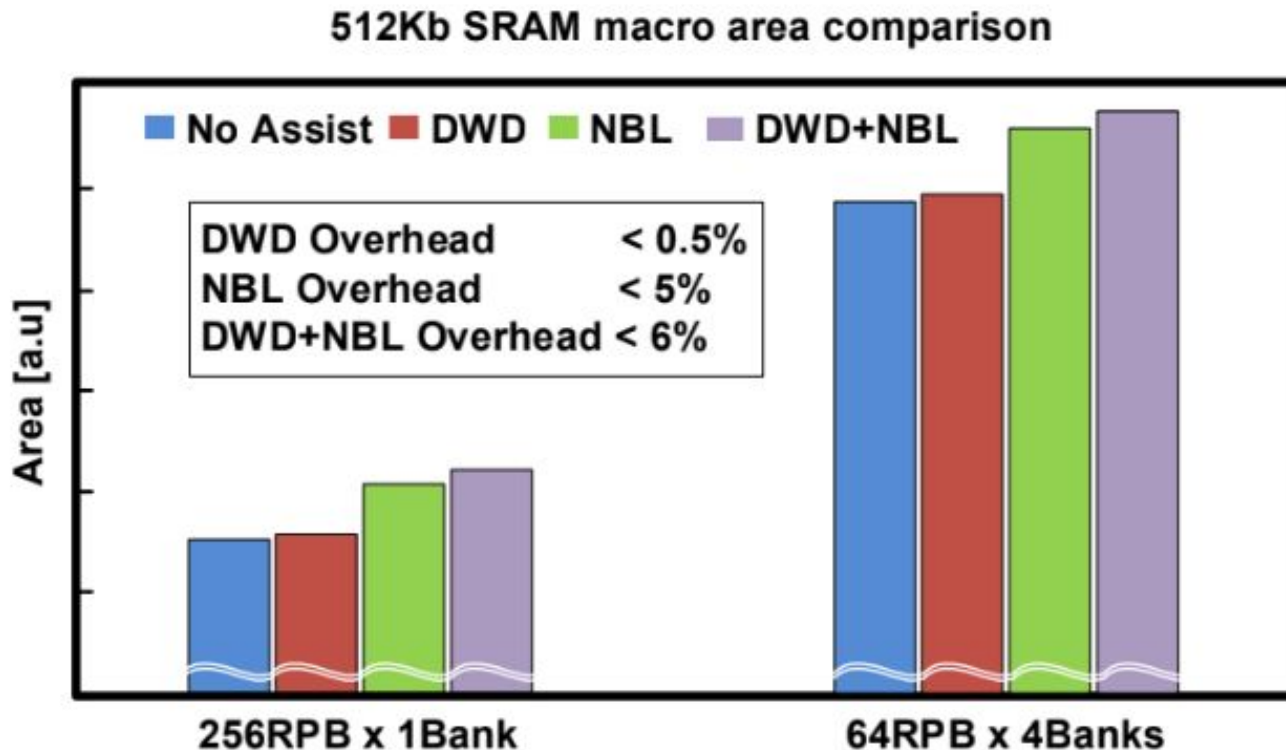
# SRAM Write and Read Margins



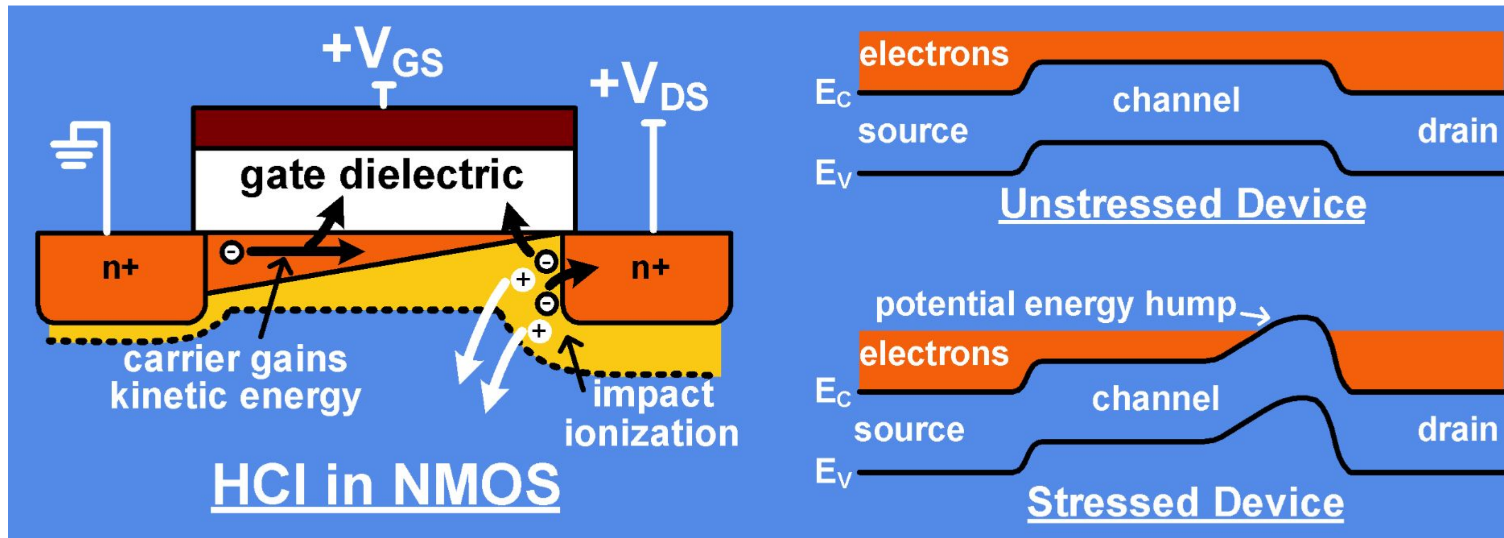

Guo et al, ISSCC 2018

# Assist Circuitry Overhead




Song at al, ISSCC 2016

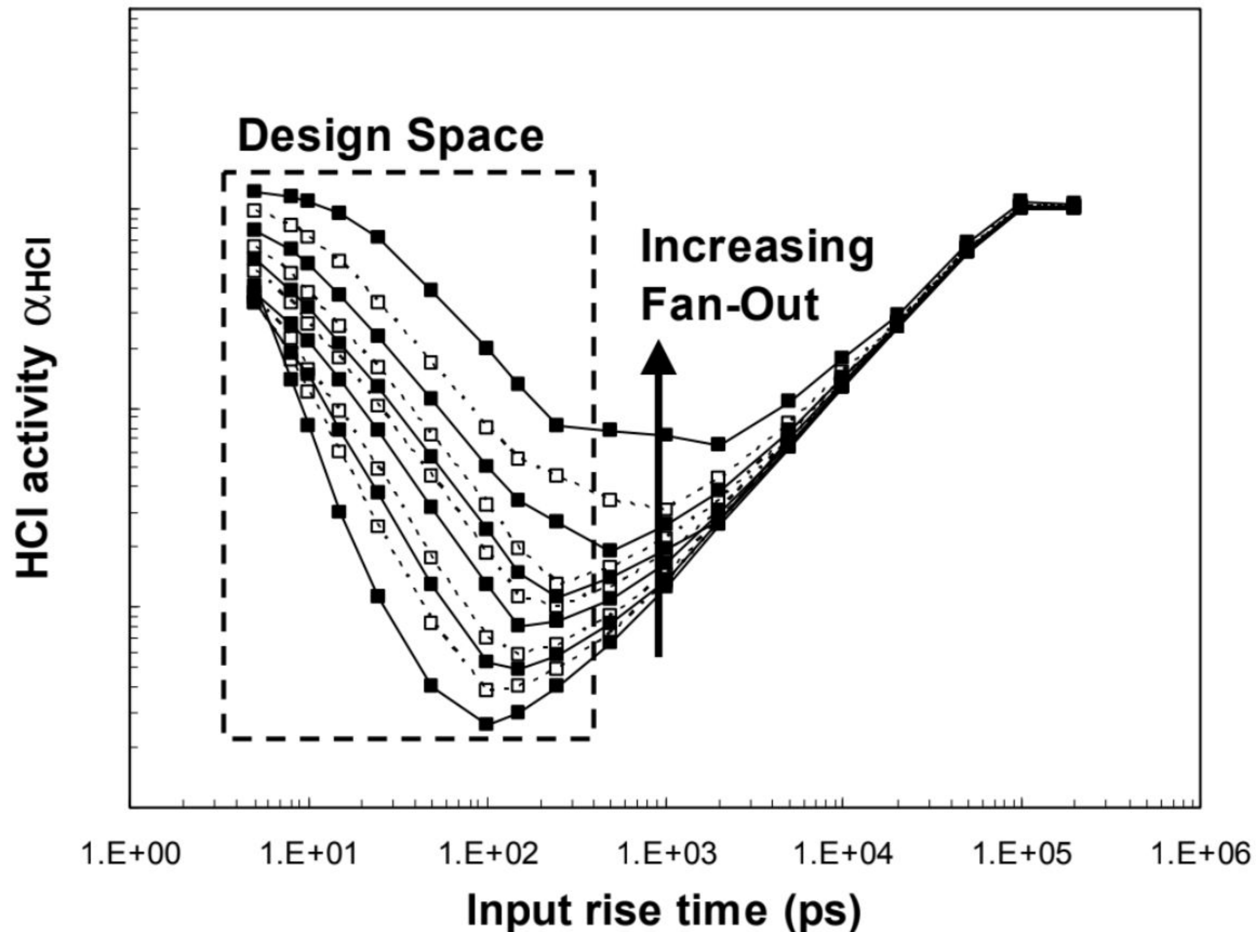
# HCI basics




Keane, et al., VLSI Symp. 2009

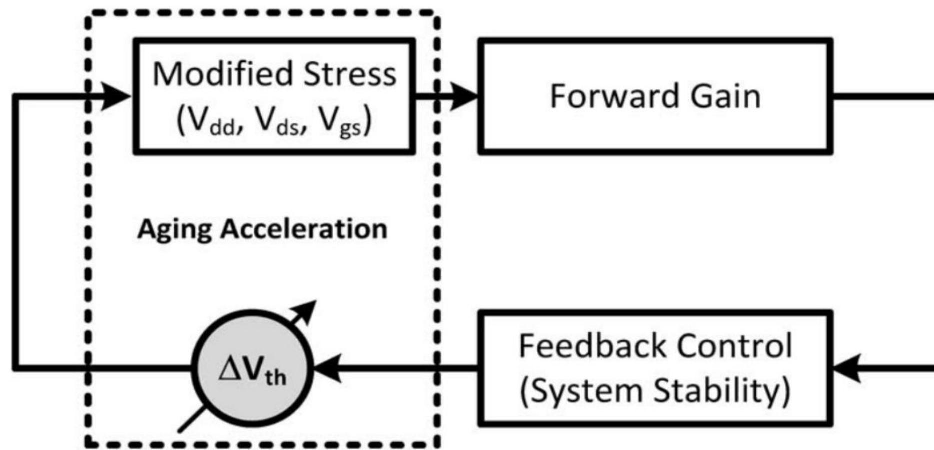
- Causes degradation of gate dielectric Interfacial and oxide traps
- Negatively trapped charges create potential hump
- Degradation not reversible

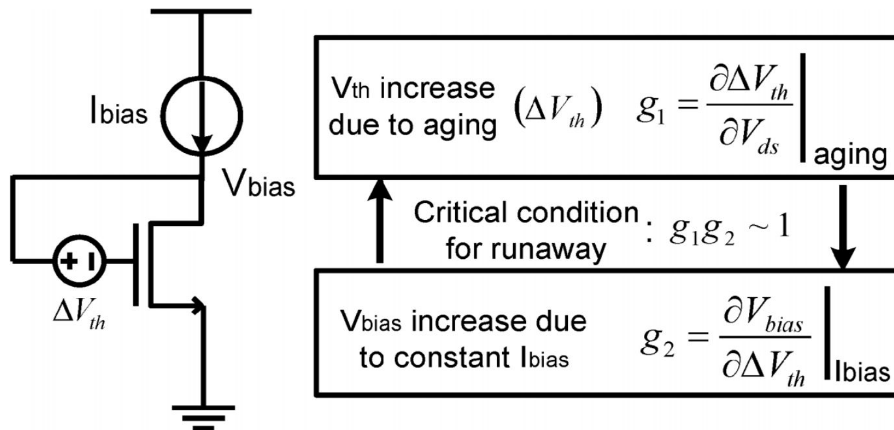
# HCI Dependency on Input Slew Rate and Fan-out (Load)




Huard et al, IEEE 2012

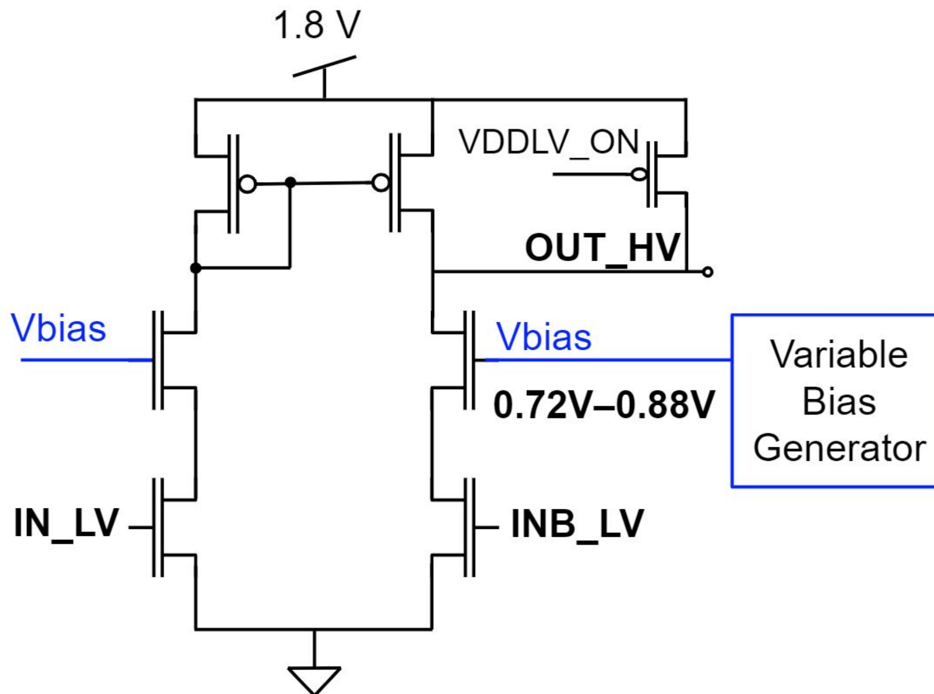
# Run-Away in Feedback loops




Sutaria et al, IEEE Trans on Material and Devices, Sep 2015

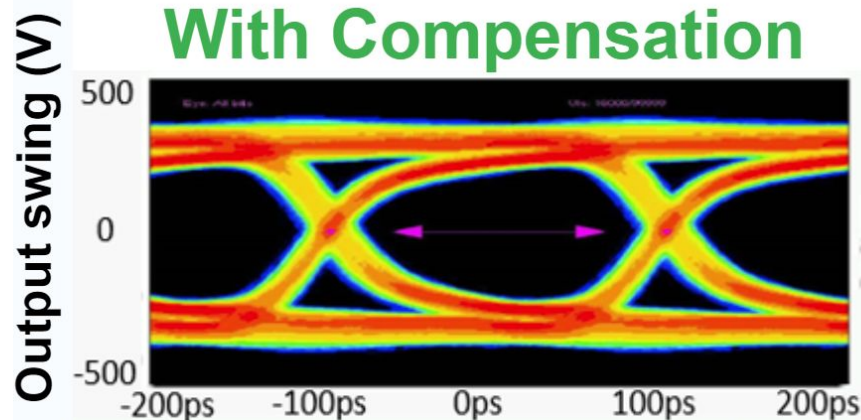
# Impact on 5Gbs LVDS

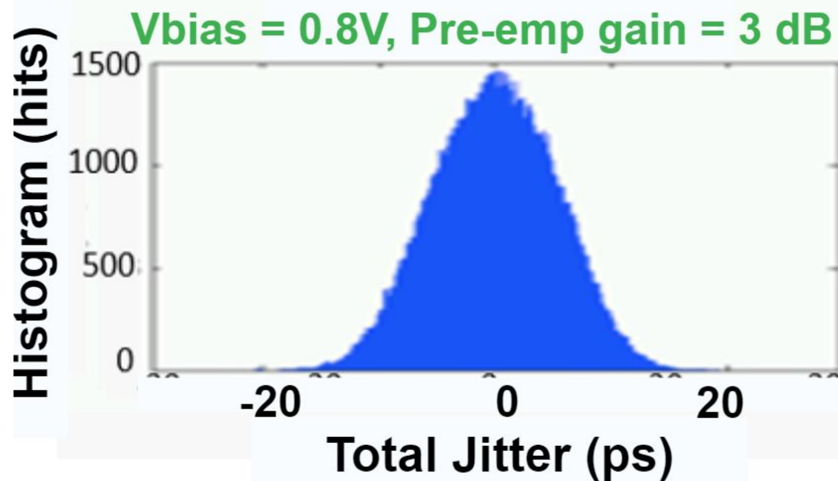


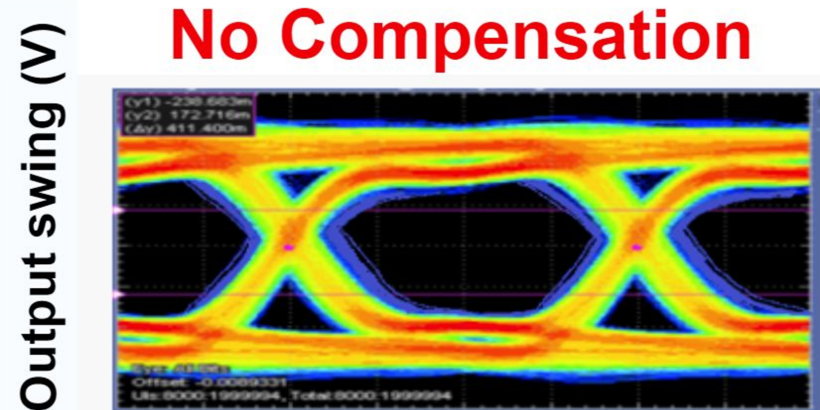

- Constant Vbias replaced by variable DC bias
- Vbias can be selected to compensate for $V_{TH}$ @ PVTs or aging degradation
- Duty cycle can be measured on-chip to and automatically adjust Vbias
- Without the compensation, the circuit failed after HTOL. The compensation scheme managed to restore functionality

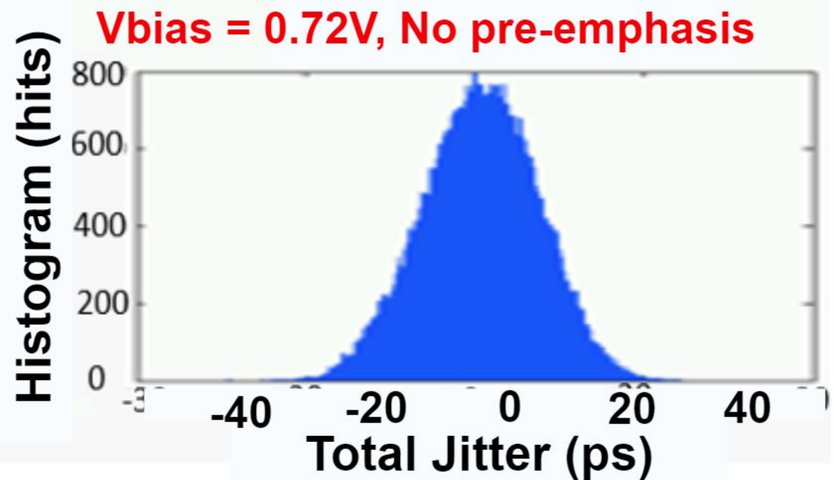
Jagannathan et al, IRPS 2018

# Aged with/without Compensation



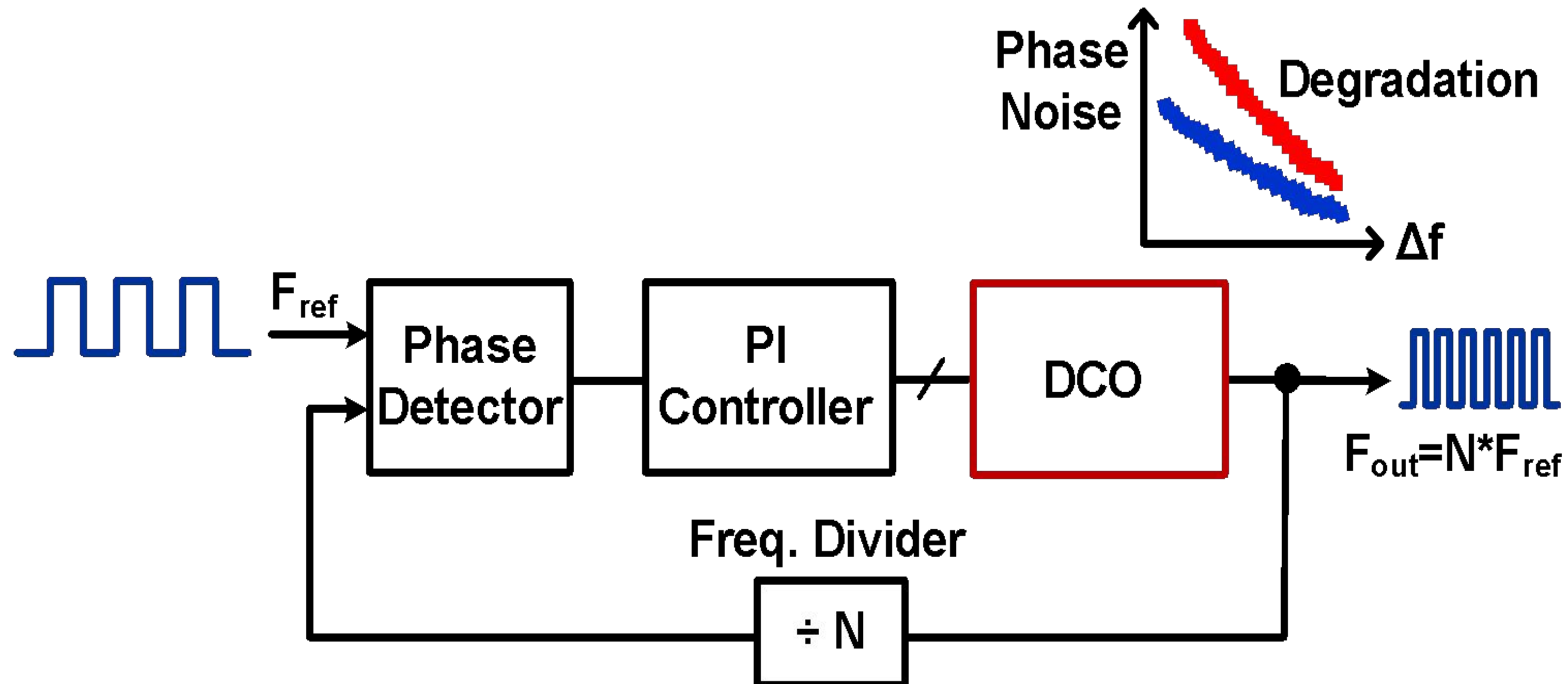




- Vbias and pre-emphasis gain increased from 0.75V and 1dB to 0.8V and 3dB to compensate for aging induced degradation
- Able to achieve output swing, jitter & duty cycle well within specs

Jagannathan et al, IRPS 2018,

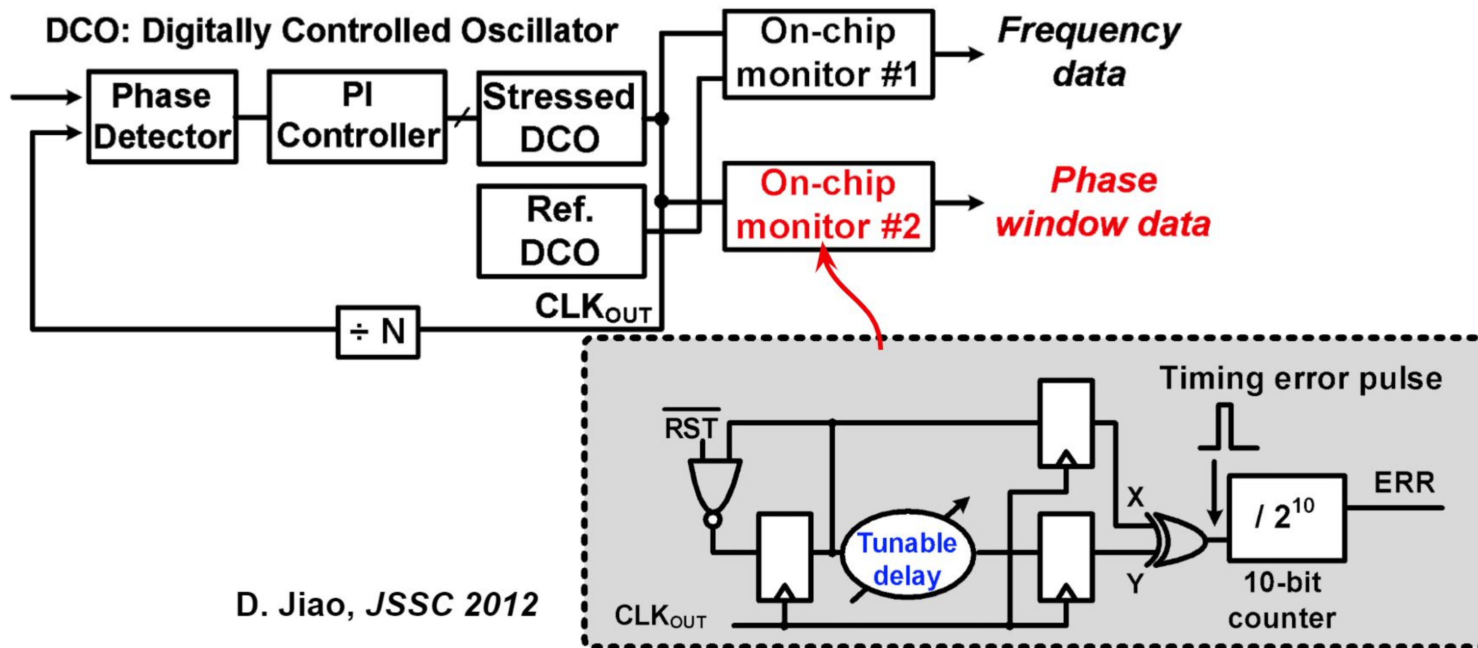
# ADPLL Reliability - Impact on Jitter




Park et al, IRPS 2018

- **Aging affects jitter and reduces design margin**
- **Jitter measurements requires high speed probes or packages, off-chip drivers and connectors**
- **On chip degradation monitor provides higher jitter measurement accuracy**

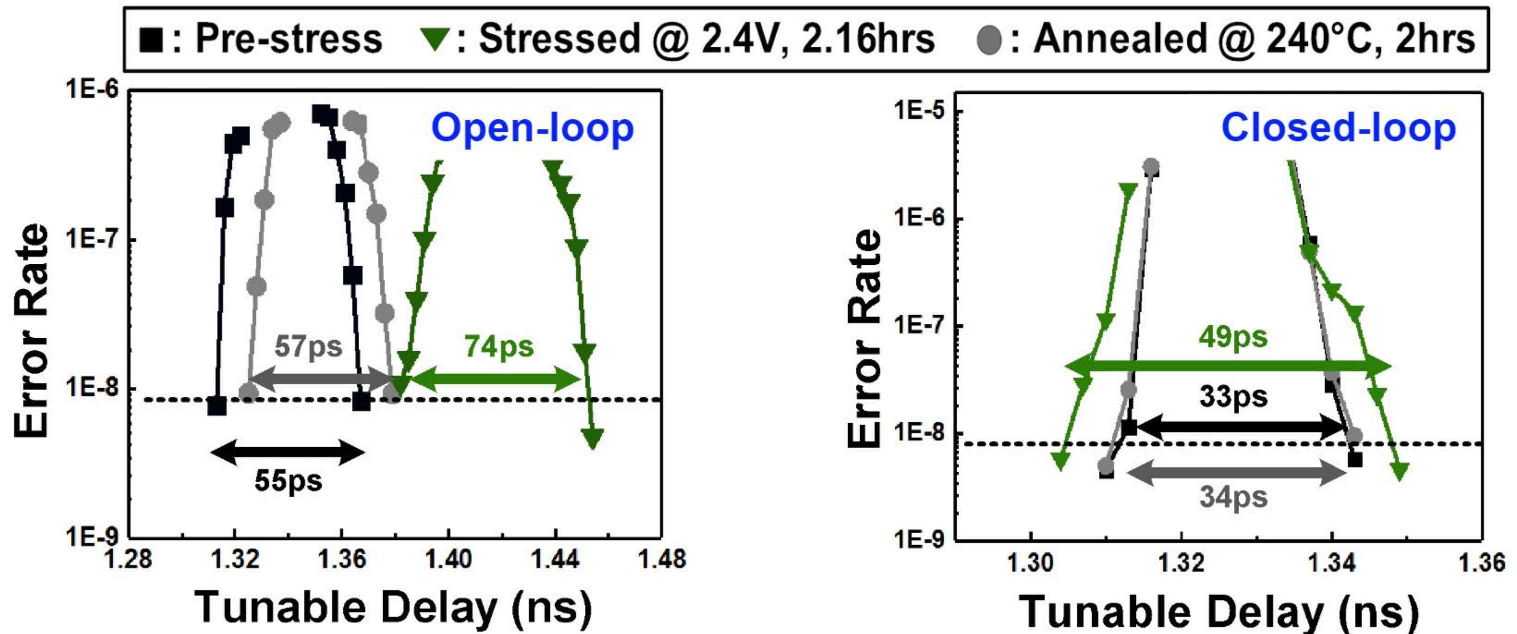
# Phase Window Monitor




- **Clock period (including jitter) compared with tunable delay**
- **Indirectly measure phase noise by sweeping tunable delay**

Park et al, IRPS 2018

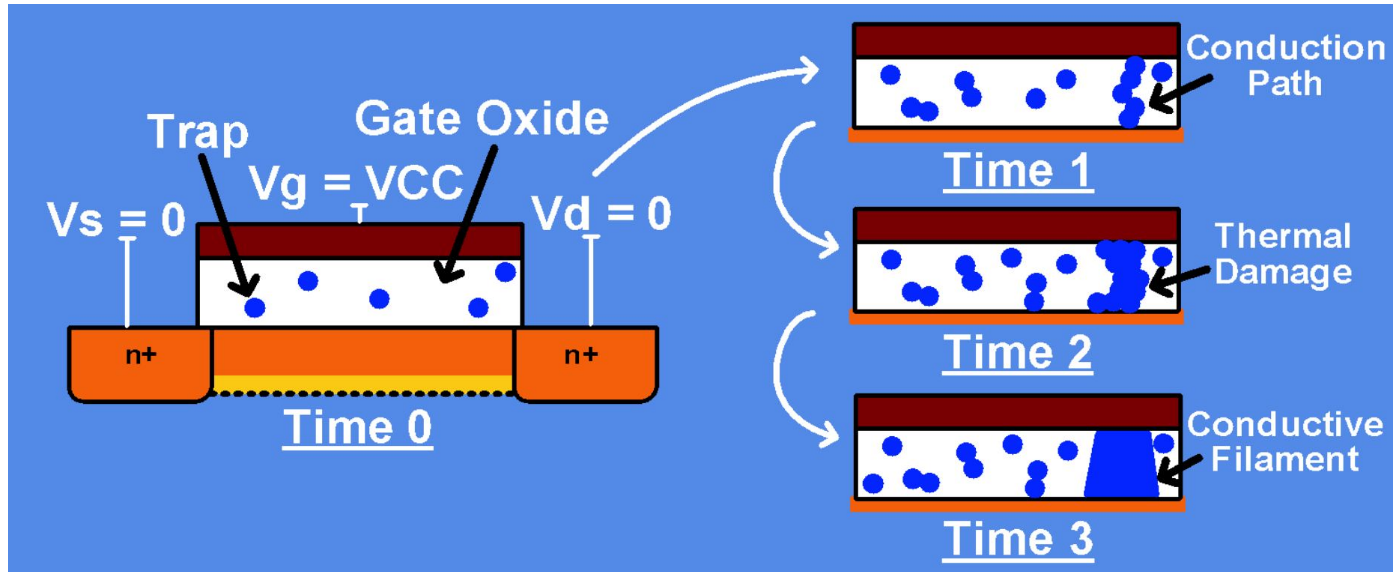
# Phase Window recovery




- **Phase window almost fully recovered after annealing @ 240°C**

Park et al, IRPS 2018

# TDDB basics




Keane, et al., VLSI Symp. 2009

- Traps generated under influence of electric field
- Traps overlap
  - Conductive path between gate and substrate
- Gate dielectric no longer a reliable insulator
  - Parametric or functional failure

# Power Delivery Network (PDN)

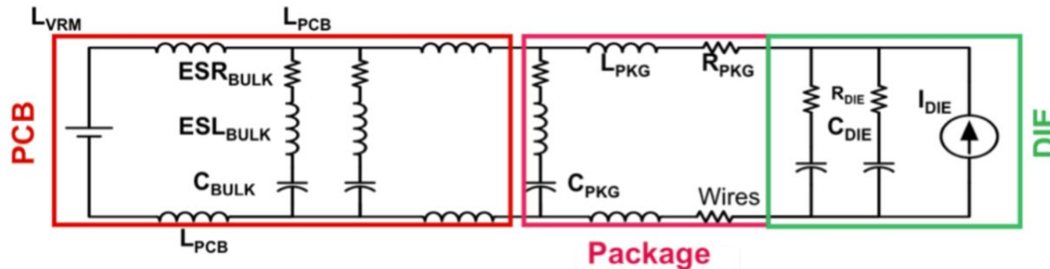



Figure 1. Simplified PDN model showing the Chip, Package and PCB components

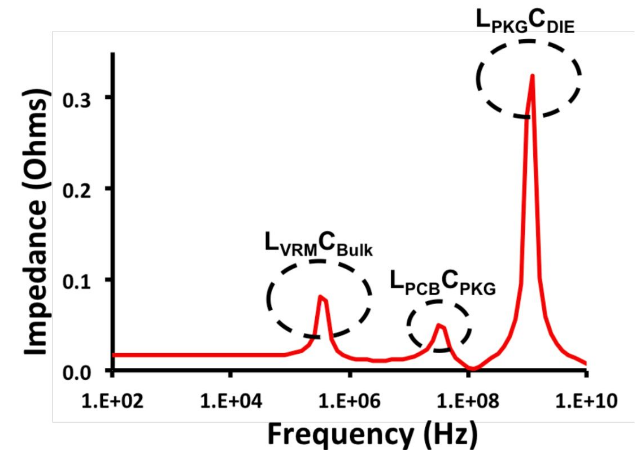



Figure 2. Frequency Response of the simplified PDN. The dominant resonance frequencies are labeled against their impedance peaks [6].

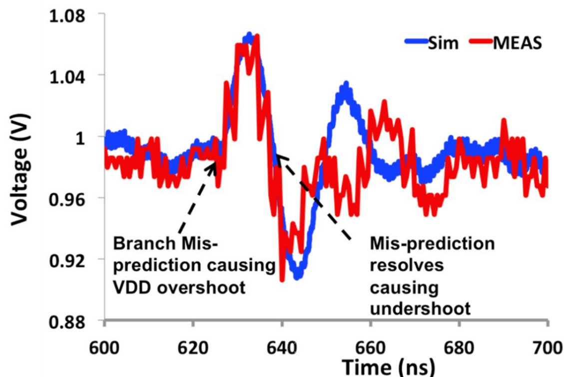
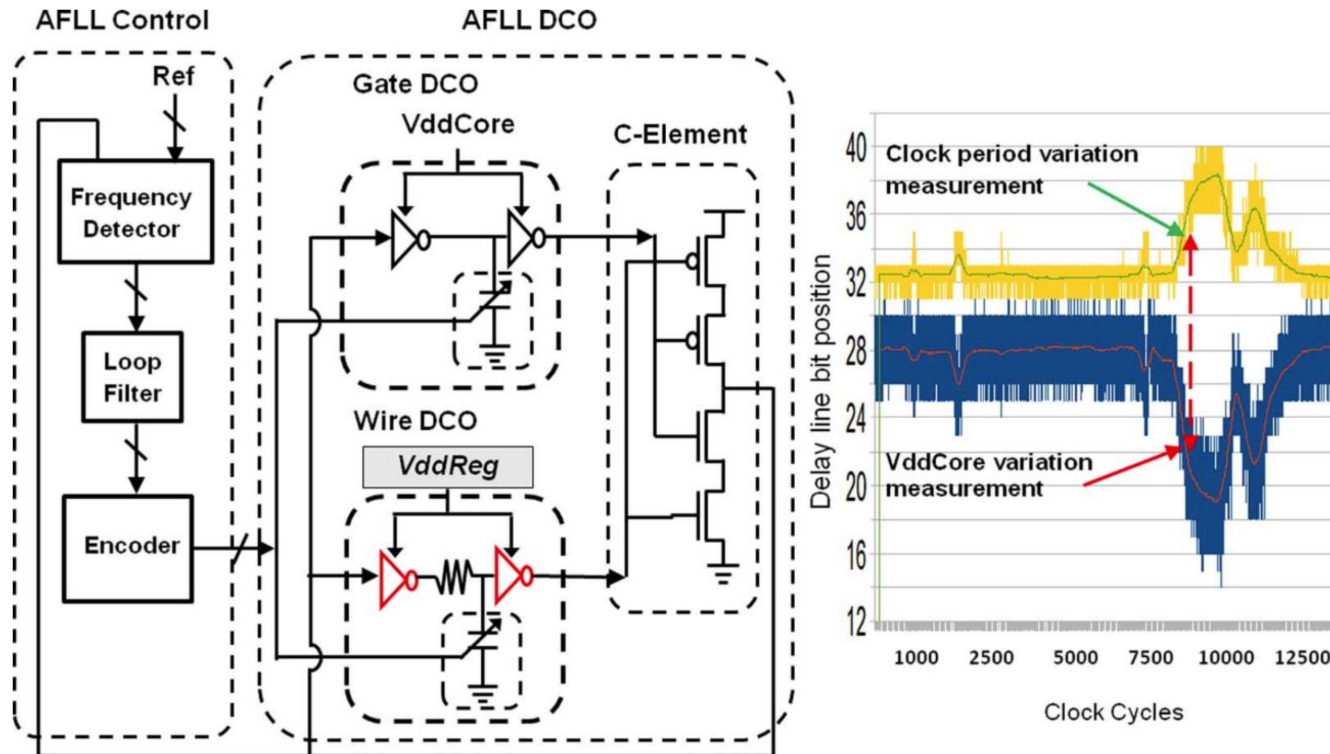



Figure 15. Time-domain simulated and measured waveforms showing PDN response to a branch-misprediction induced voltage overshoot.

- Depending on the workload variations it can create voltage undershoots or overshoots

Das et al, ISLPED 2015

# Ldi/dt droop mitigation- FLL
## (Frequency Locked Loop)

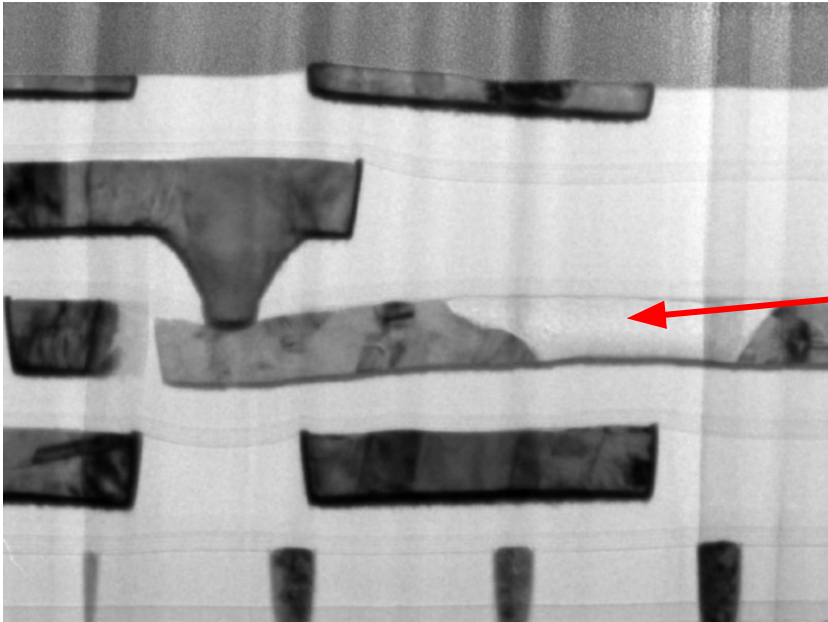


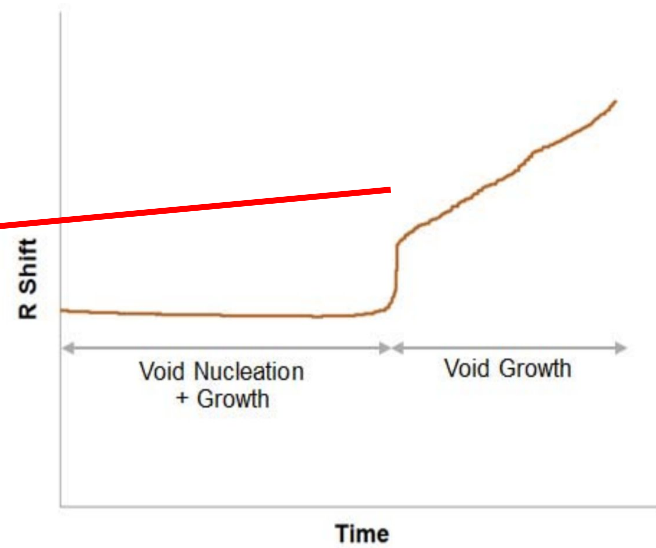

AFLL block diagram and Ldi/dt compensation.

- Reduces clock frequency temporarily when a sudden VDD droop is detected.
- Undershoot would have been 2x larger without the FLL mitigation

Konstadinidis et al, JSSC 2016

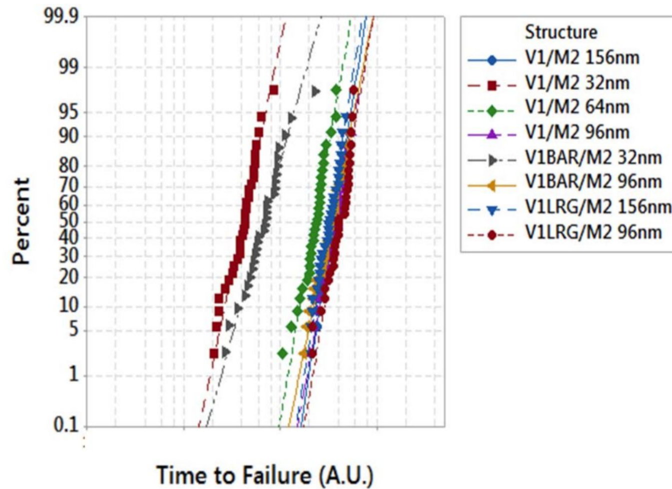
# EM Failure Mechanism

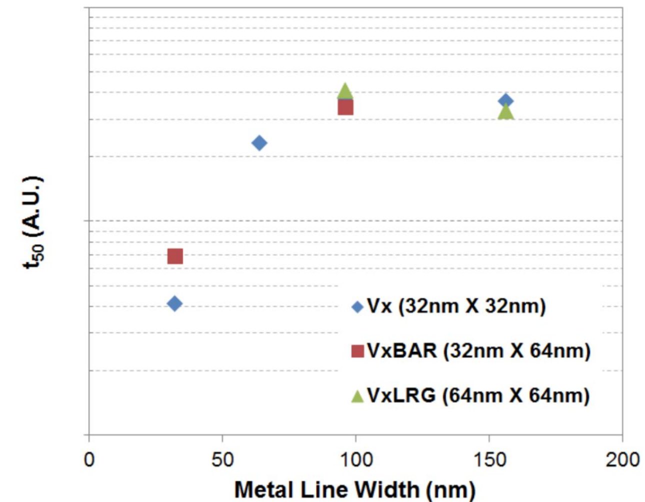





Choi,et al, IRPS 2018

# EM failure vs Metal Width, Grain Size




32nm width

64nm width

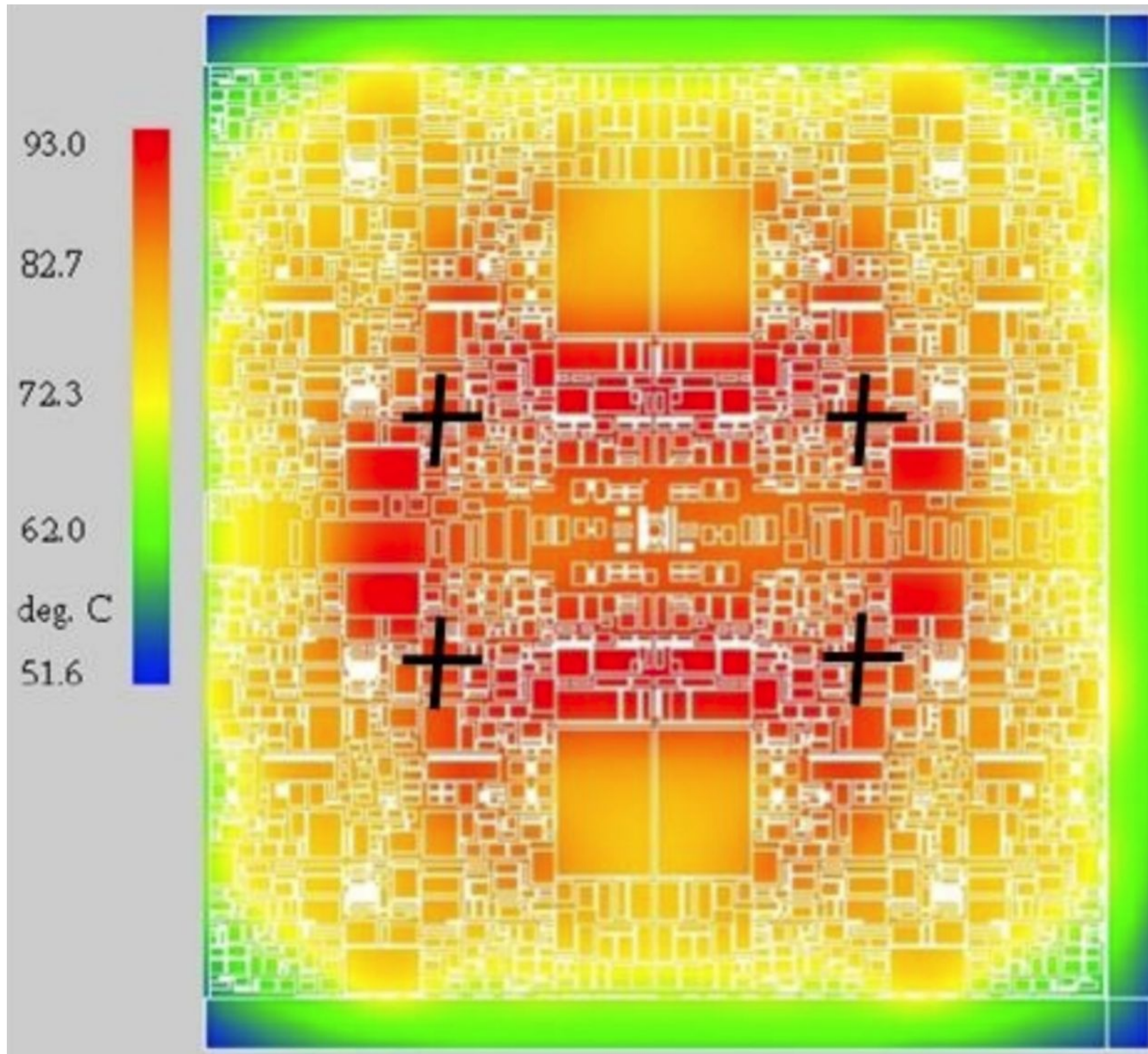
96nm width

156nm width

- EM improves for up to 3x increase in width and then saturates.
- Strong dependency on the grain size and Cu drift velocity

Choi,et al, IRPS 2018

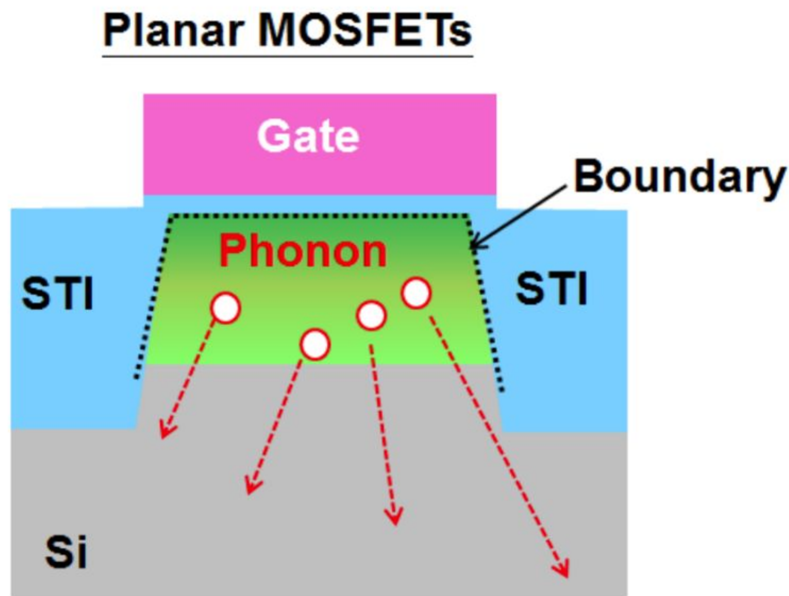
# Thermal Map

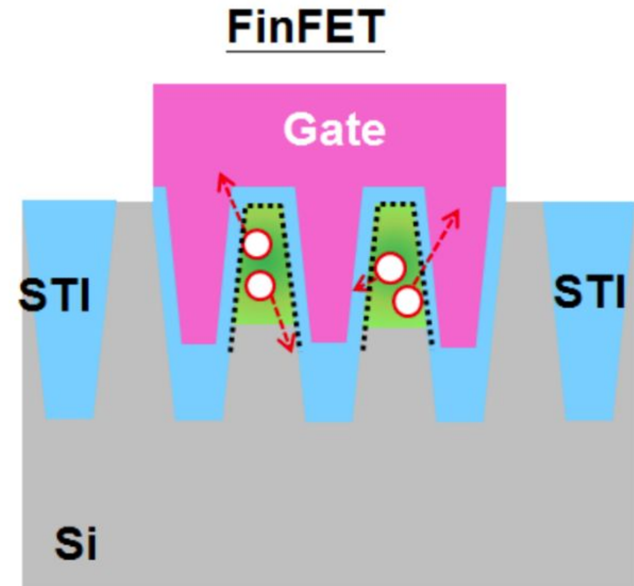



Konstadinidis et al, JSSC 2009

# Self Heating Effect (SHE) in FinFET

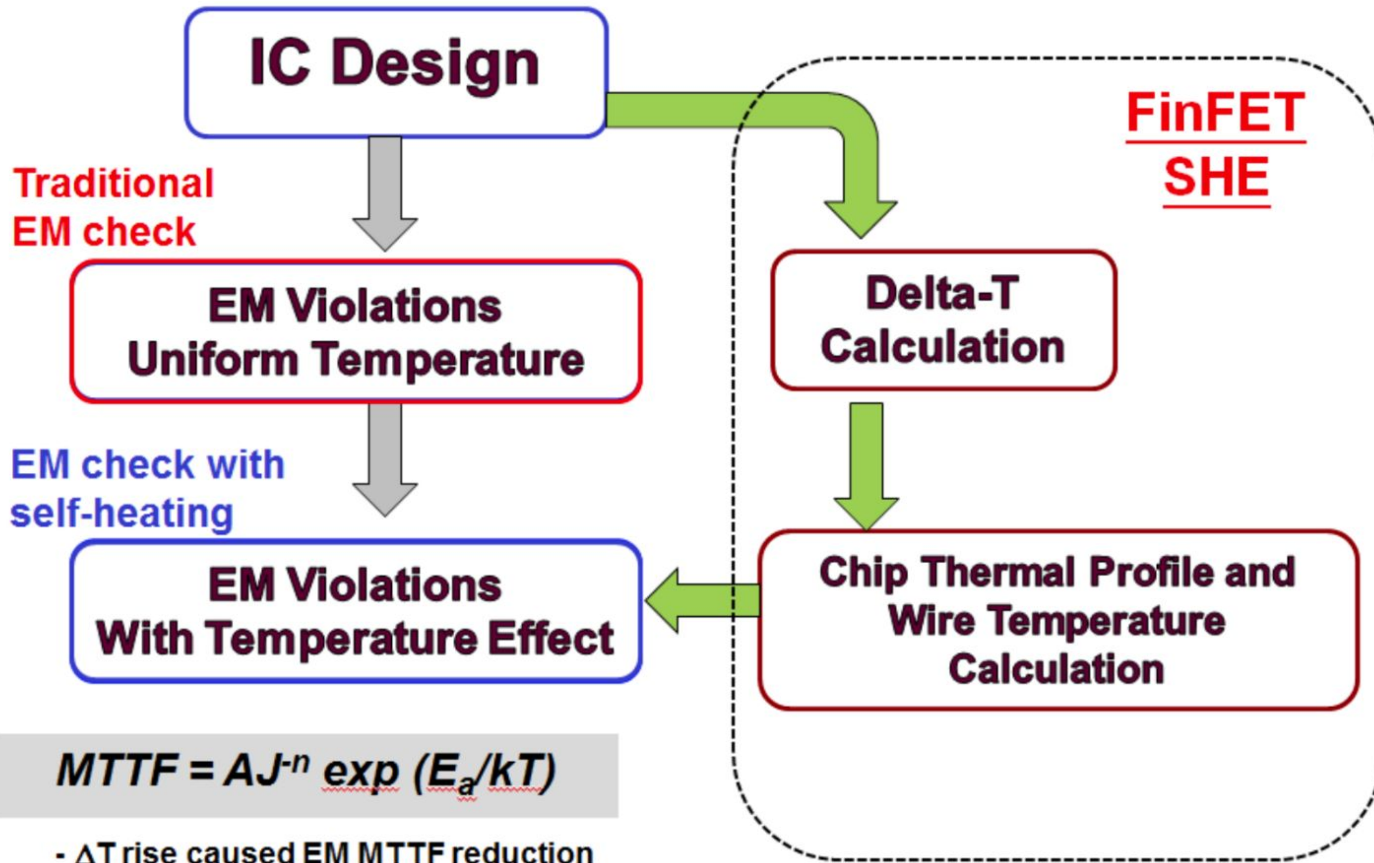
- Heat is carried out by phonons
- Phonon travelling is controlled by boundary scattering i




TSMC FinFET, IRPS 2014, Lu, IEDM 18

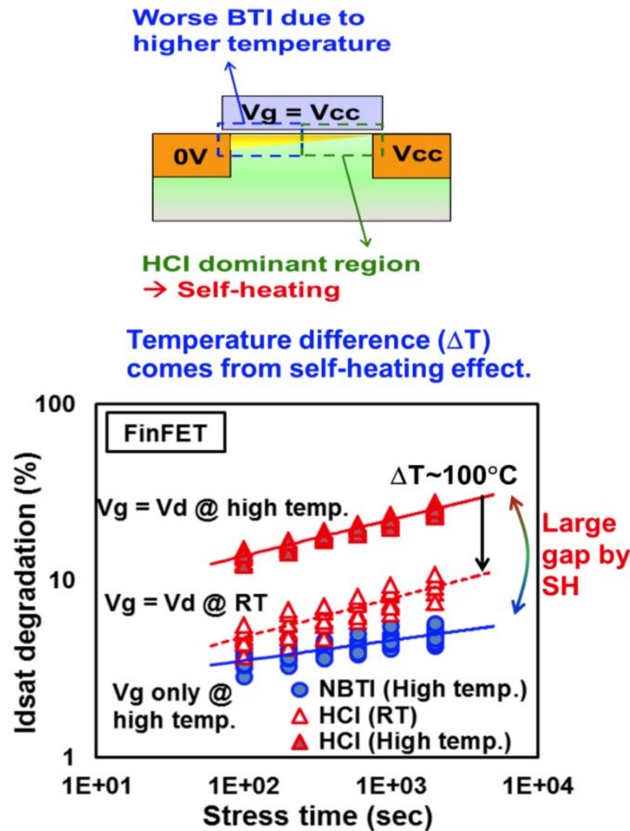
# EM simulation for FinFET Self-Heating

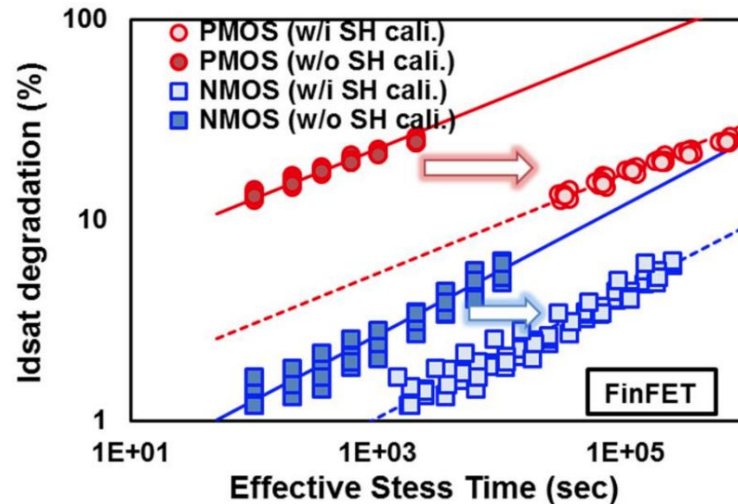



TSMC FinFET, IRPS '14

# Impact of Self Heating Effect on HCI in FinFETs

- Self heating will degrade HCI in FinFET



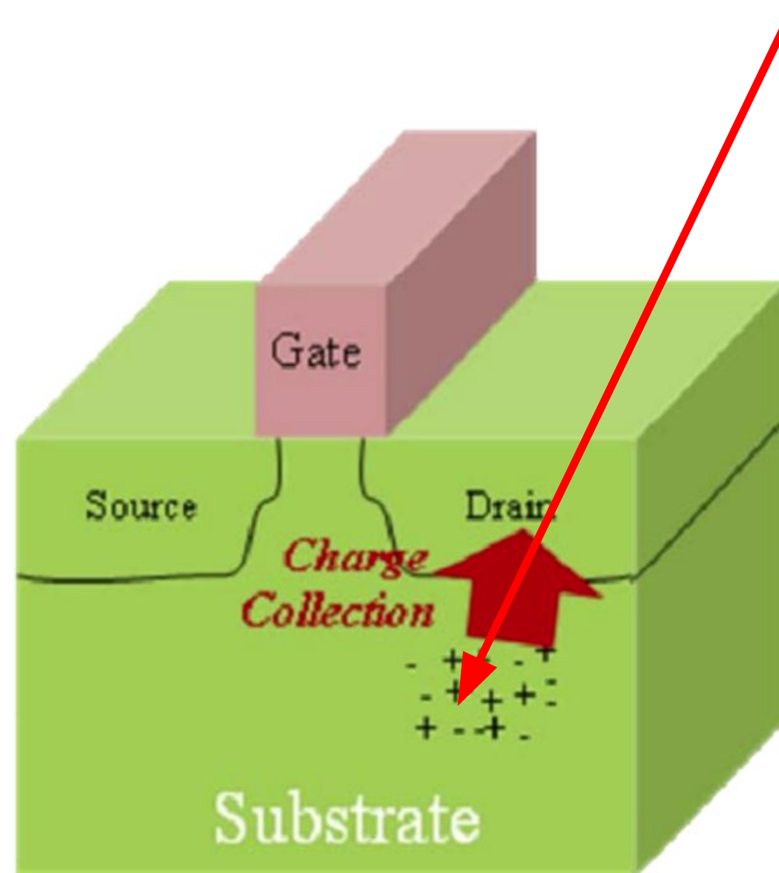




$$t_{eff} = t \times exp\left(\frac{E_a}{k(Tamb + To_p)} - \frac{E_a}{k(Tamb + R_{TH} I_D V_D)}\right)$$

*amb: ambient temp*

*TSMC FinFET, IRPS '14*

# SER basics

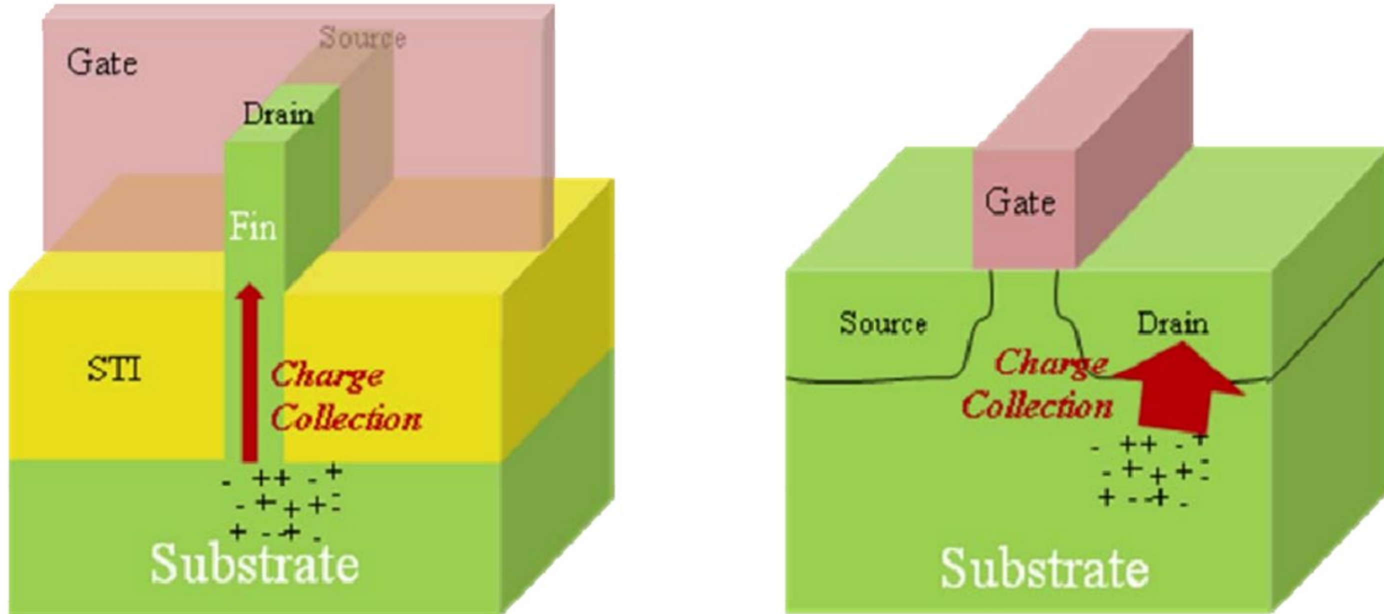



cosmic radiation
alpha particle

creates a current path
that can disturb storage nodes
like SRAM bits, Flops

Lee et al, IRPS 2015

# SER in FinFETs vs Planar

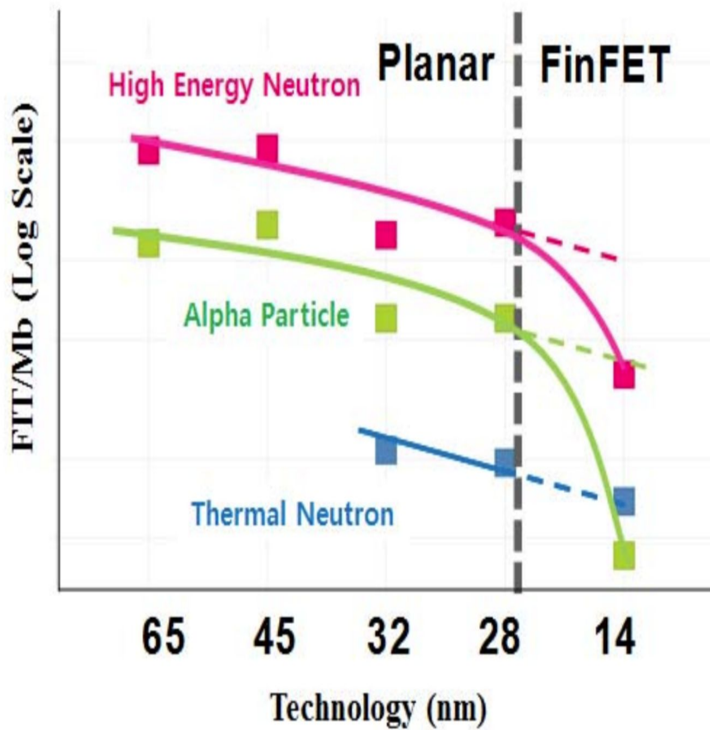


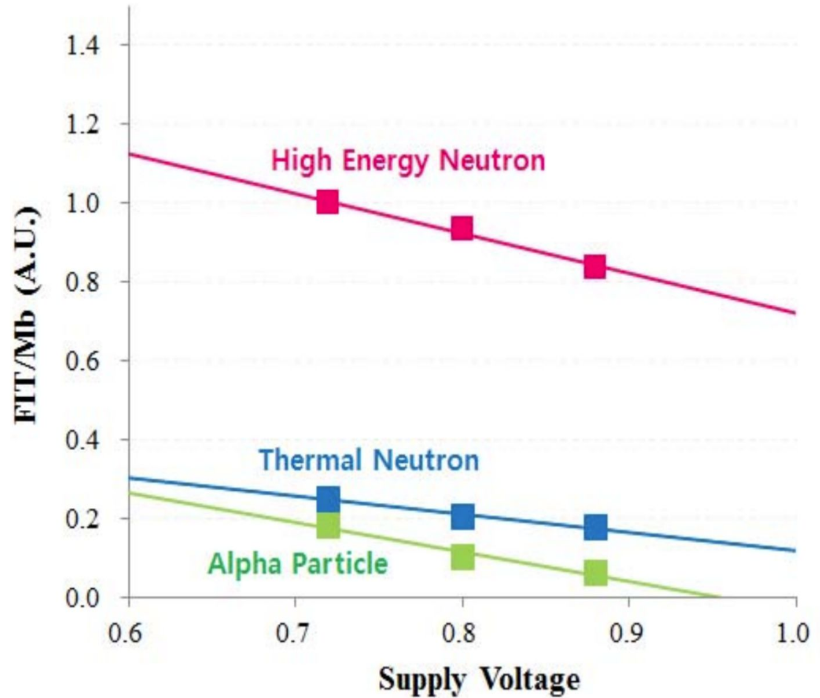

SER induced charge collection in (a) FinFET and (b) Planar FET.

FinFET presents lower charge collection area

Lee et al, IRPS 2015

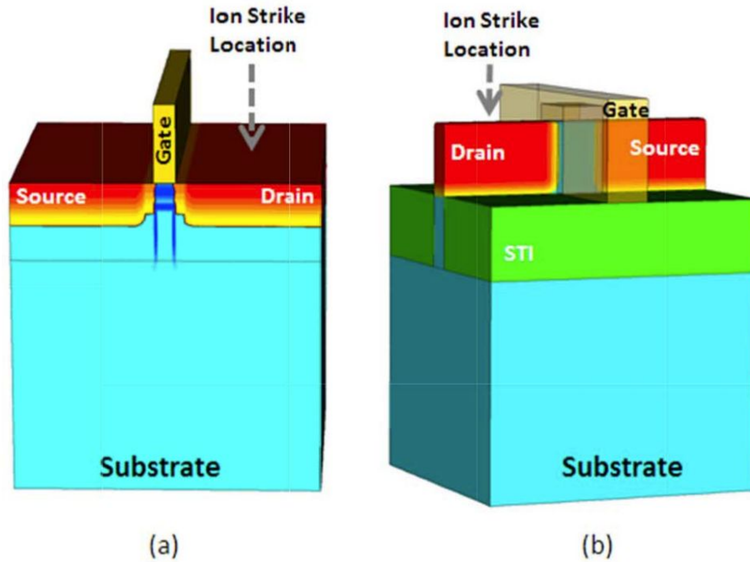
# SER in SRAMs



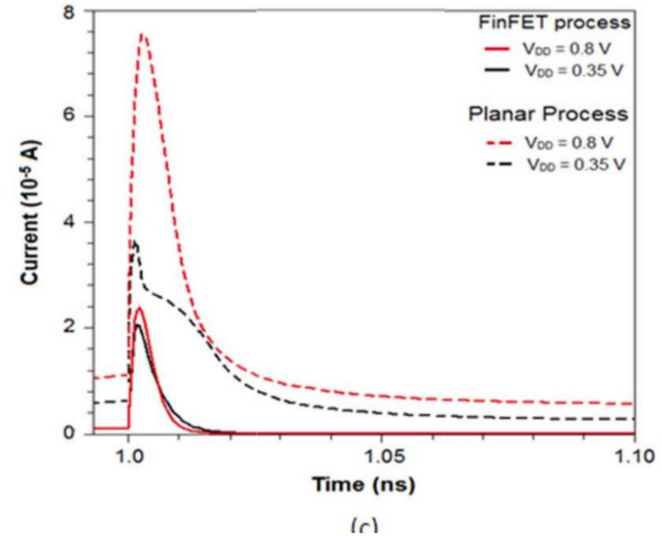




Lee et al, IRPS 2015

# SER in Flops

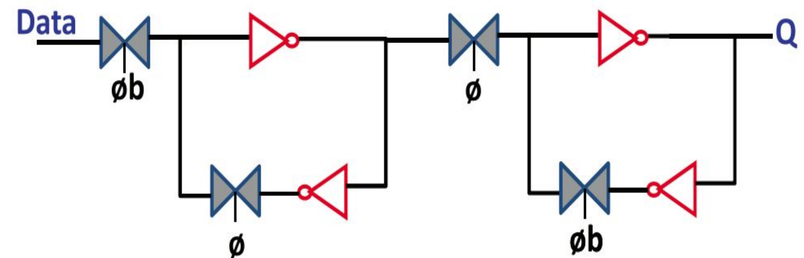



current pulse waveforms




3D-TCAD model of
(a) planar and
(b) FinFET n-channel transistor
showing the ion-strike location.

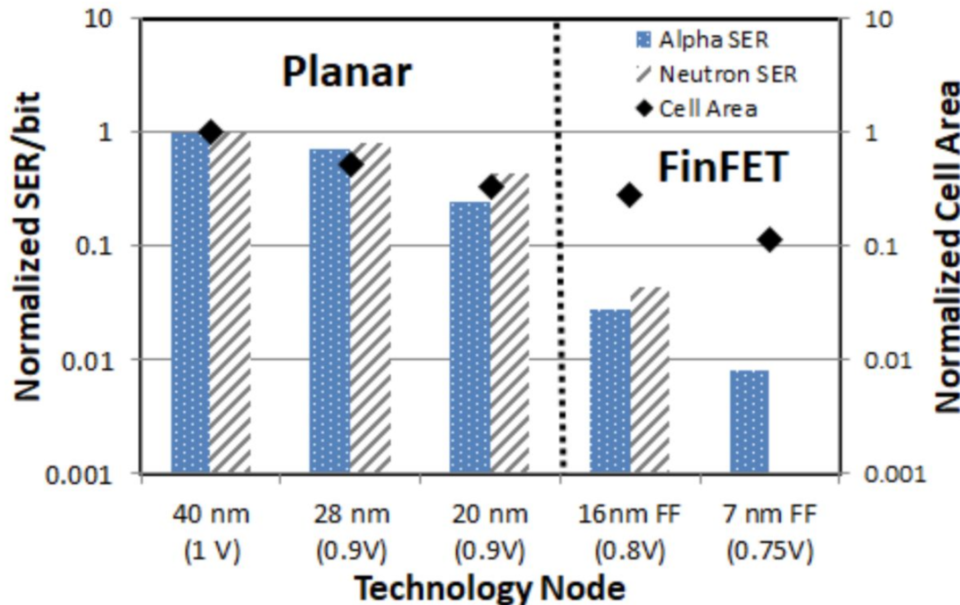
.



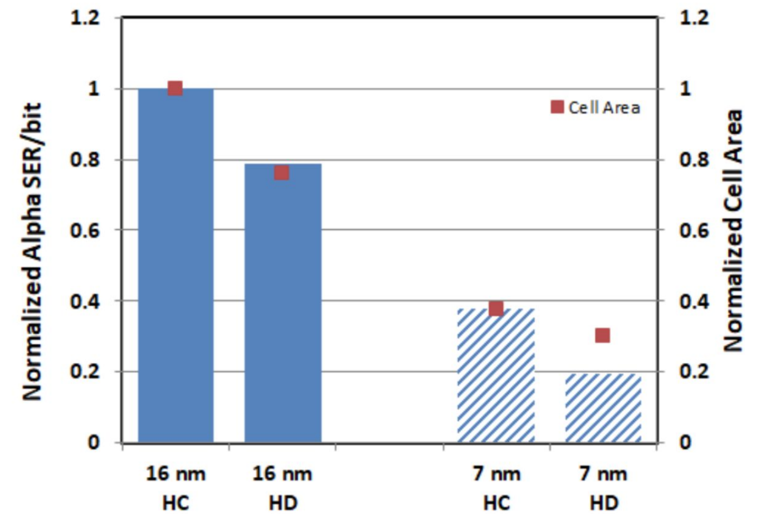

D-flip-flop

Narasimham et al, IEEE Trans. Nucl. S, 2015

# SER vs Technology Node




Normalized scaling trends in the per-bit alpha and neutron SER
of SRAMs as a function of technology node;
Secondary y-axis shows
the normalized SRAM bit-cell cell area comparison.

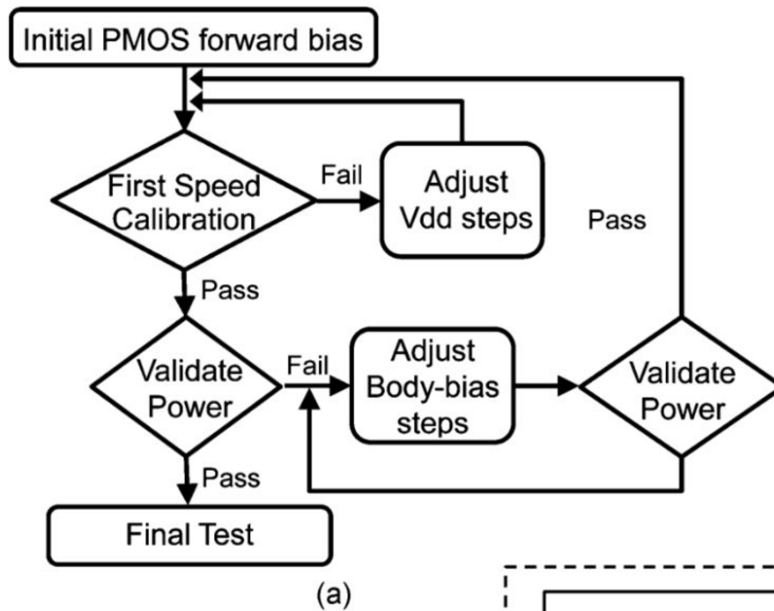


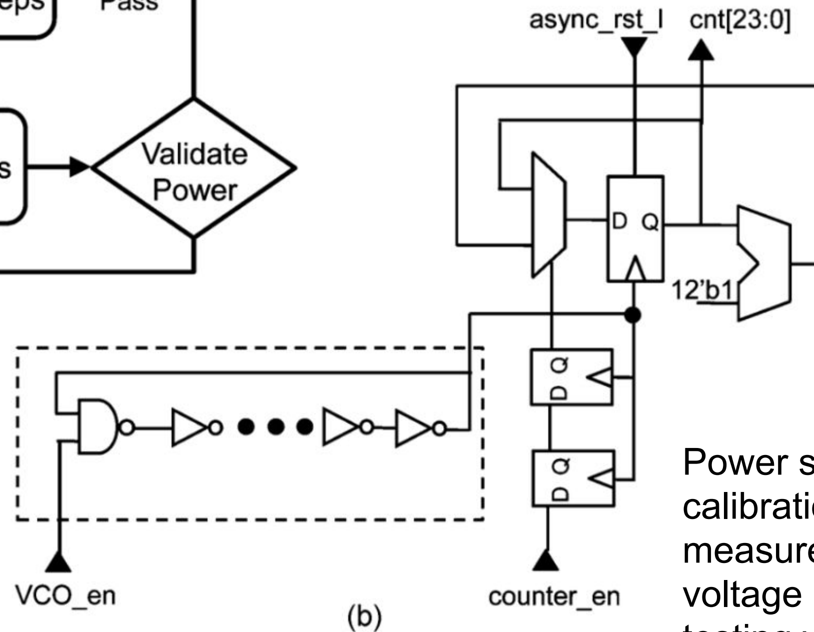

Normalized Alpha SER comparison between High-Current (HC)
and High-Density (HD) SRAM cells in 16 nm and 7 nm FinFET
processes. Secondary y-axis shows the normalized bit-cell area

comparison.

Narasimham, et al, IRPS 2018

# Body Bias Adaptation



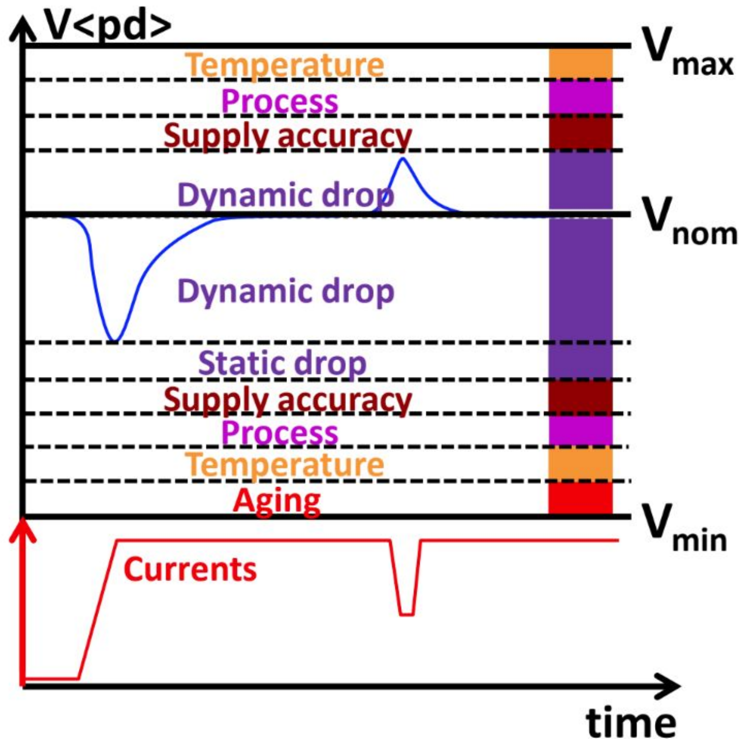



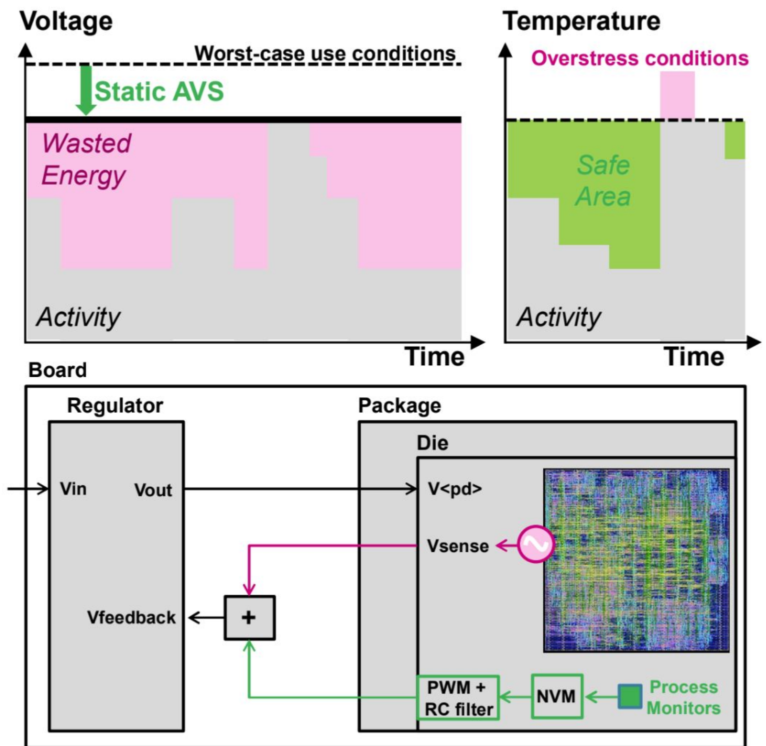

Body-bias and per part VDD to screen out parts that meet both speed and power targets

Power supply calibration circuit measures the exact voltage during testing with a voltage controlled ring oscillator

Shin et al, JSSC 2013

# Adaptive Voltage Scaling

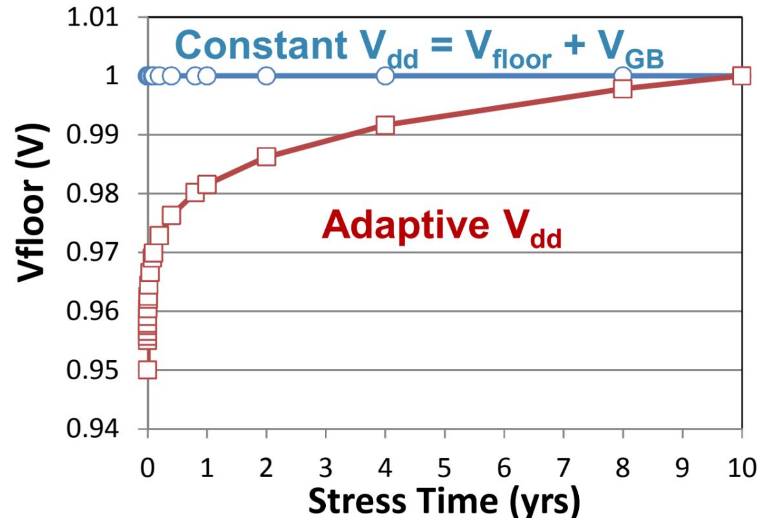


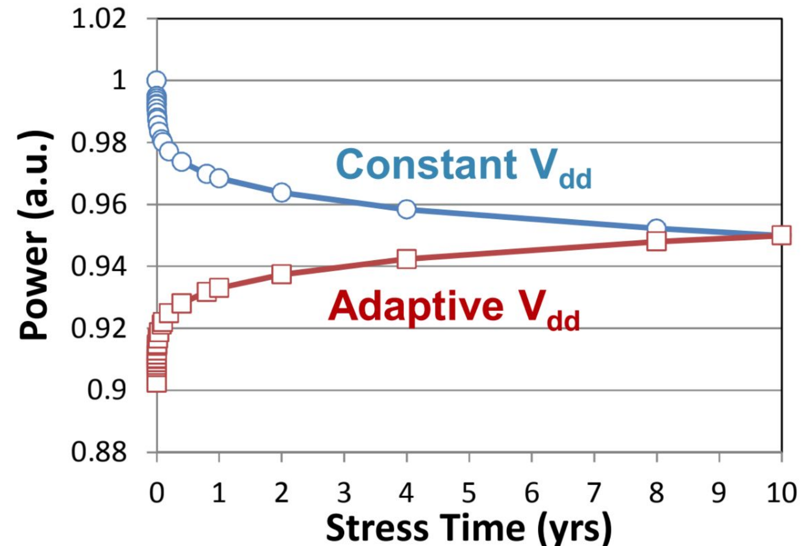




To cope with worst-case (WC) scenario conditions, voltage margins are added on top of nominal minimum voltage to account for various sources of variations either static (process or IRdrop) or dynamic (aging, temperature and workload).

Huard et al, IRPS 2018

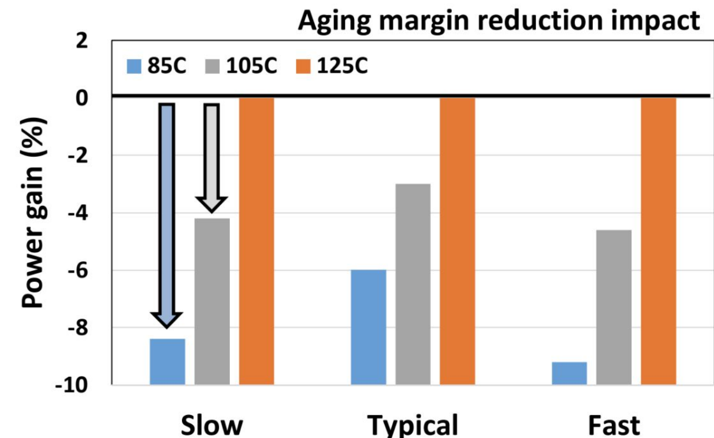
# AVS impact on Power



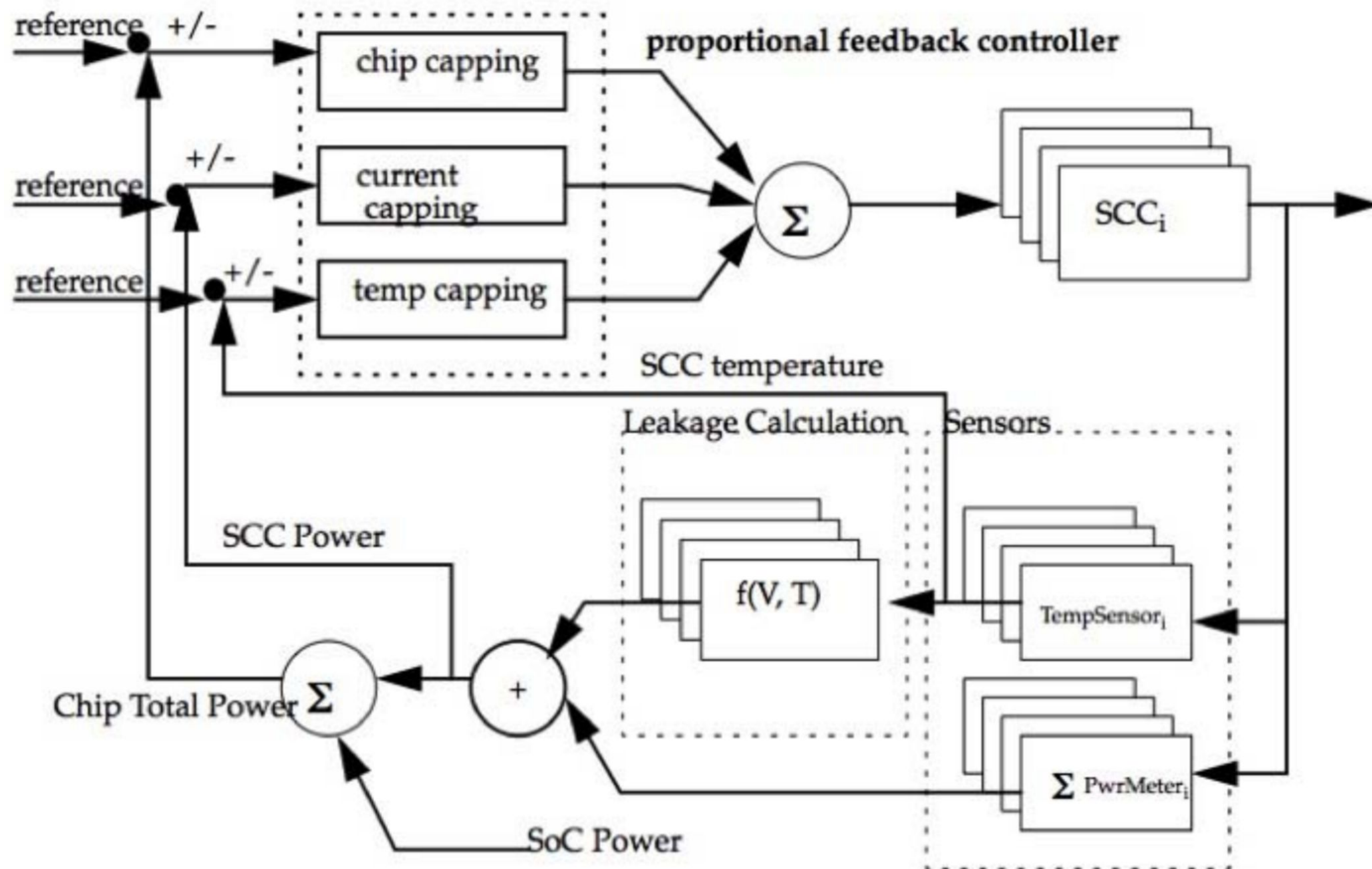




- Fresh parts need lower voltage to operate at the required frequency
- As the parts ages the voltage is gradually increased to compensate for the speed loss due to aging.
- Accounting for EOL margin form the very beginning leads to waste of power.

Huard et al, IRPS 2018



# Power Management Control




Based on key nodal activity predicts the power consumption and applies DVFS to maintain Temperature and power under constraints while achieving maximum performance

Konstadinidis et al, JSSC 2016

# HTOL Survival Guide

- Symmetrical stress, balanced activity, marching algorithms keep balanced count of 0 and 1 written into the SRAMs
- Free running PLLs
- Disable clock gating
- Main clock trunks in bypass mode at low frequency but running all time during HTOL
  - avoids PLL duty cycle distortion & and timing failures in B phase memories.
- Balanced scan clock stress
- Bottom line: Count of 0->1 and 1->0 transitions per device during HTOL needs to be balanced/ symmetrical

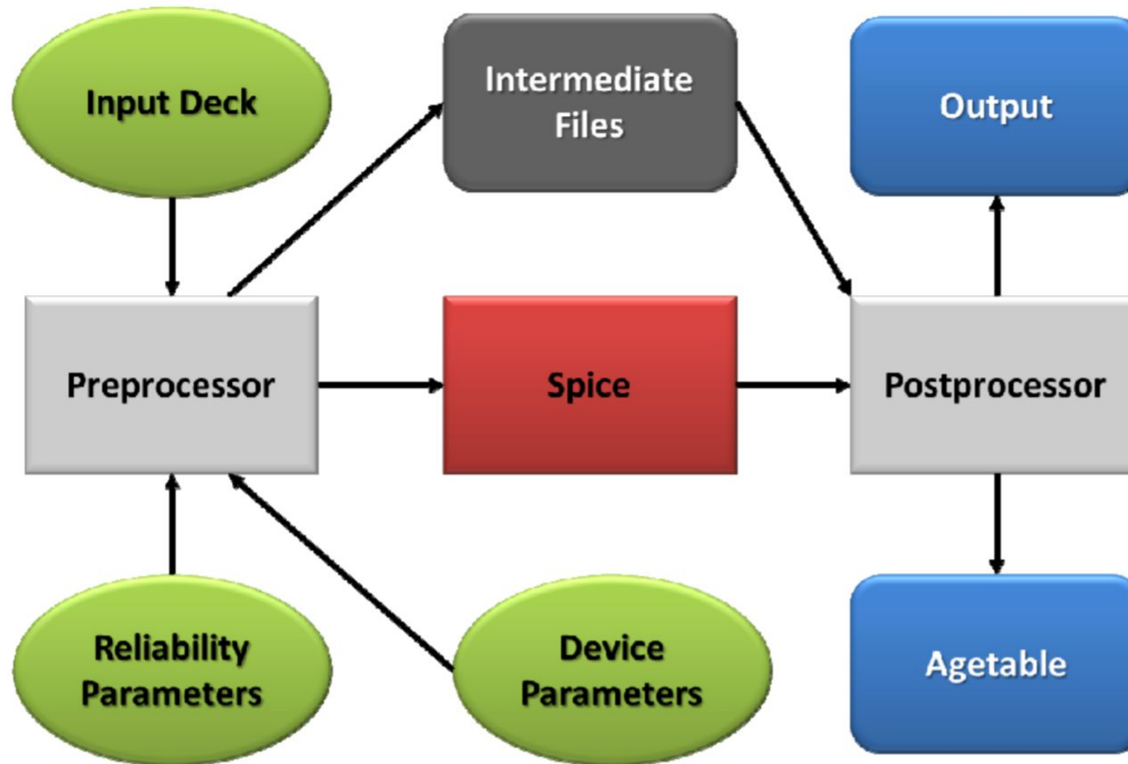
# Outline

- Introduction
- Main Reliability Degradation Mechanisms
  - Voltage, Temperature, Activity dependencies
- Impact on Circuits and Products
  - Reliability Circuit Analysis & optimization
  - Aging monitors
  - Adaptive techniques
  - HTOL Best practices
- **EDA requirements**
- Conclusions

# Reliability Simulators

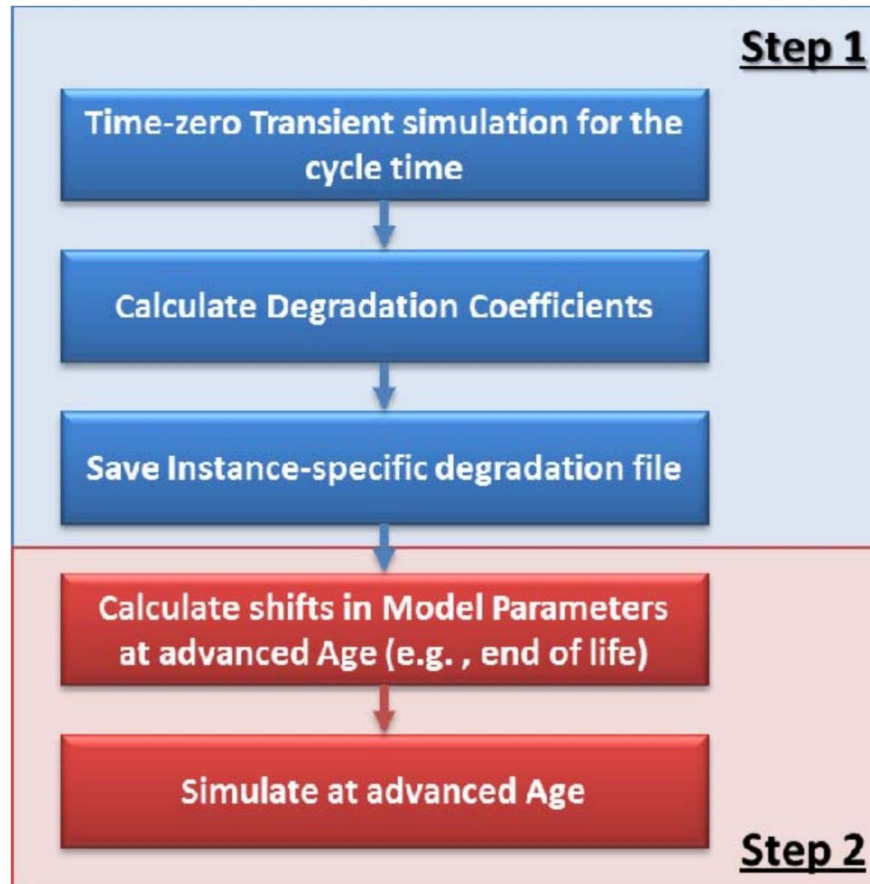
- The Need:
  - Excessive Design margins add time to market, loss in performance, may kill product competitiveness
- It does not affect only HPC devices
- Consumer Electronics and Automotive are equally affected
  - Need fast and accurate reliability simulators to handle not only transistor level circuits but large VLSI

# BERT




Rosenbaum, IEEE Trans CAD 1993

# Generic Reliability Simulation Flow




Ramadan, CMC, IEEE 2013

# Compact Modeling Council (CMC) & Silicon Integration Initiative (Si2)

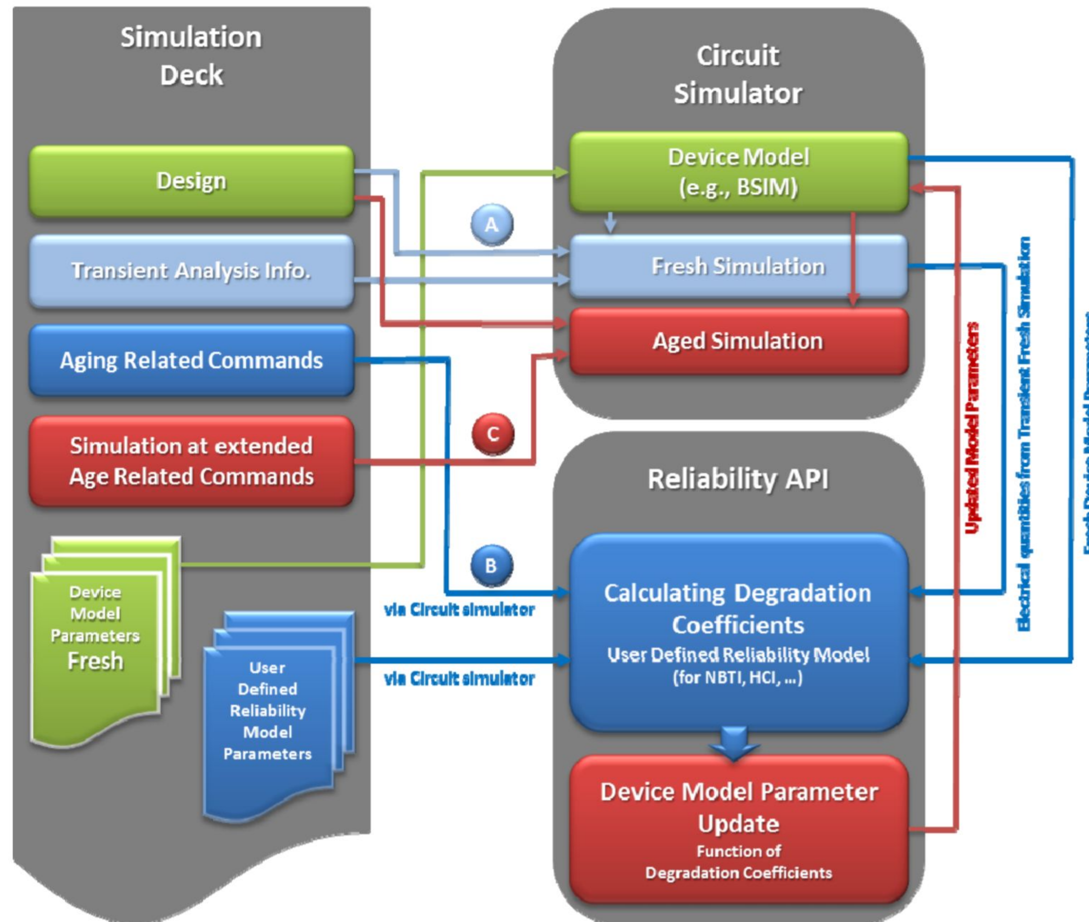
- Model interface standardization

- BSIM-CMG     Common Multi Gate model
- BSIM-CMG 110.0.0 was released on Jan. 1, 2016.

- Most reliability models are custom per foundry.

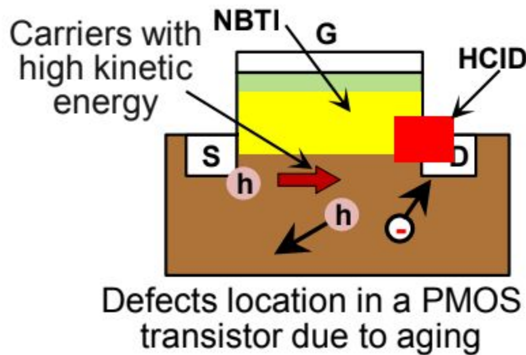
- Open Model Interface open standard is released
- to serve as  an add on to the Design Kit
- Will not be part of the fresh models

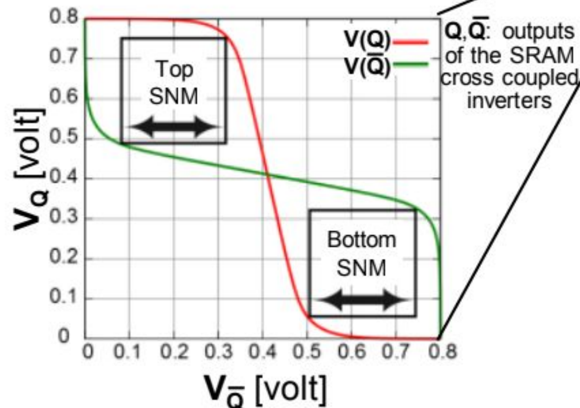
# Generic Reliability Simulation Flow

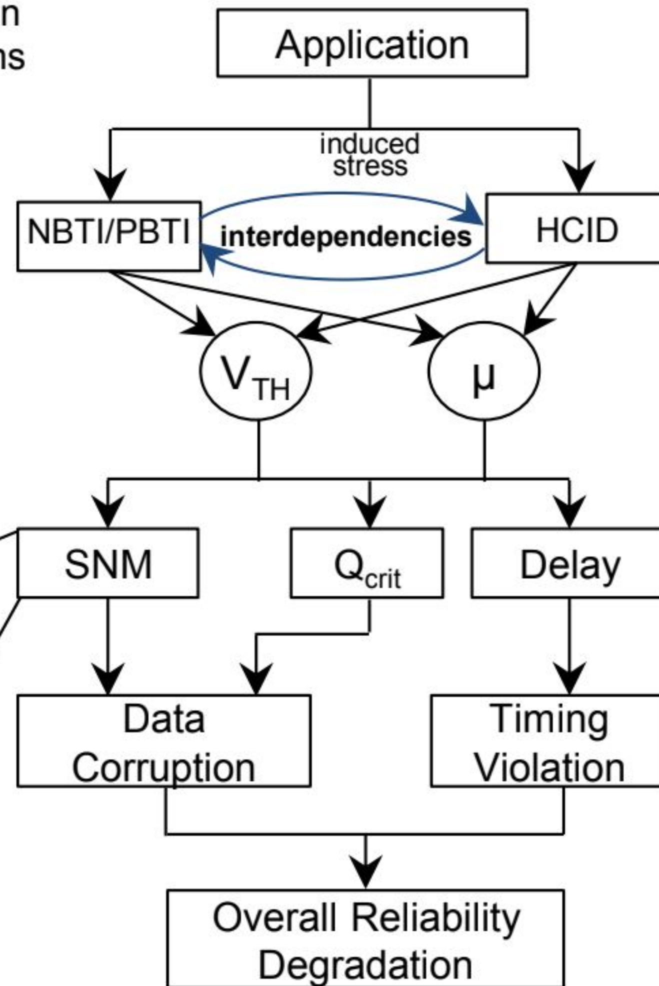



Ramadan, CMC, IEEE 2013

# Reliability Simulation Framework (example I)

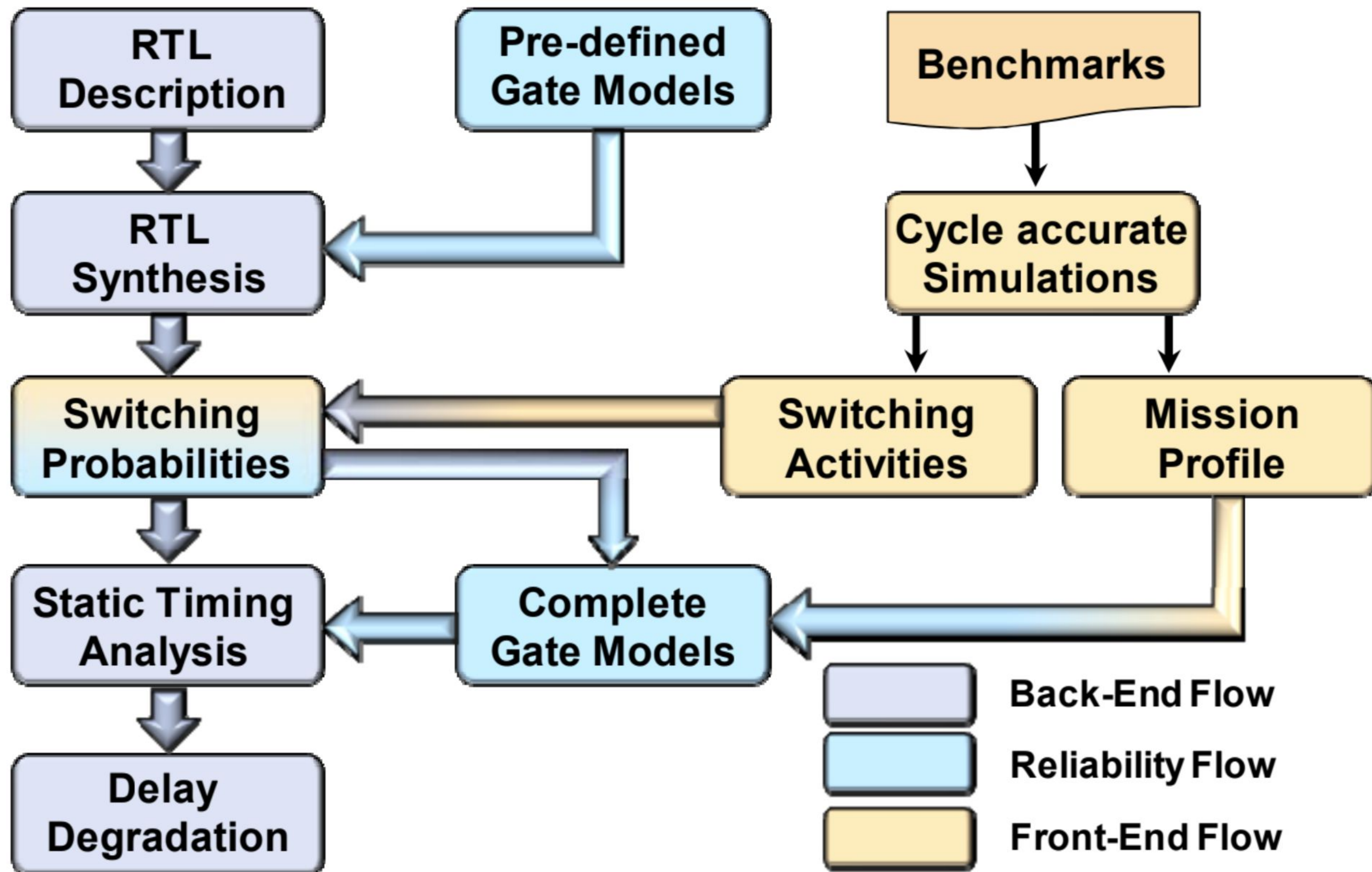



Amrouch et al, 2014

# System Reliability Framework (Example II)




Huard et al, IRPS 2012

# Outline

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# Conclusions

- Product Reliability analysis is a Must
- Worst case analysis is a thing of the past
- Co-optimization of product performance, robustness and time to market requires avoidance of overdesign
  - -> that requires accurate reliability analysis
    - -> that requires good understanding and cooperation between Reliability Physics, Circuit, and EDA communities...

# Thank you!

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