proteanTecs

A Deep Data Approach to Quality, Reliability and Time-to-Market

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October 4, 2019

proteanTecs At a Glance

Founded in 2017

HQ's in Israel with offices in CA and NJ

Funding of ~$50M to date

Tools in use and solution silicon proven

Shai Cohen
CEO, Founder

Previously COO and co-founder of Mellanox

Evelyn Landman
CTO, Founder

Previously VP of Engineering and co-founder of Mellanox

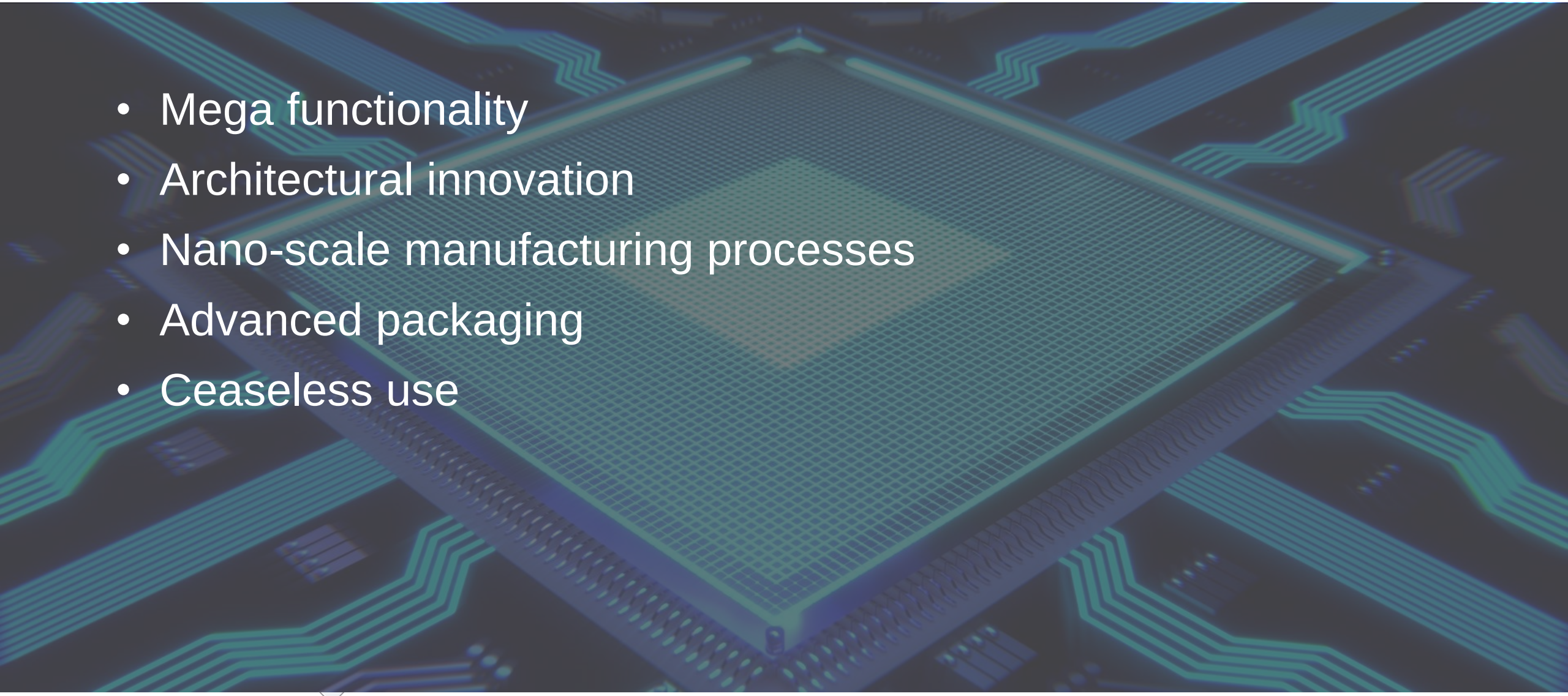
Raanan Gewirtzman
CBO

Previously CEO of BroadLight, acquired by Broadcom

Roni Ashuri
COO, Founder

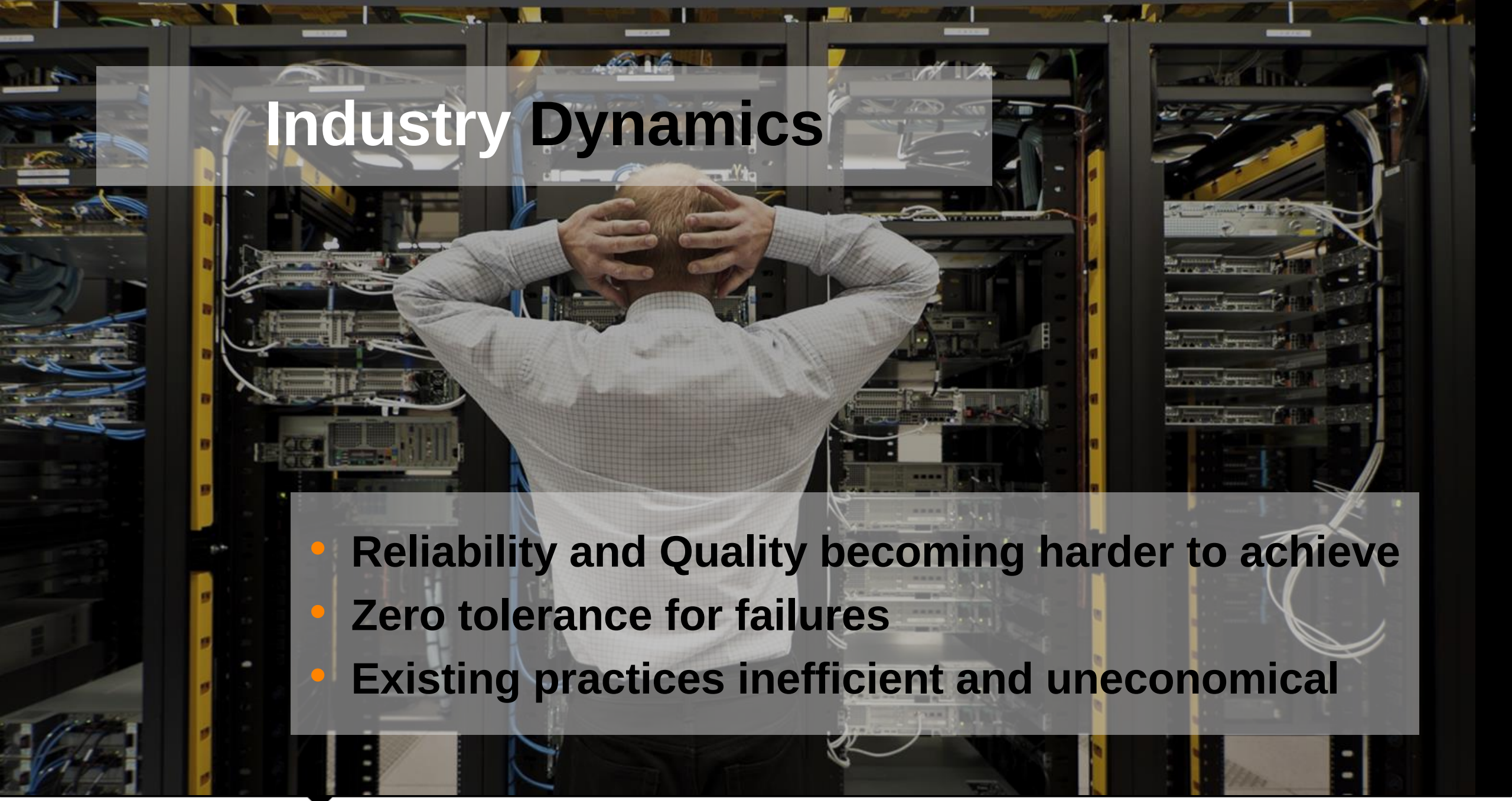
Previously Sr. VP of Engineering and co-founder of Mellanox

Accelerating Scale of Integrated Circuits



- Mega functionality
- Architectural innovation
- Nano-scale manufacturing processes
- Advanced packaging
- Ceaseless use

Industry Dynamics

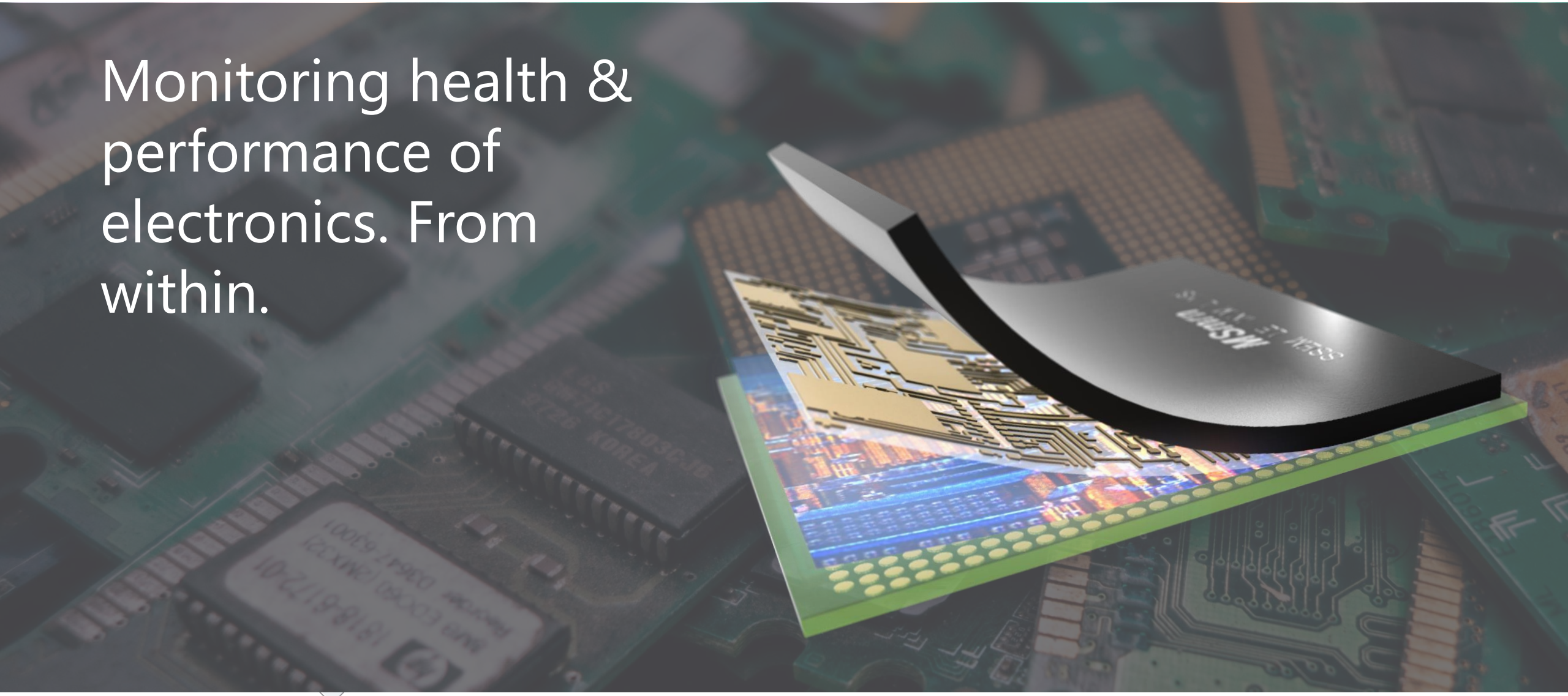


- Reliability and Quality becoming harder to achieve
- Zero tolerance for failures
- Existing practices inefficient and uneconomical

A Paradigm Shift is Needed

Providing Visibility

Monitoring health & performance of electronics. From within.

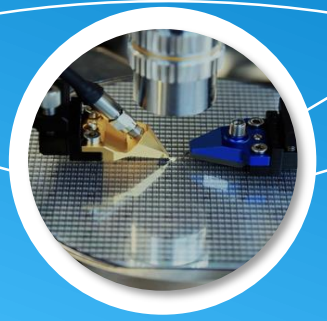


Industry Wide Value

Chip Design

Better Design,
TTM

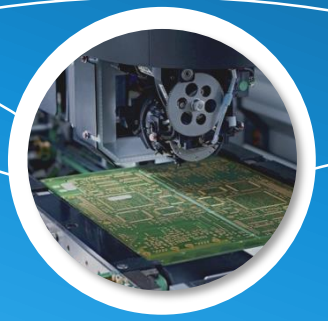
Production visibility
during design



Chip Production

TTM, Parametric Yield,
Towards Zero Defects

Design visibility
during production



System Production

TTM, Parametric Yield,
Towards Zero Defects

Chip as a
system sensor

Lifetime Service

Towards Zero Failures

Health & Performance
monitoring

proteanTecs Solution

1

Proteus-Agents
Design Stage

pre-Si

- Novel deep data creation – Design X Process
- Machine learning analysis
- Embedding Agents

2

Proteus-Platform
Production & Lifetime

post-Si

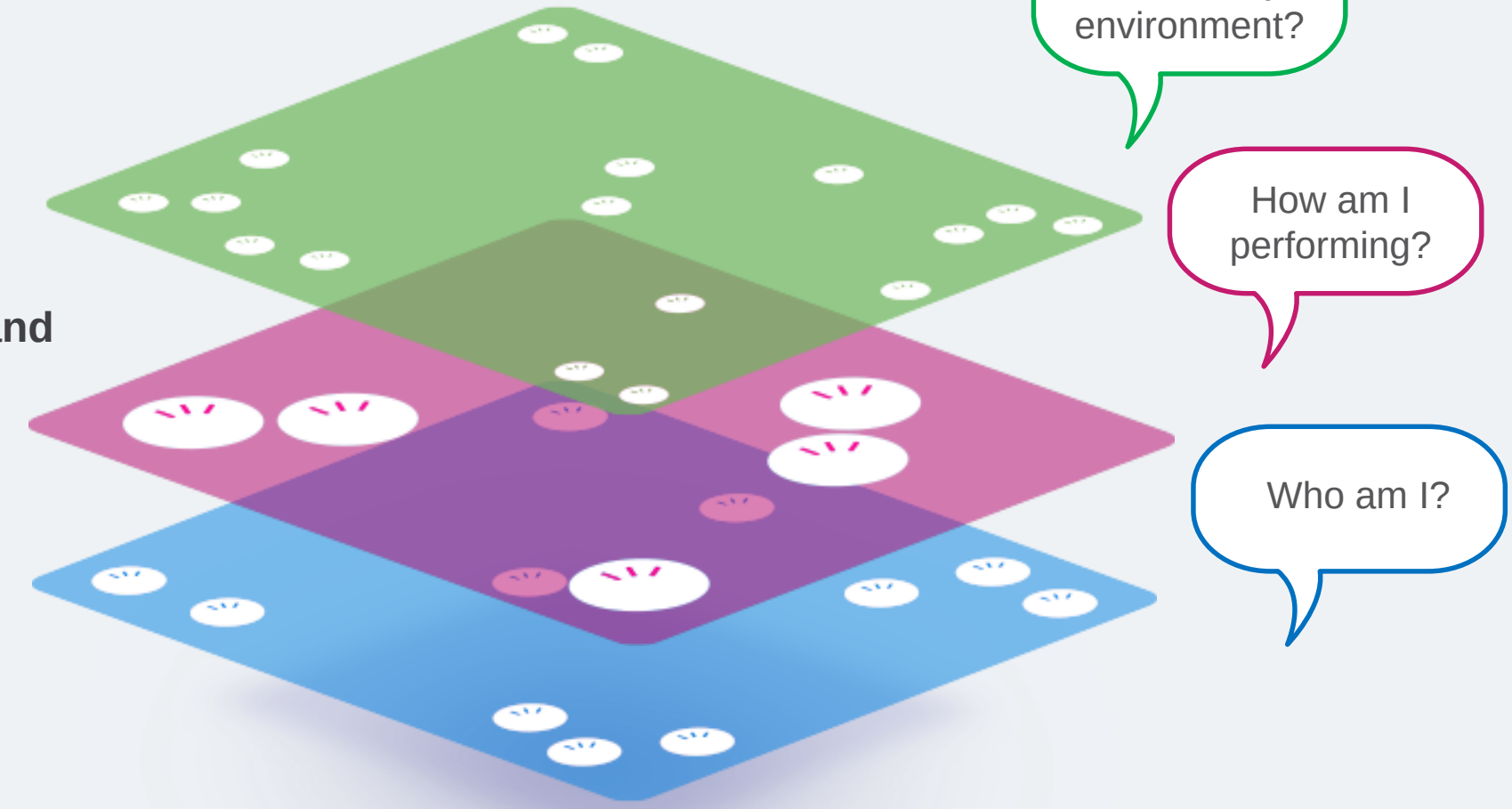
- Agents feed deep data to platform
- Machine learning algorithms and data analytics
- Insights & Alerts

Agent Types

Operational Sensing

Performance and Degradation Monitoring

Classification and Profiling

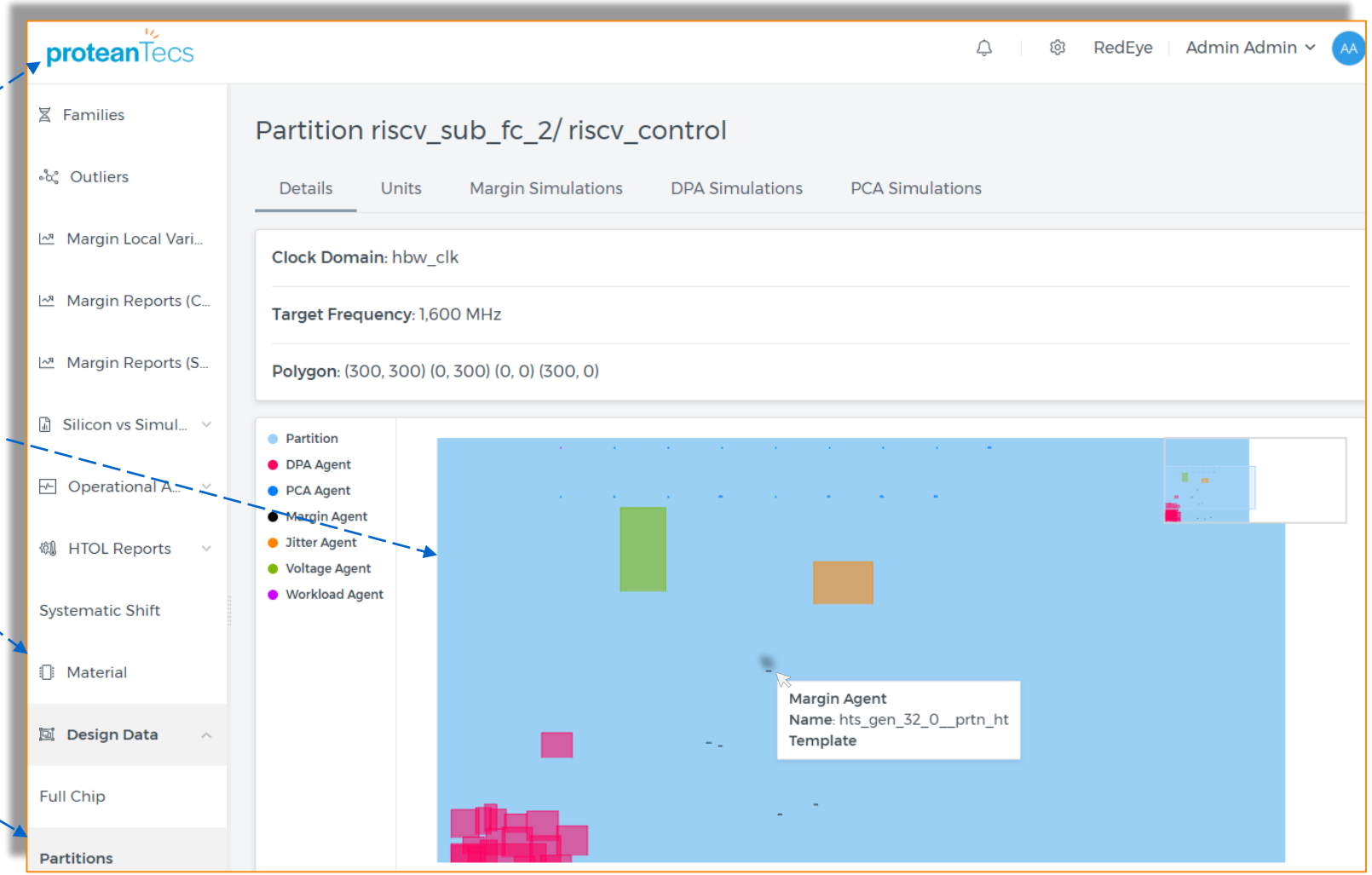


Introducing Proteus-Platform

Machine learning of design input and Agent output | Cloud based data analytics | Actionable insights and alerts

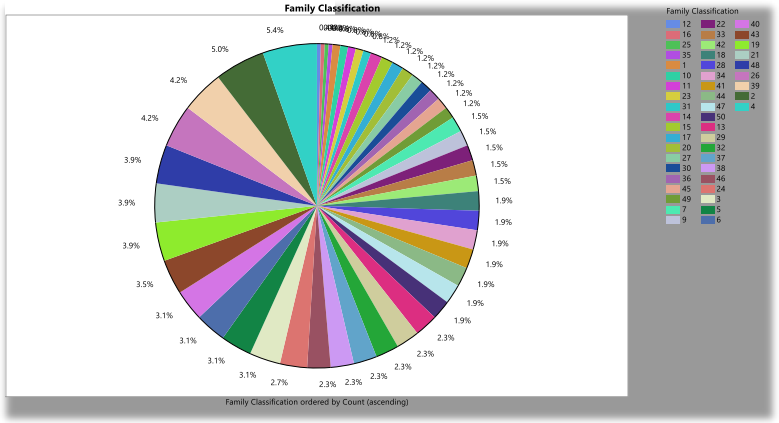
Data Pre-Loaded

- Software service in the cloud that is used while the chip is in production and in-field
- Loaded with the chip's pre-silicon details
- Accumulate Agents Readout and inferences for all units in NPI and HVM
- Providing multiple dashboards for investigations and alerts

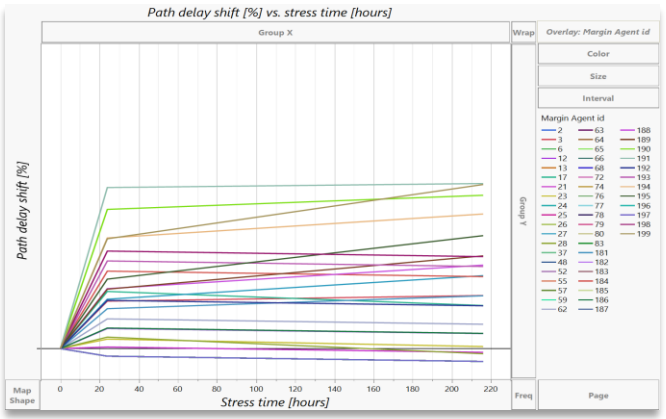


Proteus-Platform Actionable Insights

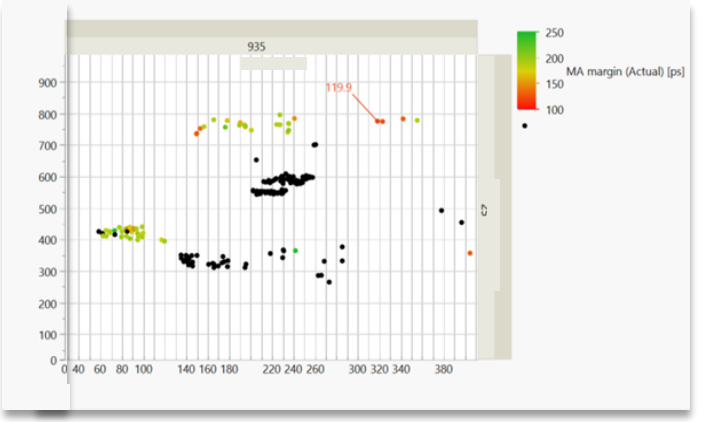
Family-Based “Fine” Binning



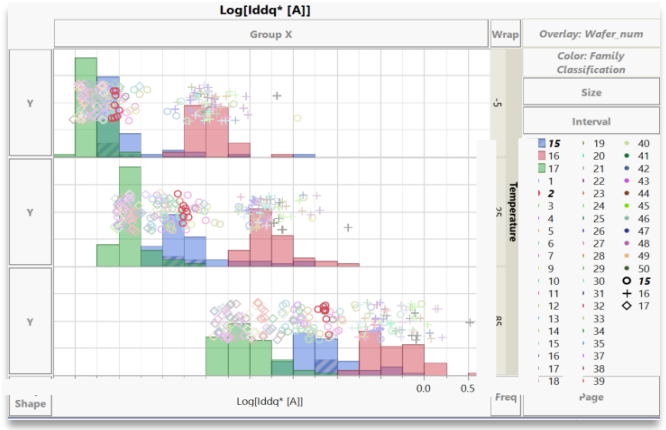
Degradation Monitoring



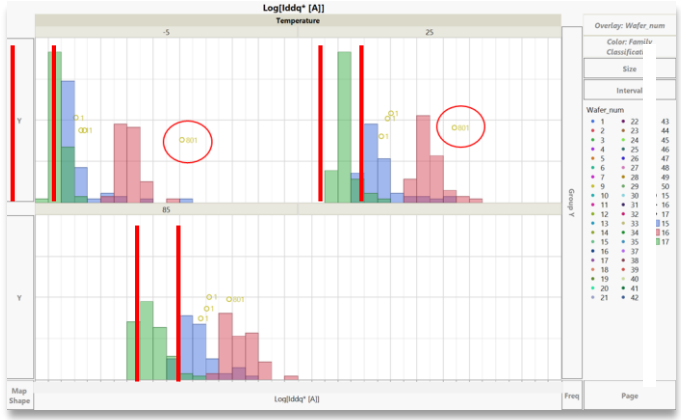
Margin Agents



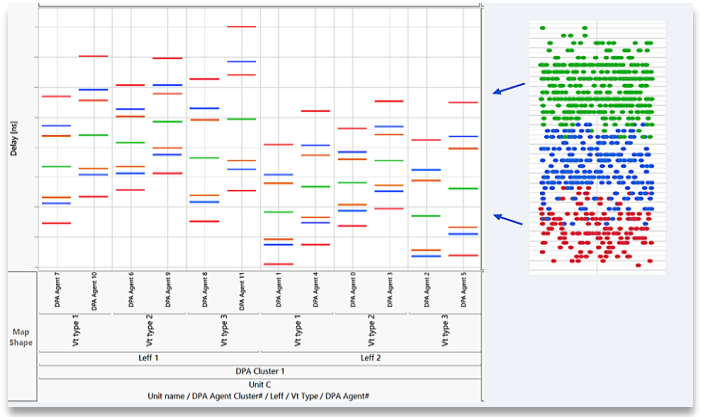
Family Expected Measurement



Outlier Detection

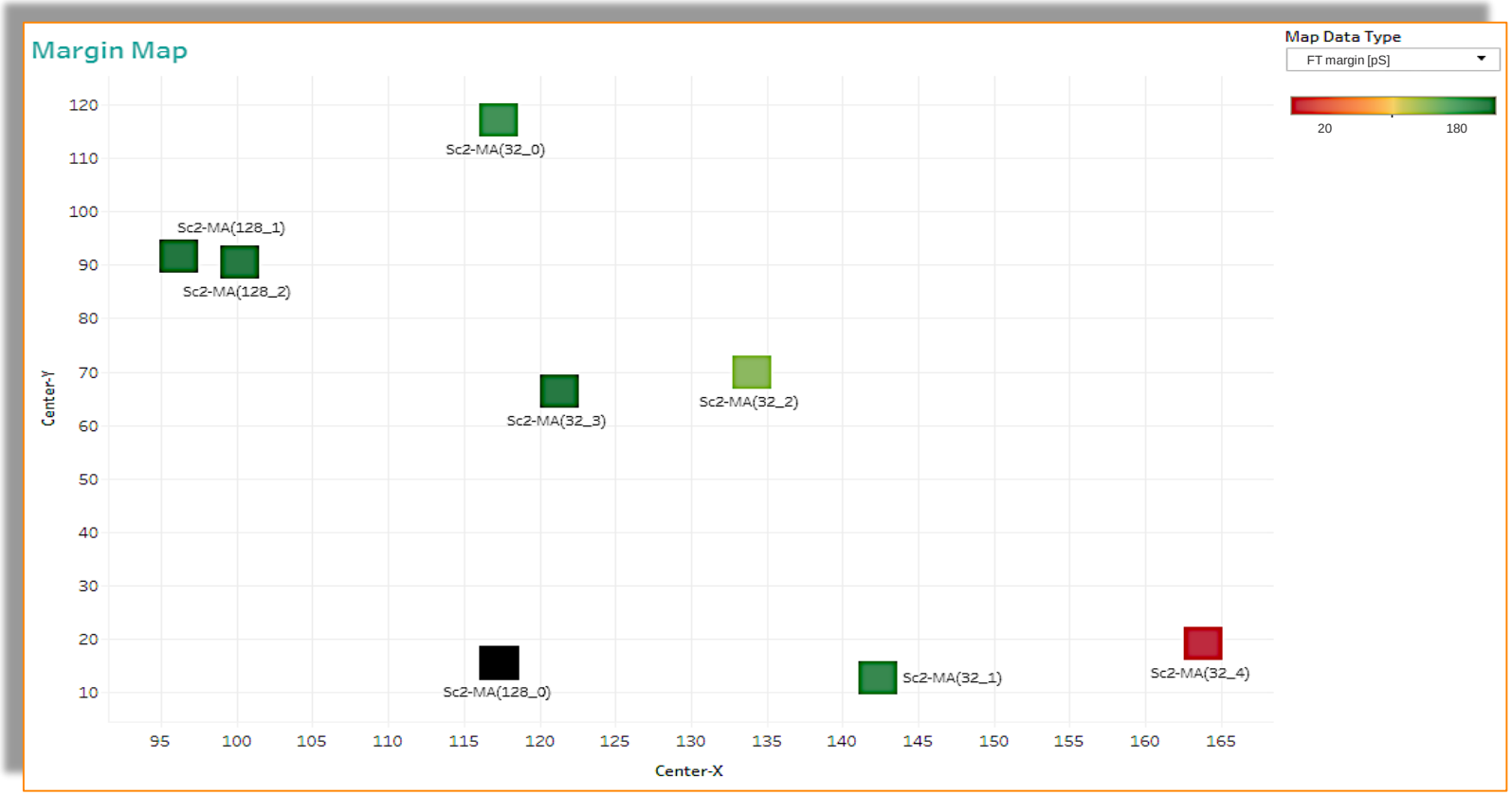


Post-to-Pre Si Correlation



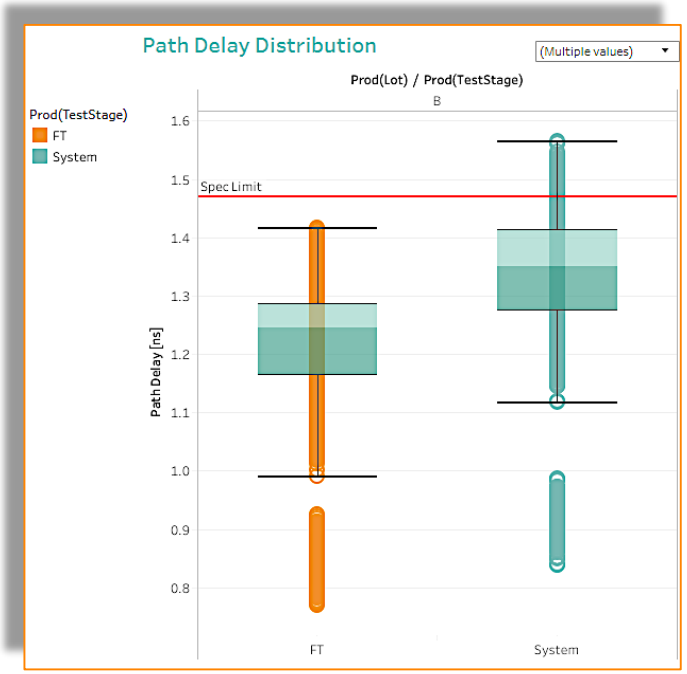
Margin Agents for Performance Mapping

- High-coverage and accurate measurements of paths' remaining margins
- Covers both time-zero margin and every step in production, as well as degradation over time

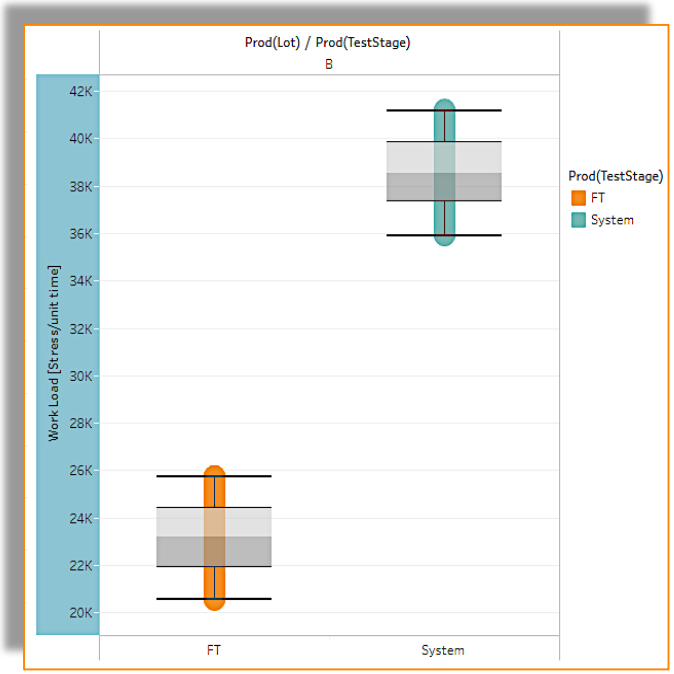


Correlation: System Level Application/ Test to Functional Test at ATE

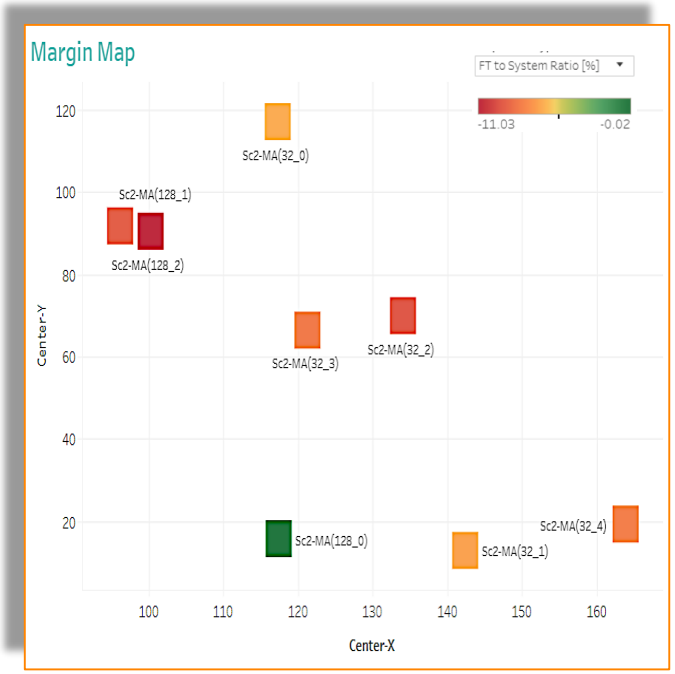
Correlation between System Application/ Test and Final-Test, making sure that the similar stress will be used at the ATE environment



Margin Agents show: higher path delays in System-Test, compared with Final-Test



Workload Agents show: Higher stress in System-Test, compared with Final-Test

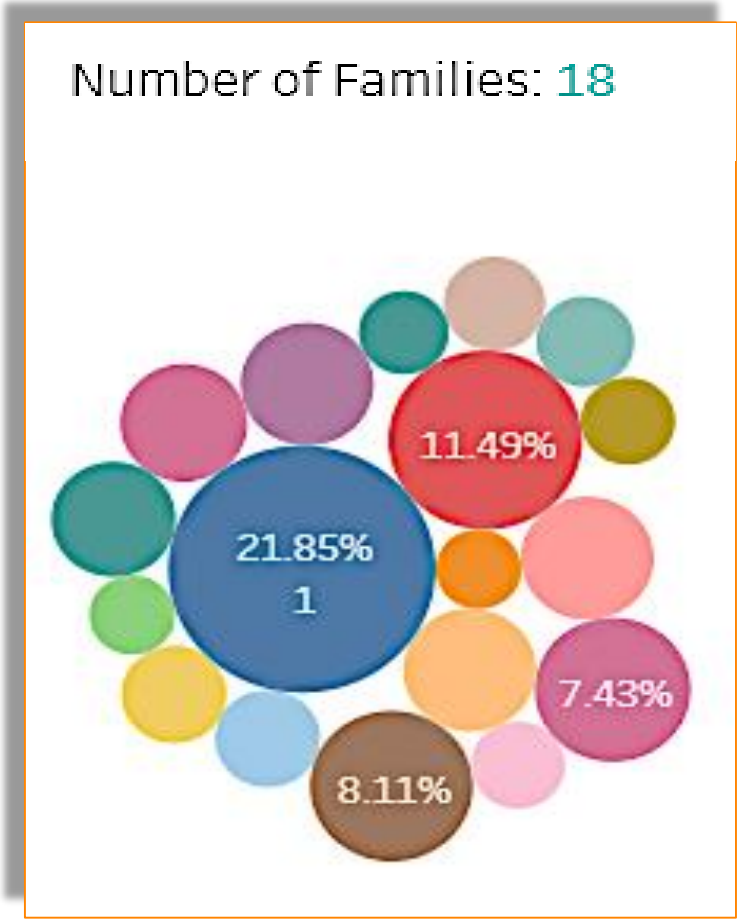


Proteus-Platform provides an efficient tool to match ATE & real System application stress

Introducing Families

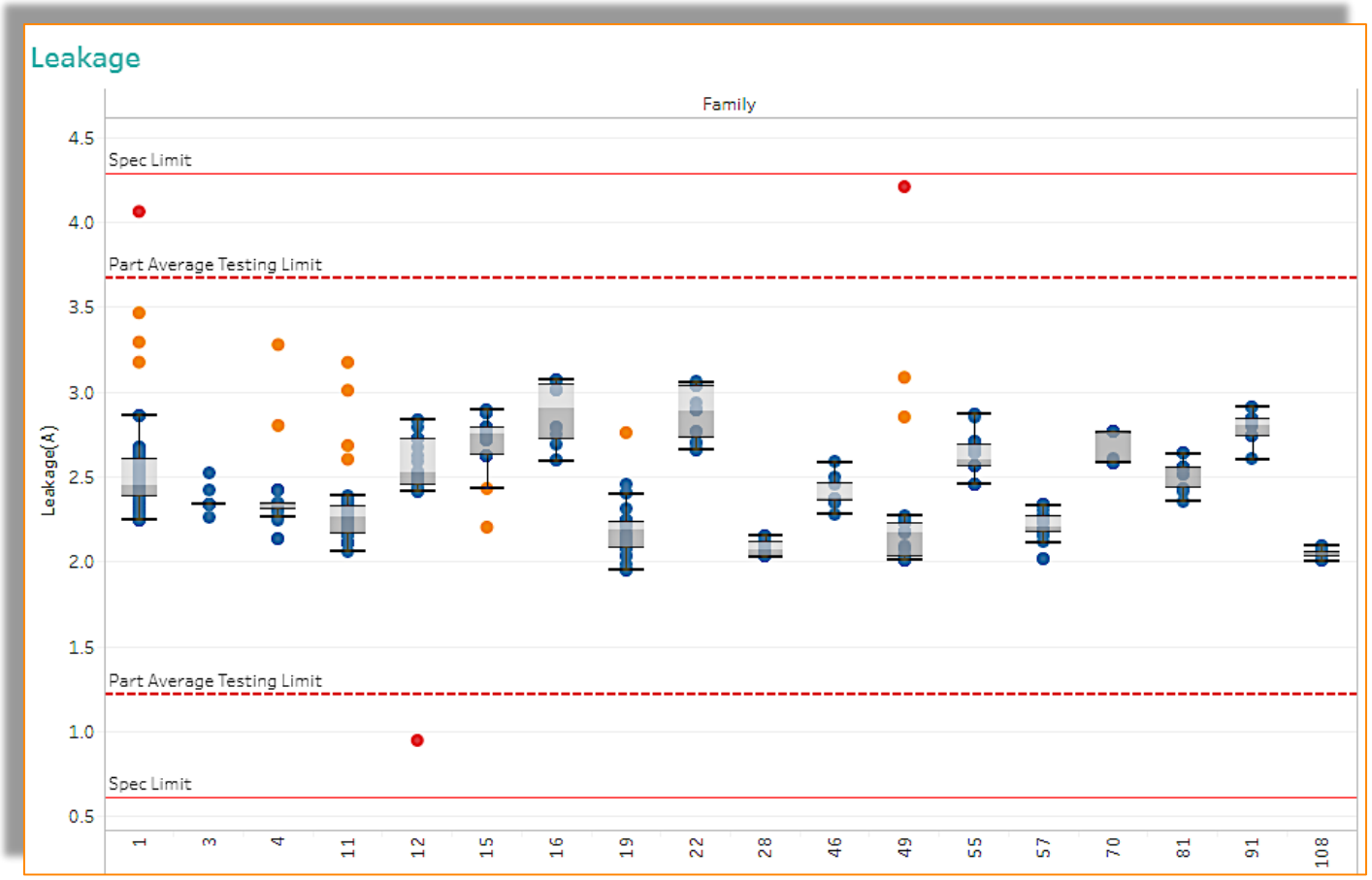
Family is a group of chips that are “located” within a radius of 1 sigma

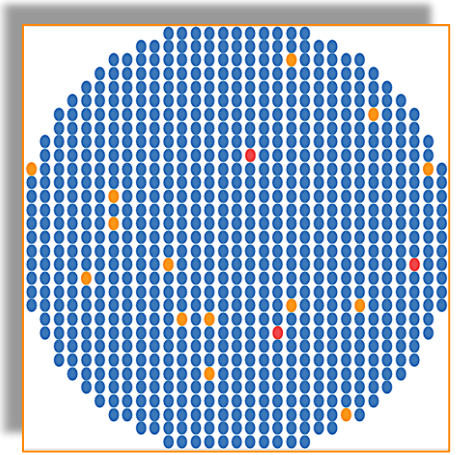
- For every measurable parameter: delay, leakage, dynamic power, etc.
- At any operating condition (V/T) and production stage



Families in Action: 10x DPPM Reduction

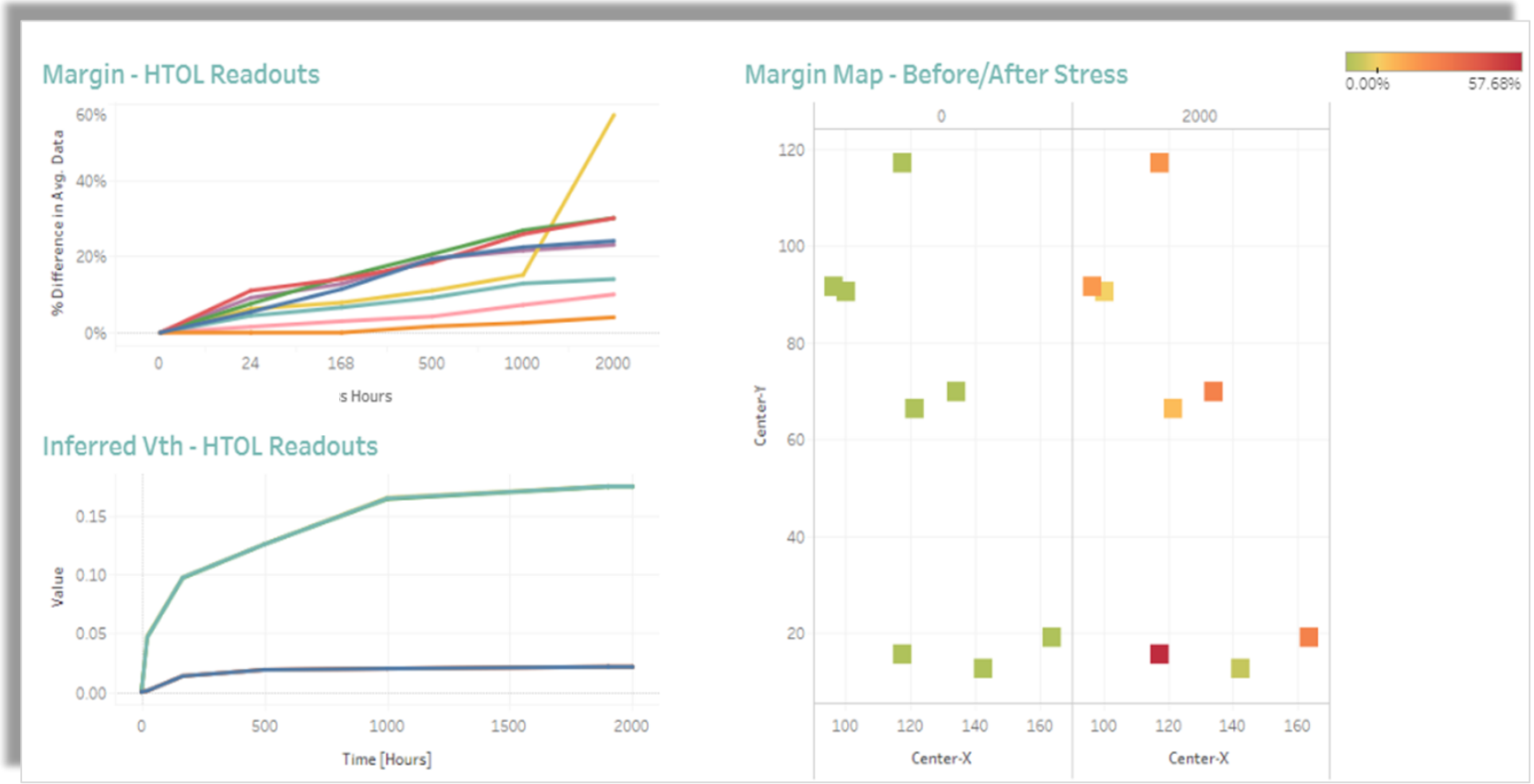
- Outlier detection becomes more accurate, based on relevant reference group (Family instead of wafer)
- Significantly less false-negative/positives





Performance Degradation Monitoring

- Circuit degradation leading to failure can be localized in lifetime accelerated tests, i.e. HTOL
- High-resolution visibility to performance degradation and more efficient reliability issue debug and resolution
- In-field use for failure prediction



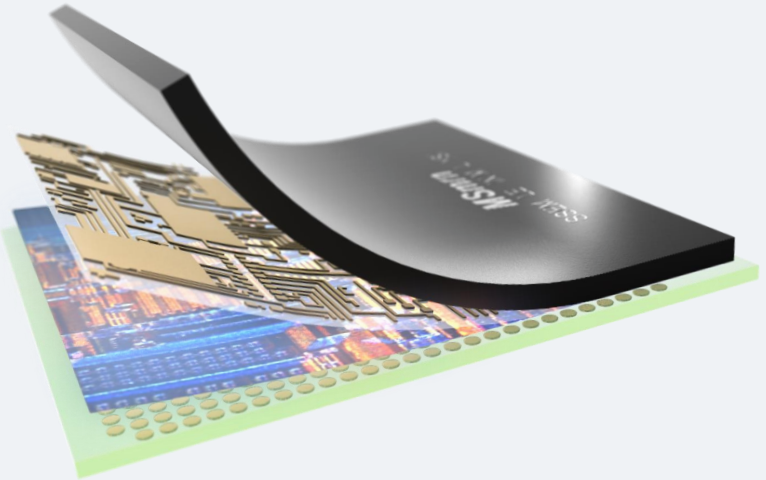
Universal Chip Telemetry UCT™

- New approach for performance, quality & reliability based on visibility
- Embedded surveillance of chip health & performance
- Deep-data driven decision taking
- Shared language across the value chain

Driving a New Standard of Visibility

Driving Design for Reliability

- Unprecedented visibility
  - Margin, hot spots, on-chip variation, bump/ channel grading
  - Infer process parameters and Monte Carlo corners
  - Correlation with pre-si data
  - Degradation monitoring during lifetime and HTOL/ BI
- Early yield fluctuation detection
- Test time reduction
- Correlation with system level application/ test



Faster Time to Volume

10x DPPM Reduction

Operational Savings

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Thank you.