SYNOPSYS®
Silicon to Software™

Where are we on the road to Artificial Intelligence in Chip Design?

Dr. Thomas Andersen

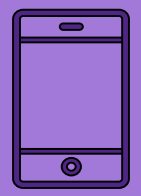
Head, Machine Learning and AI, Design Group

Artificial Intelligence – Avenue to Innovation

ICs Across All Markets to Include AI Capabilities

MOBILE

All Smartphones will integrate AI Processing Capabilities by 2021



DATA CENTER

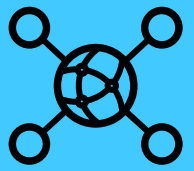
More than 50% of enterprises will deploy AI accelerators in their server infrastructure by 2022

AUTOMOTIVE

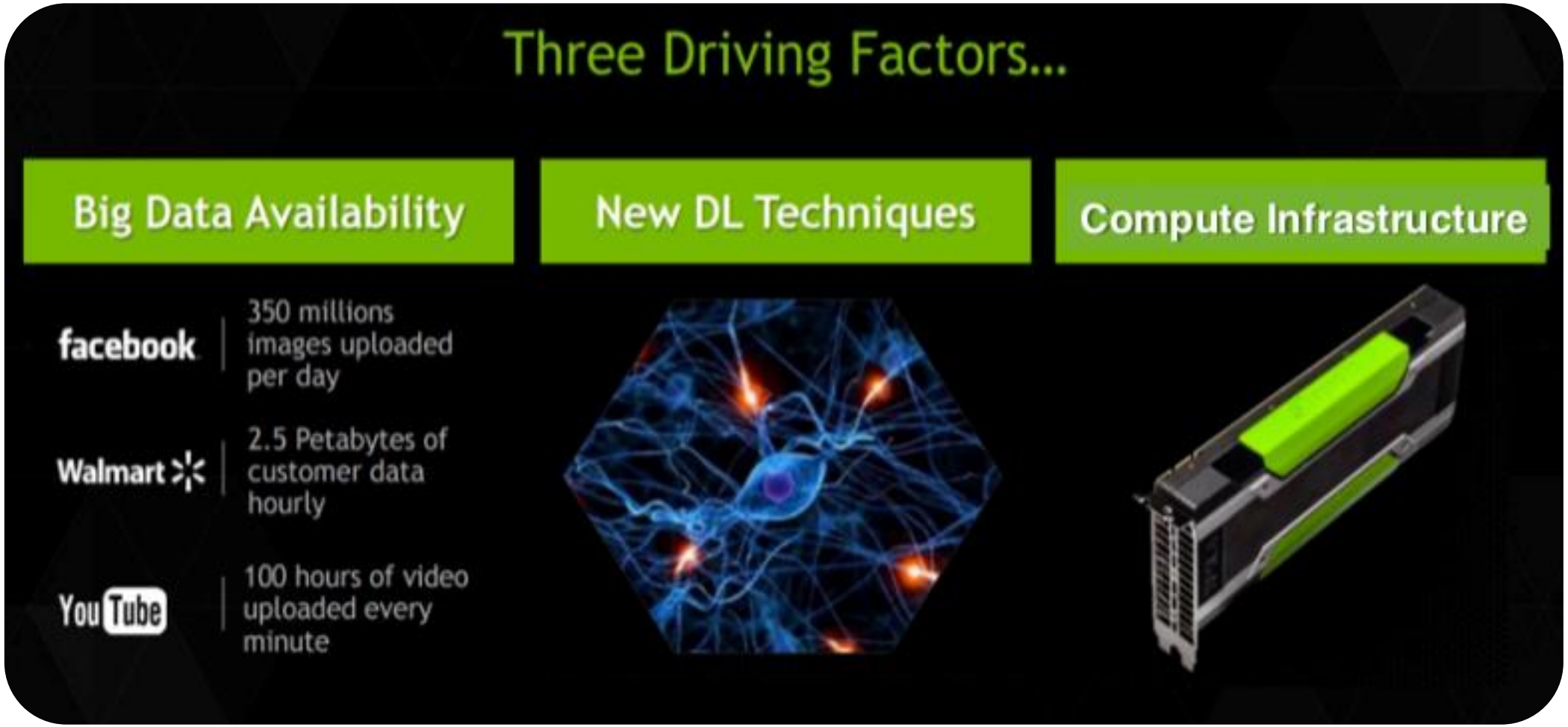
Volume production of autonomous vehicles will begin in 2020

IOT

More than 20% of IoT devices will have AI processing Capabilities by 2022



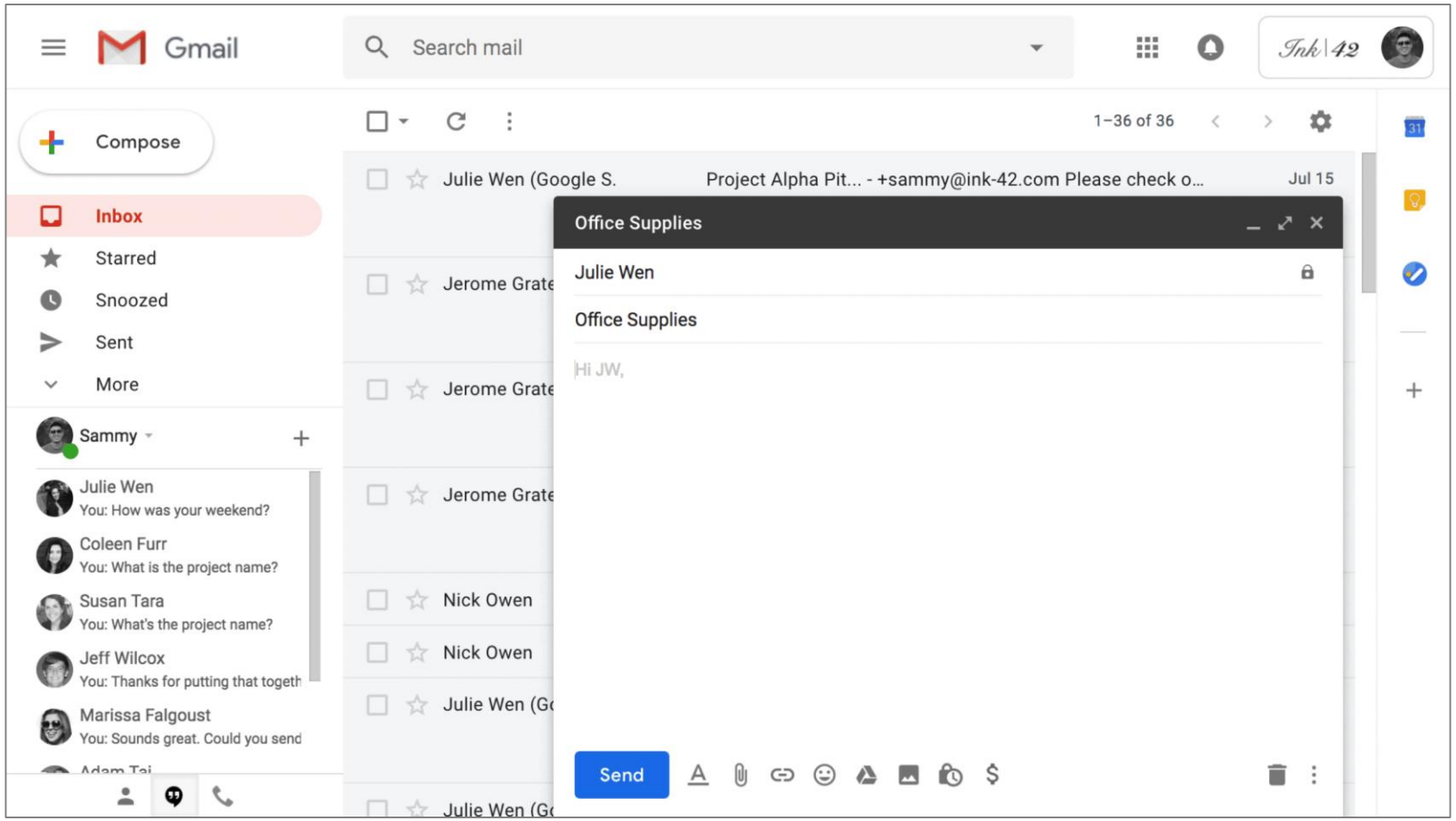
Why Is this Happening Now?



Ref: NVIDIA

Recent AI Advancements

1 - Natural Language Processing



- Supervised learning
- RNN Language Modeling (LM) architecture
  - Predict next word in a sequence, within conversation context
- Model capacity for 1.4+ billion users
  - Make tailored suggestions
- 100ms response time
  - Running on TPU2

Recent AI Advancements

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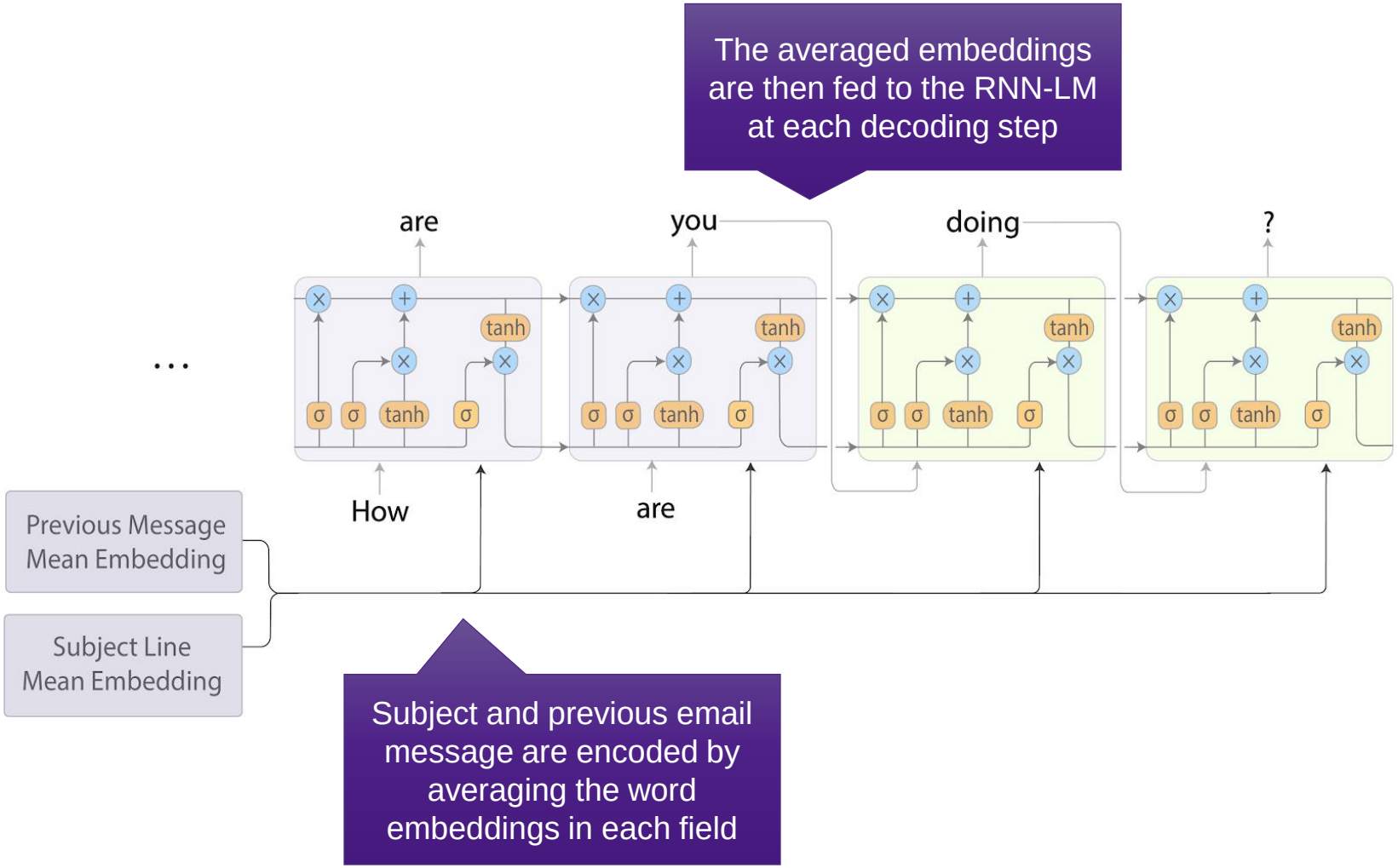

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Recent AI Advancements

2 - Generative Adversarial Networks

Which Face is Real?

https://skymind.ai/wiki/generative-adversarial-network-gan

- Unsupervised learning
- 2 neural nets competing
  - One generates images
  - One attempts to tell the difference
- Each network optimizes a different and opposing objective function
  - Zero-sum game

Recent AI Advancements

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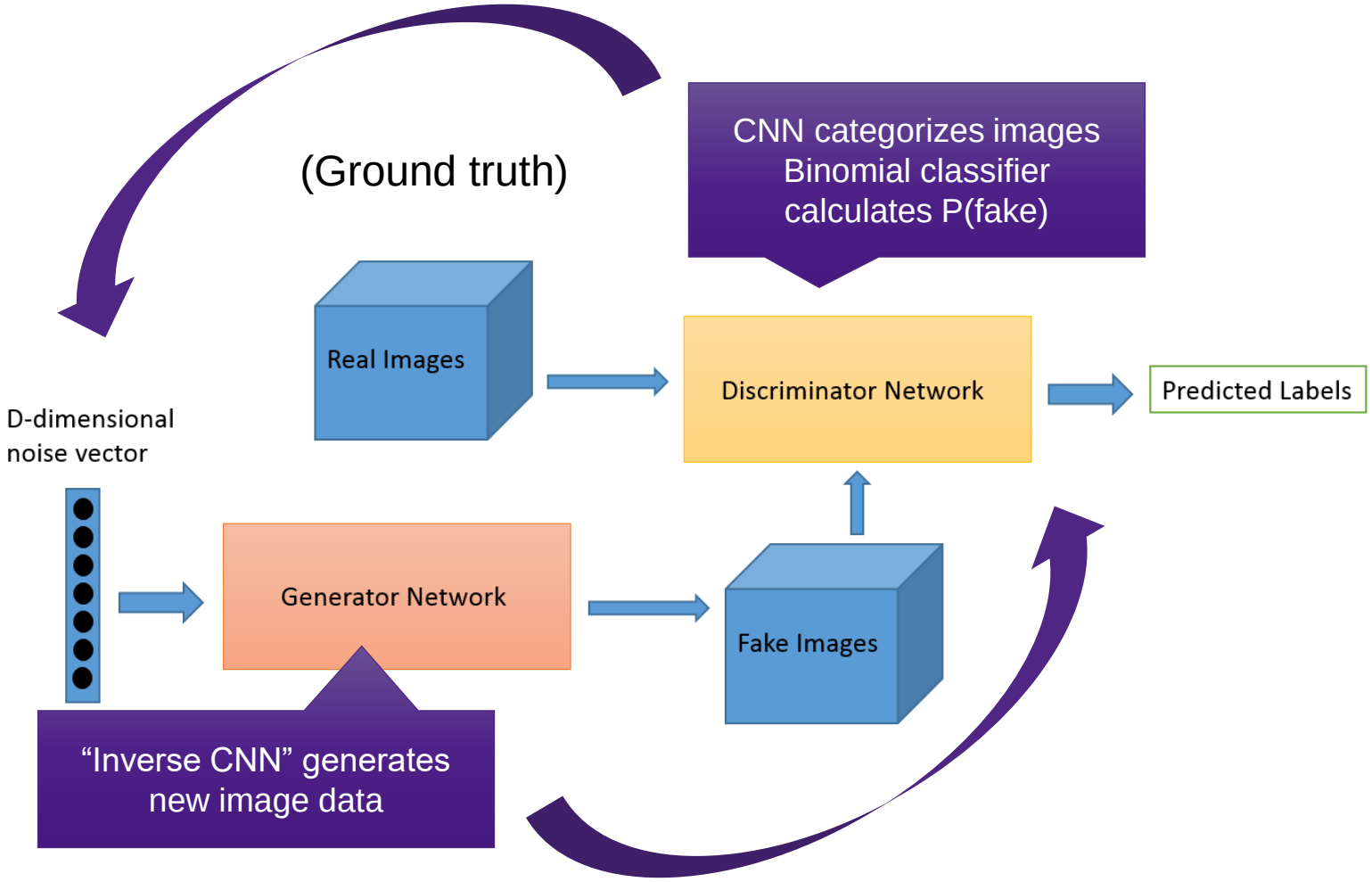

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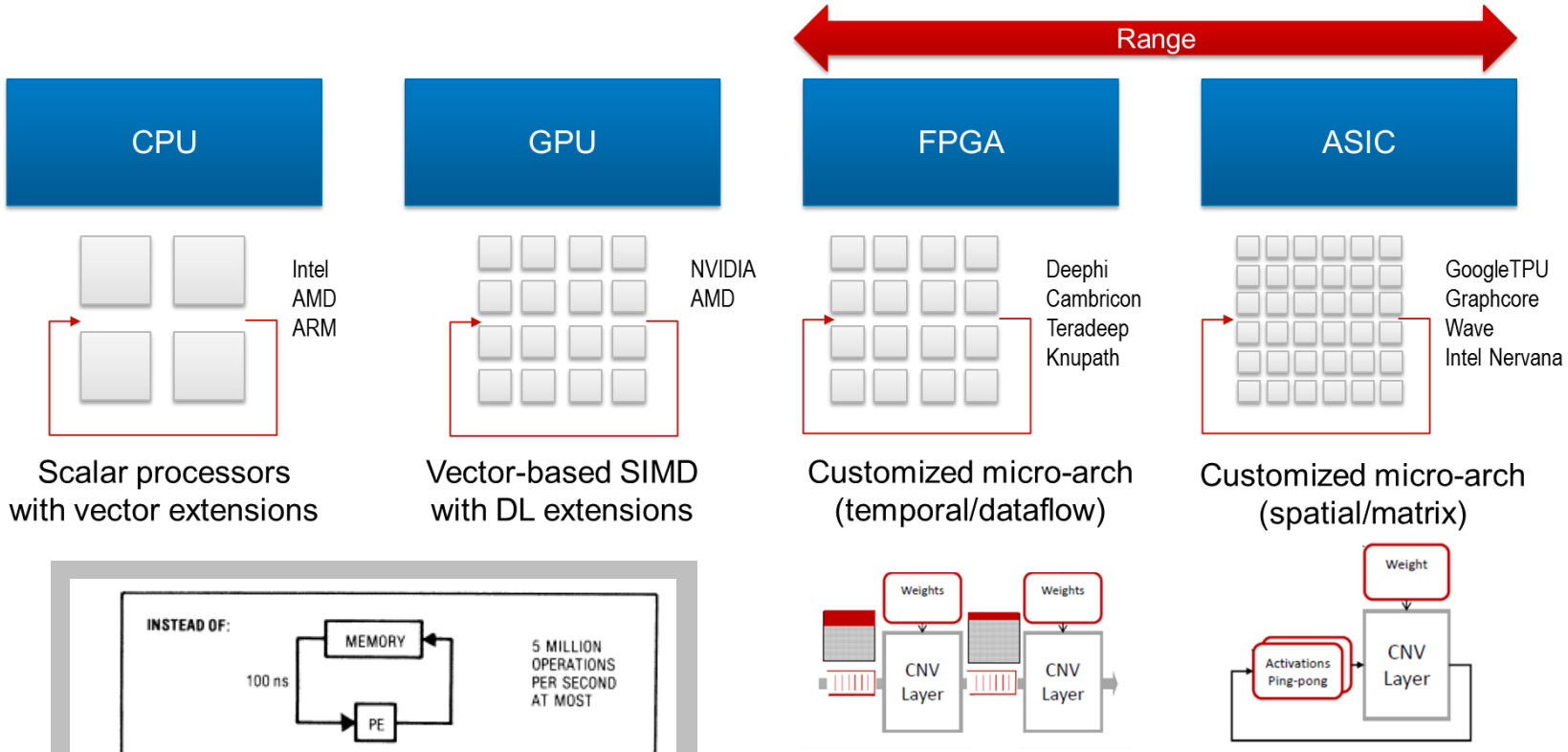
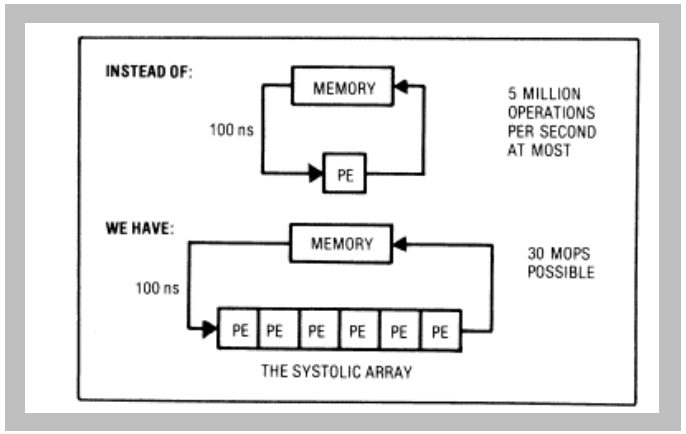
Recent AI Advancements

3 - AI Accelerators

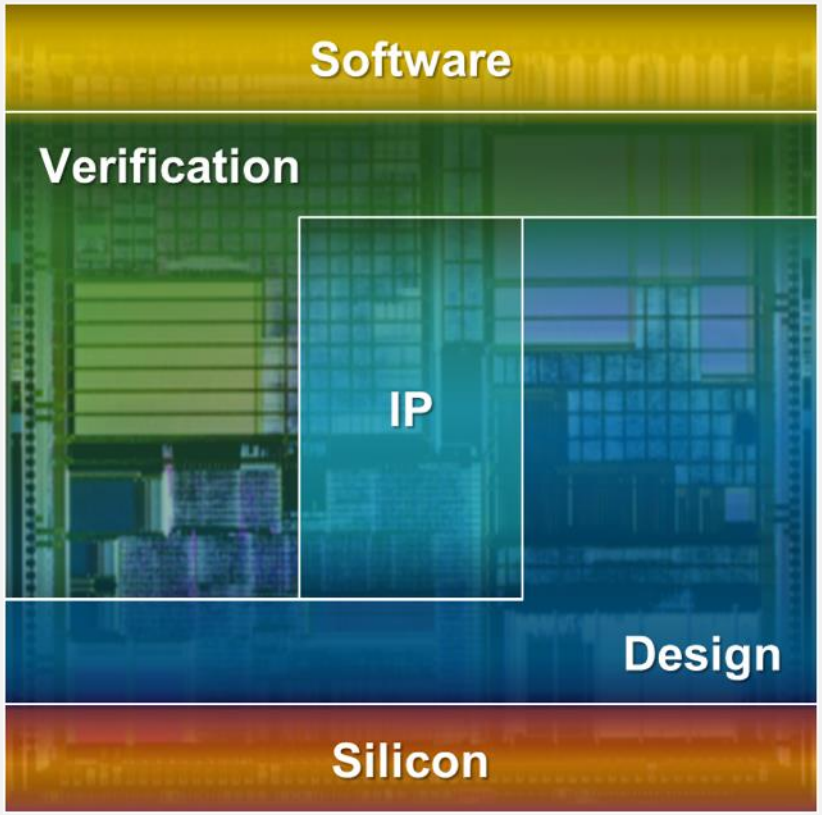




Architectures for Accelerating Deep Neural Networks, Xilinx, Hot Chips 2018

- Data center chips for deep learning training & inference
  - 20B+, 800mm^2 designs
  - Thousands of processing elements @ 100+ TOP/s
- Edge IP (primarily) for deep learning inference
  - Mixed scalar/vector/spatial compute
  - Ultra energy efficient: Several TOP/s/W

Synopsys: Silicon to Software



Software
- Application security testing & quality
- Leader in Gartner's Magic Quadrant

Verification
- Fastest engines & unified platform
- HW/SW verification & early SW bring-up

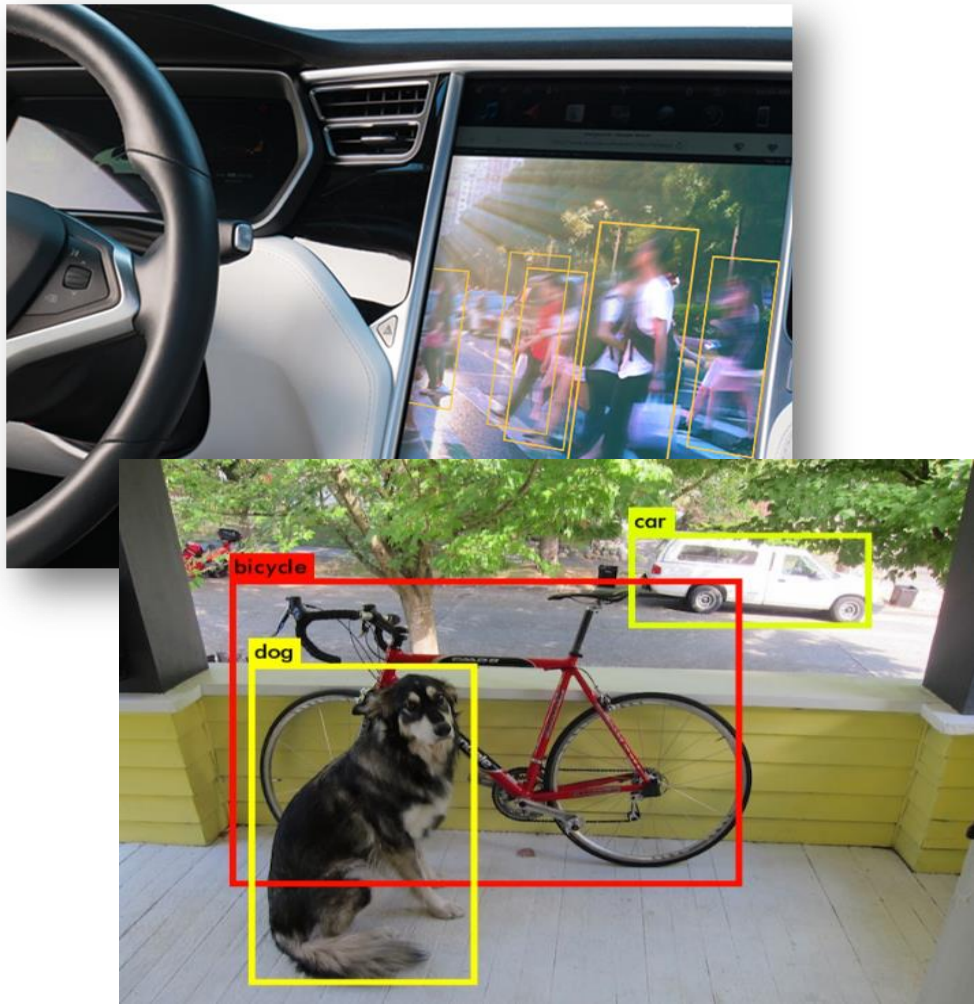
IP
- Broadest portfolio of silicon-proven IP
- #1 interface, analog, embedded mem. & phys. IP

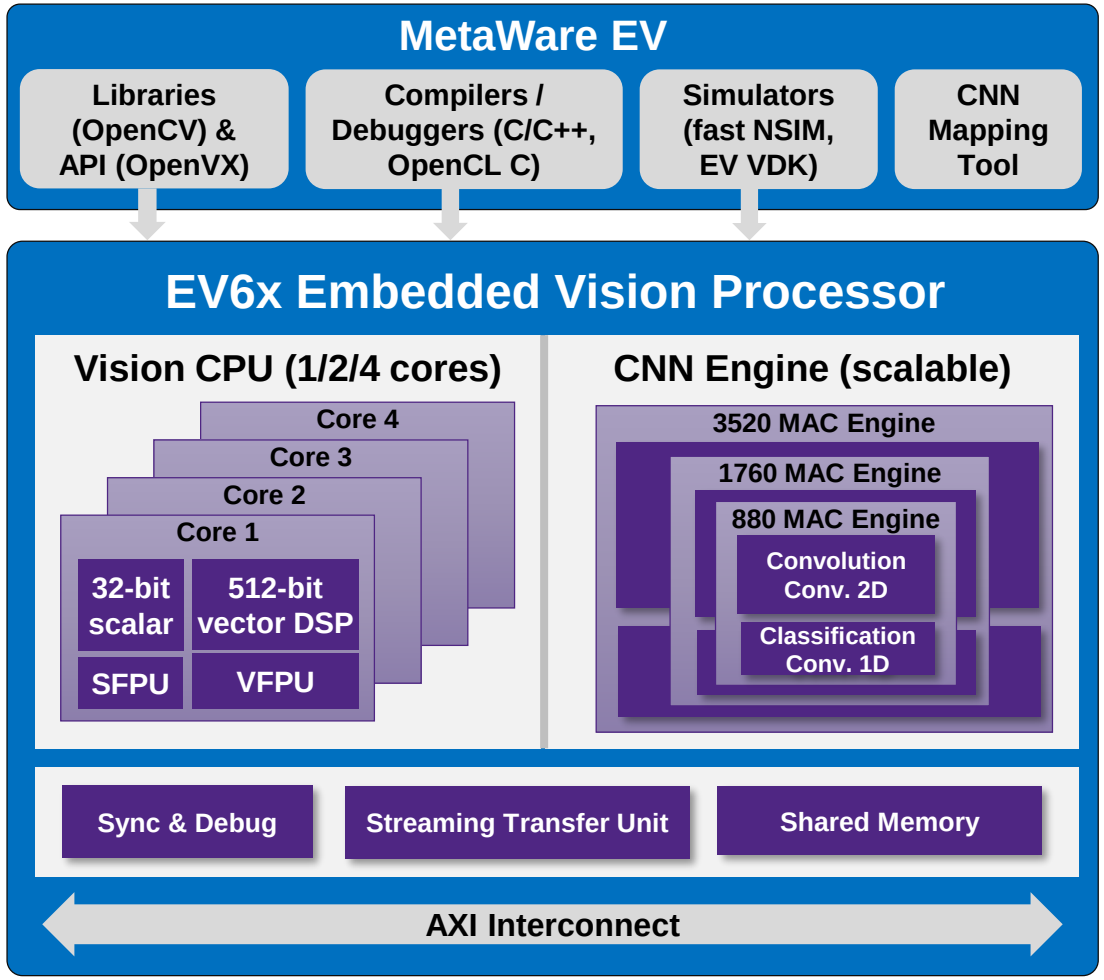
Design
- Digital & custom AMS platforms
- Best quality of results & highest productivity

Silicon
- TCAD, lithography tools & yield optimization
- Down to 5nm & below

On-Device Intelligence: AI Super-chips at the Edge

Example: Synopsys DesignWare EV6x Vision Processor



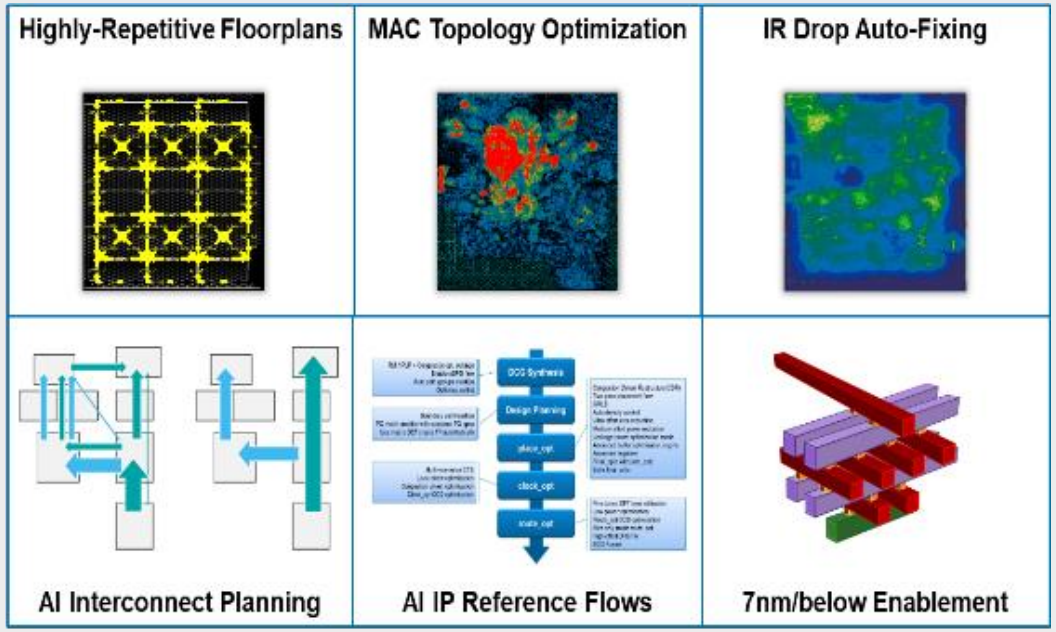


Achieving Best Performance-Power-Area

Intelligent Architectures

Fusion Design Platform

Technologies Enabling the Future of AI Accelerators



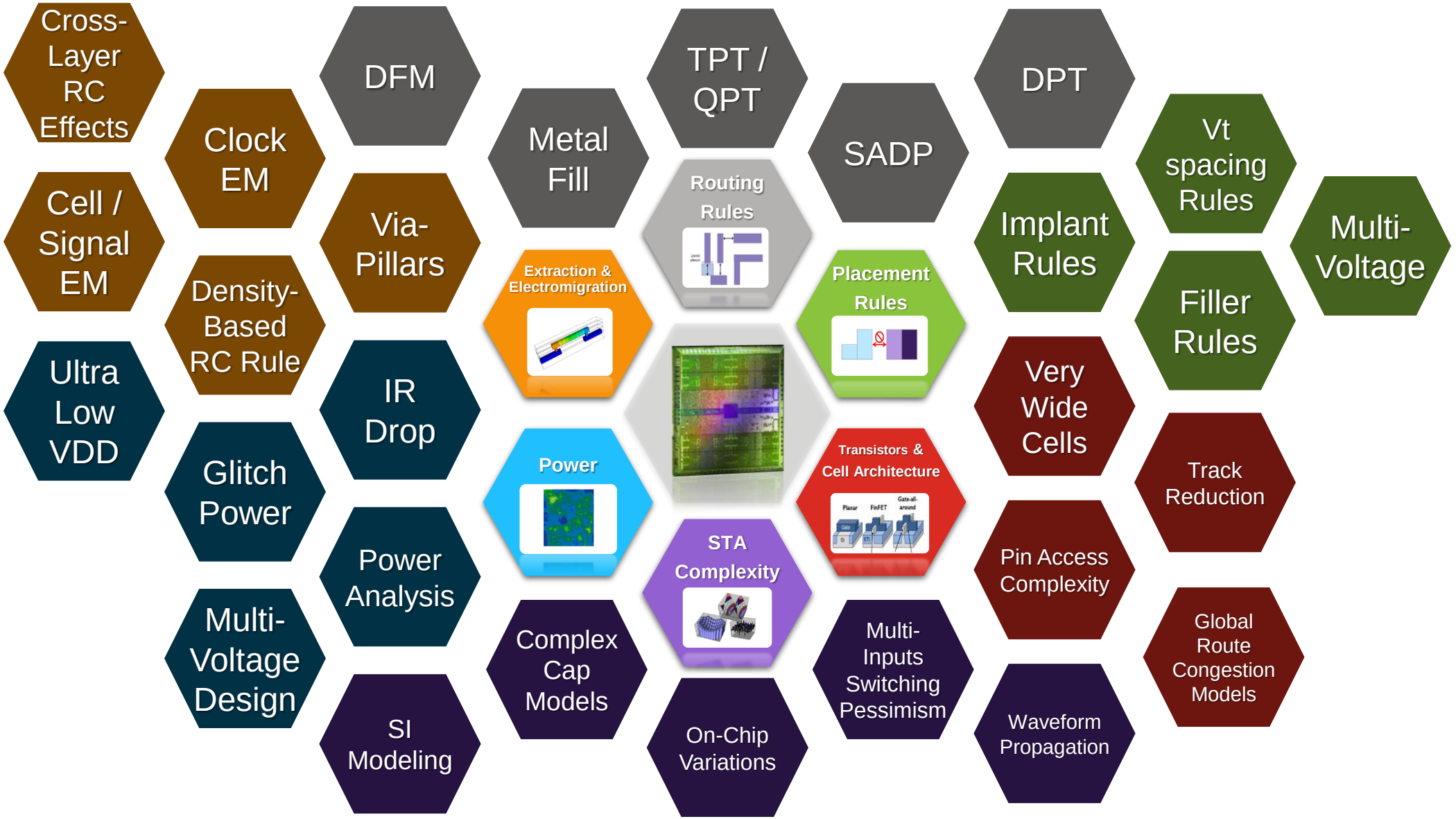
GRAPHCORE

The Synopsys Design Platform with Fusion Technology provides all of the capabilities we need to achieve superior processing performance for artificial intelligence and machine learning.

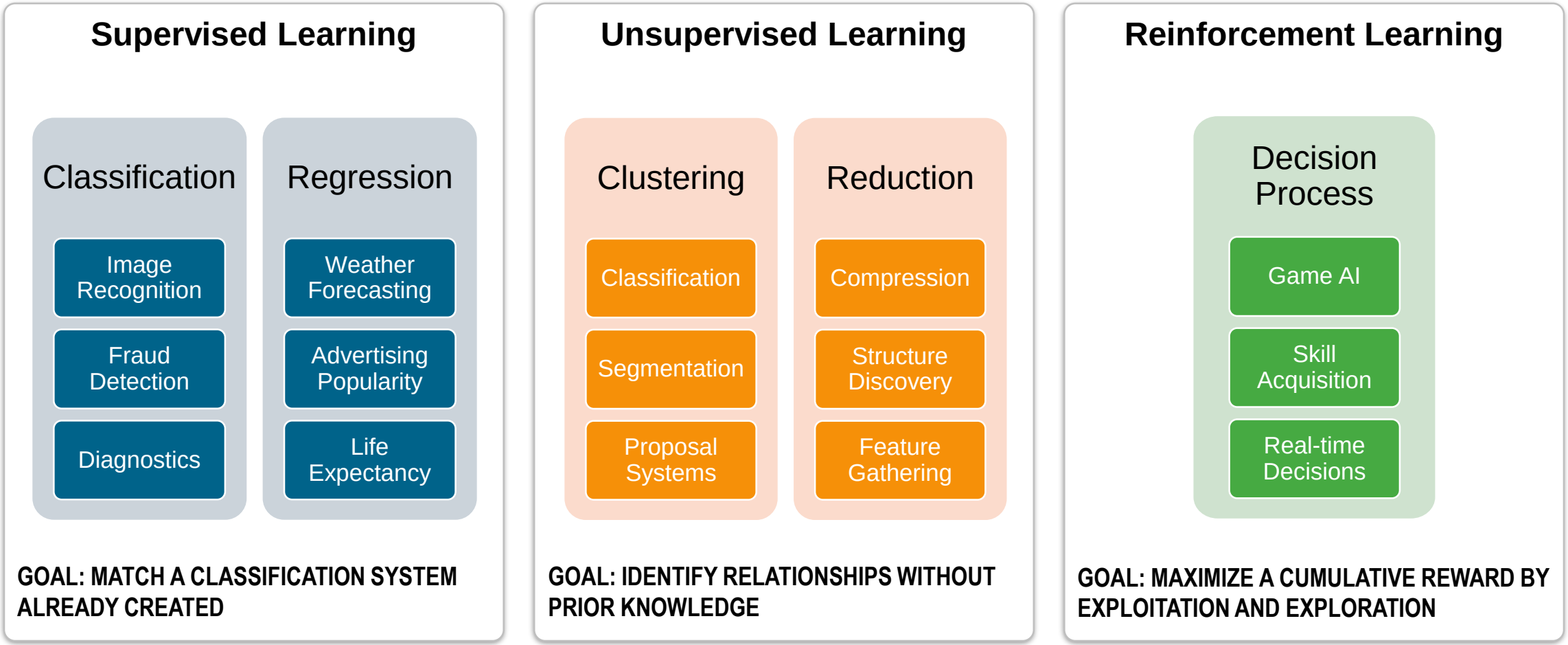
Phil Horsfield
Vice President of Silicon

Synopsys Fusion Technology Enables Superior PPA for AI Chip Design

Today's Design: A Deluge of New Challenges

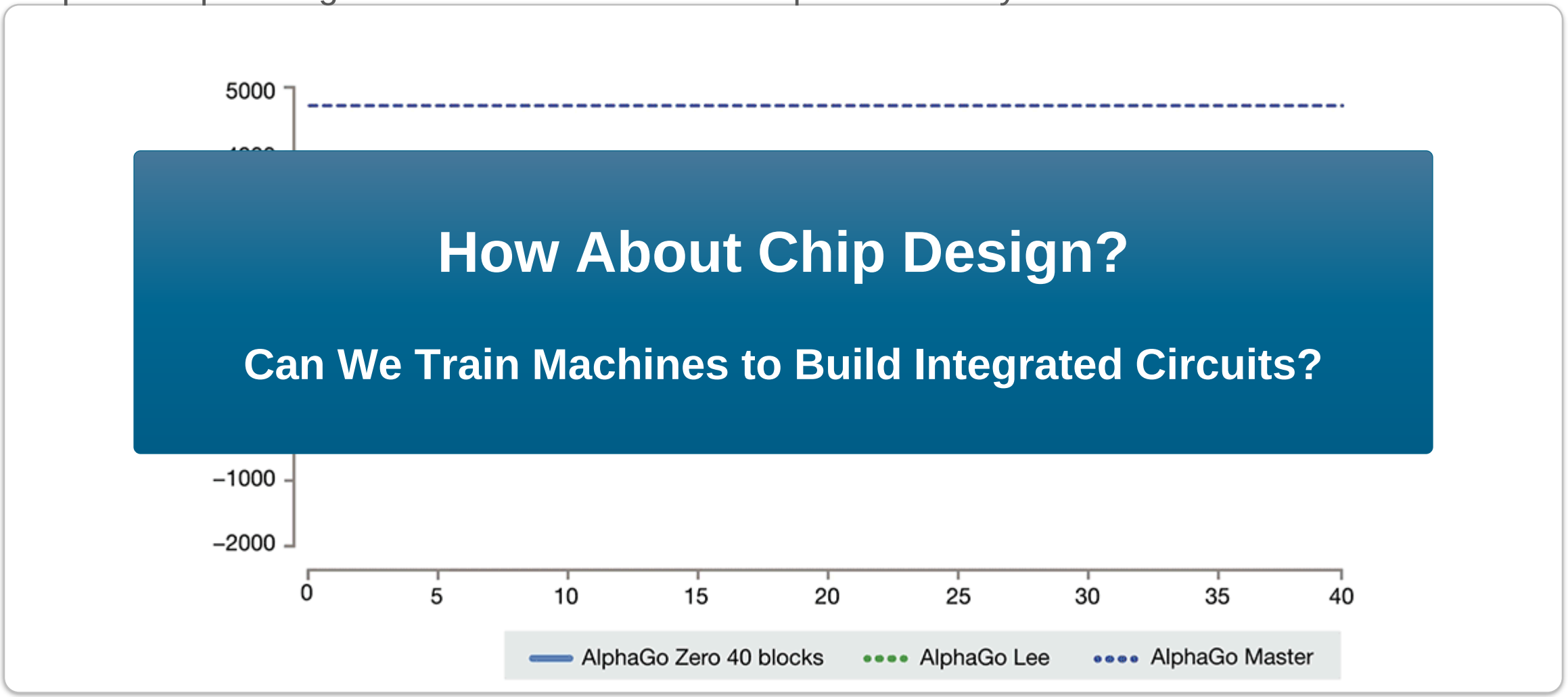


Types of Machine Learning



Learning to play GO

DeepMind AlphaGo goes from zero to world champion in 40 days



Example: https://deepmind.com/blog/alphago-zero-learning-scratch/

Reality Check: Chip Design is a Tough Game to Play

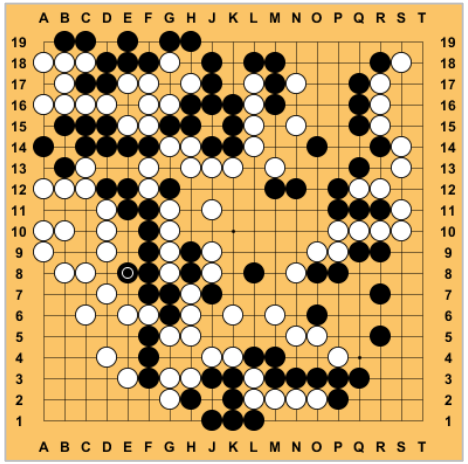
Chess

Number of states ~ 10^{123}

41x '000'

1 quadragin-tillion

Go

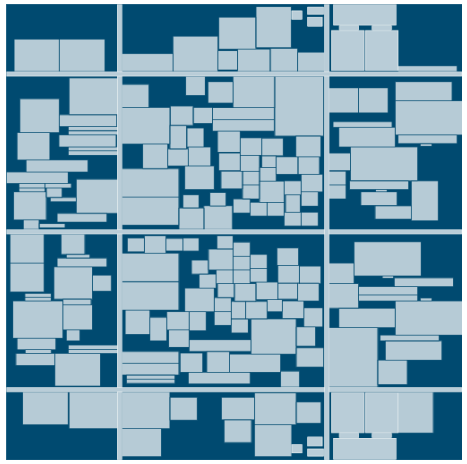


Number of states ~ 10^{360}

120x '000'

1 cen-novem-dec-illion

Placement



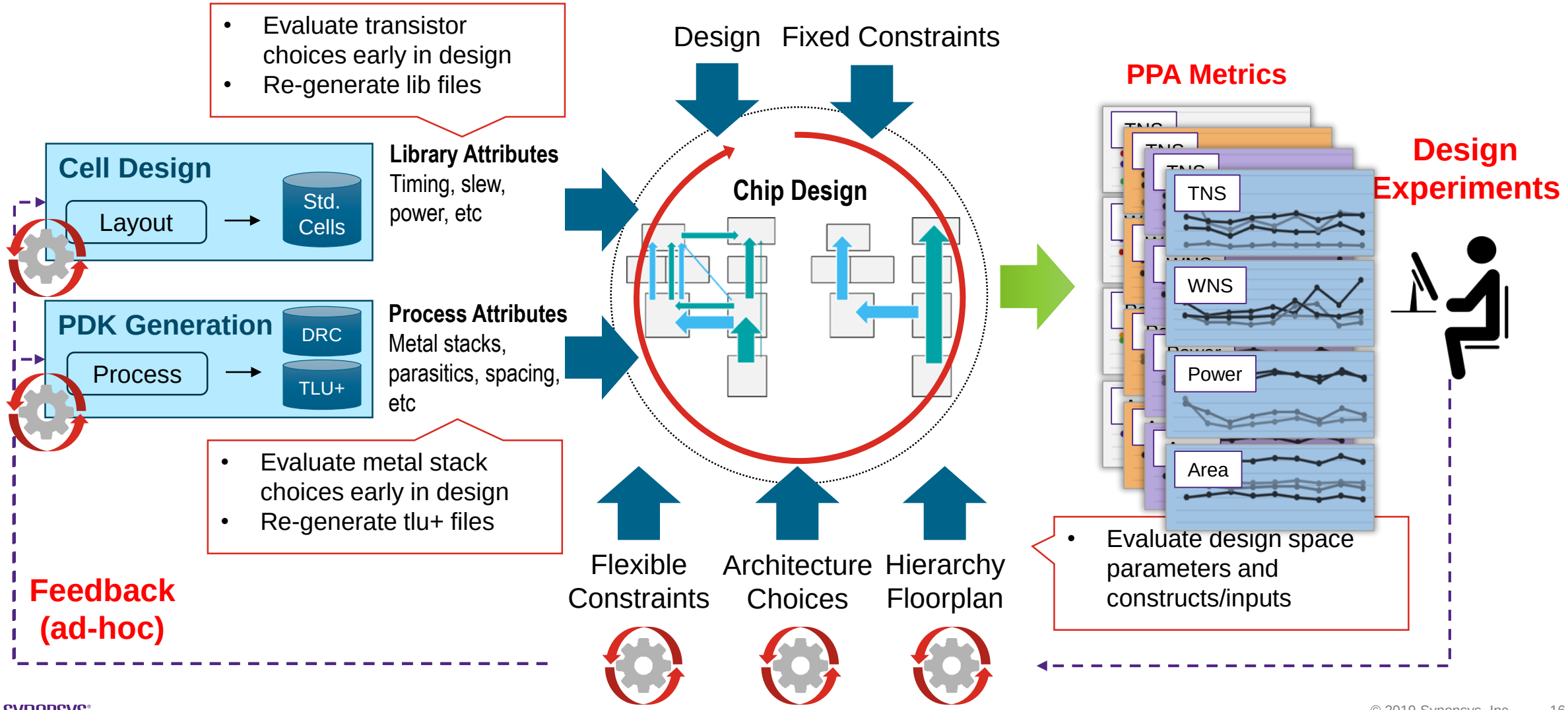
Number of states > $10^{90,000}$

(way too many '000')

1 novem-vigin-millia-nongen-novem-nonagin-tillion

A Closer Look at the Chip Design Process Today

Intelligent design processes

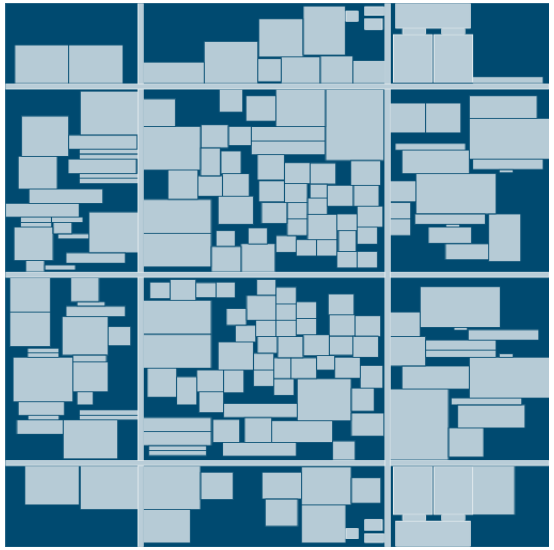


Highly Complex “Intelligent Search” Problems

Clear need to tackle the enormous problem spaces of physical design and verification

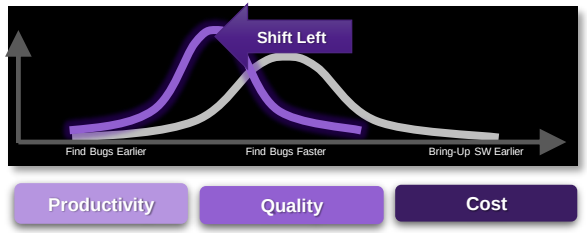
Design: Feasibility

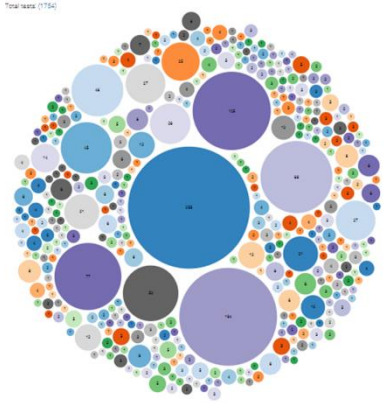
- 1,000s macros, millions of standard cells
- Complex spacing relationships
- Non differentiable response functions
- NP-complete problems



Verification: Shift Left with Exponential Growth

- Enormous volumes of verification data
- No use of results across time and designs
- Unguided and manual processes
- Computationally intractable problems

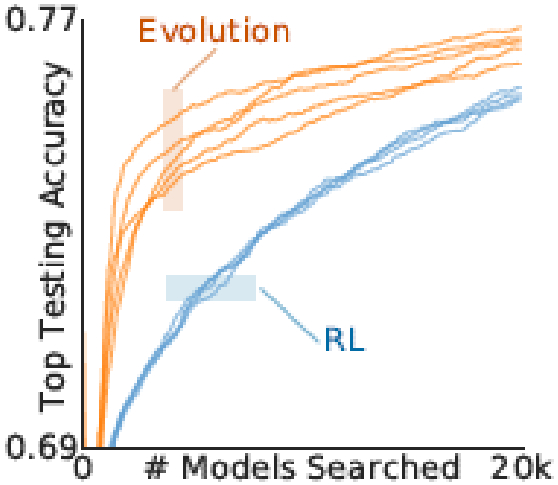




AI Becoming Pretty Good at Search

Recent success outside of EDA paving the way for design and verification innovation

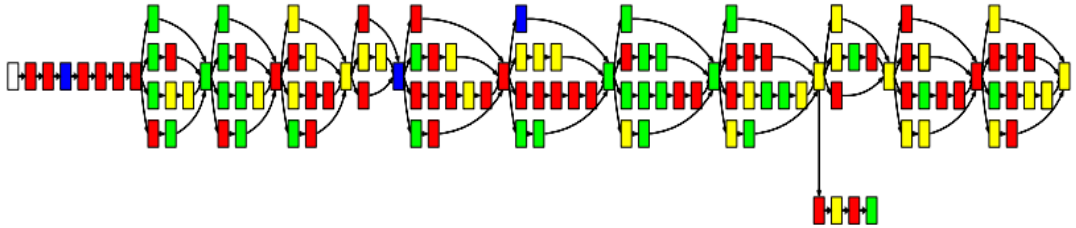
Example: Neural Architecture Search



- Automatically discovers image classifiers
- AmoebaNet-A surpasses hand crafted NNs
- 96.6% (#1) ImageNet accuracy, ~40B FLOPS

Regularized Evolution for Image Classifier Architecture Search
Esteban Real, Alok Aggarwal, Yanping Huang and Quoc V. Le, AAAI 2019, https://arxiv.org/abs/1802.01548v7

Example: Neural Acceleration Search



- Automatically discovers best scheduling for neural network computational graphs
- 20% faster runtime vs. experts, self-trains in hrs

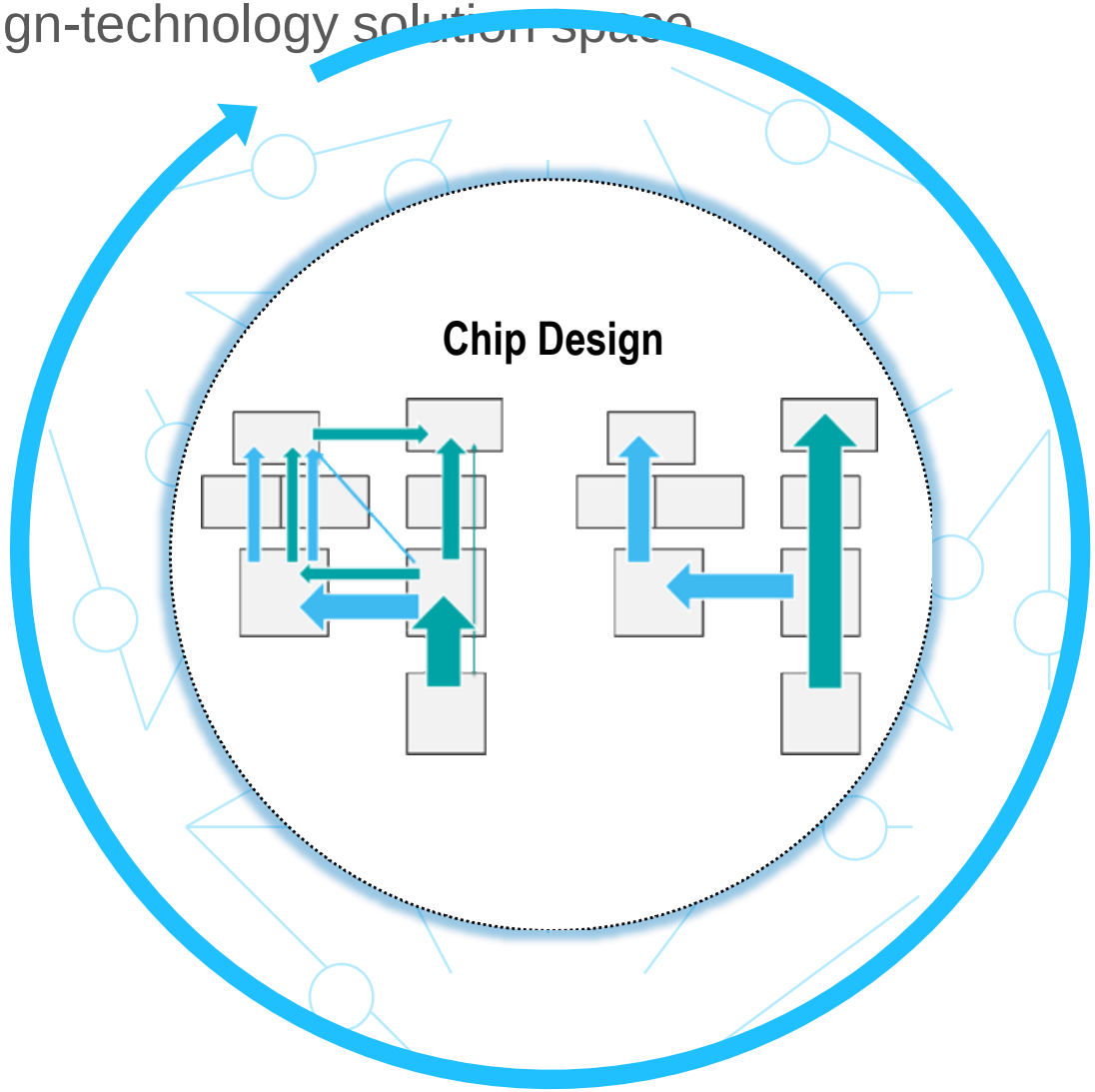
Device Placement Optimization with Reinforcement Learning,
Azalia Mirhoseini, Hieu Pham, Quoc Le, Mohammad Norouzi, Samy Bengio, Benoit Steiner, Yuefeng Zhou, Naveen Kumar, Rasmus Larsen, and Jeff Dean, ICML 2017, arxiv.org/abs/1706.04972

Towa lf-Optimizing Design Processes

Brea esign-technology solution space

Architecture

Flow

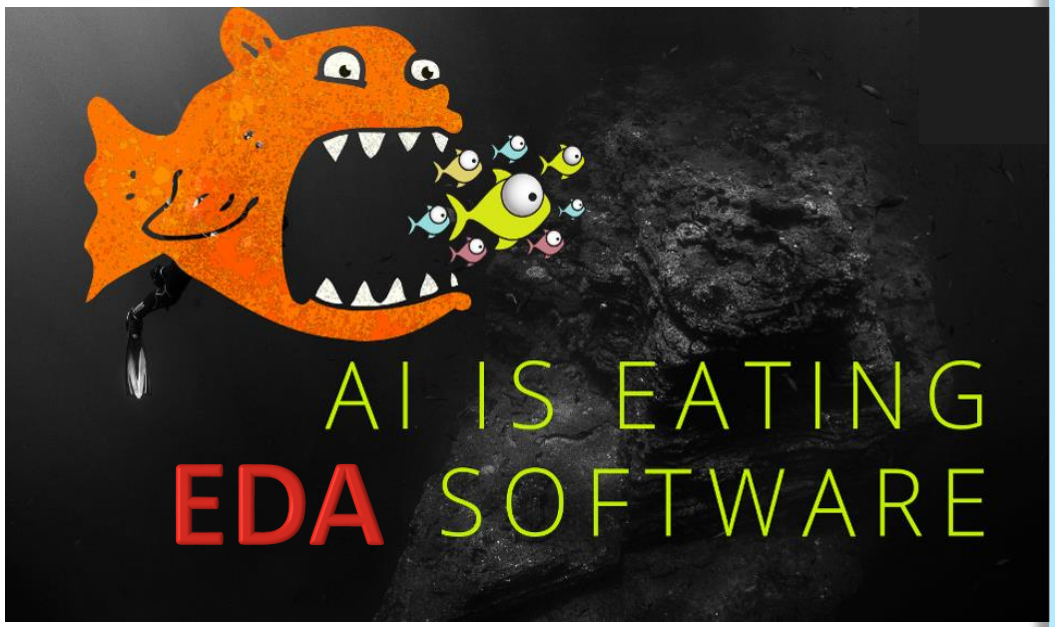


Process

Constraints

Software Has Eaten the World…

Machine-learning is changing the way we think about design automation



As scaling continues, deluge of challenges causing more margin, iterations

Advances in AI technology offering great promise but design is a tough game to play

New breed of AI-enhanced tools breaking silos, enabling novel applications

Strength in numbers!

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Thank You


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