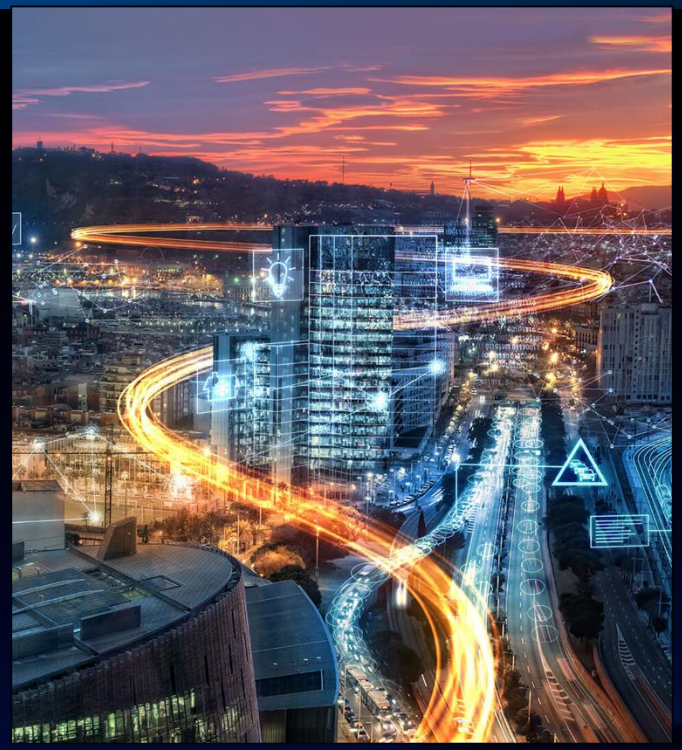


The Impact of AI on Semiconductors and EDA

Joseph Sawicki

Executive Vice President, IC EDA

Mentor, a Siemens Business

Mentor®
A Siemens Business

Artificial Intelligence & Machine Learning Brings Opportunity

"… artificial intelligence will likely be the catalyst that will drive another decade-long growth cycle for the semiconductor sector…

… The semiconductor firms that are able to take the most advantage of this growth and fully realize their market potential will likely be those that harness the possibilities that AI brings."

Source: PWC, Opportunities for the Global Semiconductor Market, April 3, 2019

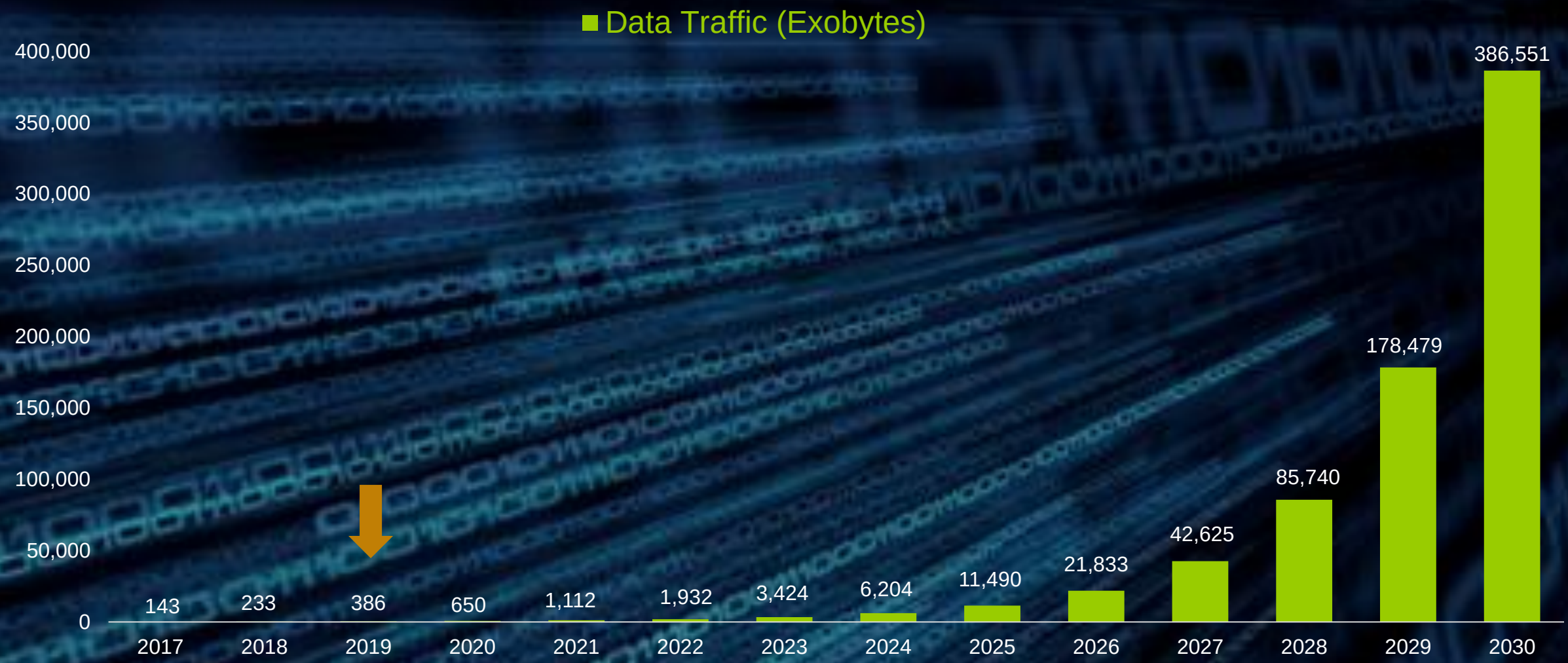
Artificial Intelligence & Machine Learning Brings Opportunity

"Artificial Intelligence is opening the best opportunities for semiconductor companies in decades …

… AI could allow semiconductor companies to capture 40-50% of total value from the technology stack"

Source: McKinsey & Company, "Artificial-Intelligence Hardware: New Opportunities for Semiconductor Companies", December 2018

Exponential Increase in High-Speed Data Communications



Source: IBS Research

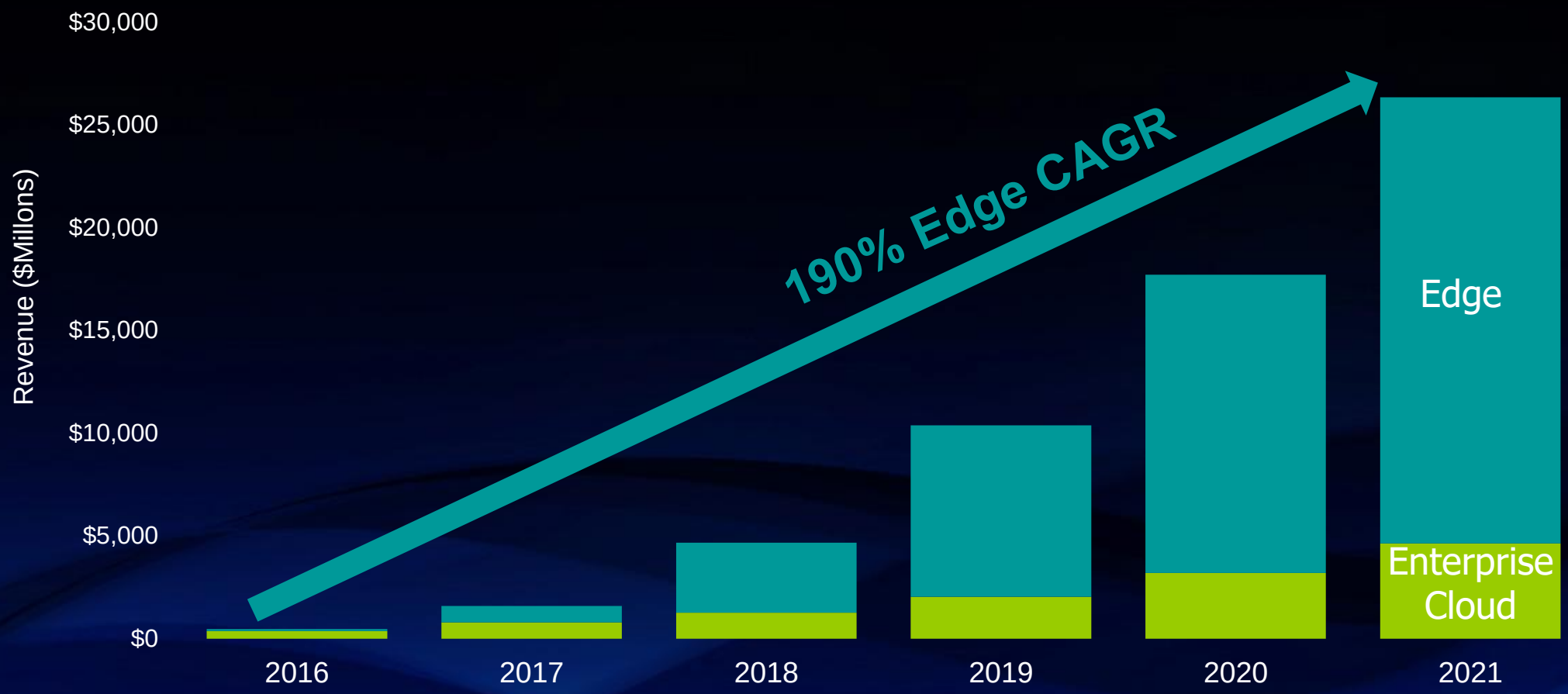
“Two seemingly opposite goals are propelling AI…

One goal is to strengthen the brute-force capacity of data centers…

The other goal is to push more processing toward the edge”

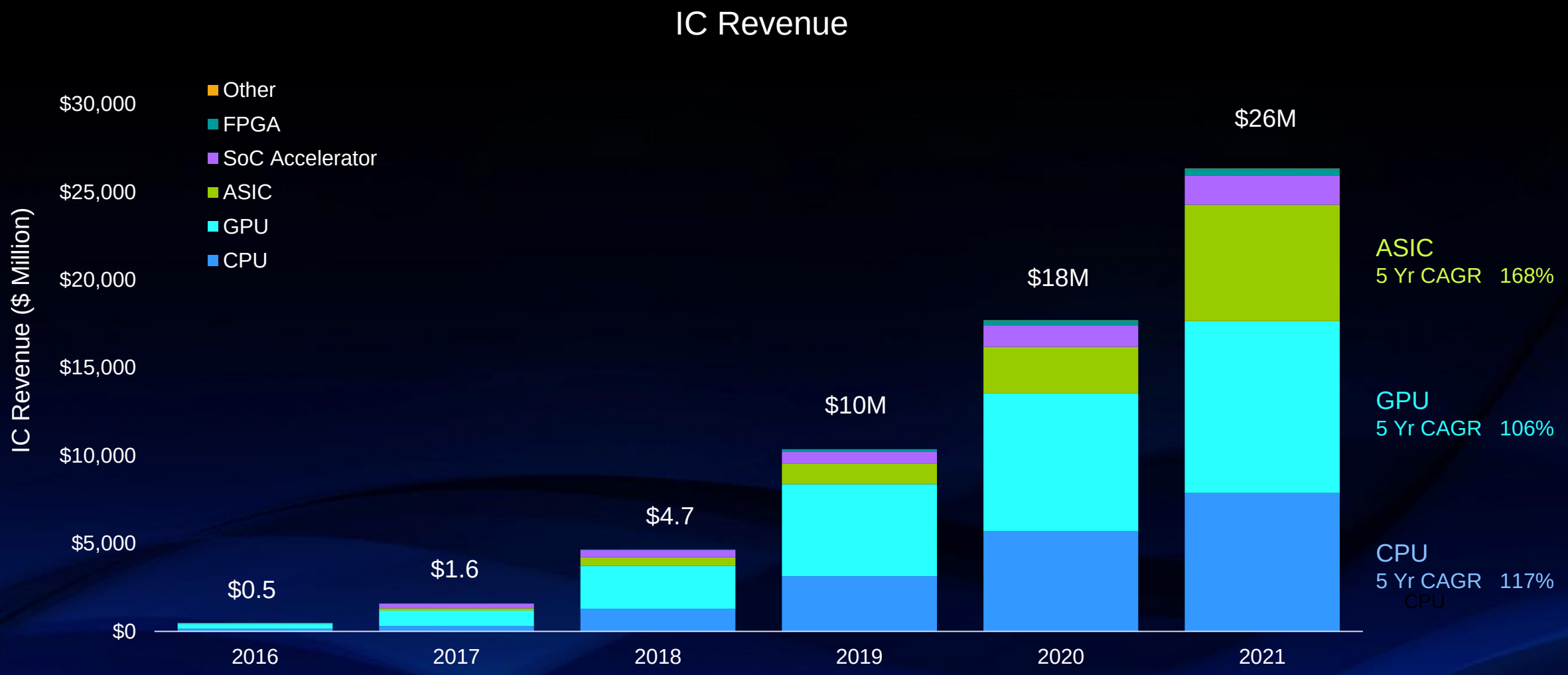
Microprocessor Report, December 31, 2018

AI/ML Chipset Market Growing at Triple Digits, Dominated by Edge Devices



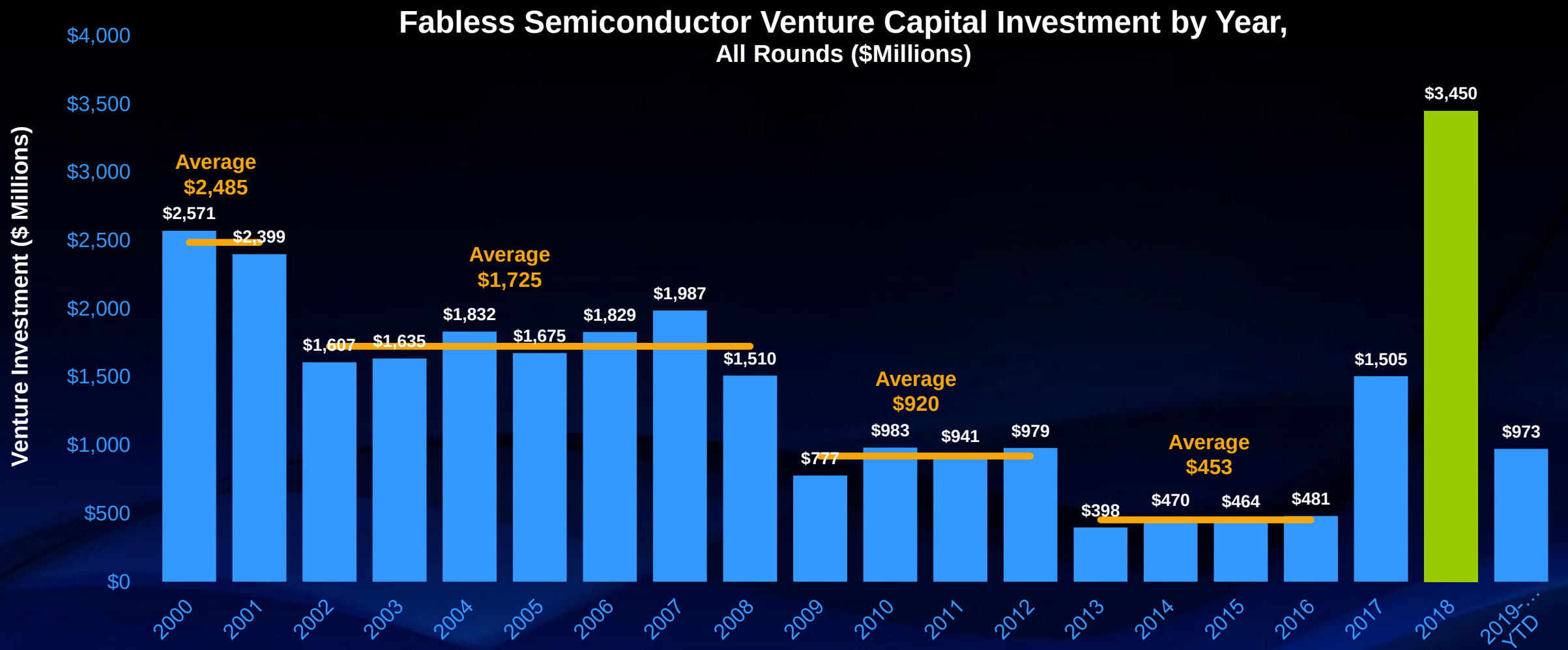
Source: Tractica, "Deep Learning Chipsets"

GPU's Will Remain the Largest Sector Through 2021,
ASIC's are Fastest Growing Major Sector



Source: Tractica, "Deep Learning Chipsets" 2Q 2018

Venture Capital Investment in Fabless Semiconductor Startups



Source: Global Semiconductor Alliance (GSA) , IMF, VentureSource, Pitchbook, Crunchbase, & Mentor Graphics Analysis Rev 05/06/19

Mentor® A Siemens Business

Startups Dominated by Domain Specific Architectures

Worldwide Fabless Company Venture Capital Funding (Rounds 1-3)

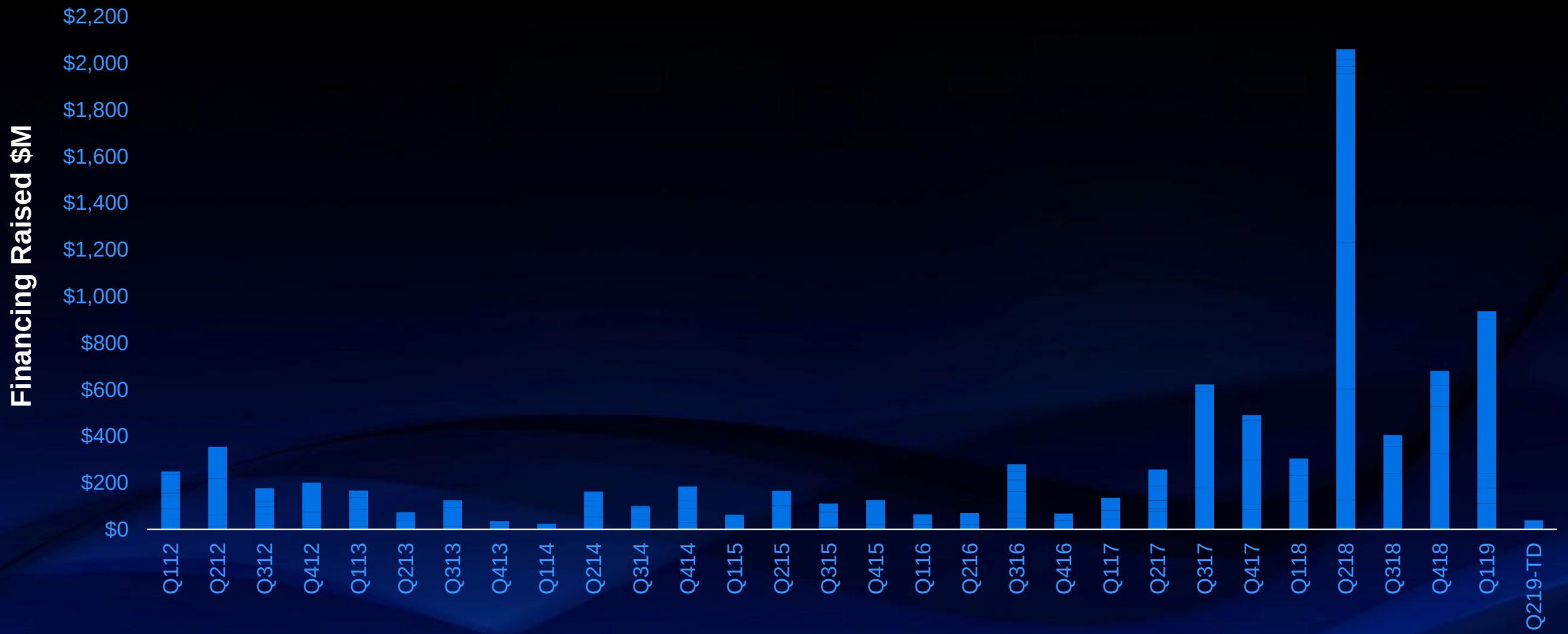
Market Segments Funded 2012 – 2019 YTD

By Funding Dollars ($M)

Source: Global Semiconductor Alliance (GSA) , VentureSource , PitchBook & Mentor Graphics Analysis
Revised 5/6/19

Mentor® A Siemens Business

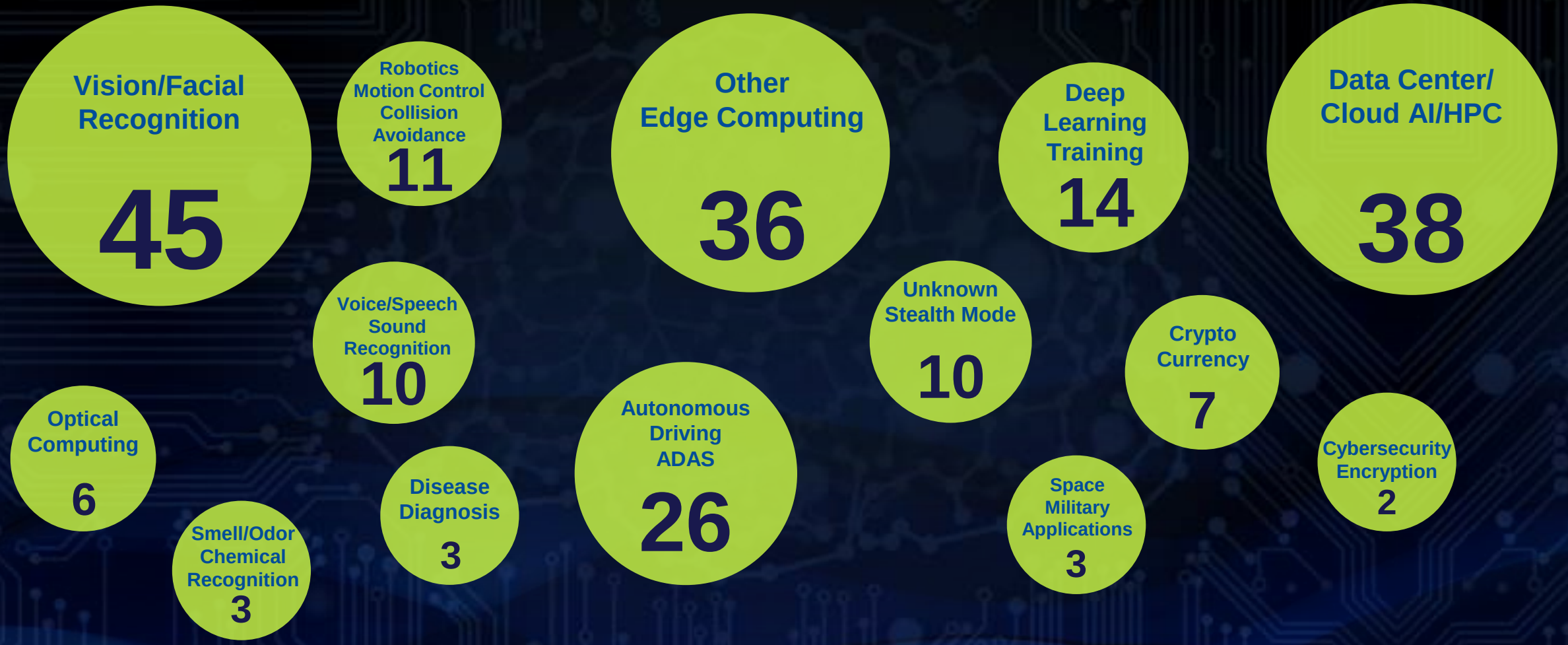
Fabless AI Companies Received Venture Capital Funding



Source: Global Semiconductor Alliance (GSA) , VentureSource , PitchBook & Mentor Graphics Analysis
Revised 5/6/19

Mentor®
A Siemens Business

Numerous Companies Creating Domain-Specific AI/Deep Learning Chips



Early Round China Fabless Funding Passes the U.S.

Worldwide Fabless Company Venture Capital Rounds (1-3)

Source: Global Semiconductor Alliance (GSA) , VentureSource , PitchBook & Mentor Graphics Analysis
Revised 1/9/19

Mentor®
A Siemens Business

Domain-Specific Architectures Require New Design Methodologies and Tools

Next Level of Abstraction Accelerates Design of AI/Machine Learning ICs

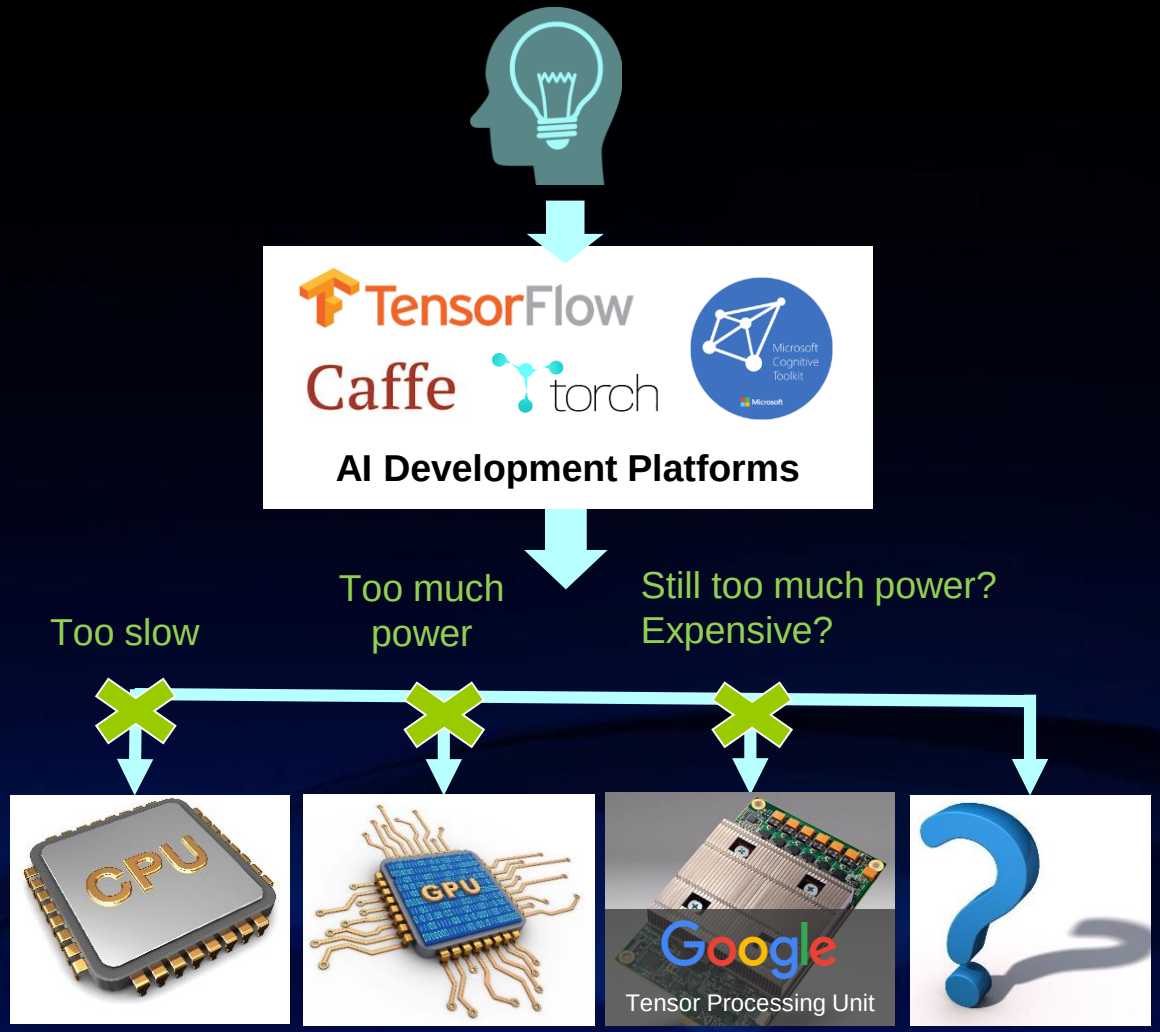
Market drivers for high-level synthesis

- Reduces time to market with good QofR
- Supports FPGA prototype and SoC/ASIC
- Enables Architectural Exploration
- Reduces verification and debug cost/time

Computer Vision and Neural Computing	High Bandwidth and Cellular Comm	Image Processing, Compression and Video
		

AI/ML Applications at the Edge

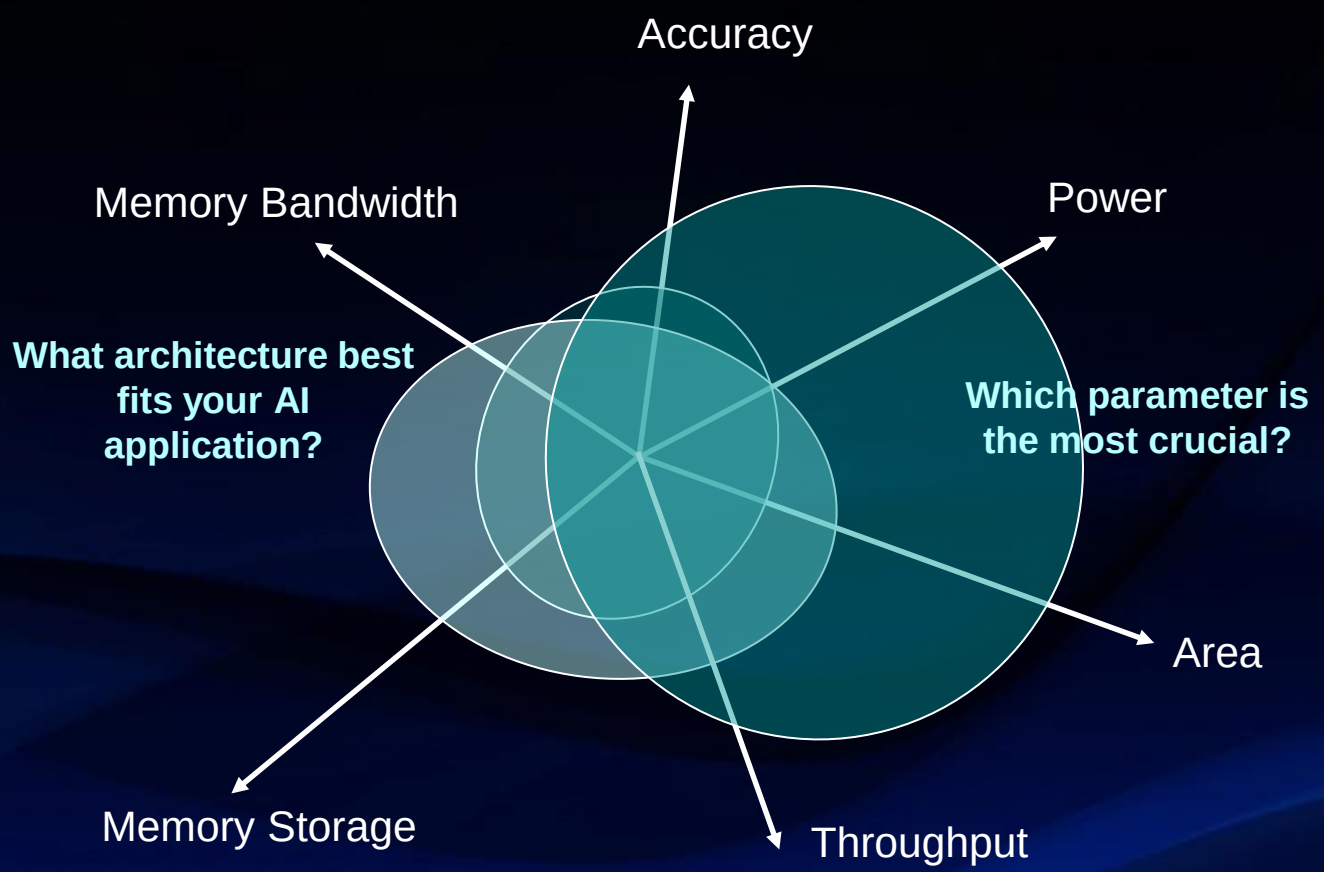
From Idea to Implementation Can Be Challenging



- Edge ML Applications - critical requirements for performance and power
- CPU/GPU – too slow/too much power
- Even generic ML accelerator solutions will not be optimal for all networks **especially for power**
- **Should you build your own? What architecture is best?**

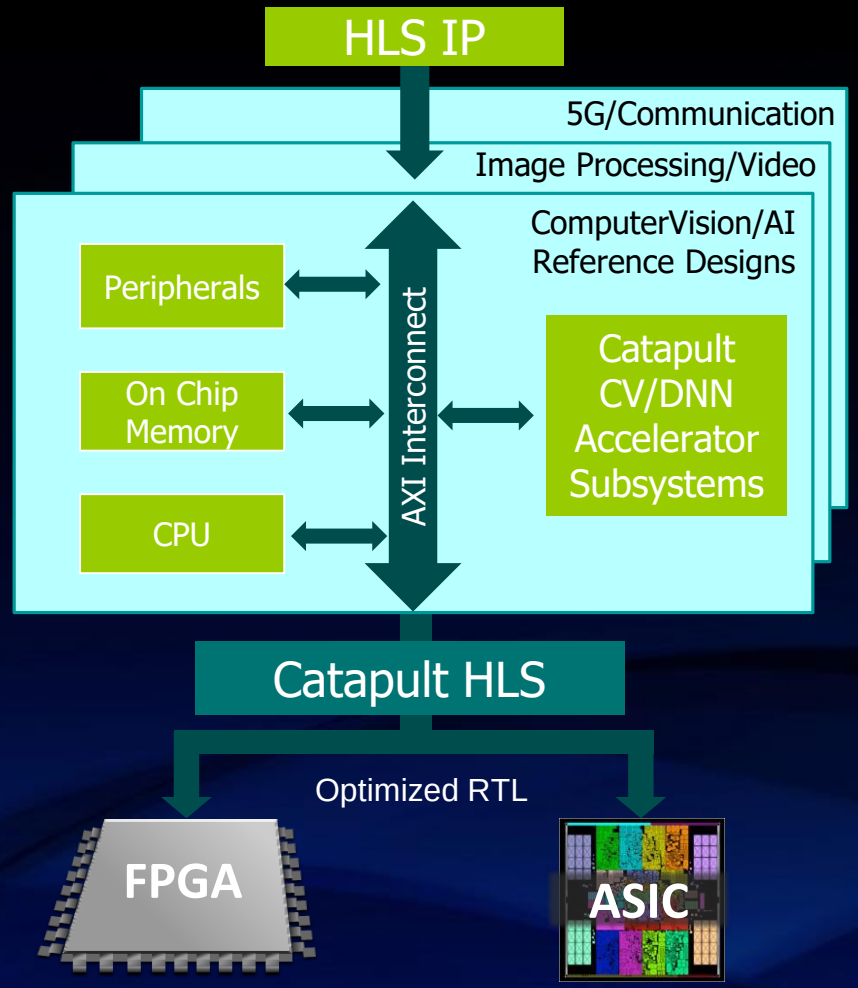
HLS Enables Fastest Path to Build Optimized AI/ML Accelerators for Edge Applications

- HLS enables architecture exploration critical for ML especially around memory
  - Find right power performance
- Delivers high-performance FPGA demonstrator
- Delivers power, performance and area for ASIC IP

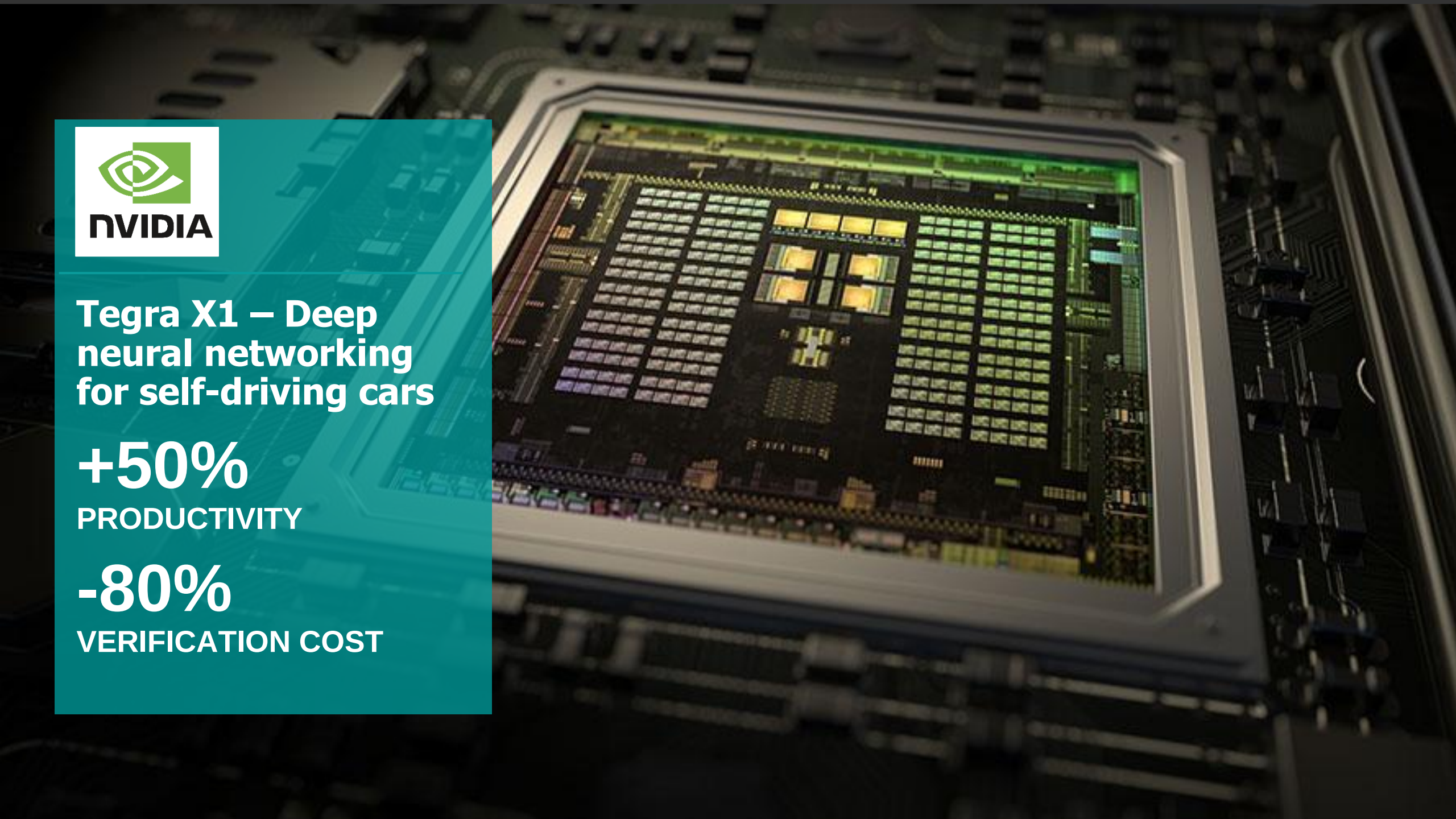


New Catapult HLS Toolkits

Jumpstart Building Low-Power AI/ML Accelerators



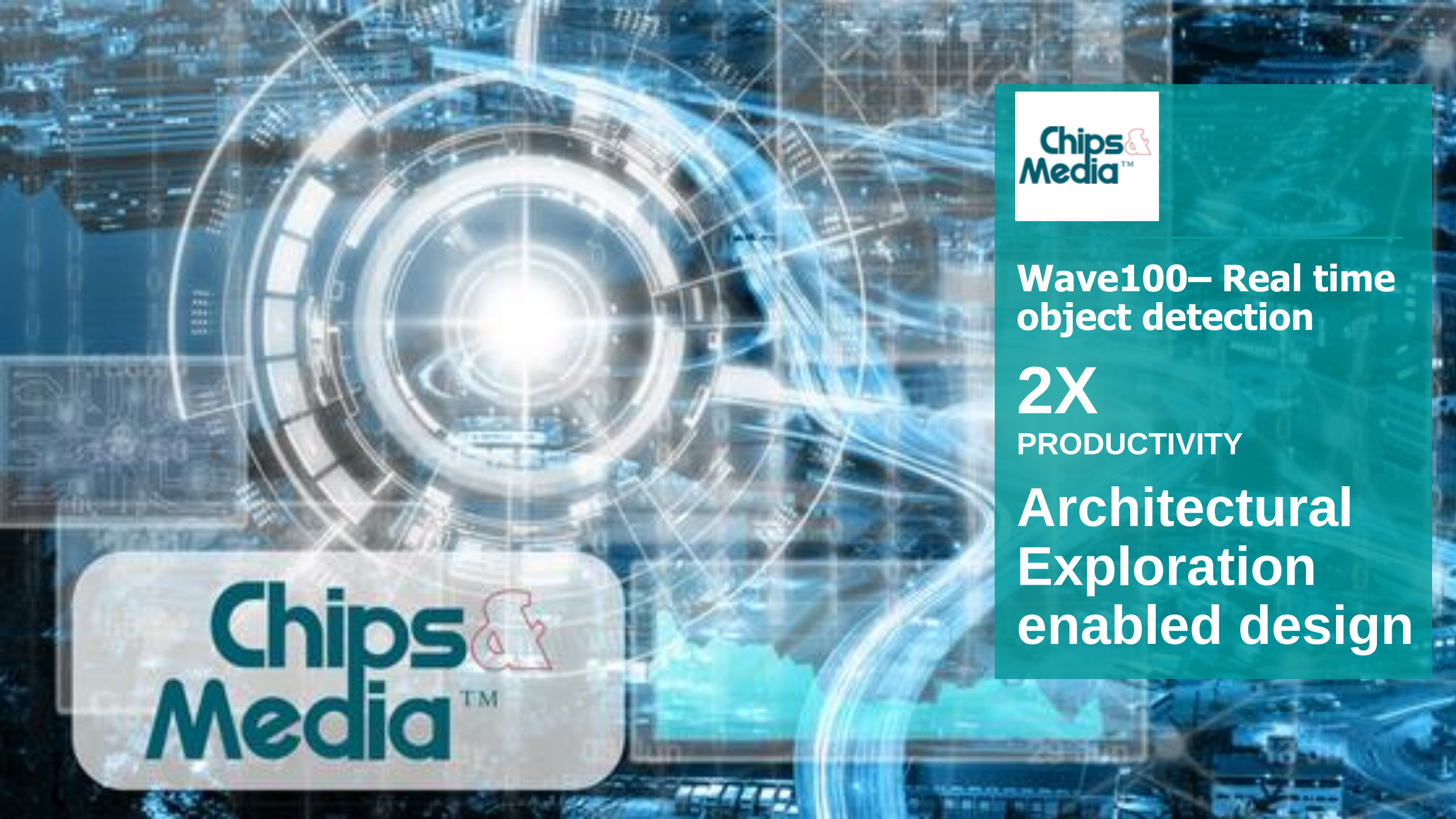
- Quality, working reference designs in vertical applications
- Four AI/Vision Toolkit designs available
  - Edge detection from HOG line-buffer architecture
  - 2-D convolution engine reconfigurable PE Array
  - 9 layer CNN full custom fused architecture
  - 9 layer CNN reconfigurable Eyeriss PE Array
- Includes FPGA demonstrator
- Platform includes CPU subsystem, HW/SW interface and HLS accelerator example for system integration



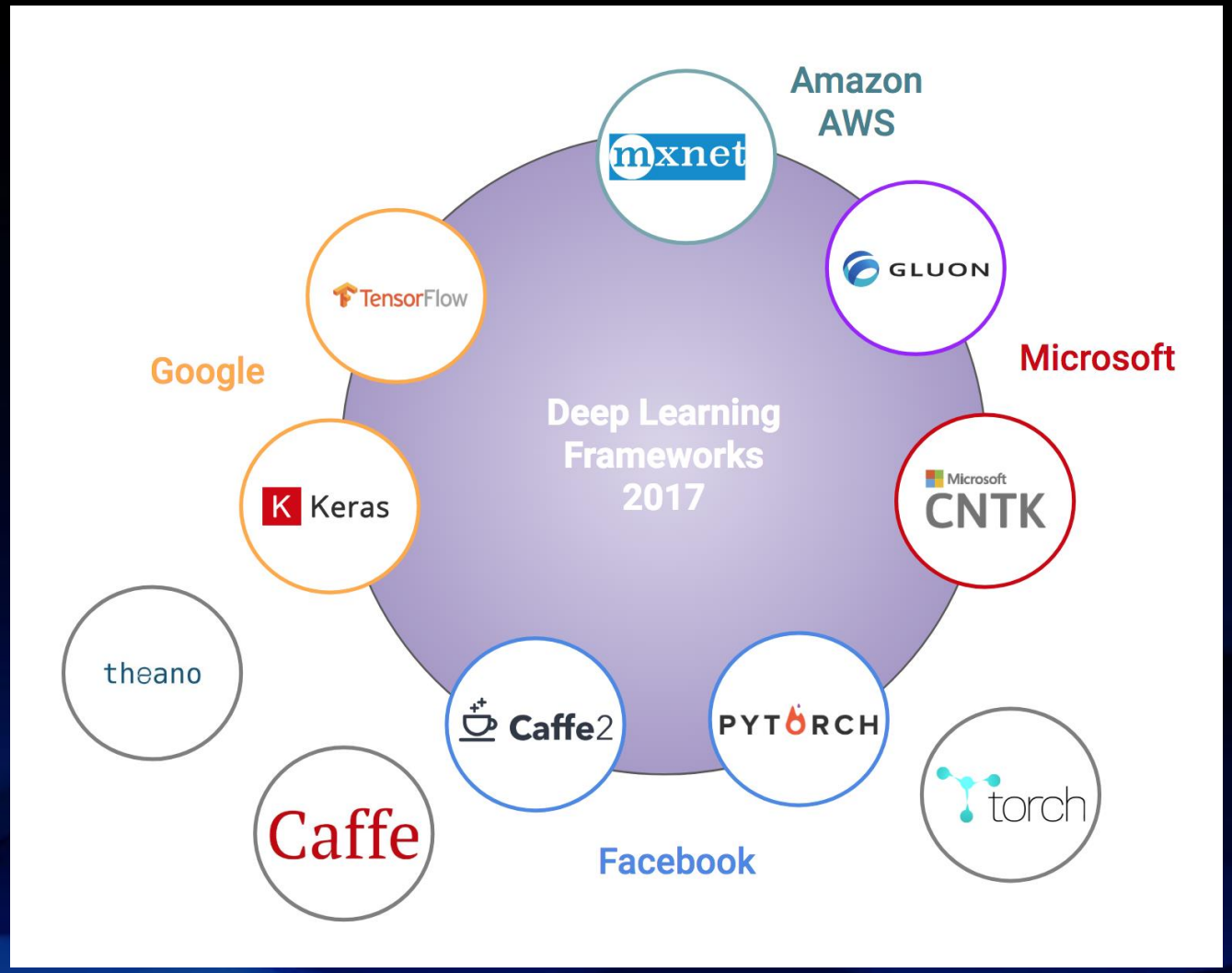
Tegra X1 – Deep neural networking for self-driving cars

+50%
PRODUCTIVITY

-80%
VERIFICATION COST


Chips & Media™
Wave100– Real time object detection
2X
PRODUCTIVITY
Architectural Exploration enabled design
Chips & Media™

AI/ML/DL Designs Need to Run Frameworks to Collect Benchmark Results



MLPerf

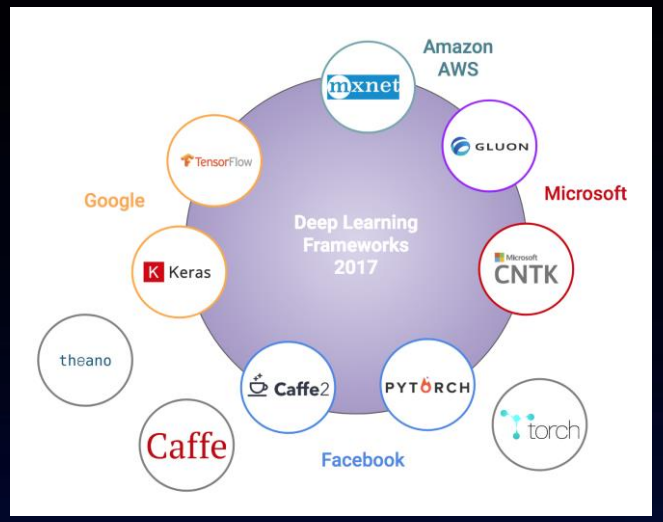
A broad ML benchmark suite for measuring performance of ML software frameworks, ML hardware accelerators, and ML cloud platforms.

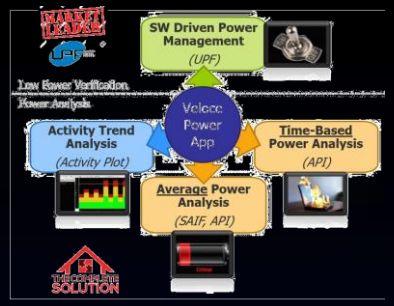
DAWNBench

An End-to-End Deep Learning Benchmark and Competition

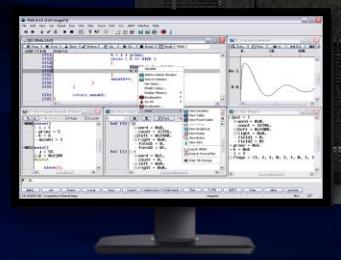
STANFORD DAWN

Emulation Virtualization: AI/ML/DL Frameworks under Performance Benchmarks

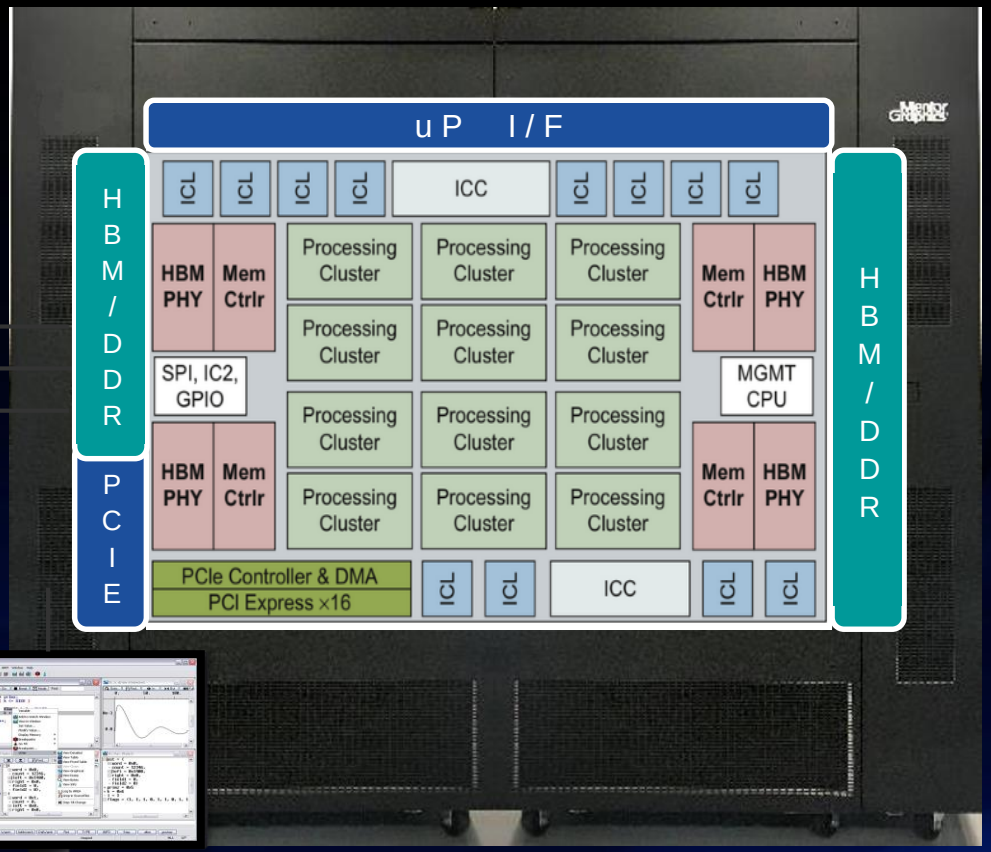




Comodel Host(s)



SW Debug



MLPerf

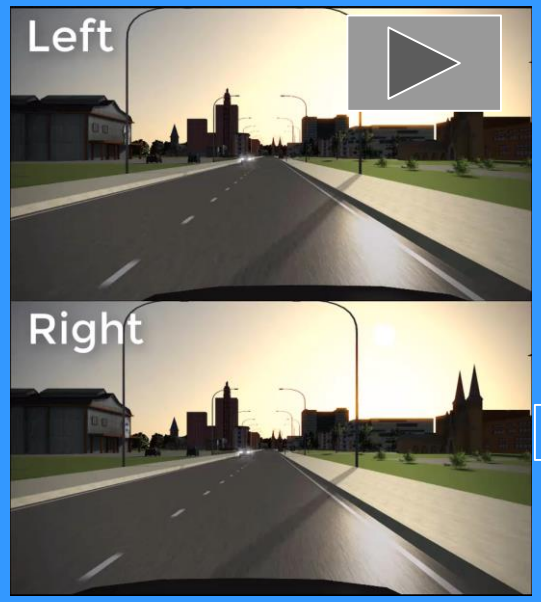
DAWNBench

Applications: Power, DFT, Fault, Coverage
VirtuaLAB and VTL protocols
Enable Performance Benchmarks like MLPerf and DAWNBENCH

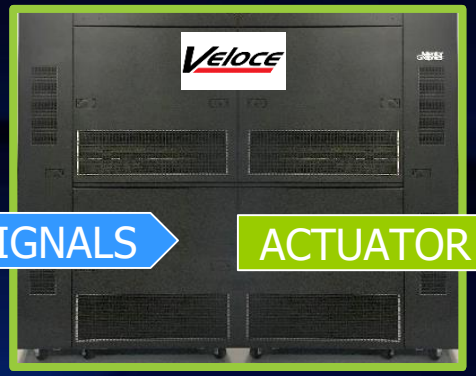
Both Electrical and Mechanical Must Be Verified Virtually

Simcenter Prescan

ACCIDENT DATABASE



AUTO DYNAMIC STATE

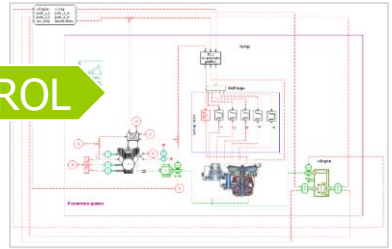


SENSOR SIGNALS

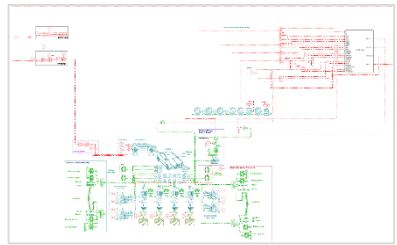
ACTUATOR CONTROL

Simcenter Amesim

Powertrain model



Chassis model



Mentor®
A Siemens Business

Mentor®

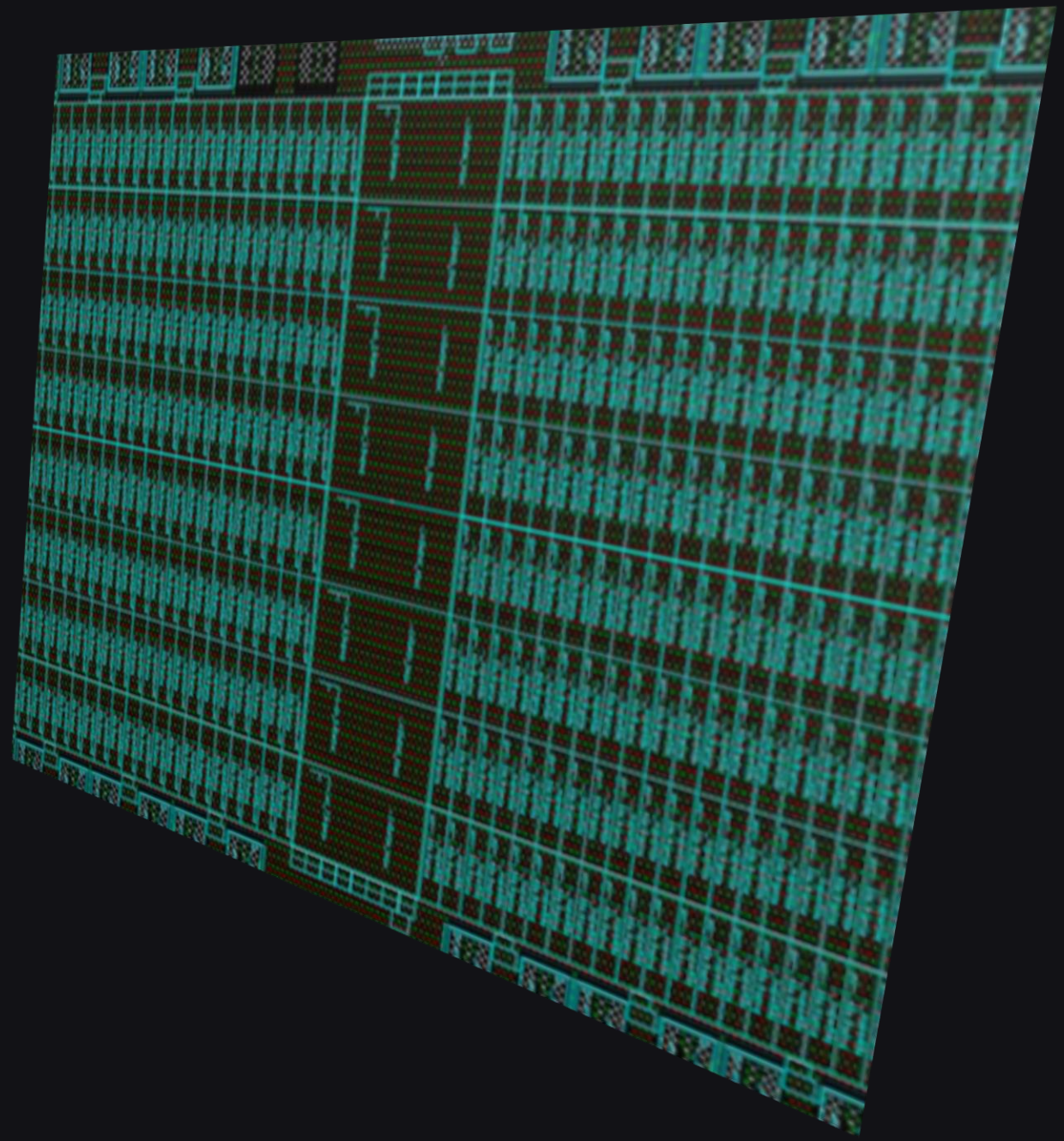
A Siemens Business

GRAPHCORE

AI Accelerator for Data Centers

+4x
DFT Productivity
(Using hierarchical test)

3 day
Test Bring-up



New Nodes Continue to Deliver Silicon Capacity

						
Year	2013	2014	2015	2016	2017	2018
Phone	5s	6	6s	7	8 and X	Xs and Xr
Technology	28nm	20nm	14/16nm	16nm	10nm	7nm
Die Size	102mm2	89mm2	94mm2	125mm2	89mm2	83mm2
# of Transistors	>1 Billion	≈2 Billion	>2 Billion	3.3 Billion	4.3 Billion	6.9 Billion
CPU Performance (Geekbench 4 single core)	1264	1382	2258	3403	4212	4796
GPU Performance (GFXBench 2.7 Trex off screen)	28.7	42.8	54.6	77.3	102.5	167.2

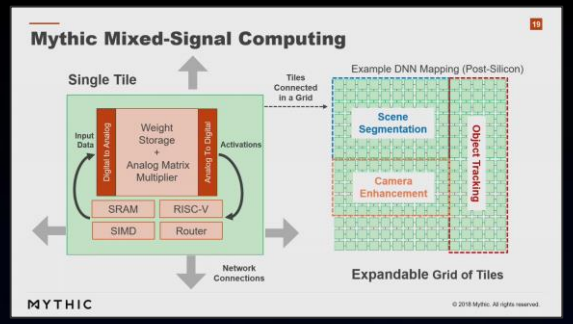
Sources: Teardown.com, Apple, Chipworks, ArsTechnica, Anandtech

AI Accelerators Ideal for Hierarchical Test

Many Identical Cores with Distributed Memory

GRAPHCORE

- **1216 processing tiles**
- 300MB distributed memory

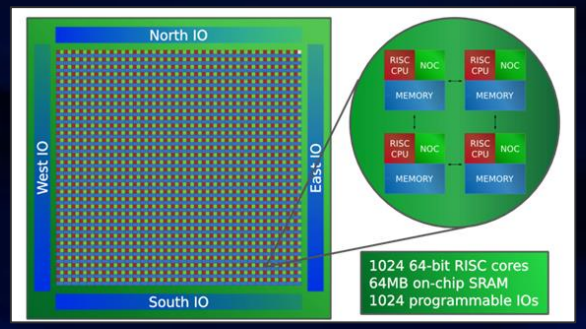


MYTHIC

- **100s tiles**
- 50M weights capacity

BITMAIN

- **2048 processing units**
- 16MB memory

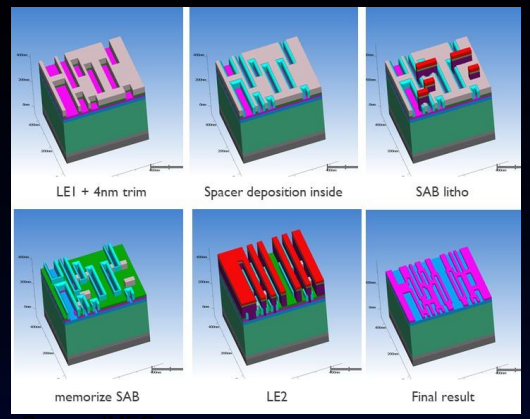


adapteva

- **1024 RISC cores**
- 64M data RAM

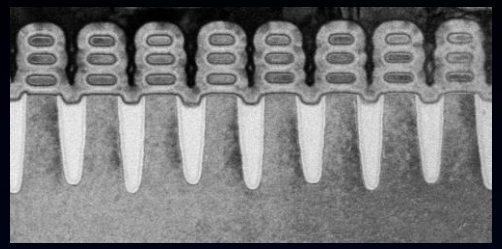
Mentor®
A Siemens Business

3nm Node Manufacturing Technology Challenges



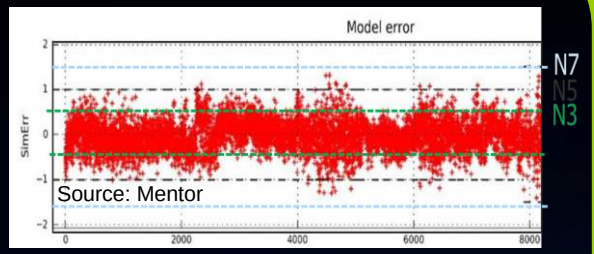
Source: IMEC

EUV Multi- Patterning required for achieving pattern resolution

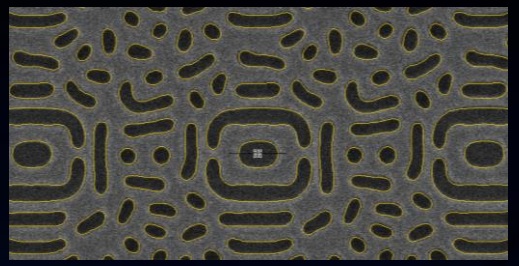


Source: IBM

Gate all-around transistors trigger new extraction requirements and physical failure modes



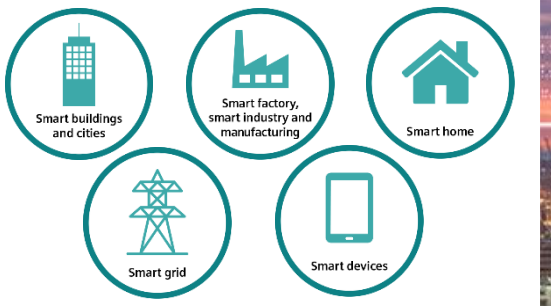
PPA metrics drives accuracy of lithography process model below 0.3nm RMS



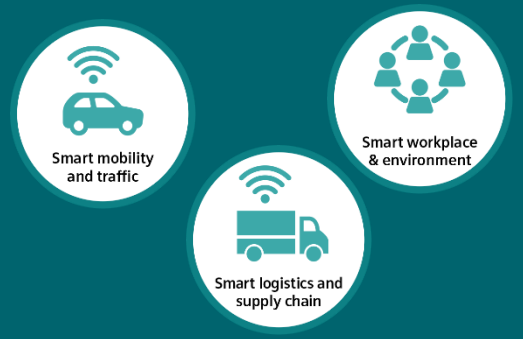
Source: IMS

Multi-beam mask writing enables curvilinear masks for most advanced lithography

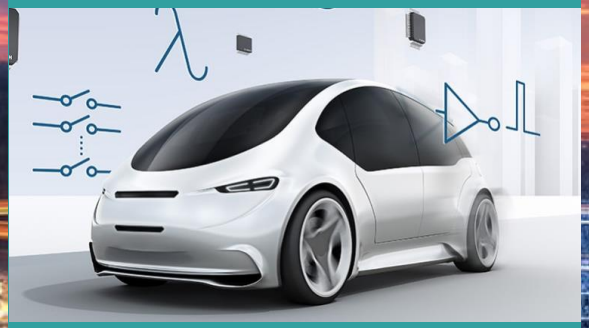
Mentor®
A Siemens Business



Smart systems are driving intelligence everywhere



Accelerating specialized IC design based on AI and machine learning



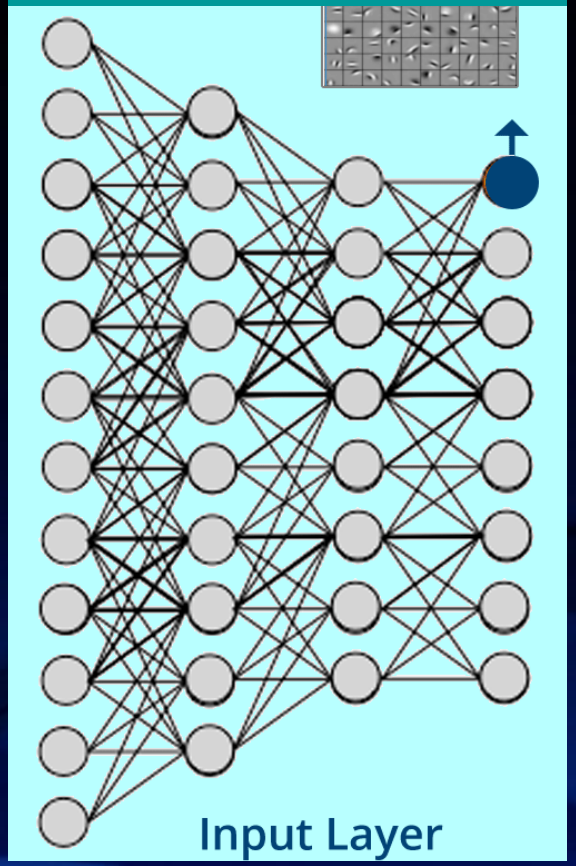
To enable intelligence at the edge, requires IC innovation fused with deep system design expertise

Mentor®
A Siemens Business

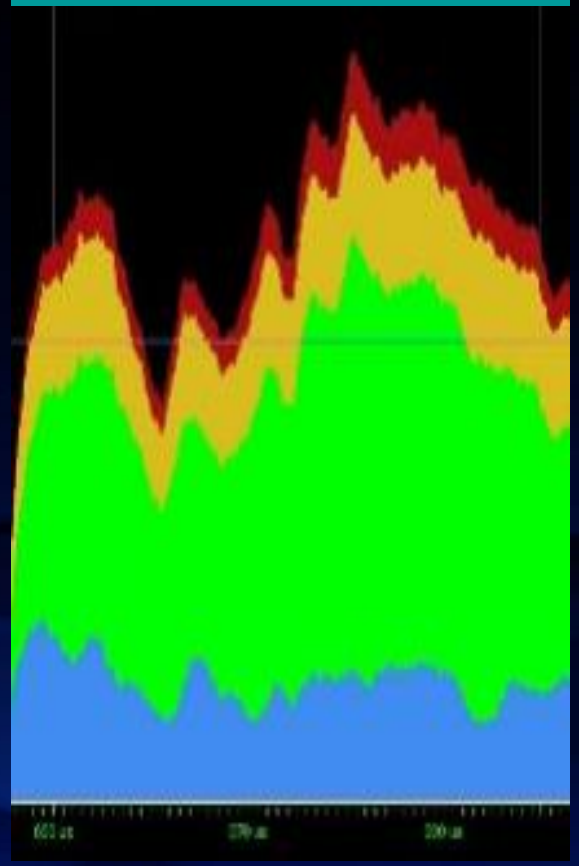
Companies need an EDA partner with deep expertise from smart IC to systems, factories and cities

AI/ML IP and IC Design Challenges

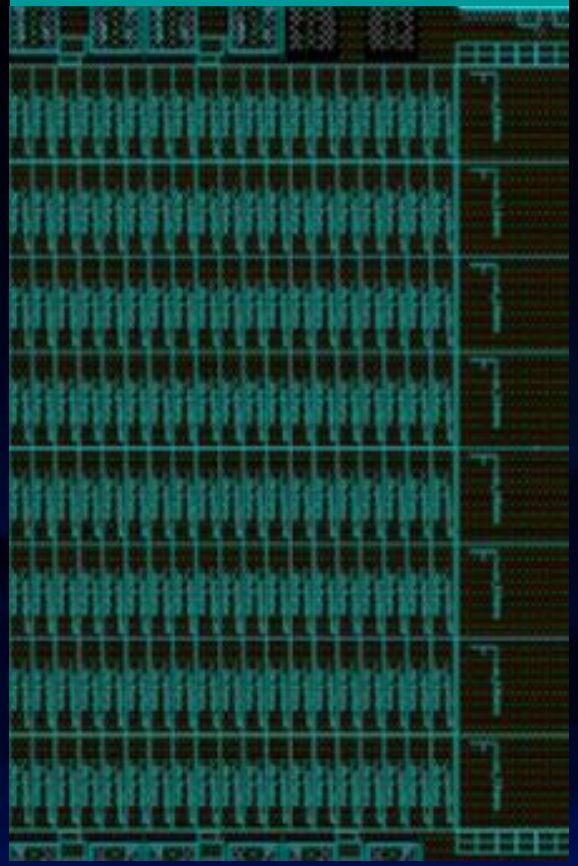
Architectural Optimization



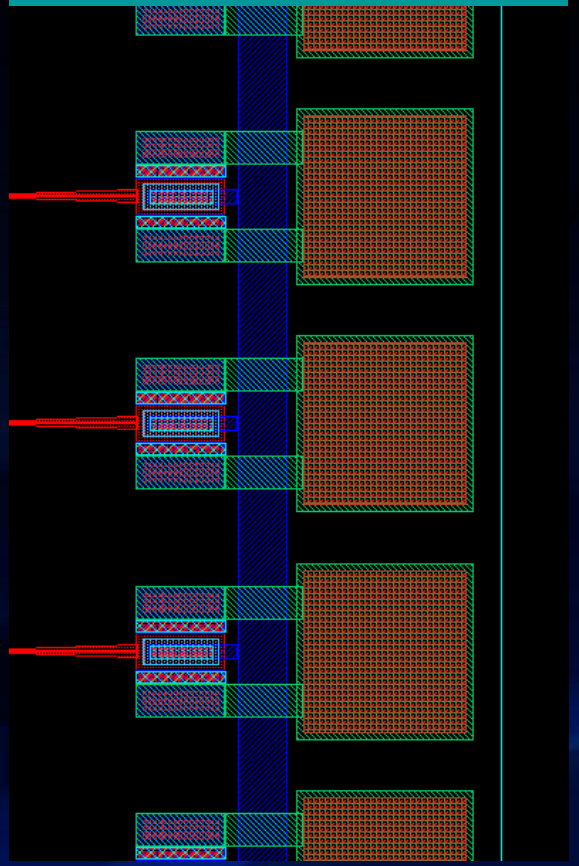
Power Budgeting



Increased Silicon Capacity



High-speed IO



AI/ML IC Tool Requirements

Top-down optimization C++

```
definition of a model u
MODULE( my_lsf_model )
sca_lsf::sca_out      out

sca_lsf::sca_signal   si

y_lsf_model( sc_module_

// instantiate pre-defi
sub1 = new  sca_lsf::

sub1->y( out );

dot1 = new  sca_lsf::

dot1->y( sig );
}
```

High-Level Synthesis

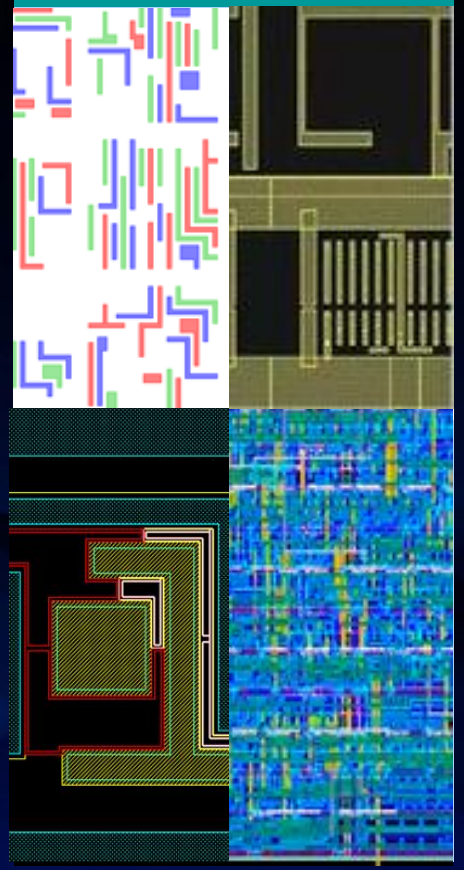
Power Optimization

Verification

Power Analysis

Higher capacity

Faster, scalable tools



Power budget management

RTL

PowerPro®

Redundancies

Power Optimization

Power Analysis

Flexible AMS Flow