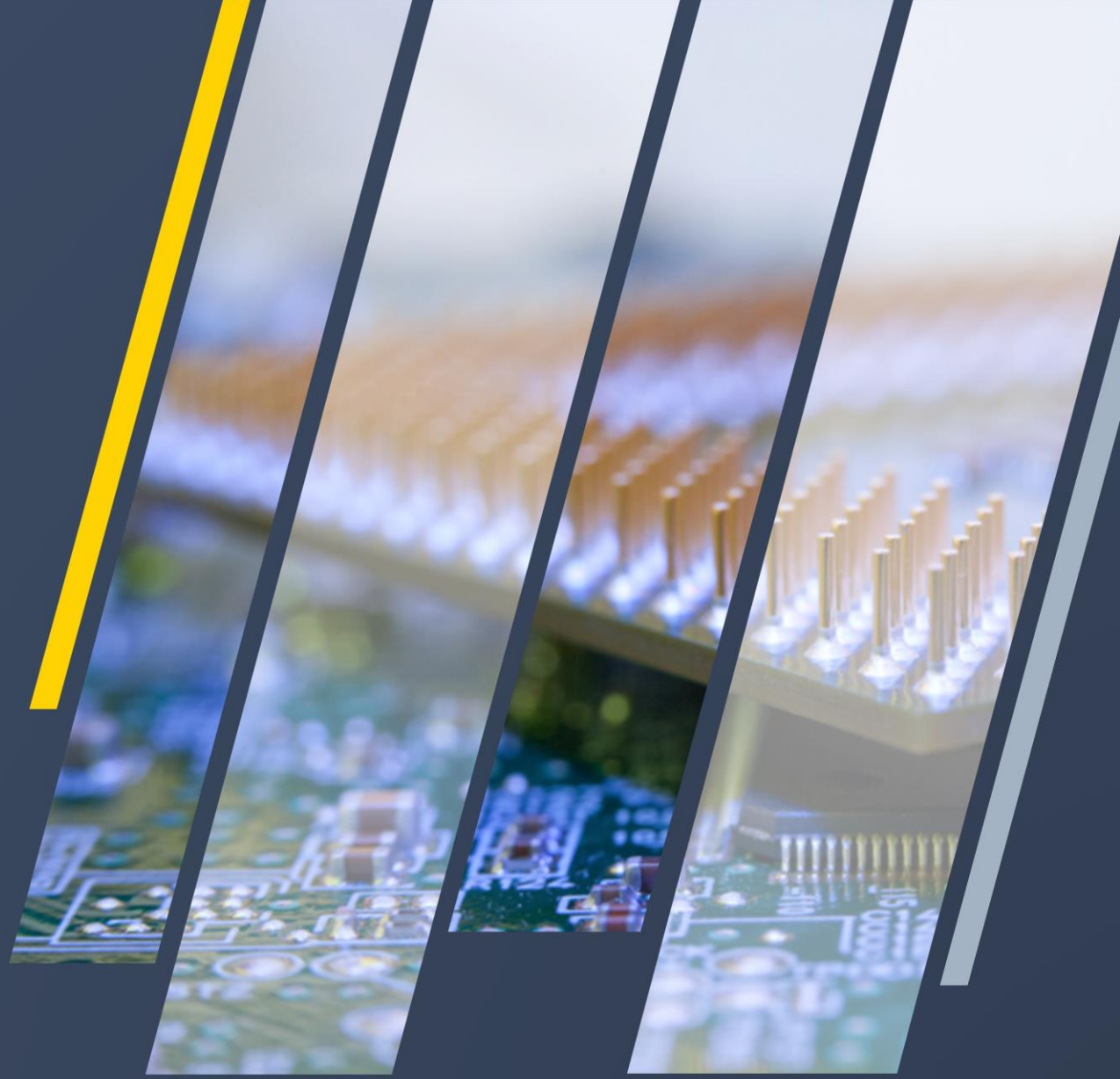
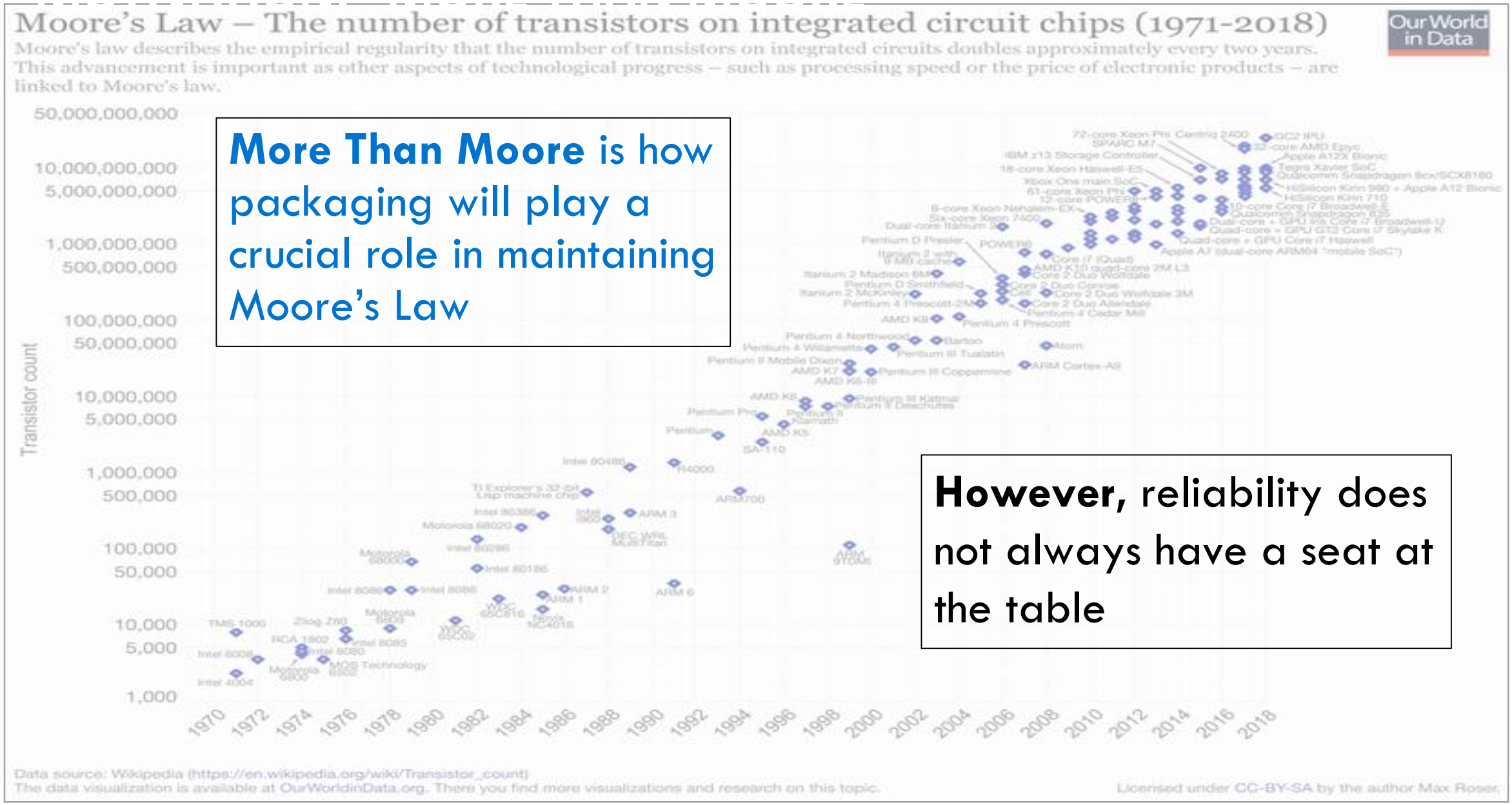
Reliability Challenges in Advanced Packaging



IEEE Electronic Design Process Symposium

Milpitas, CA

October 3, 2019



More Than Moore is how packaging will play a crucial role in maintaining Moore's Law

However, reliability does not always have a seat at the table

Major Challenges in Reliability of Advanced Packaging

Key Mechanisms

- Low-K Cracking
- Solder Joint Fatigue
- Microvia Separation

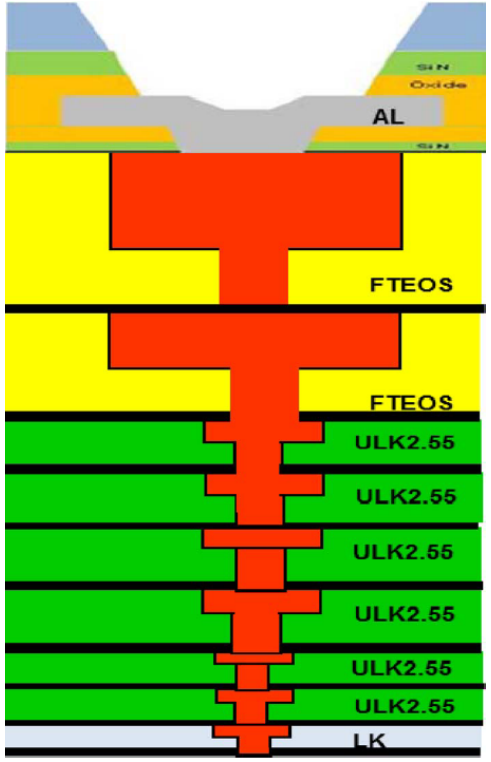
Key Drivers

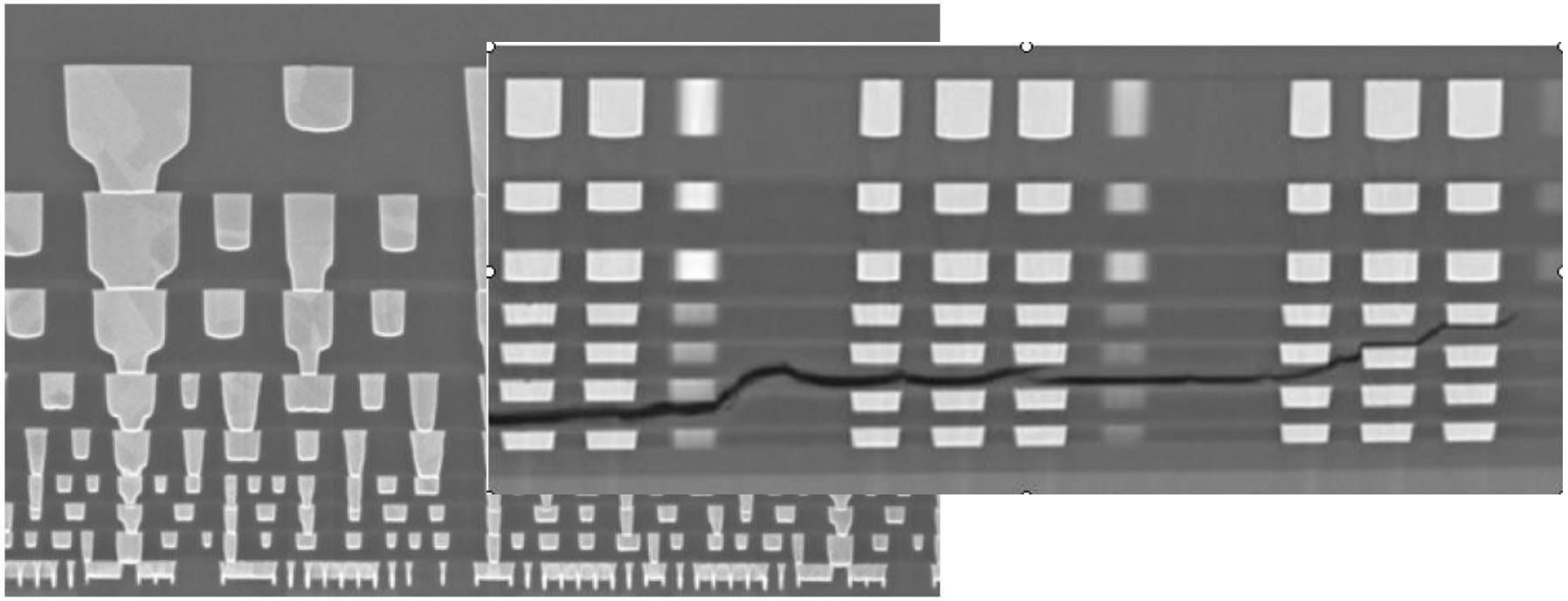
- New Materials
- 2.5D/3D Packaging
- Extended Lifetimes

LOW-K CRACKING

WHAT IS ELK / ILD CRACKING?

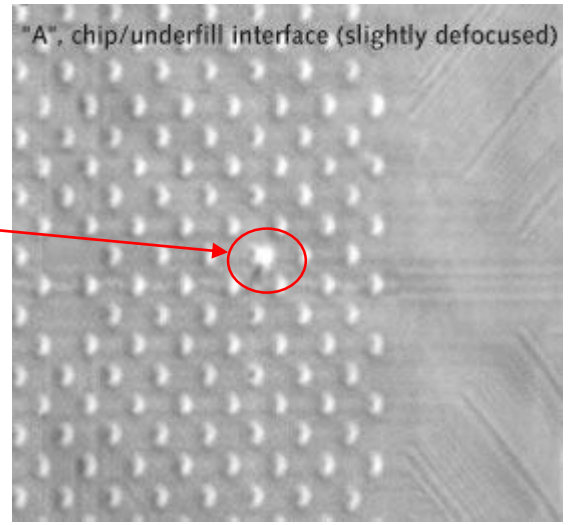
- Metal layers (Cu) send power and route signals from the active region (transistors)
- Each metal layer has an inner layer dielectric (ILD) composed of some form of SiO_2
- Elevated mechanical/thermo-mechanical stress will crack the ILD





ELK/ILD CRACKING (cont.)

- Known issue for over 15 years
  - Described as ‘white bump’ based on acoustic signature
- Has typically occurred at either flip chip attach or underfill cure processes
- One of the big drivers for switch to low Tg (underfill)



Thursday, July 3rd 2008

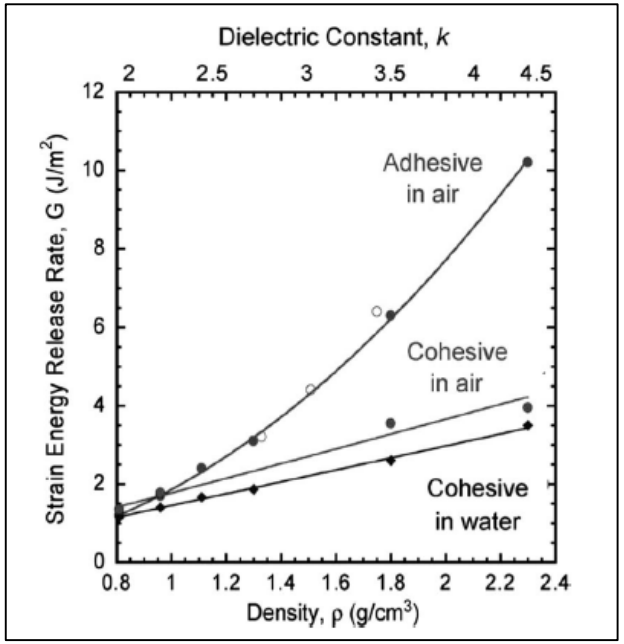
NVIDIA Admits to Selling Faulty Mobile GPUs, Shares Plummet

by btarunr | Thursday, July 3rd 2008 03:13 | Discuss (68 Comments)

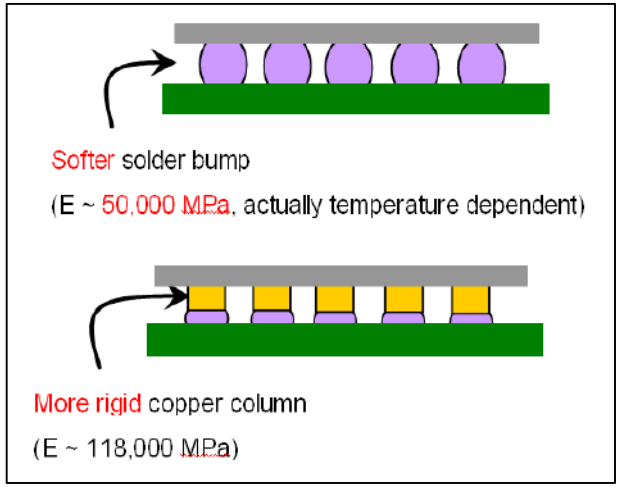
NVIDIA Admits to Selling Faulty Mobile GPUs, Could Cost it up to $200 M

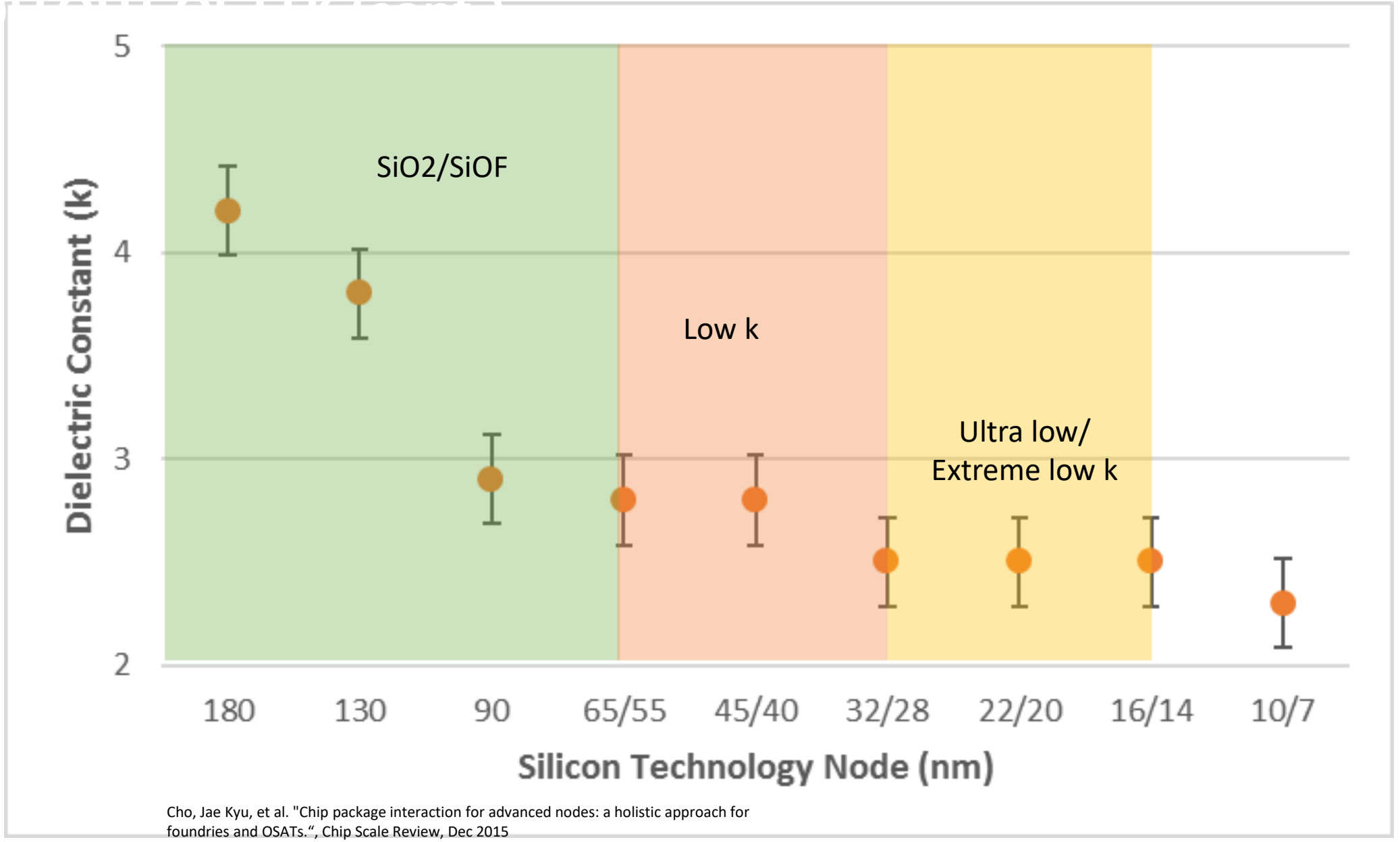
Why is ELK Cracking Becoming More Prevalent?

- Combination of transition to ELK/ULK dielectric material and transition to copper pillar and larger die
- Lower k (ELK/ULK) material is weaker and softer
  - By comparison, glass has a G_{Ic} of 7 J/m^2
- Copper has a much higher (2X) modulus than solder
  - Drives a lot more stress into the ILD



Vanstreels, Kris, Chen Wu, and M. R. Baklanov. "Mechanical stability of porous low-k dielectrics." ECS Journal of Solid State Science and Technology 4.1 (2015): N3058-N3064.





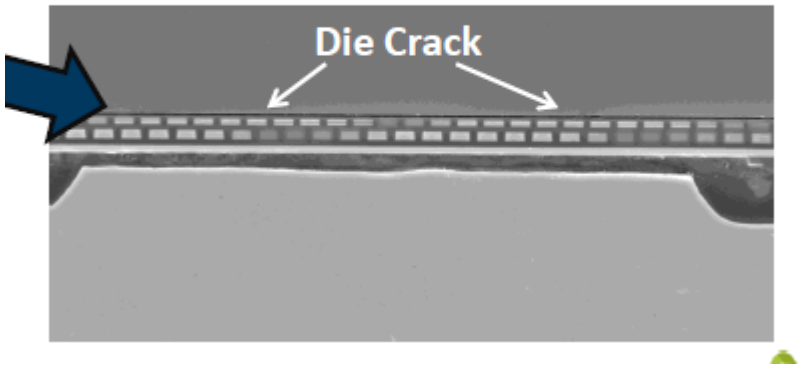
Cho, Jae Kyu, et al. "Chip package interaction for advanced nodes: a holistic approach for foundries and OSATs.“, Chip Scale Review, Dec 2015

WHY IS ELK CRACKING BECOMING MORE PREVALENT?

- Increasingly, failures are detected/occurring during thermal cycling
  - Not flip chip attach and not underfill cure

- Key issues
  - The interplay between applied and residual stresses
  - Debate about the presence or absence of cracks
  - Possibility of things changing over time
  - Poor/insufficient approaches to mitigation

Low-k failure in SOP packages after 1500cycles

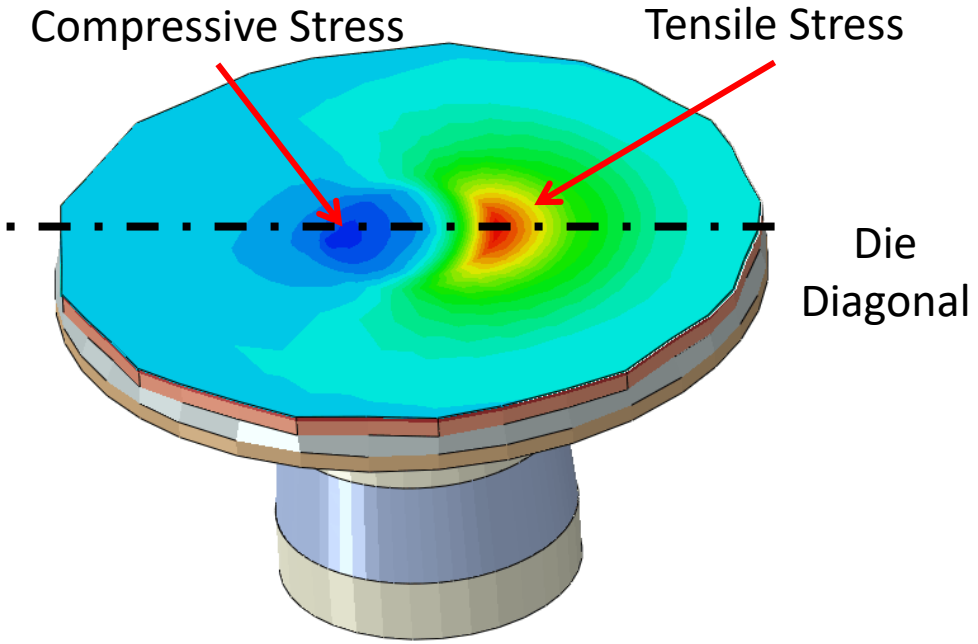


R. Katkar et. al., Reliability of Cu Pillar on Substrate, 2011

APPLIED VS. RESIDUAL STRESS

- Difference in coefficient of thermal expansion (CTE) between die and substrate causes a moment on the copper pillar
  - Drivers compressive and tensile normal stresses in ELK layer

- Therefore, the corner I/O is typically the bump of concern



APPLIED VS. RESIDUAL STRESS (cont.)

- The interplay between applied stresses and residual stresses are not necessarily well understood

- Higher temperatures during thermal cycling increase applied stresses, but lowers residual stresses

- Real risk that standard JEDEC thermal cycling can not be extrapolated to field conditions
  - -40°C to 10°C > -40°C to 125°C?
  - Where have we seen this before?

CRACKS OR NO CRACKS?

- Modeling and mitigation approaches change if ELK cracking is driven by the presence of an initial crack (i.e., during die singulation)
- The presence of an initial crack may explain time-dependency of ELK cracking

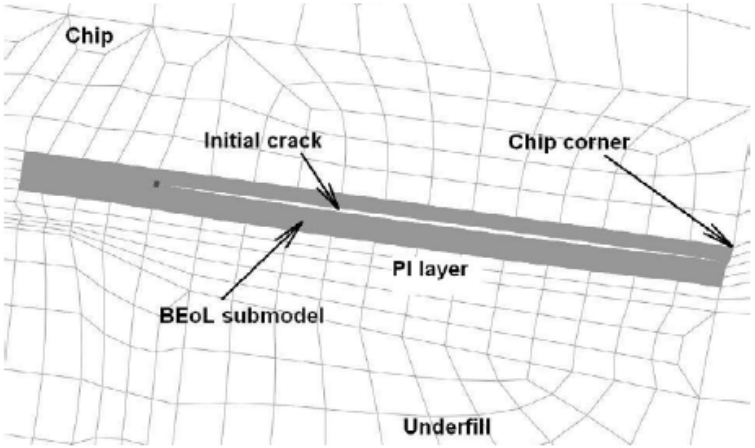


Fig. 2. Submodel of the BEoL stack in a FC-assembly

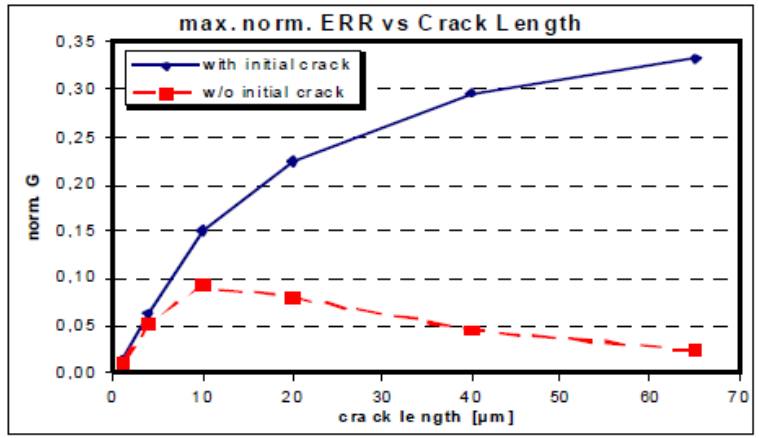


Fig. 3. Normalized ERR at the crack tip with and without an initial crack in the global model

Auersperg, J., et al. "Crack and delamination Risk Evaluation in low-k BEol." ICF12, Ottawa 2009. 2013.

Energy Release Rate (ERR)

ELK CRACKING OVER TIME

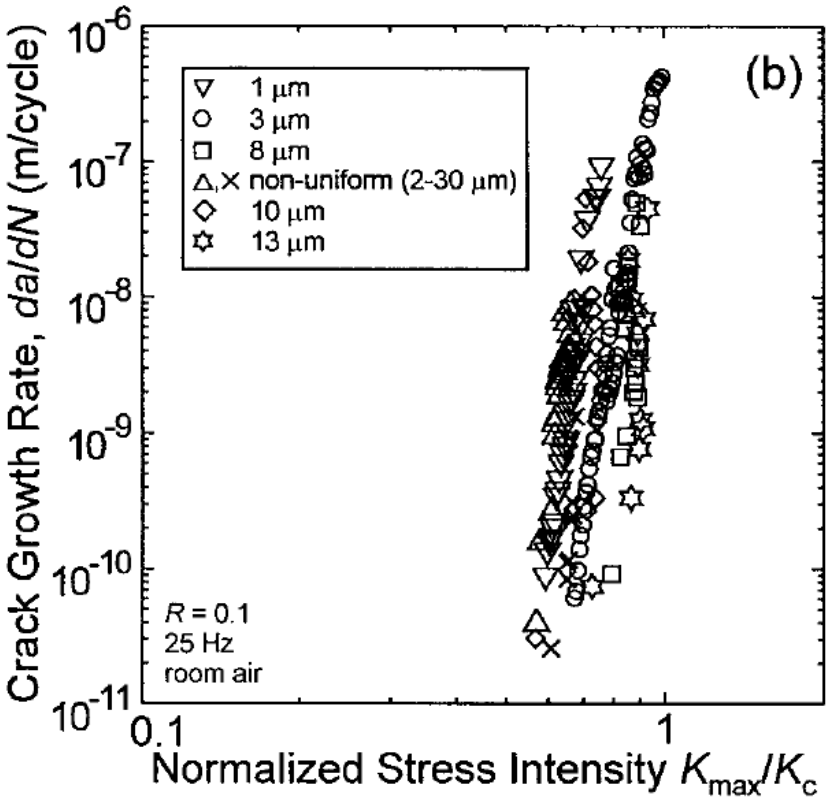
- Failure after several hundred cycles does not correlate with typical brittle fracture
  - Brittle fracture is typically deterministic (binary)
  - It either fails or it doesn't

- Theory 1: A material property is changing over time
  - Work hardening of solder? Degradation increases compliance
  - Work hardening of copper? Requires high stresses (100 to 200 MPa)
  - Work hardening of polyimide? Not reported in the literature

ELK CRACKING OVER TIME (cont.)

- Theory 2: Microdamage Evolution / Brittle Fatigue

- Softer material with intentional stress concentrations (porosity) could drive fatigue crack growth
  - Growth until it reaches a critical size



Ritchie, R. O., C. J. Gilbert, and J. M. McNaney. "Mechanics and mechanisms of fatigue damage and crack growth in advanced materials." International Journal of Solids and Structures 37.1 (2000): 311-329.

POOR/INSUFFICIENT APPROACHES TO MITIGATION

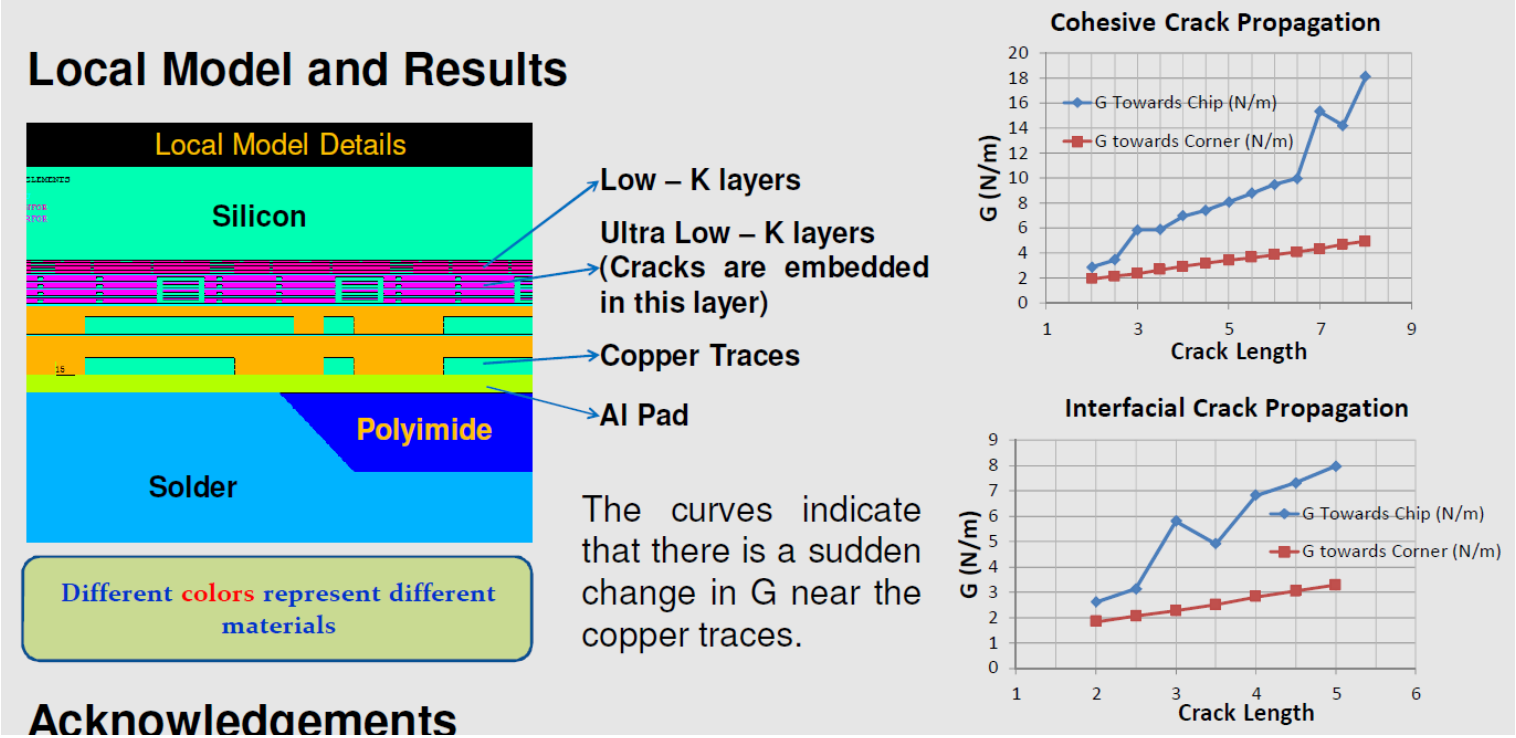
- Mitigation is dominated by design rules
  - Limited to no correlation to actual stress states within the ILD

- Examples of design rules
  - Large pad diameter
  - Rigid requirements regarding metal density
  - Coarser spacings
  - Copper pillar dimensions

- Different design rules from different suppliers (foundry vs. OSAT)

TRANSITIONS ARE KEY

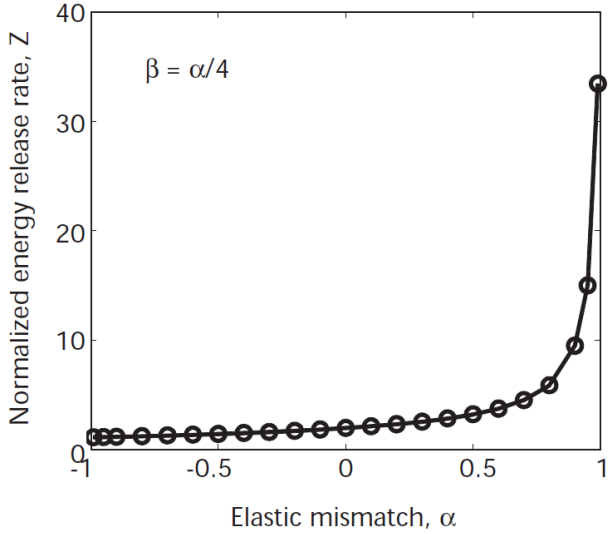
- Strong indication that design guidelines on metal density are insufficient



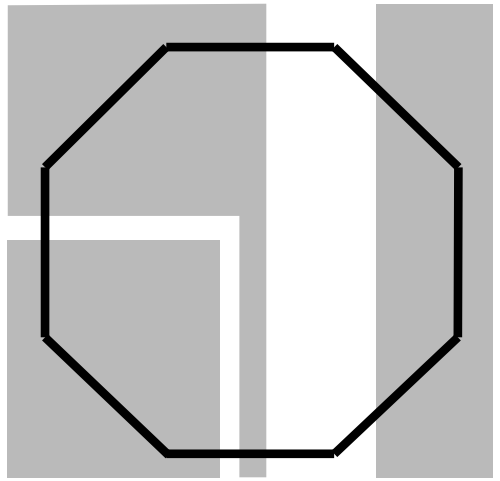
Fundamental and Applied Fracture Characterization of Thin Film Systems

TRANSITIONS ARE KEY (cont.)

- Transition between different dielectric materials
  - ULK/ELK to LK, ULK/ELK to USG, etc.
- Large variation in areas of metal and dielectric under bond pad
- Large variation in concentration of vias under or adjacent to the bond pad



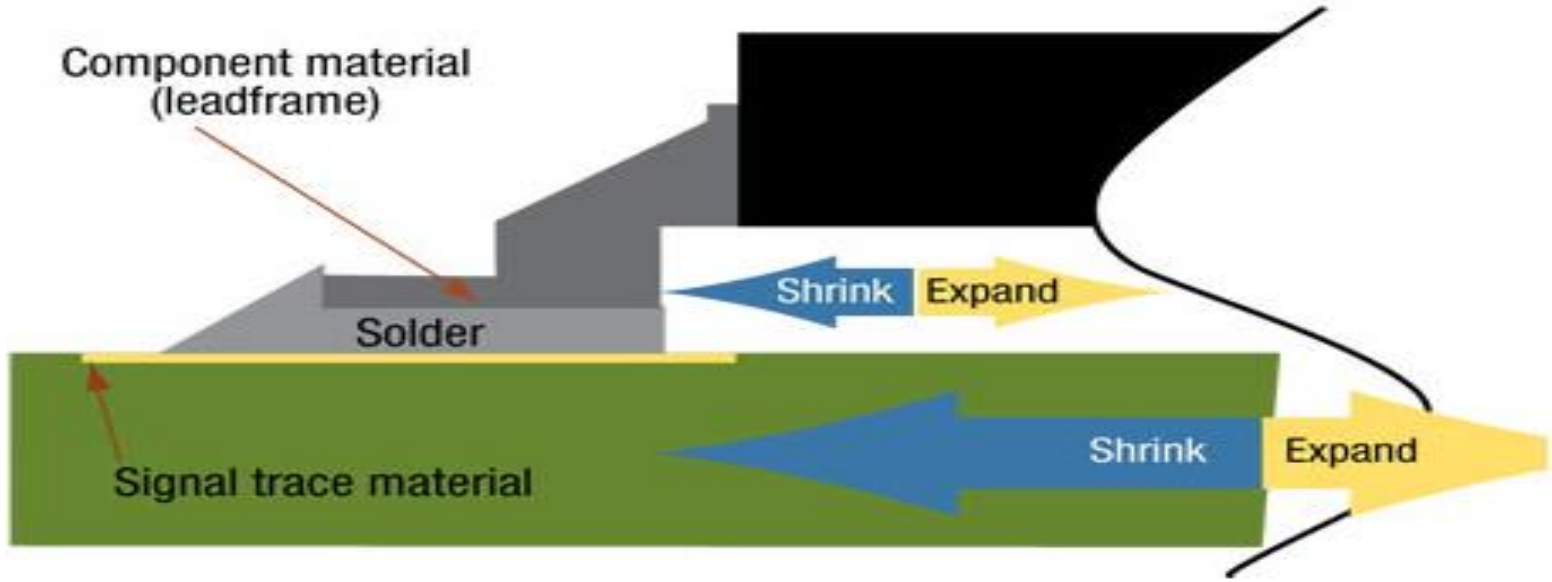
Zhang, Xuefeng, et al. "Chip-package interaction and reliability impact on Cu/Low-k Interconnects." Electrical, Optical and Thermal Interconnections for 3D Integrated Systems (2008).



SOLDER FATIGUE

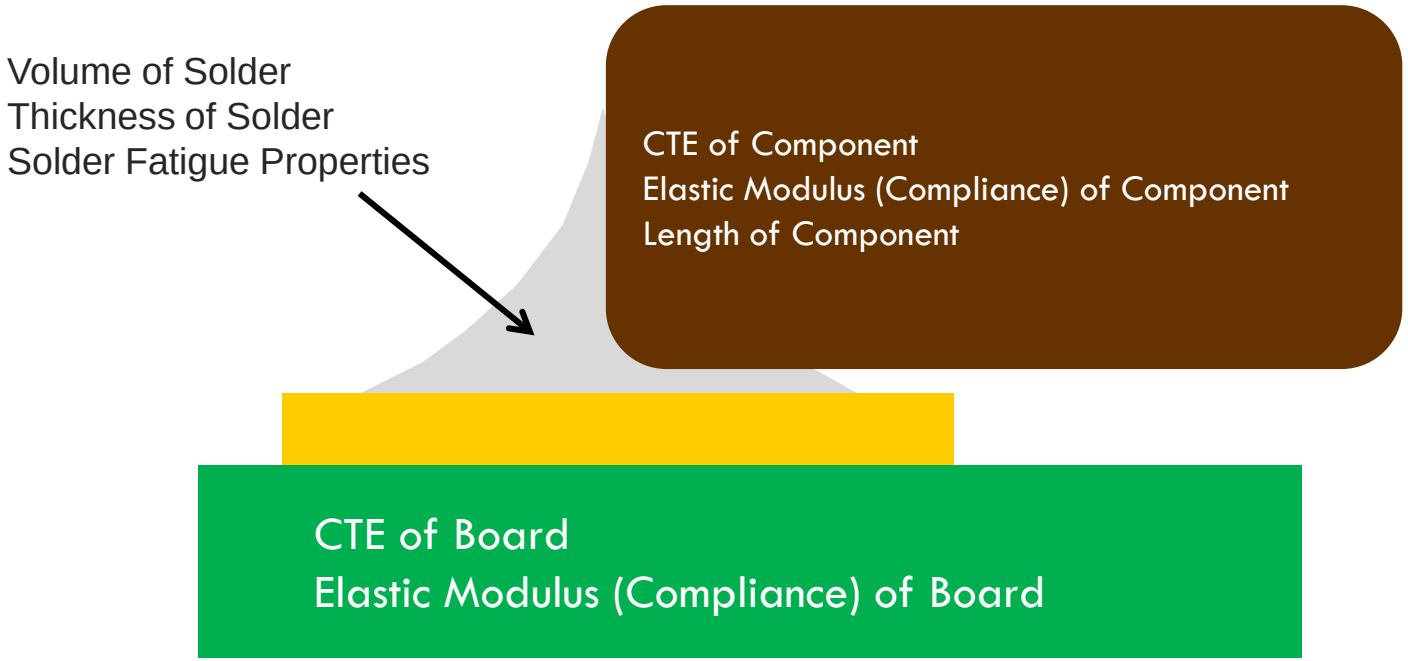
SOLDER JOINTS FATIGUE UNDER THERMAL CYCLING

Solder is connecting two objects that expand/contract at different rates



SOLDER JOINT FATIGUE

- Knowing the critical drivers for solder joint fatigue, we can develop predictive models and design rules



1D STRAIN ENERGY

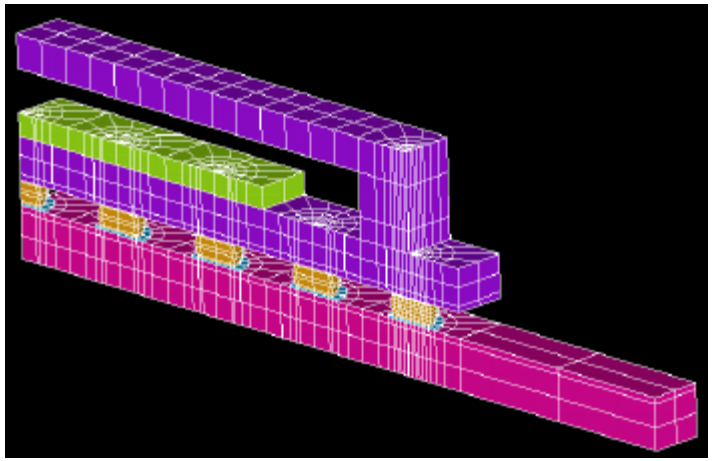
$$\Delta\gamma = C\frac{L_D}{h_s}\Delta\alpha\Delta T \qquad (\alpha_2-\alpha_1)\cdot\Delta T\cdot L = F\cdot\left(\frac{L}{E_1A_1}+\frac{L}{E_2A_2}+\frac{h_s}{A_sG_s}+\frac{h_c}{A_cG_c}+\left(\frac{2-\nu}{9\cdot G_b a}\right)\right)$$

$$\Delta W = 0.5\cdot\Delta\gamma\cdot\frac{F}{A_s} \qquad N_f = \left(0.001\cdot\Delta W\right)^{-1}$$

Closed Form, PCB Stiffness, Strain Energy, E (T), Tg, Die Shadow

N. Blattau and C. Hillman, "An Engelmaier Model for Leadless Ceramic Chip Devices with Pb-Free Solder," Journal of the Reliability Information Analysis Center, First Quarter 2007, 6-11

3D STRAIN ENERGY



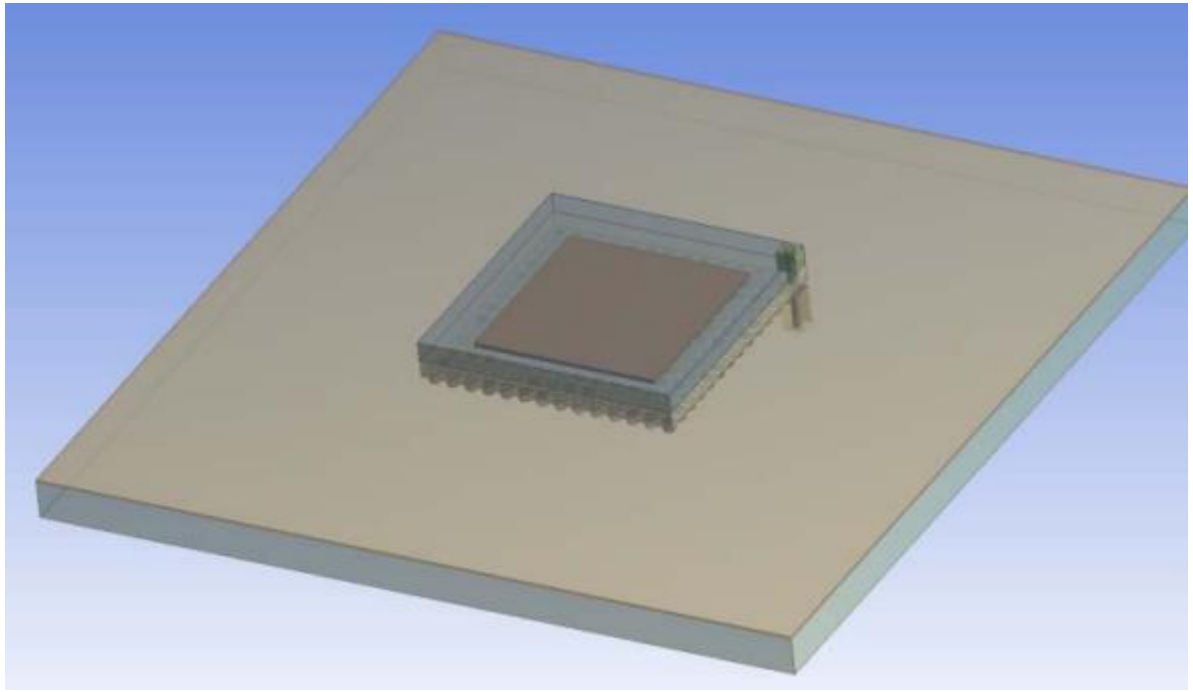
$$N_0 = K1\left(\Delta W_{avg}\right)^{K2}$$

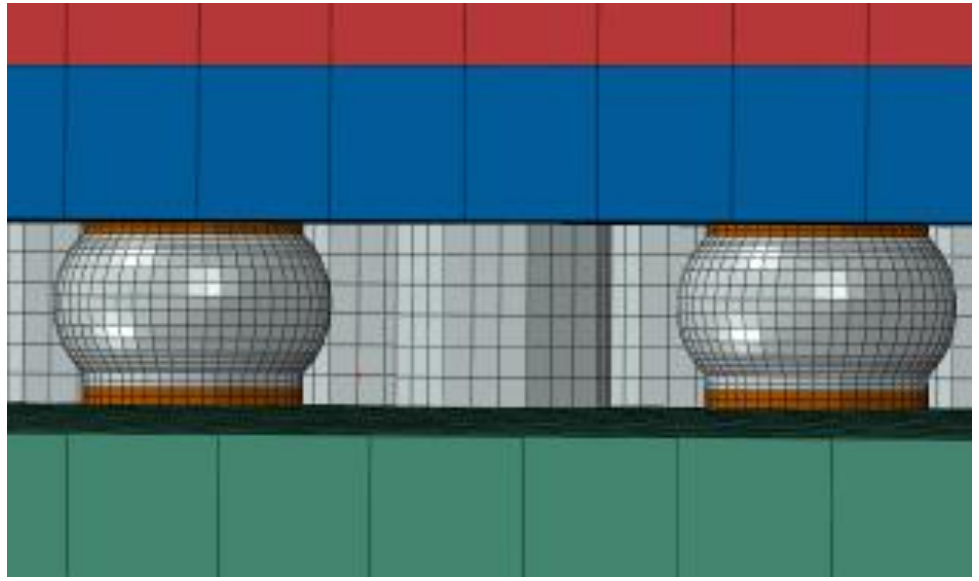
$$\frac{da}{dN} = K3\left(\Delta W_{avg}\right)^{K4}$$

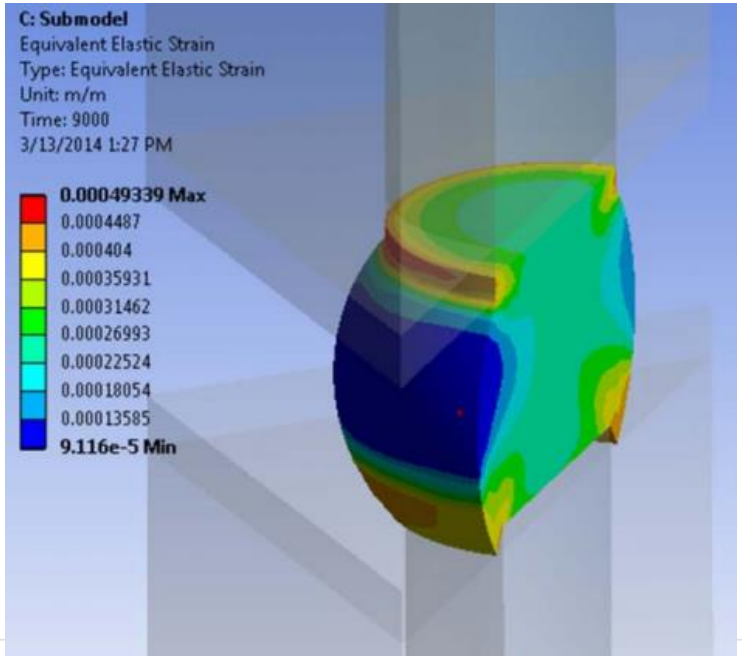
$$N_f = N_0 + \frac{D}{da/dN}$$

Darveaux, R., "Solder Joint Fatigue Life Model," Proceedings of TMS Annual Meeting, Orlando FL, February 1997, pp. 213-218

GLOBAL + LOCAL MODELING

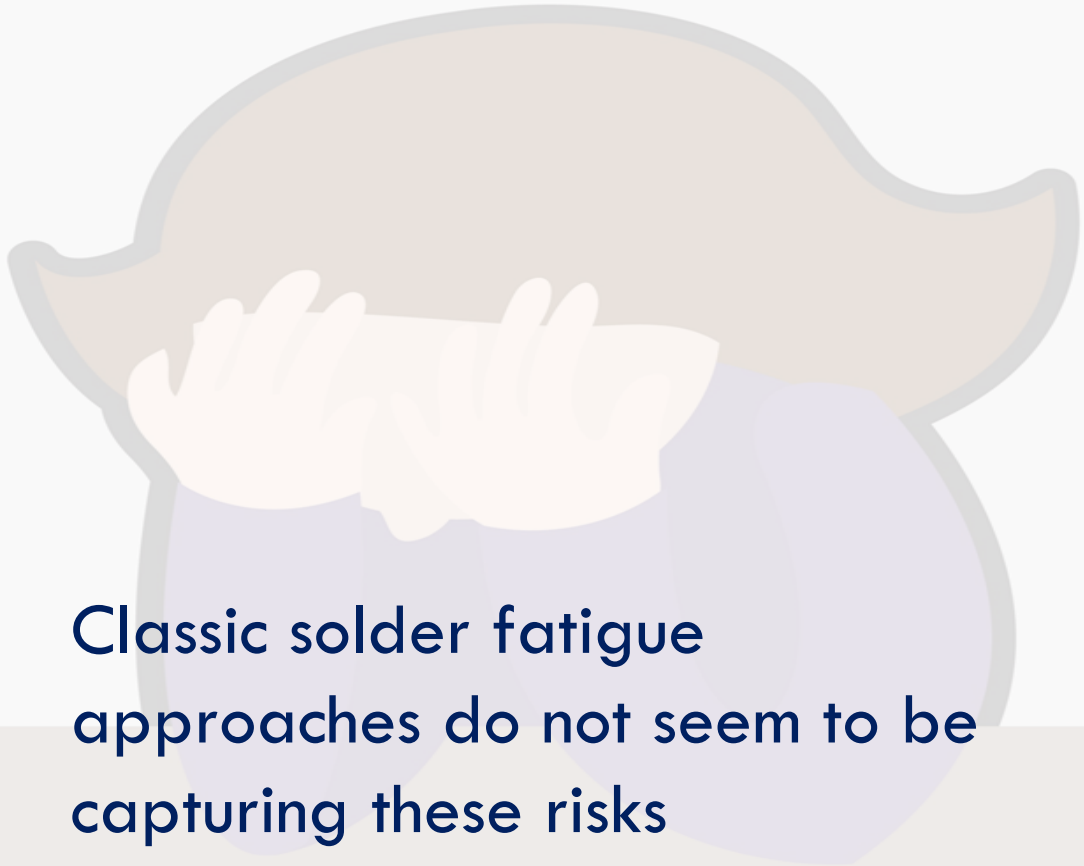






UNEXPECTED SOLDER FAILURES

Increasing number of companies reporting early life failures during thermal cycle testing or in the field



Classic solder fatigue approaches do not seem to be capturing these risks

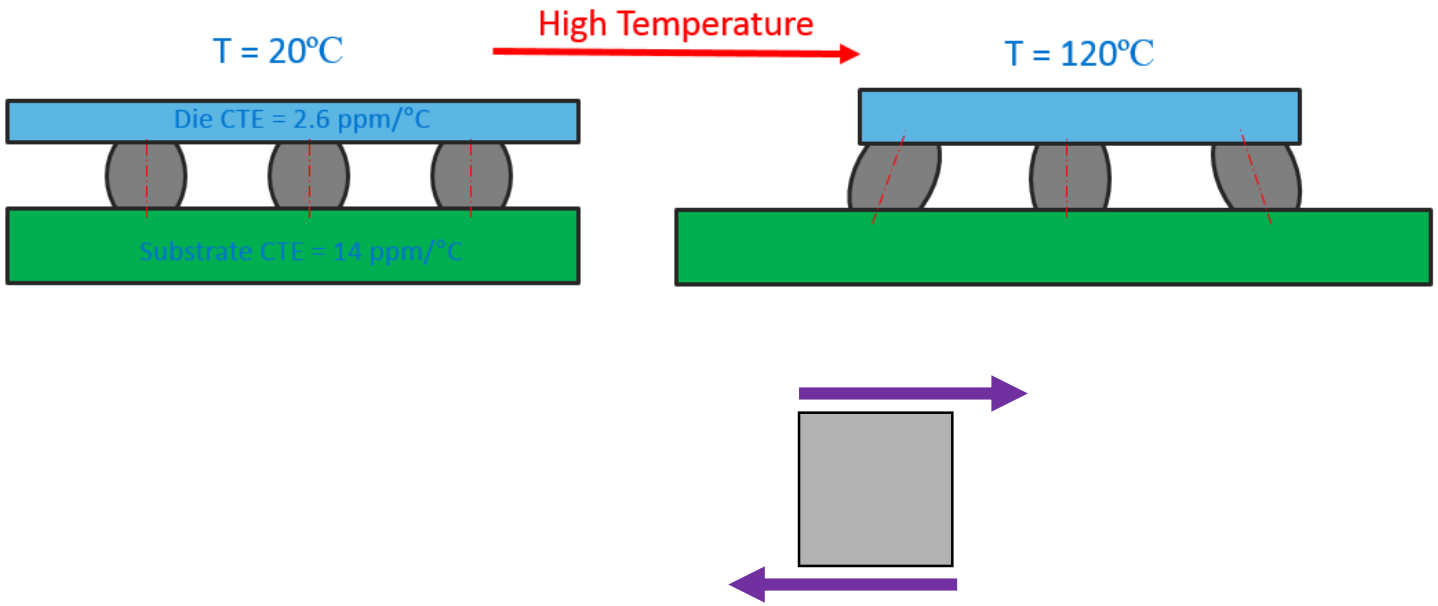
ROOT-CAUSE OF UNEXPECTED FAILURES

Strong indication that mixed-mode stresses are key drivers

CLASSIC BEHAVIOR

- Idealized CTE mismatch

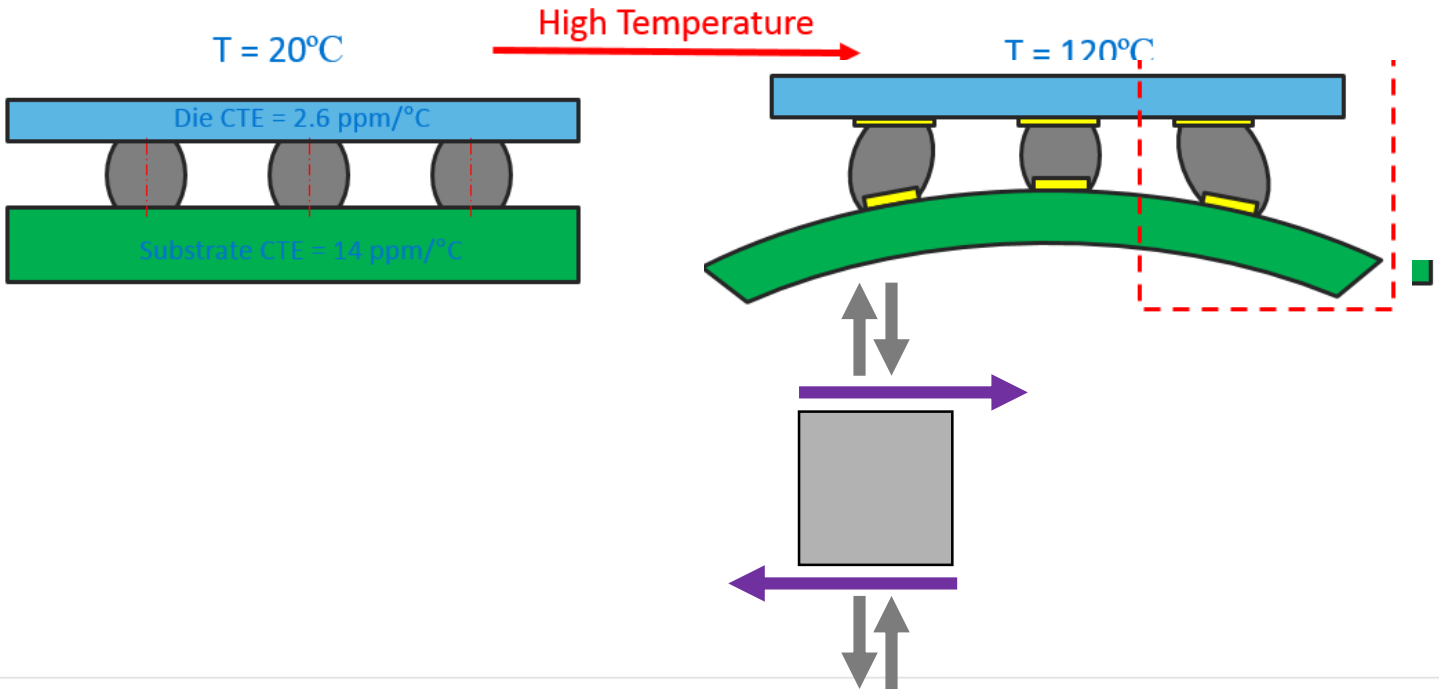
Shear strain $\gamma = \frac{CL_h \Delta T \Delta \alpha}{h}$



ROOT-CAUSE OF UNEXPECTED FAILURES

Strong indication that mixed-mode stresses are key drivers

MIXED-MODE (TRIAXIALITY) BEHAVIOR



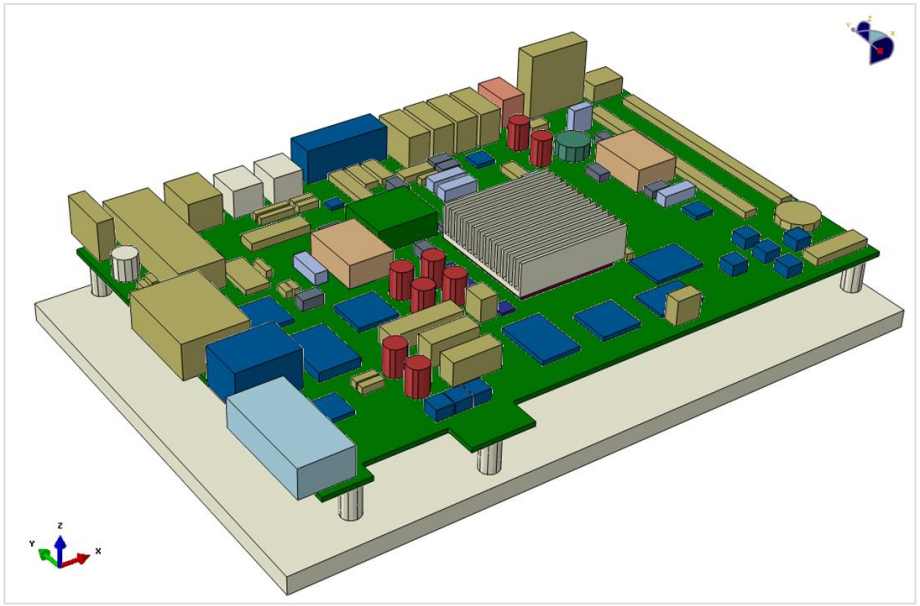
ROOT-CAUSE OF MIXED-MODE STRESSES

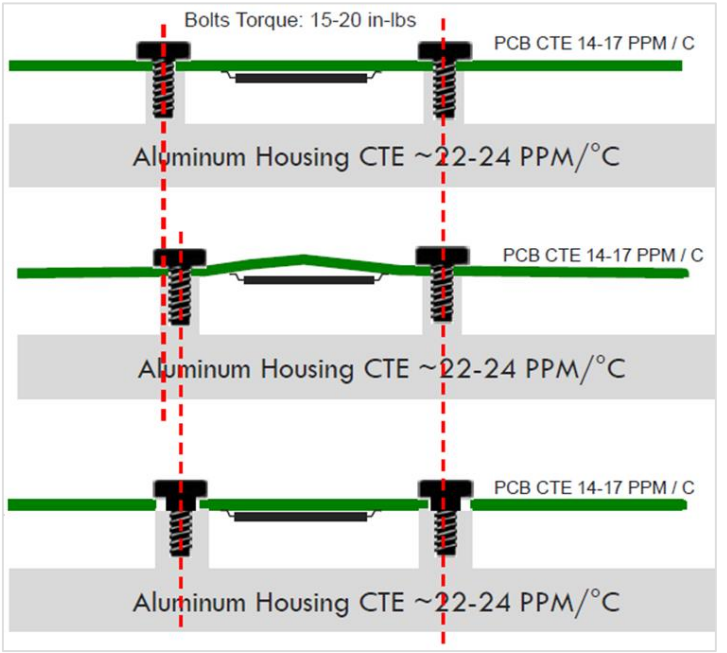
- Driven by increasing complexity and density of electronics, including adoption of mechatronics

- Three categories
  - Over-Constrained Boards / Housing Interaction (previously covered)
  - Potting/Coating/Underfill
  - Mirroring

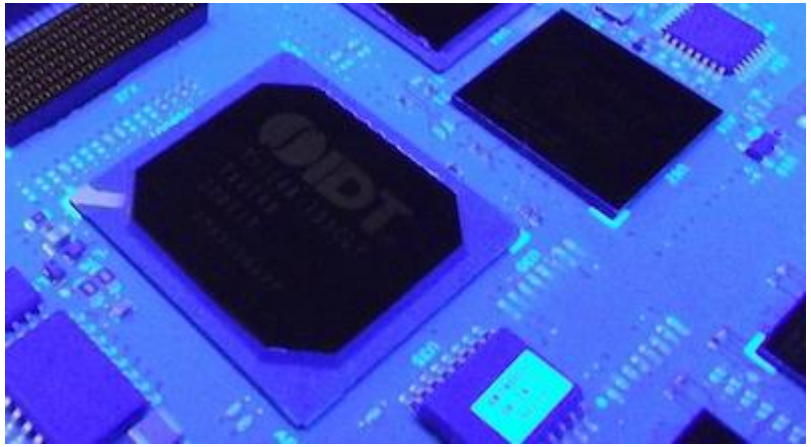
- Also described as ‘system-level’ effects

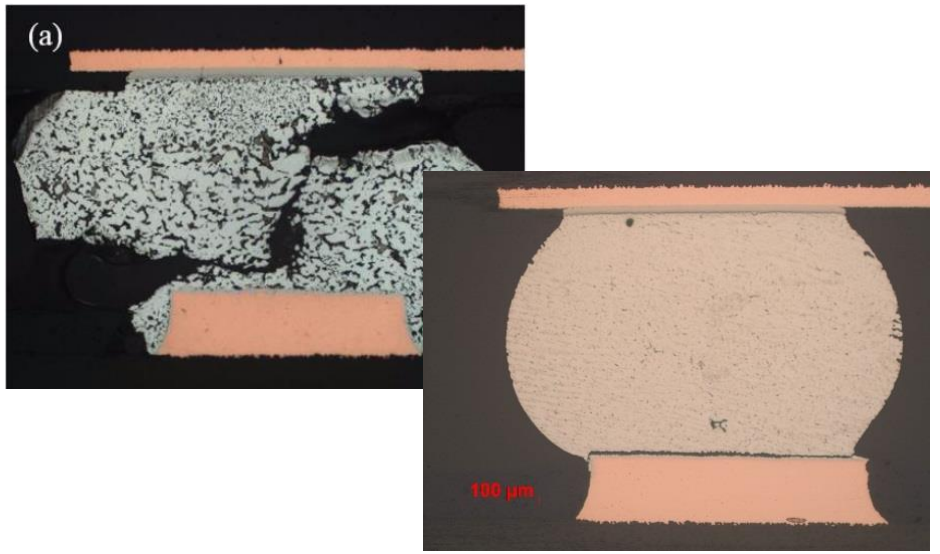
OVER-CONSTRAINED BOARDS

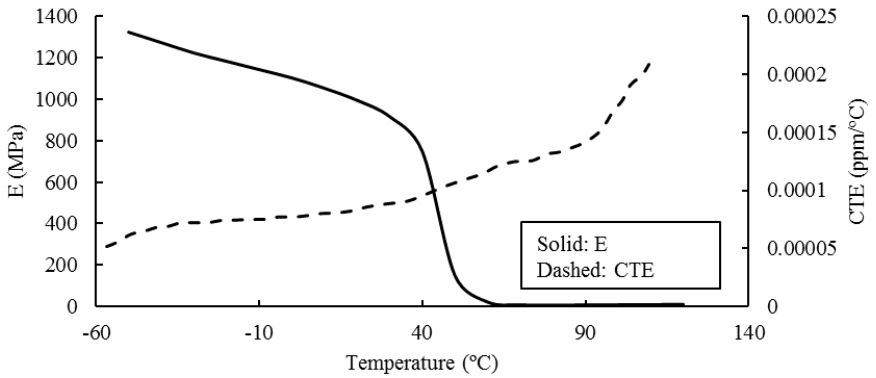


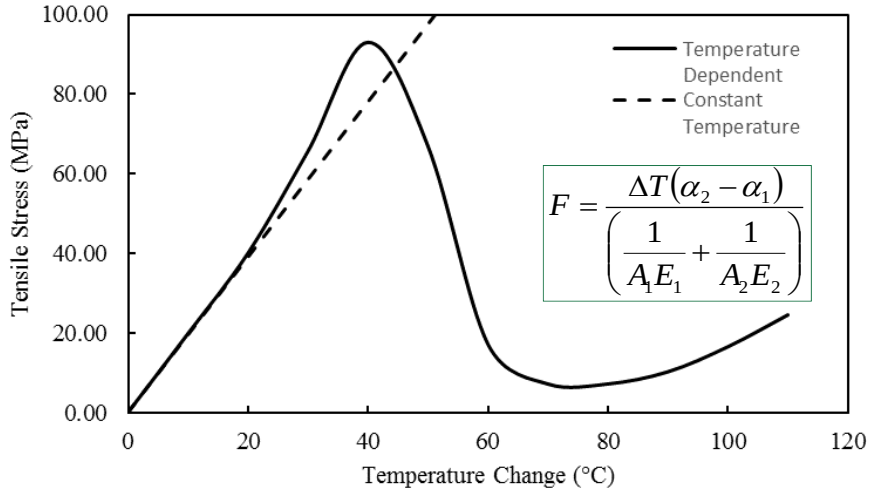


COATING/POTTING/UNDERFILL

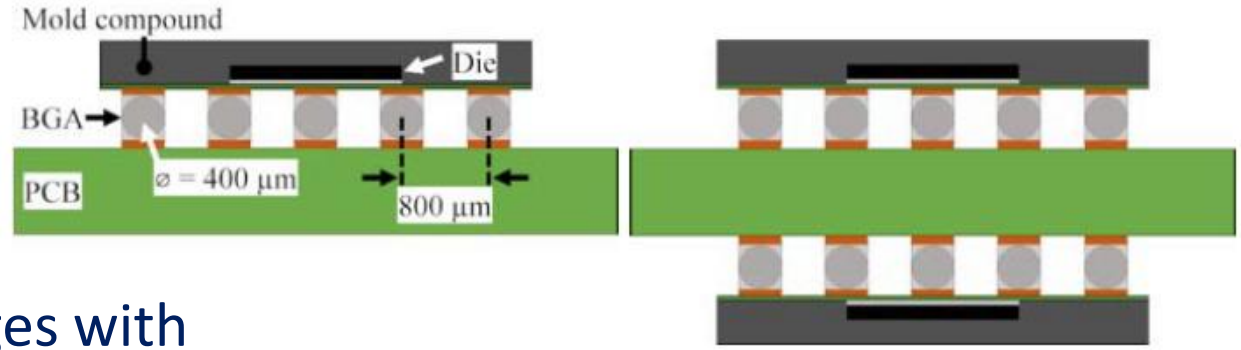








BGA/CSP MIRRORING



- Avoided in earlier designs (challenges with rework and X-ray inspection)
  - Increasingly required due to higher densities and higher speed memory
- Reduces lifetime by 1.5X to 5X, but numerous organizations struggle to predict behavior

Based on Darveaux Model

Assembly	Reliability (cycles)	
	Measured	Predicted
Single-Sided BGA (20 mil pad)	8,284	8,153
Single-Sided BGA (22 mil pad)	7,897	7,991
Single-Sided BGA (24 mil pad)	7,736	7,814
Mirror Image BGA	1,576	2,890	*
Single-Sided CSP	7,611	6,140
Mirror Image CSP	3,174	2,300	*

Meifunas, M., et al. "Measurement and prediction of reliability for double-sided area array assemblies." *Electronic Components and Technology Conference, 2003. Proceedings. 53rd*. IEEE, 2003.

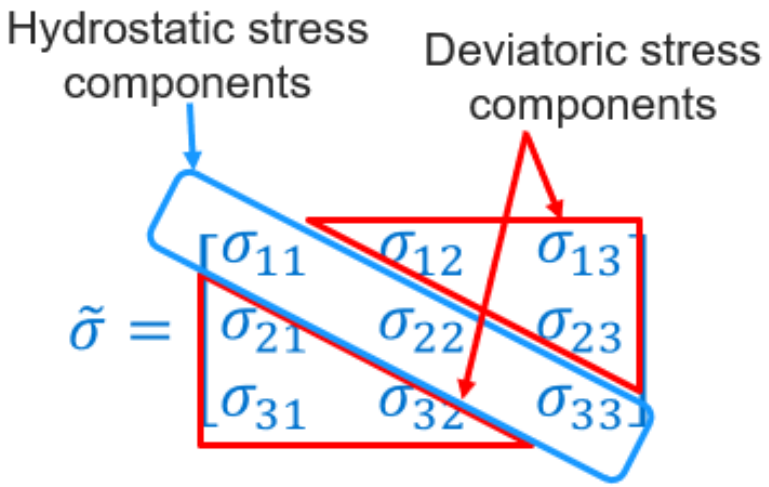
Based on Darveaux Model

Pitch mm	type	SnPb		SAC305		
		Test /FEA	Error	Test /FEA	Error	
1.27	Single	1487/1839	23%	2131/2111	-0.9%	
	Mirror	650/334	-48%	748/548	-27%	*
	Offset	716/543	-24%	851/787	-7.5%	

Ye, Yuming, et al. "Assessment on reliability of BGA package double-sided assembled." *High Density Packaging and Microsystem Integration, 2007. HDP'07. International Symposium on*. IEEE, 2007.

SYSTEM-LEVEL SOLDER FATIGUE PREDICTION

- Sherlock (Thermo-mech)



- Creep equivalent approach (Secant Modulus)
  - No time-stepping

- Energy partitioning method of shear and axial components
  - Energy calculated using closed-form equation

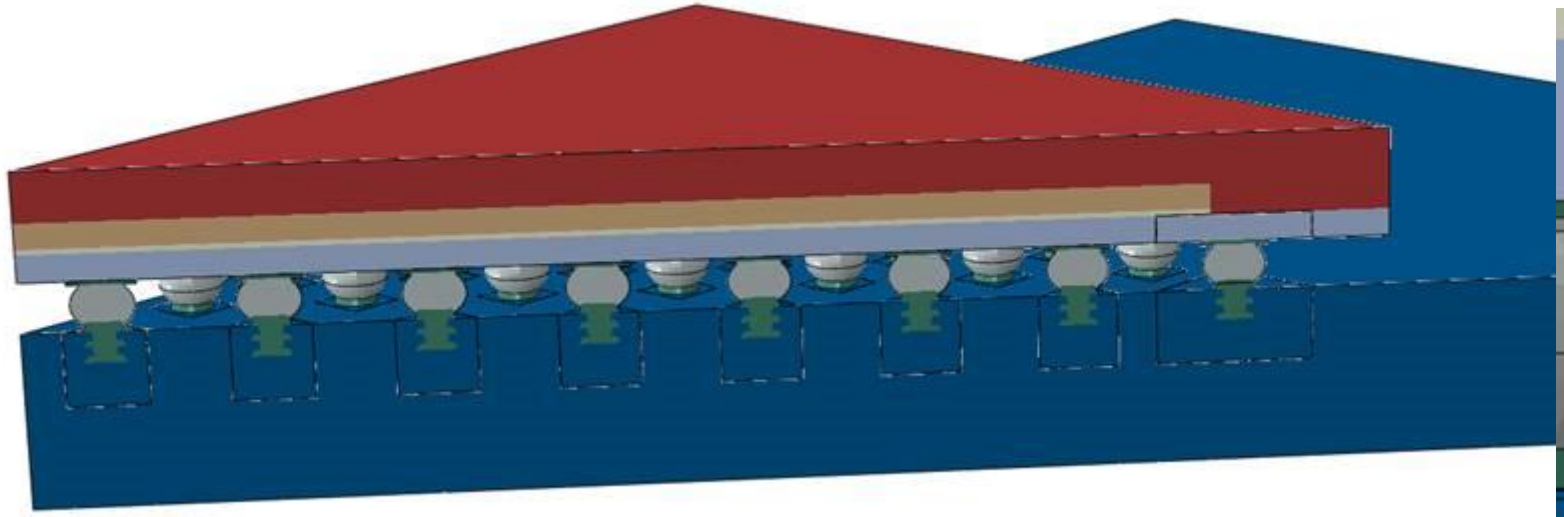
$$N_f = C_1(\Delta W)_{shear}{}^{n_1} + C_2(\Delta W)_{Axial}{}^{n_2}$$

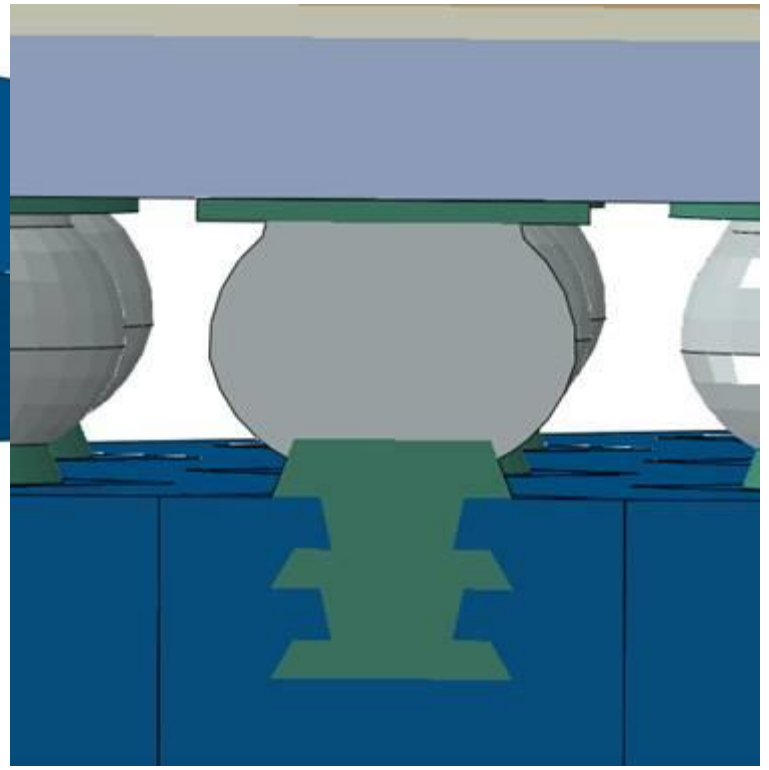
SIMULATION AND RELIABILITY OF ADVANCED PACKAGING

LOW-K CRACKING AND SOLDER FATIGUE MITIGATION

- Increasingly, failures are occurring ‘randomly’ throughout the advanced package
  - No longer only occurring at the corners (1st level or 2nd level interconnect)
- Even for packages that are ‘similar’ and follow all design rules
- Driven by increasingly package complexity (different materials, different stress states)
  - Low K cracking: metal layout, bump layout and bump collapse
  - Solder fatigue: array pattern, system effects, microvia stacks

MODELING CHALLENGES – SOLDER FATIGUE/MICROVIA STACKS





- Where and what of microvia stacks increasingly driving solder fatigue and low-k cracking behavior
- How to perform global/local without knowledge of what to model and where to model?

NEXT STAGE IN MODELING/SIMULATION OF ADVANCED PACKAGING

- ANSYS is extending scripting, modeling and element options to expand the ability to model all artifacts that could influence key failure modes
  - Interconnect geometries + die, interposer, substrate and PCB layout

- Combined with expansion of electronic material properties