Advanced Packaging – It's Changing the World of Wafer Test

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FormFactor, Inc.

The Next 25 Minutes

- Setting the stage
  - What is “wafer test”?
  - What is “advanced packaging”?
- Recognizing the challenges
  - How does advanced packaging impact wafer test?
- Responding with solutions
  - What are some practical examples and options for advanced packaging wafer test?
- Q&A

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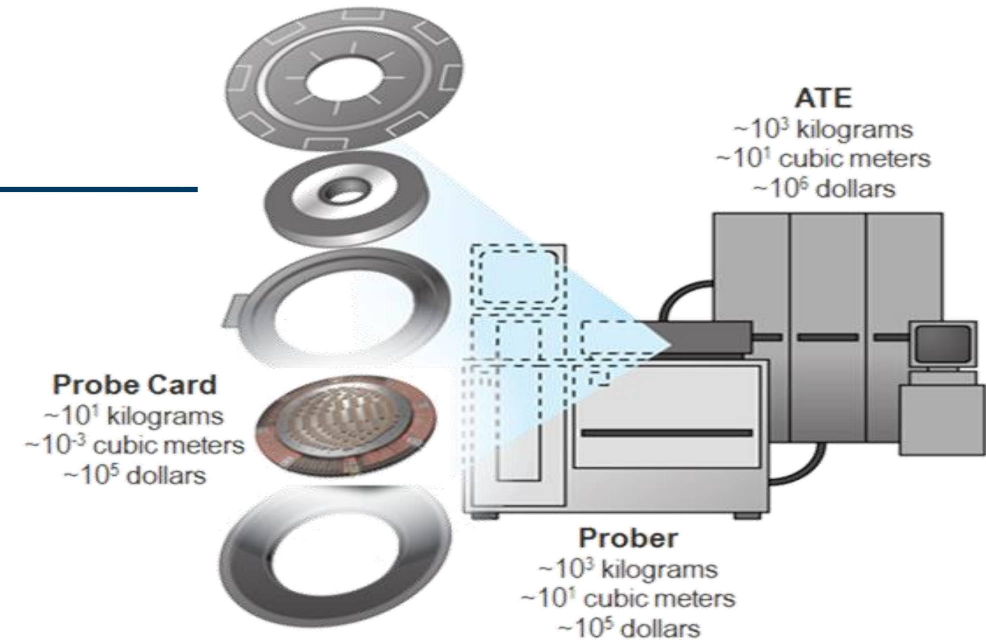
What Is Wafer Test?



- Electrical test after wafer fab, prior to backend assembly / final packaging
- DUT(s)-to-ATE connection typically made through same contacts that connect die to package
  - Wirebond pads, flipchip bumps, copper pillars, etc.
- Key components of wafer-test cell:
  - ATE: Instruments & power supplies to stimulate and interrogate the DUT(s)
  - Prober: Wafer (die) handling, positioning, and environment
  - Probe card: Device-specific interface providing DUT(s)-to-ATE connection

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A Leader in Electrical Test and Measurement

Accelerating Customer Profitability

PROBE CARDS FOR PRODUCTION

50,000,000+ MEMS PROBES/YEAR

PROBE SYSTEMS FOR ENGINEERING

10,000+ INSTALLED PROBERS

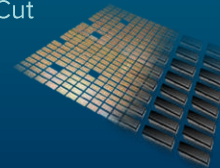
NASDAQ **FORM** SINCE 1993

2018 REVENUE OVER **$500M**

LIVERMORE CALIFORNIA HQ

GLOBAL REACH

1,600 PEOPLE



Why Do Customers Spend $$$ On Wafer Test?

- Avoid wasted cost of packaging a bad die
  - Valuable when yield low and backend cost high
  - Test cost must be << bad-die packaging cost
- Inform an adjustment/trim/change
  - Exercise redundancy (DRAM)
  - Feedback for frontend fab process changes
- As outgoing QC for product title transfer
  - Bare-die sales (or wafer-packaged die)
  - Foundry-fabless-OSAT handoffs

Wafer Test Coverage

Die Yield		Packaging Cost: Low	Packaging Cost: High
	High	Zero	Some
	Low	Some	Lots

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What Do We Mean By "Advanced Packaging"?

intel

2D AND 3D PACKAGING DRIVE NEW DESIGN FLEXIBILITY

The combination of advanced 2D and 3D packaging technologies allows Intel to flexibly combine smaller chiplets of IP to meet the demands of a huge range of applications, power envelopes, and form factors. Intel® embedded multi-die interconnect bridge (EMIB) and Foveros are advanced 2D and 3D packaging technologies, delivering high performance at low cost.

MONOLITHIC
Integrate functions on a single die for high performance on a single silicon technology

2D INTEGRATION
Combine IPs built with separate processes into a single package with Intel EMIB, helping improve yield, cost, time-to-market, and total capability

3D INTEGRATION
All the benefits of 2D integration plus a new level of density thanks to Foveros, allowing for a radical re-architecture of systems-on-chips

Source: https://newsroom.intel.com/wp-content/uploads/sites/11/2018/12/2d-and-3d-packaging-drive-new-design-flexibility.jpg

Assembly of multiple, heterogenous dies either directly to each other or through interfaces with interconnect densities and electrical performance comparable to that of the individual component die

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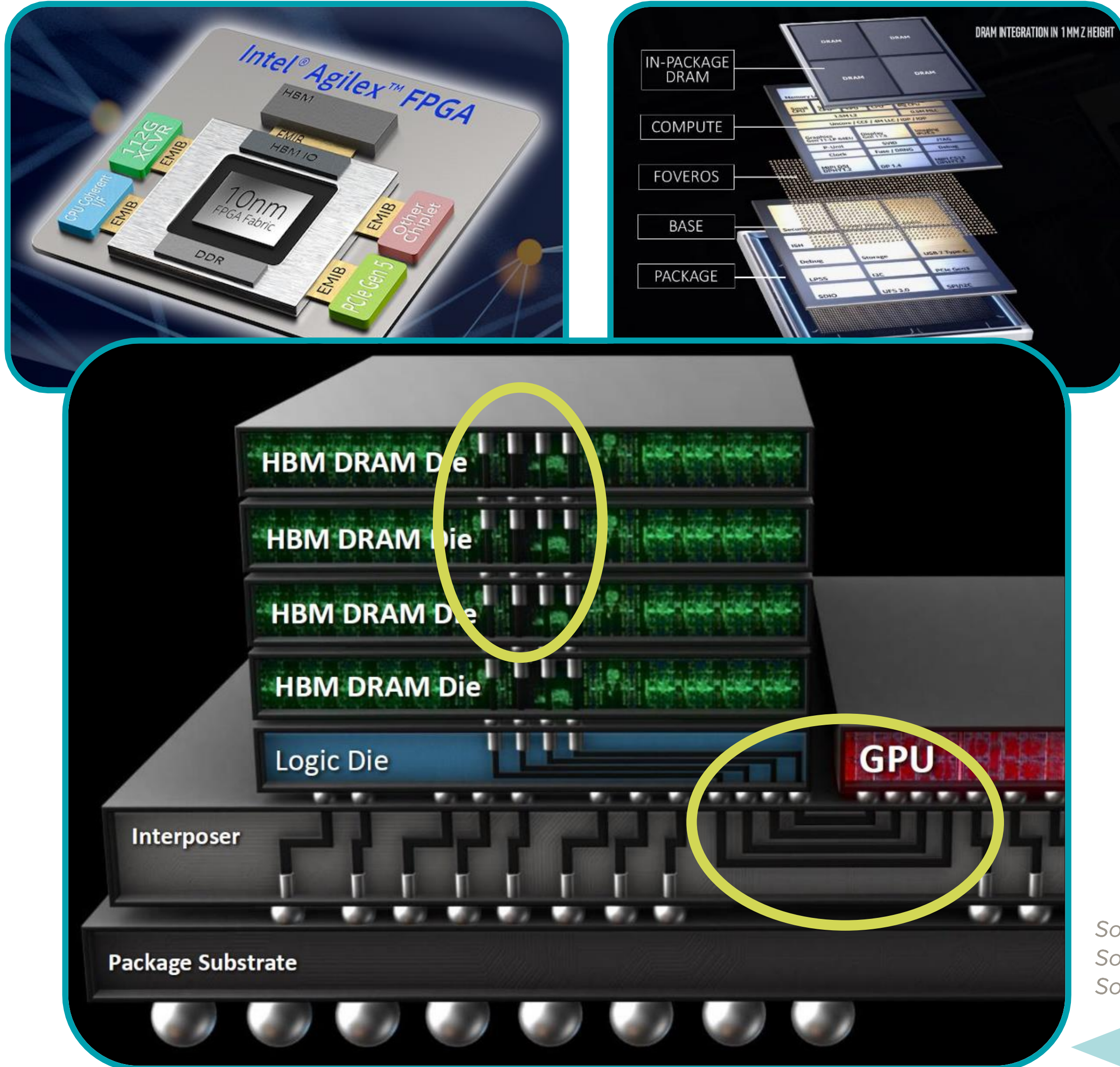
Advanced Packaging Examples – FPGA, CPU, GPU



- Heterogenous integration:
  - 7nm/10nm high-perf core GPU, CPU, FPGA
  - 1Xnm/2Xnm lower-power cores
  - 1Ynm LPDDR/GDDR – up to 8 layers!
  - Other logic, display, comm, I/O functions
  - Mix/match best technologies
- Silicon interposer density enables wide high-speed buses/interfaces
- 10,000s vertical signal pipes (TSVs) at 40µm~60µm pitch
- Smaller, faster, lower-power, cheaper

Source: https://www.anandtech.com/show/14211/intels-interconnected-future-chipslets-emib-foveros
Source: https://www.techspot.com/news/81708-intel-lakefield-cpu-using-3d-foveros-possibly-spotted.html
Source: https://www.anandtech.com/show/10527/sk-hynix-adds-hbm2-4-gb-memory-q3

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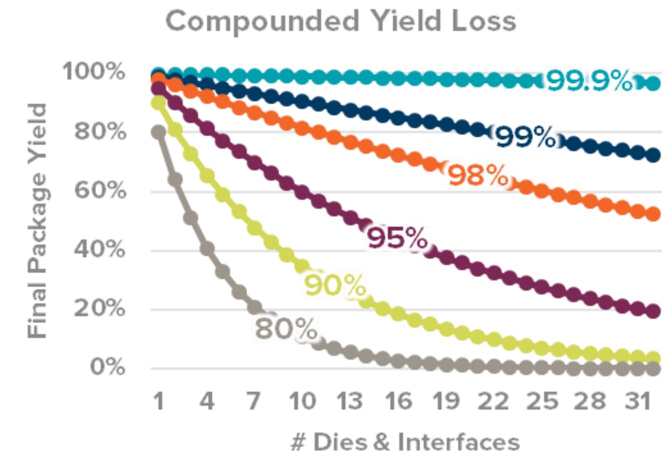
How Does Advanced Packaging Impact Test? Coverage!

- Final test of assembled package is necessary, but provides limited insight to improve performance and yield
- Ideally, each component is good before integration
  - Nirvana is Known Good Die (KGD)
  - Test every individual die, and every stacking step along the way?
- Economics dictate something shy of KGD
  - Pre-package wafer test is fundamentally scrap-cost avoidance
  - Final-test and system-test opportunities prevent escapes
  - Schedule, risk tolerance, etc. are other practical considerations
- Cost vs. coverage optimization comes down to math
  - Compromise = Probably Good Die (PGD)
  - Hedge bets – e.g., design interposers/ bridges with redundant vias, and build repairability into each HBM sub-die
  - Balance test coverage to catch higher-probability/impact issues, while accepting risk of lesser issues slipping through to final test



Wafer Test Coverage

Die Yield	High	Zero	Some
	Low	Some	Lots
		Low	High
		Packaging Cost	

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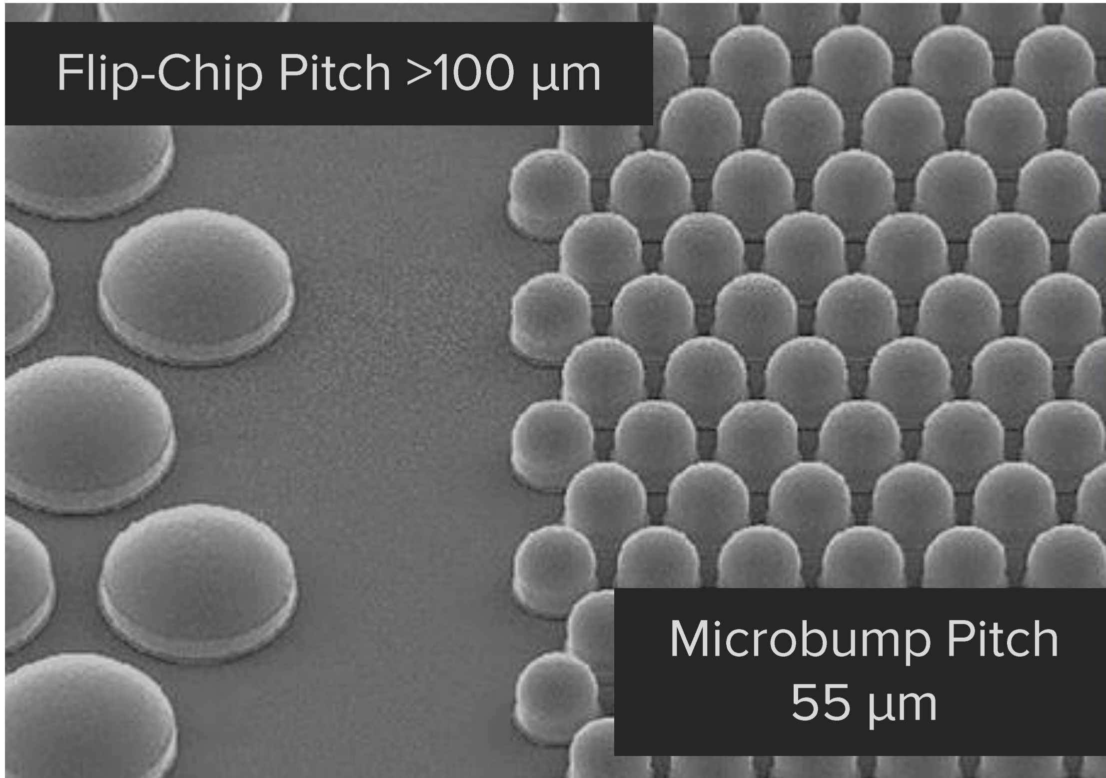
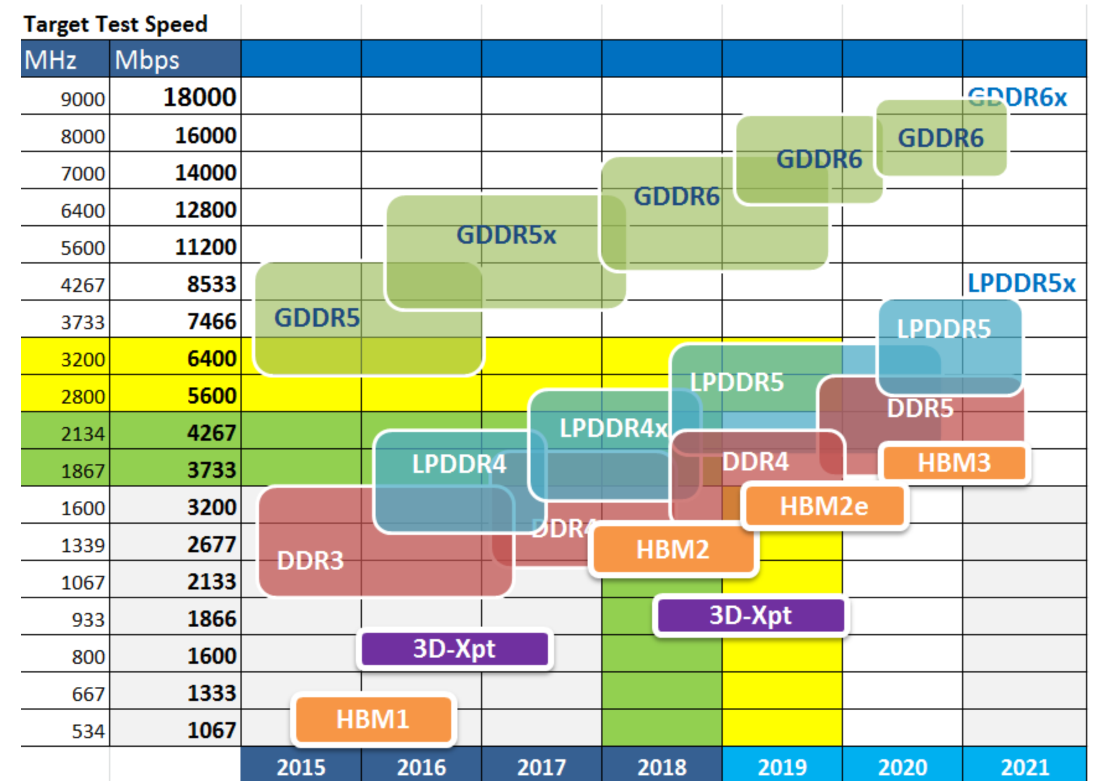
How Does Advanced Packaging Impact Test? Complexity!



https://www.tomshardware.com/news/intel-emib-interconnect-fpga-chiplet,35316.html



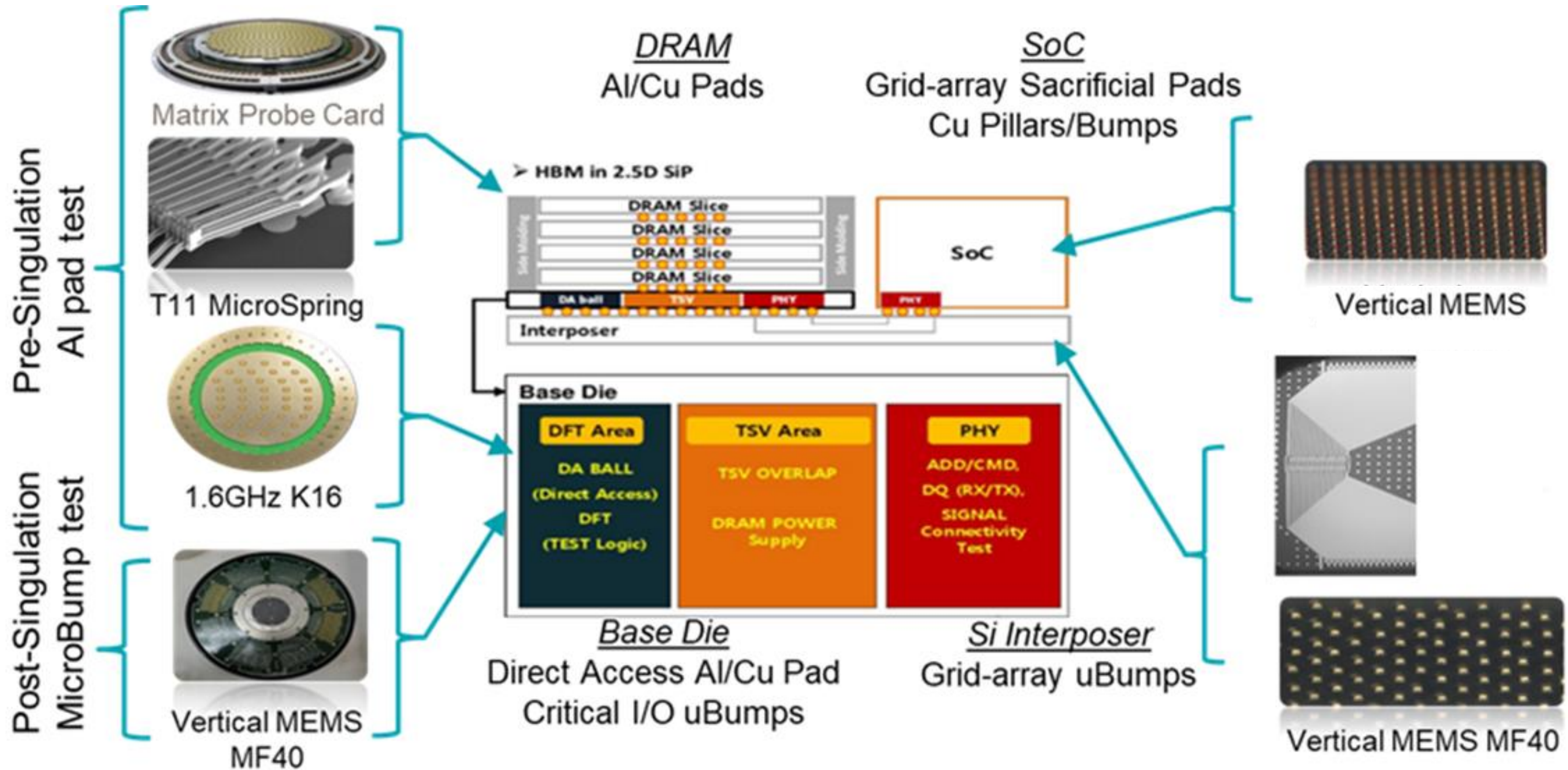
Spatial/Mechanical – Higher Density

- Smaller pitches and higher probe counts
- More delicate contacts (new materials)

Electrical – Higher Performance

- Higher clock speeds, nearing RF frequencies
- Increased current per contact, higher power density

What to Test? So Many Possible Test Insertions...



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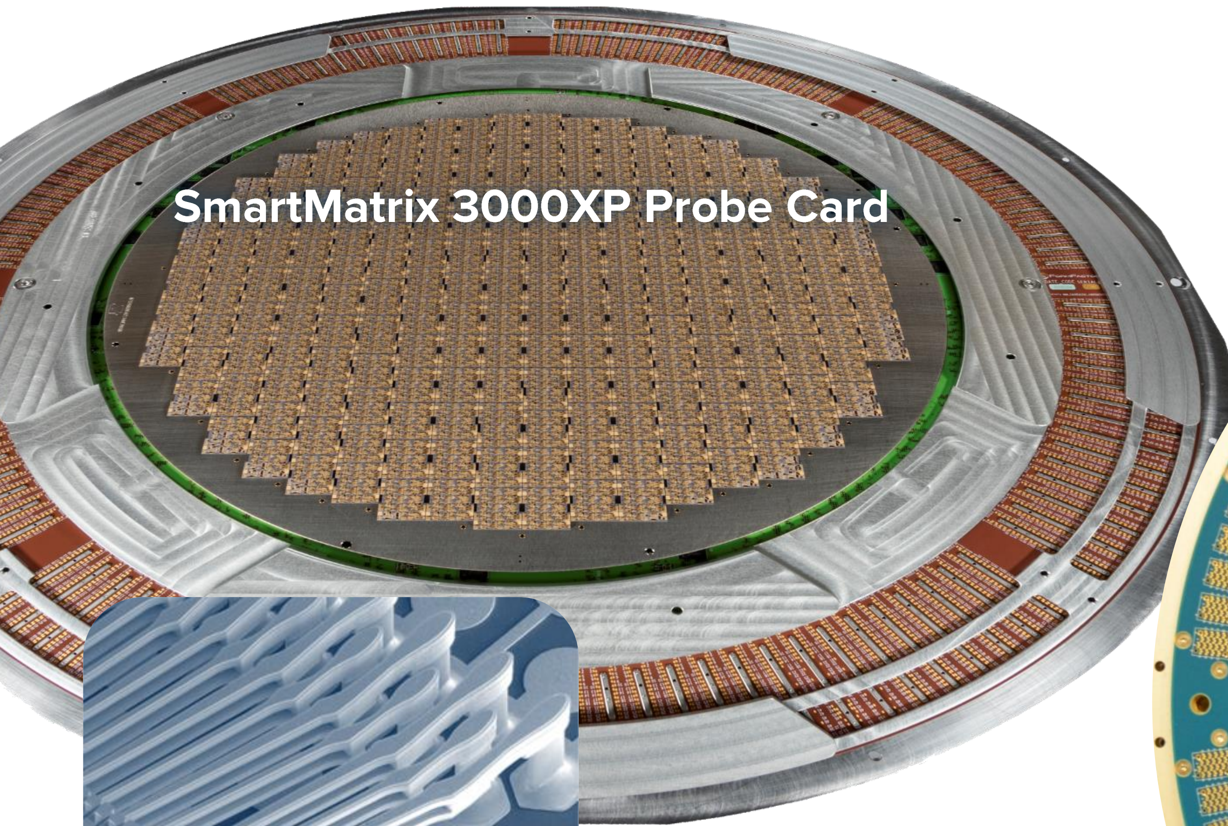
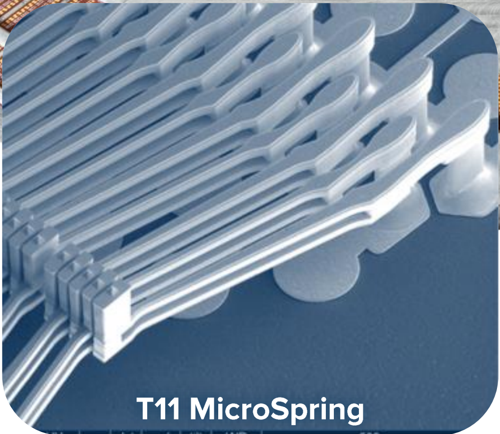
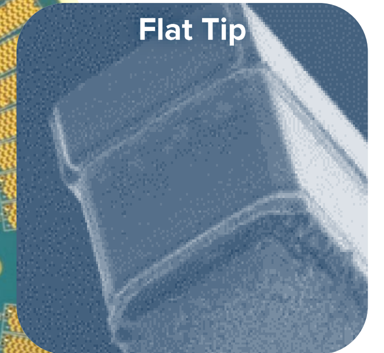
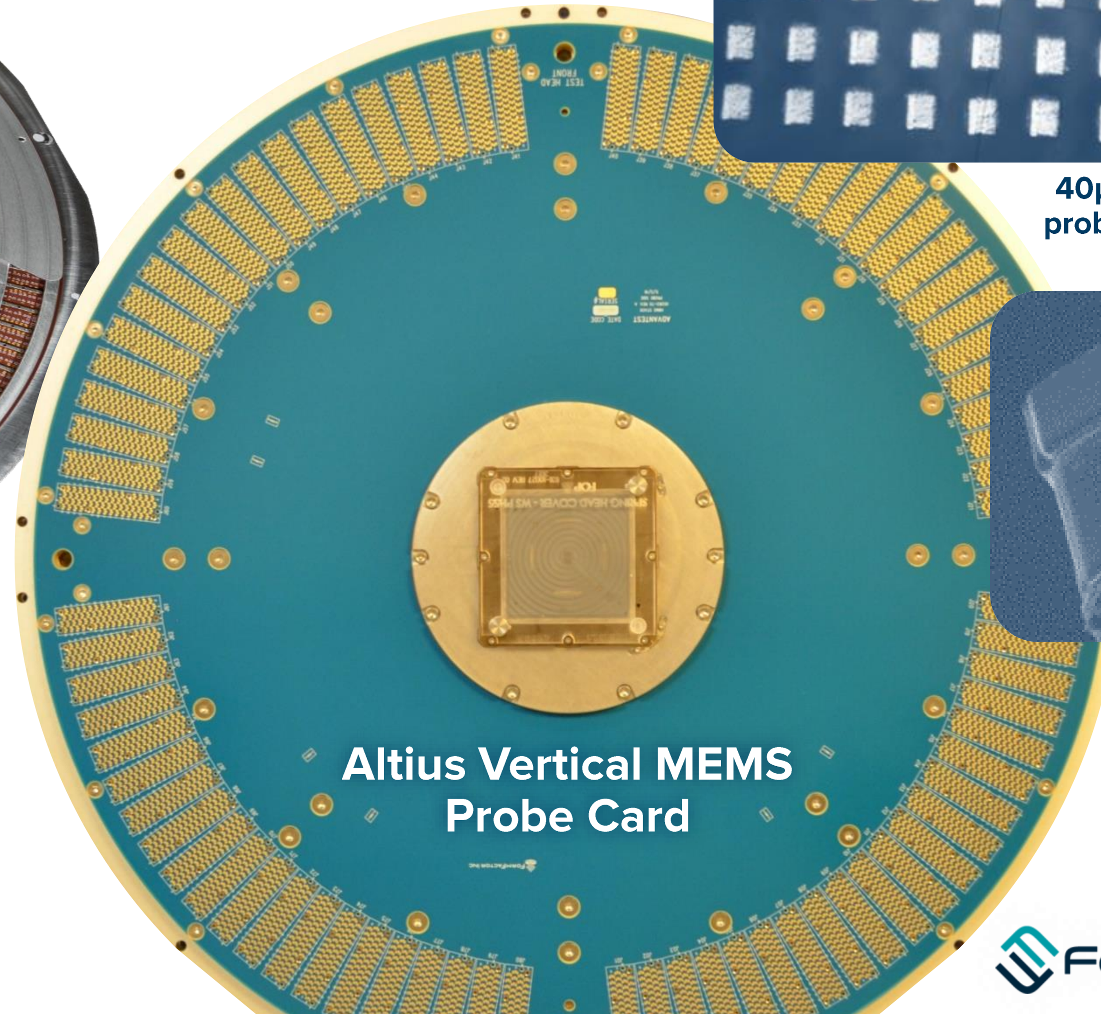
Fortunately, Good Solutions Exist Today



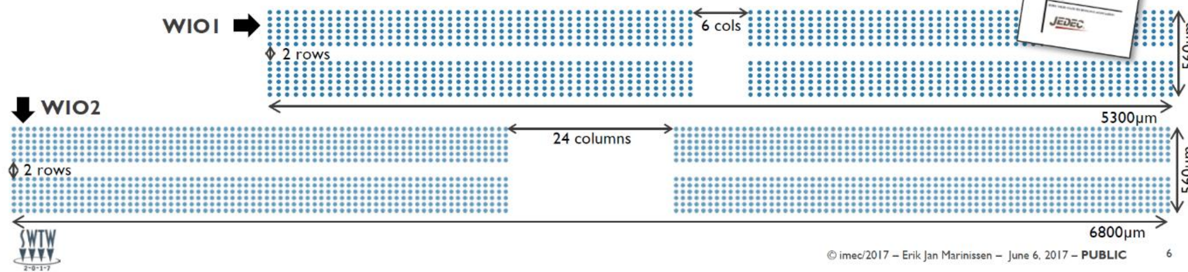


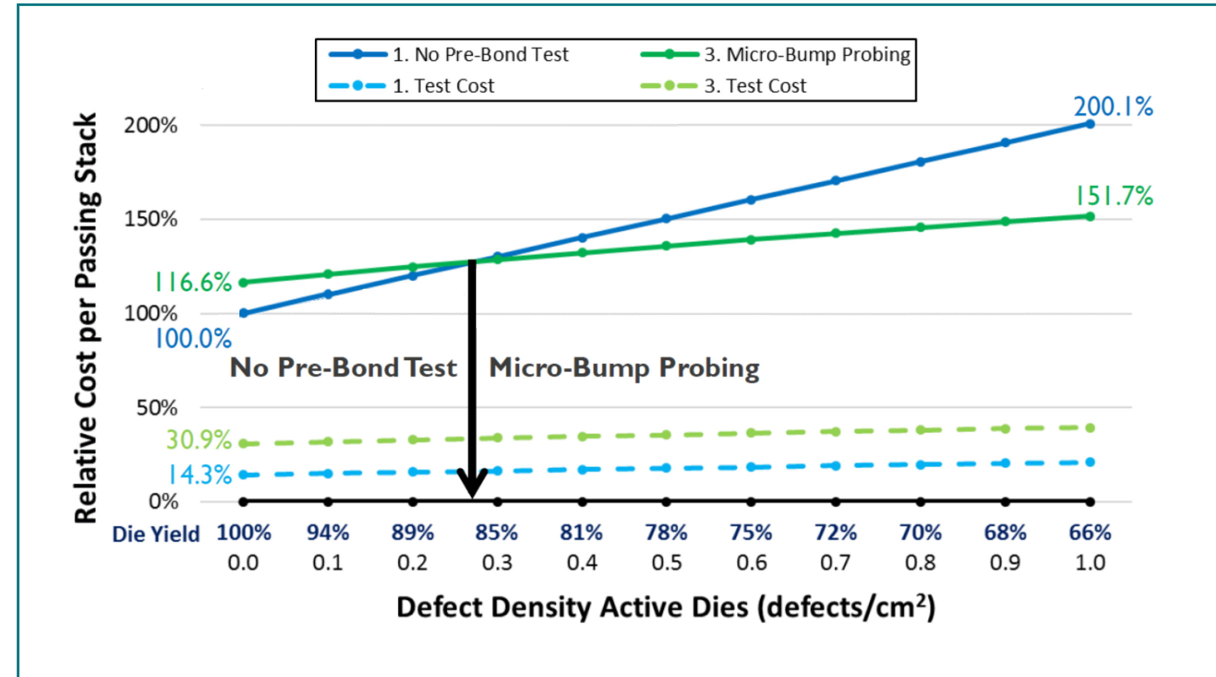
40µm pitch MEMS probe tip grid array





Example – Directly Probing Microbumps on Interposer on Wafer





Source: Marinissen (IMEC) and Kiesewetter et al (FormFactor), SWTW 2017

- Probing directly on microbumps on wafer prior to packaging can be done

- Depending on yield, it might (or might not) save money in the end – decide using data

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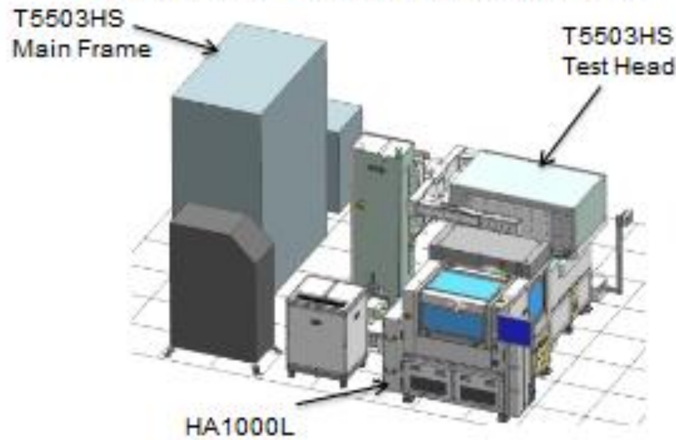
Example – Probing Microbumps on Singulated HBM

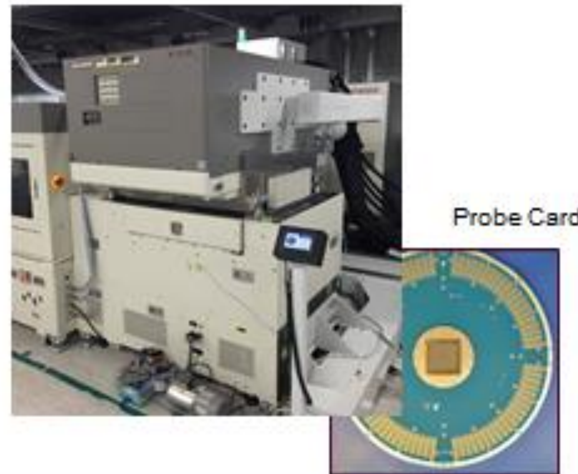
Direct micro-bump probing – Bare Die Handler

Die Handling & Micro Bump Contact are needed

HBM KGSD Test Solution

- HA1000L : Die Level Handler (Advantest)
- T5503HS : Memory Test System (Advantest)
- Probe Card : Probe Card for HBM (FFI)

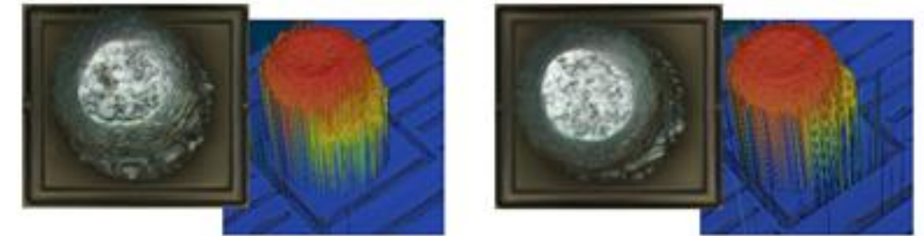


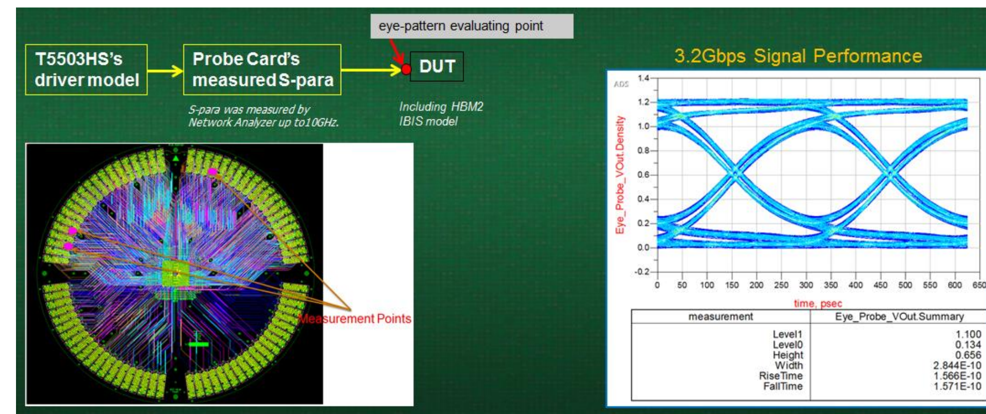


COMPASS 10

Source: Kiyokawa (Advantest) and Nhin (FormFactor), COMPASS 2019

Condition	T.T:600sec 1 time	T.T:600sec 2 times
Scrub depth[um]	2.61	2.99
Scrub diameter[um]	14.81	15.04





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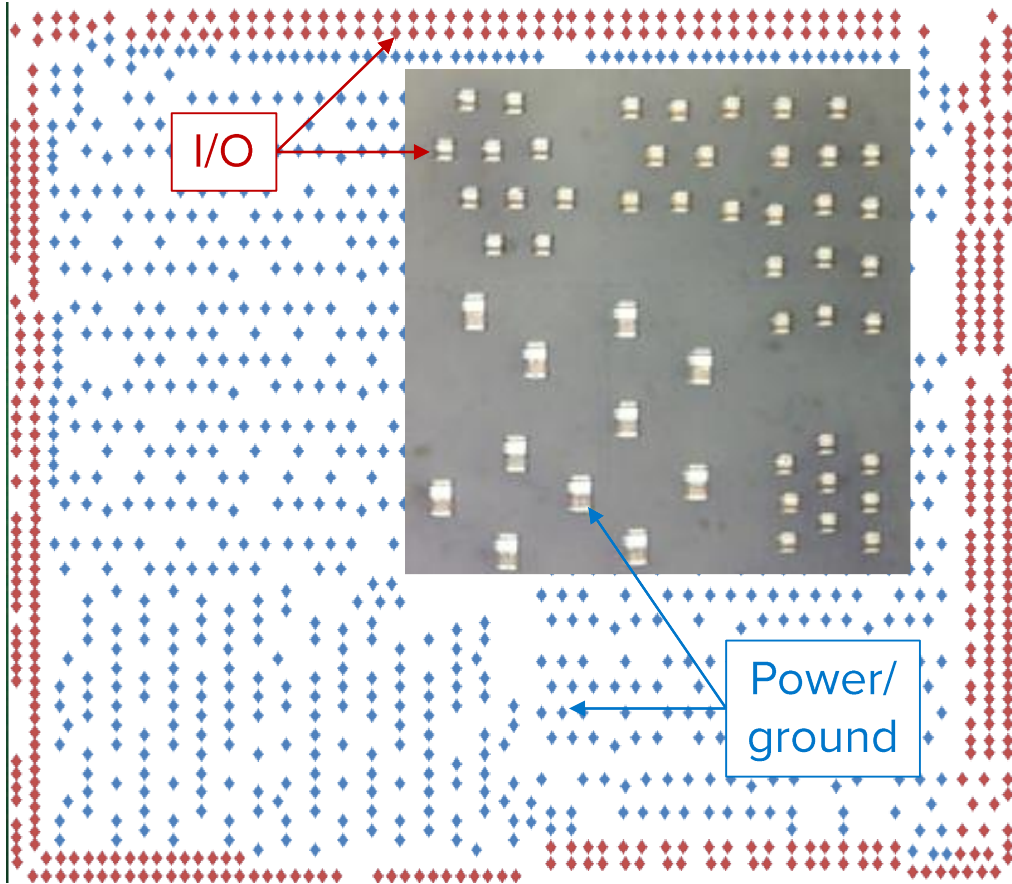
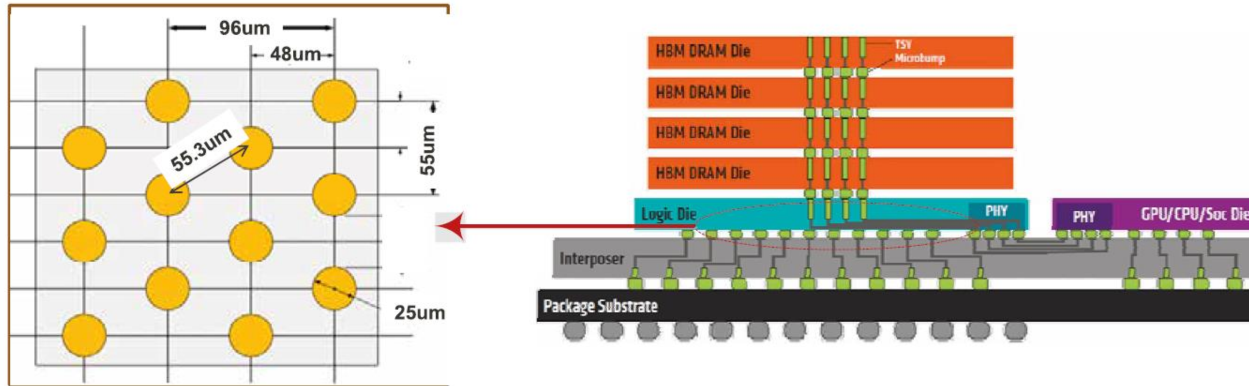
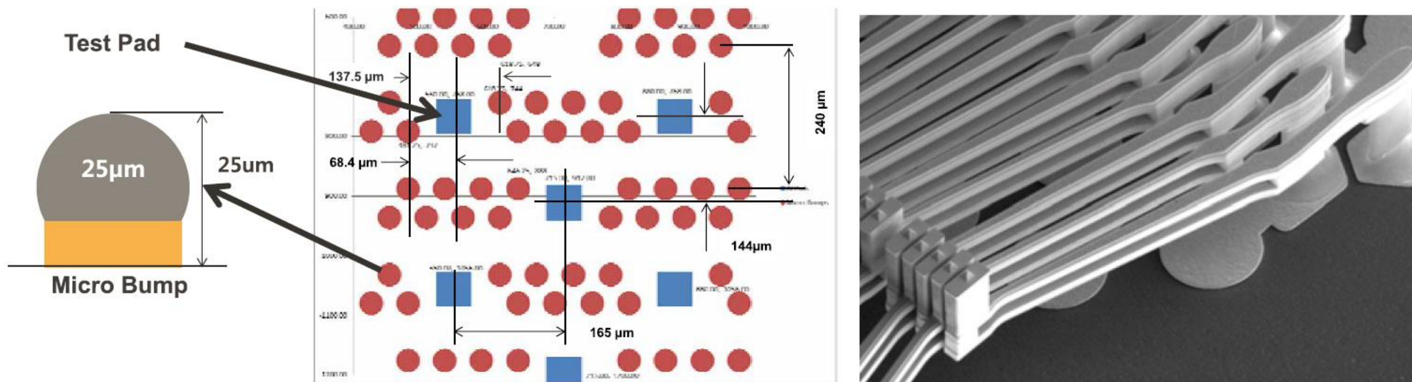
Example – In-Die Microbump Optimization



- Small I/O bumps – small/gentle probes
  - But smaller I/O probes risk burnout and reduced life for higher-current power/ground connections
- Higher-current power/ground bumps – larger/stiffer probes
  - But power/gnd probes risk damaging I/O bumps
- Rather than compromise, decouple require-ments with a Hybrid MEMS probe card
  - Composite metal MEMS technology to match force, wear, etc. per probe
  - Much higher uptime (reduced probe burn events)
  - 40% improvement in power impedance
  - Many permutations possible

Example – HBM with Test Pads Instead of Microbumps



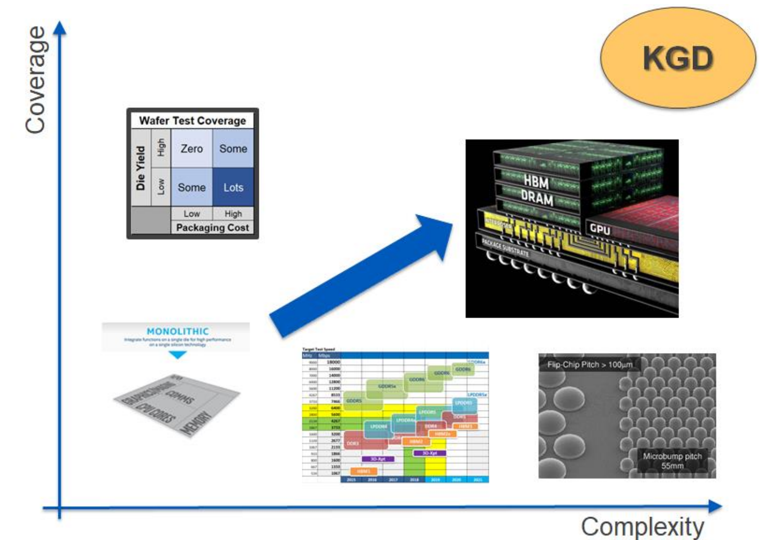


- Redundant pads = possible alternative to directly probing microbumps
- Advantage:
  - Doesn't damage microbumps
- Challenges:
  - May consume/increase die real estate
  - May constrain test coverage (fewer signal connections)
  - May impact high-speed signal performance (different routing)

Source: Loranger+Yaglioglu (FormFactor) and Oonk (Teradyne), IEEE Design & Test 2016

Summary and Conclusions

- Advanced packaging will fill the vacuum left by the end of Moore’s Law
  - Burden shifts from front end (lithography/inspection) to back/middle end (assembly/test)
- Technical challenges
  - Microbumps can be probed directly, with sufficiently advanced probe card technology
  - But it’s not easy – trends include smaller/denser/non-flat targets, higher frequency signals
- Economic challenge
  - Packages are expensive (many steps, component dies)
  - Final test alone provides no info to correct/improve
  - KGD is ideal, but expensive
  - Balance test coverage cost vs. package yield loss cost
  - Test multiple insertion points to optimize test coverage
- Optimized test program requires data
- Solutions available today



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Thank you!

Q & A