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Packaging Material Characterization and Modeling

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Binghamton, New York?

New York and beyond

Syracuse

SUNY Albany

Rochester Infotonics

Buffalo Bioinformatics

Syracuse Photonics, Phillips,…

Albany Sematech, GE…

SUNY Buffalo

Rochester RIT

Rome AF base

Cornell

Alfred

SUNY Binghamton

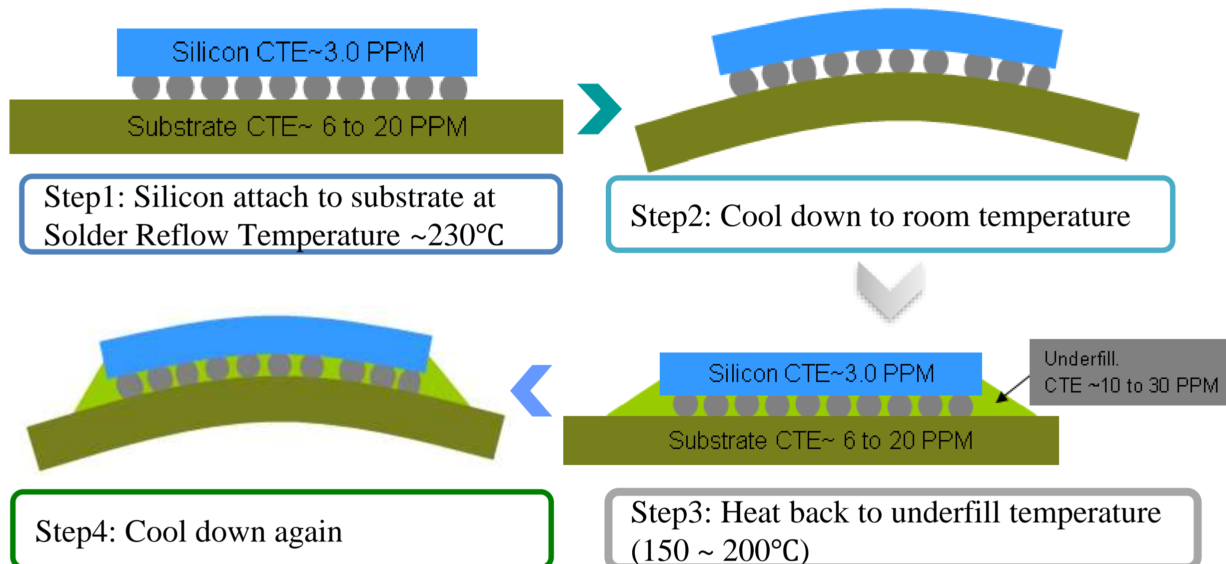
Hudson Valley IBM,…

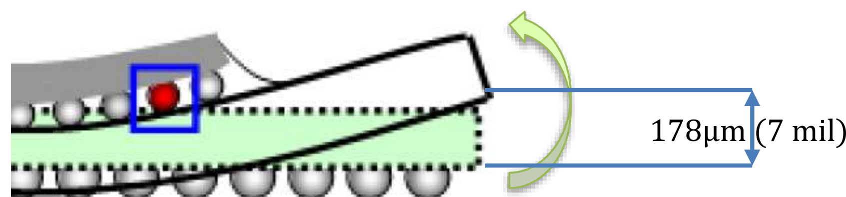
SUNY S.B.

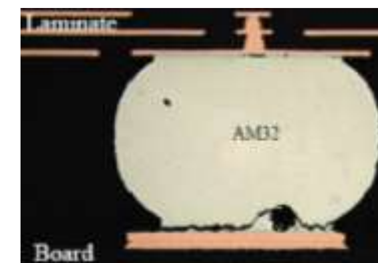
CUNY

Composite Nature and Warpage

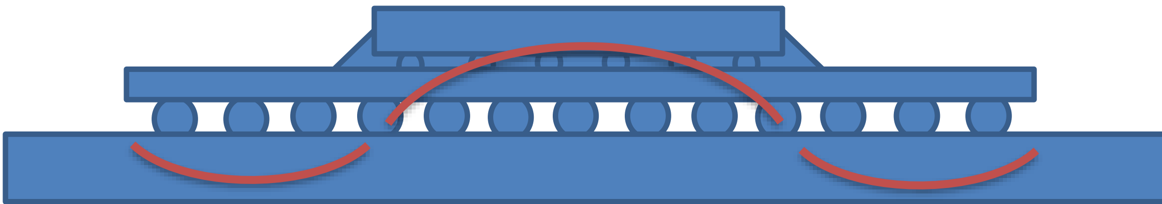
- In most packaging architectures, manufacturing steps occur at elevated temperatures when the assembly is nearly plat. As cooling takes place, out-of plane deformation can occur due to CTE mismatches.
  - Non-uniform expansion/contraction of die and substrate in temperature cycle.
  - Results in warpage of the package which is major reliability concern.







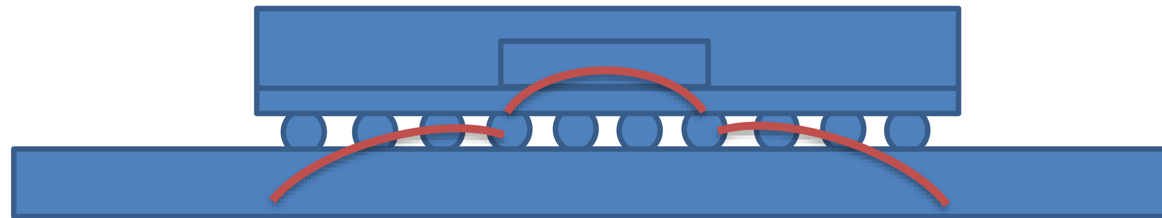
Warpage of Advanced Packages/Assemblies
a Prime Driver of *BGA Failure*

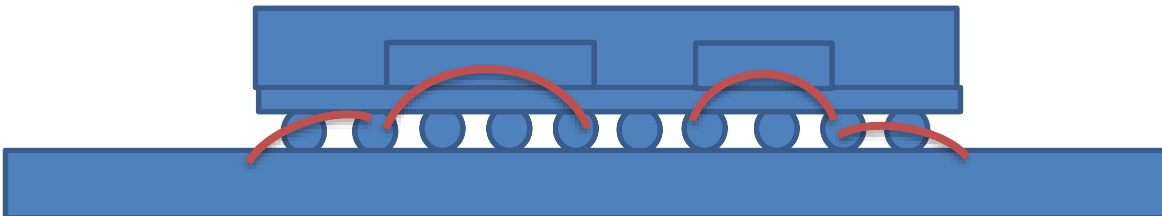


Typical FC-CSP

Die Shadow Effect

Largest DNP BGA





FOWLP / MUF Packages

Die Shadow Effect

Largest DNP BGA

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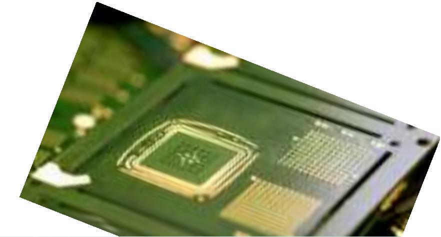
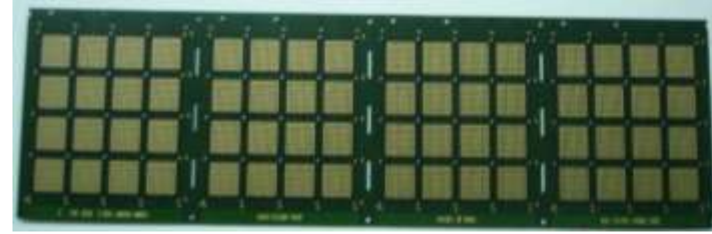
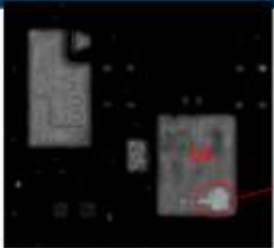
Warpage Driven MUF Delamination



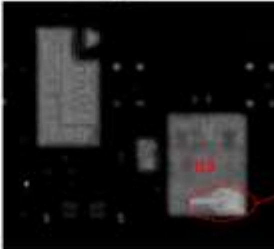
Laminate Strip



MSL3



3362540.2_#17



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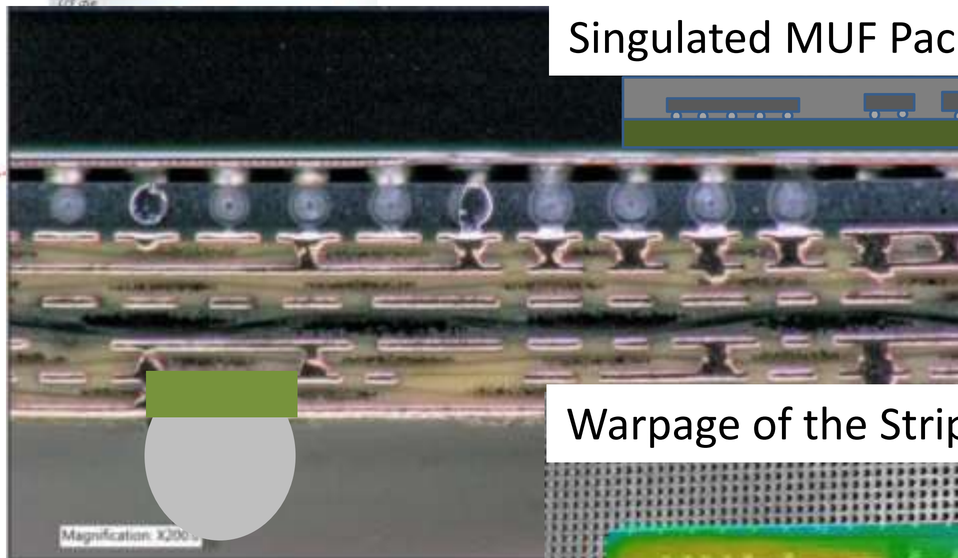
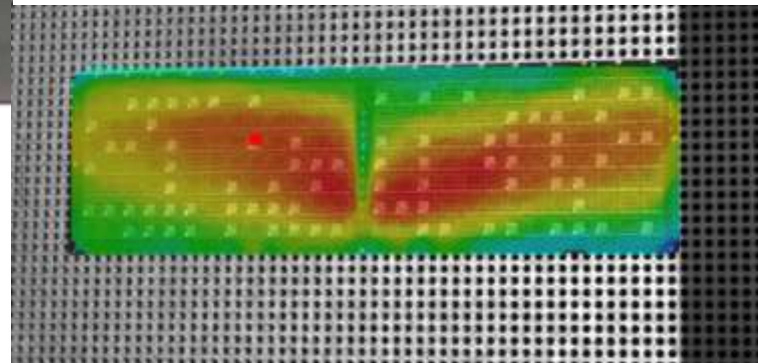


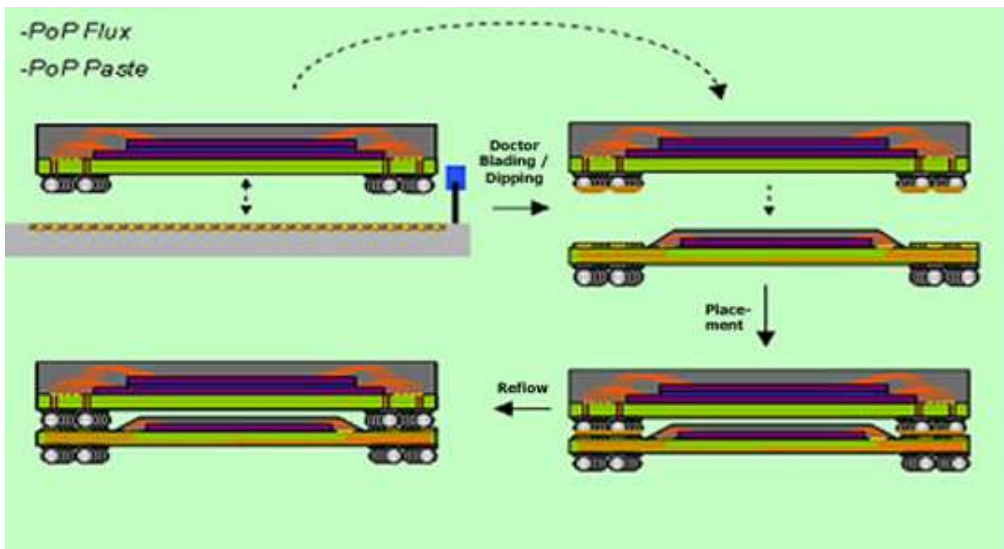
Singulated MUF Package

Warpage of the Strip in Reflow Temp

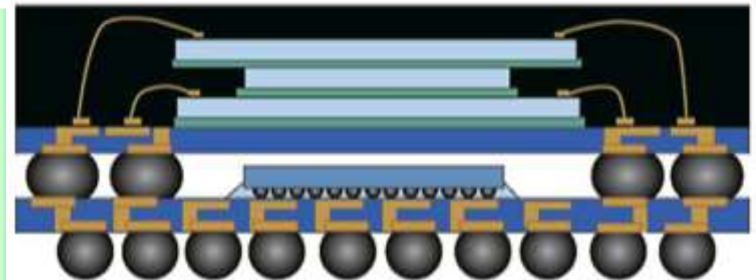


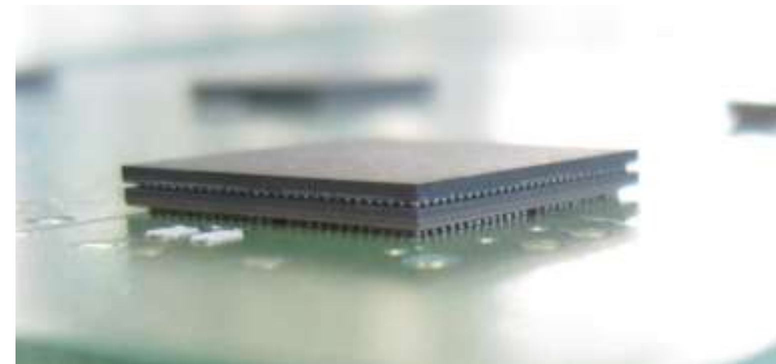
Warpage

- Moore's Law: the number of transistors in a dense integrated circuit doubles approximately every two years.
- Advanced Solution: The integration level becomes higher and higher. More and more layers are stacked on each other.



Package to package method





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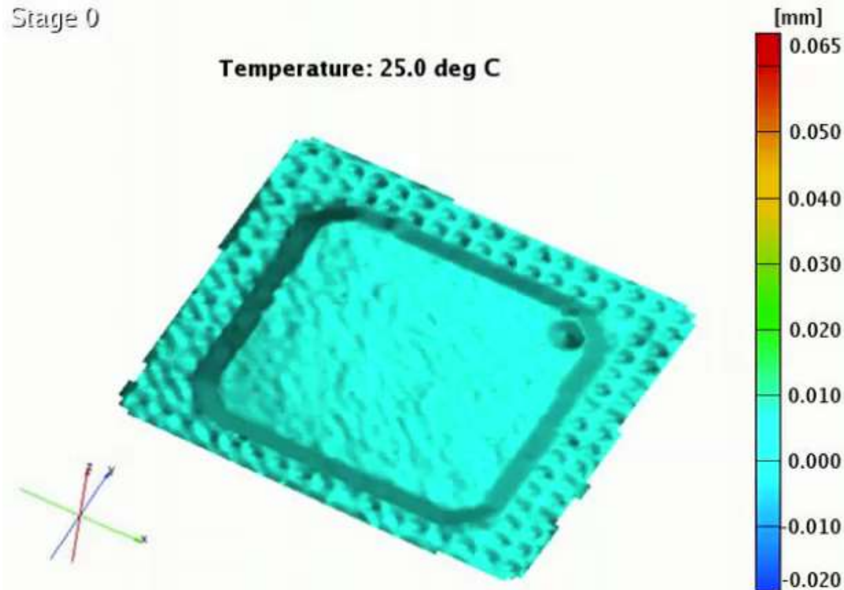
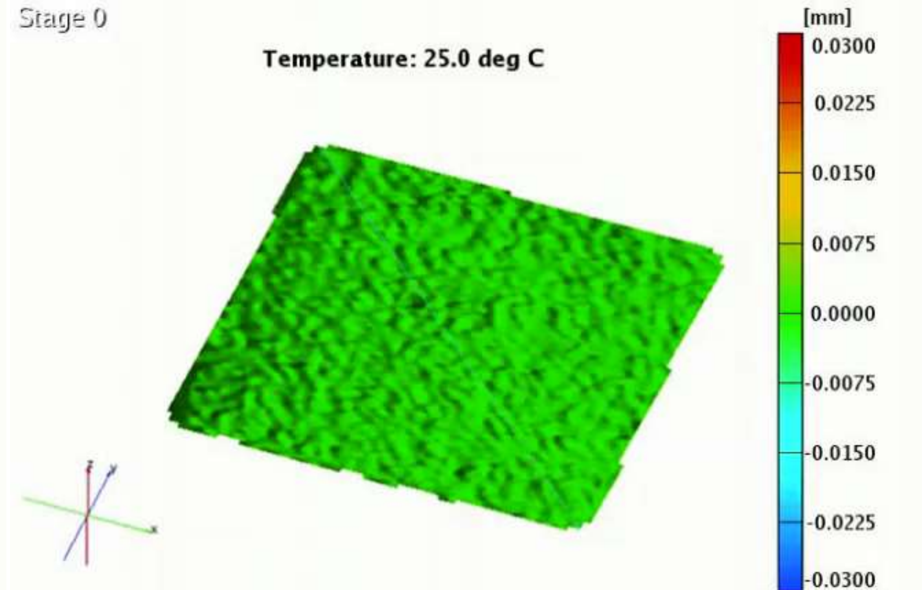
Warpage Measurement of 15x15 PoP



Top side of bottom Package



Bottom Side of Top Package

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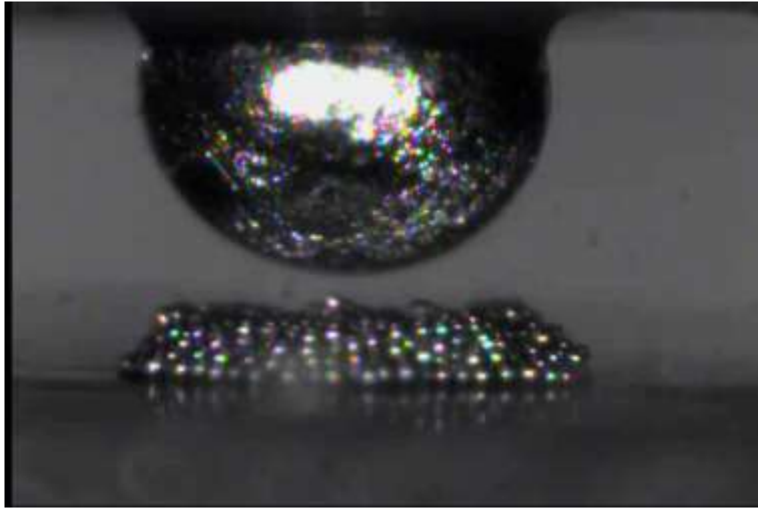
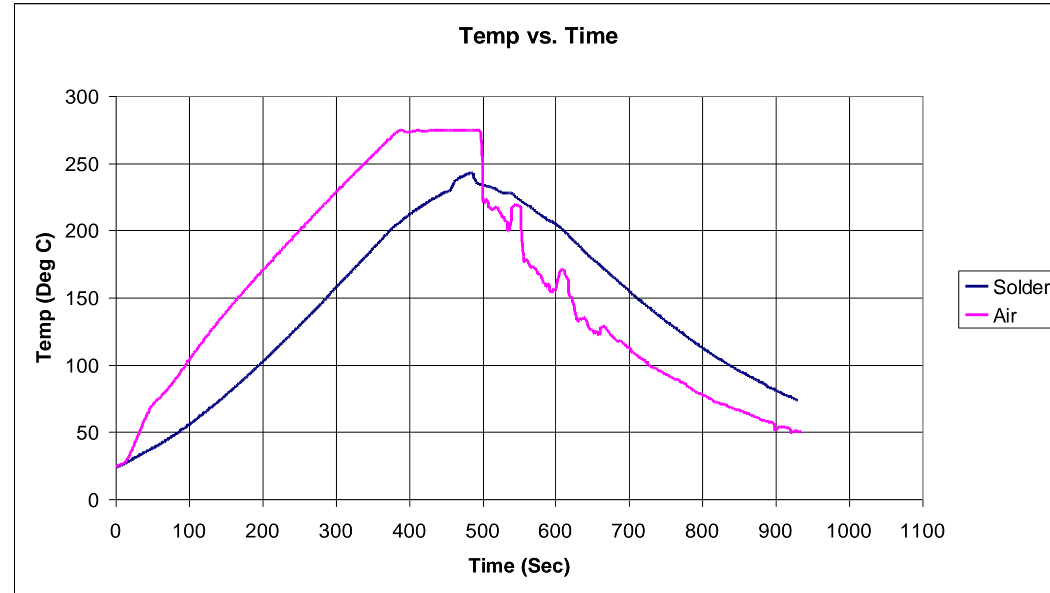
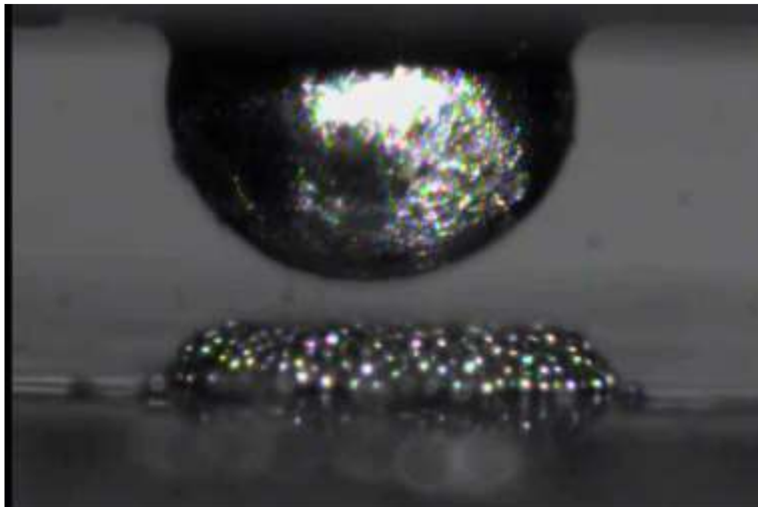
Warpage Driven Yield Loss

Wettable Gap Measurement

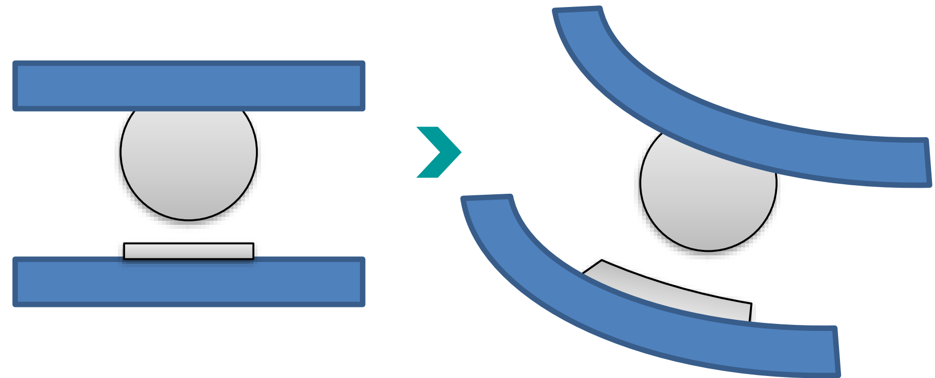


80μm





85μm not pop



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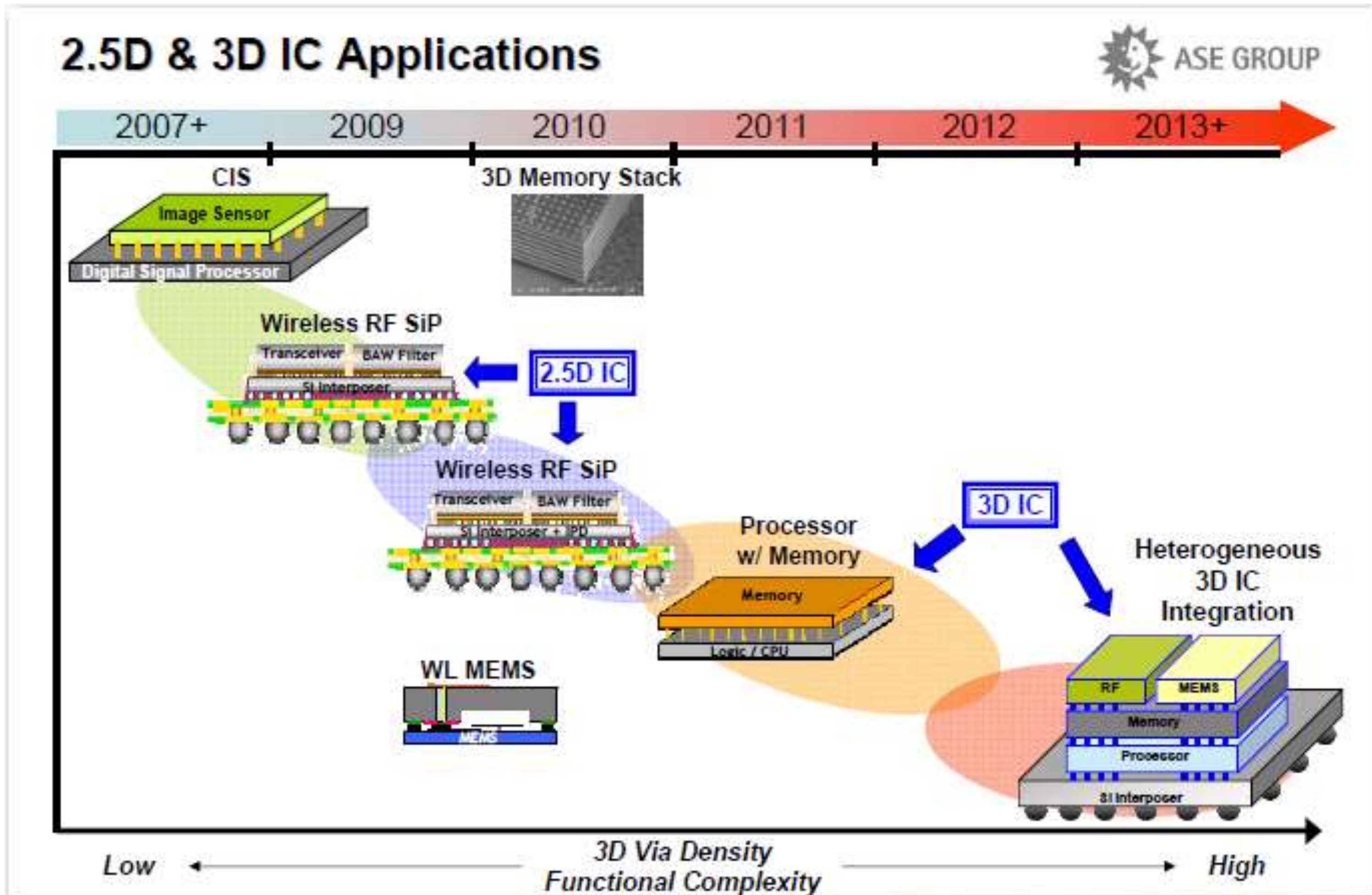
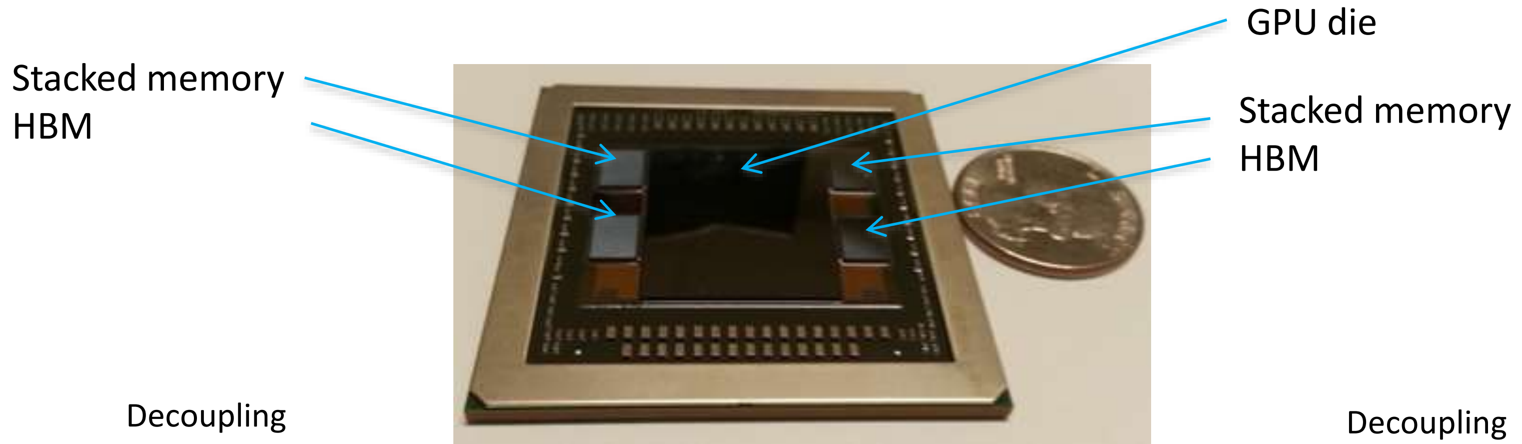
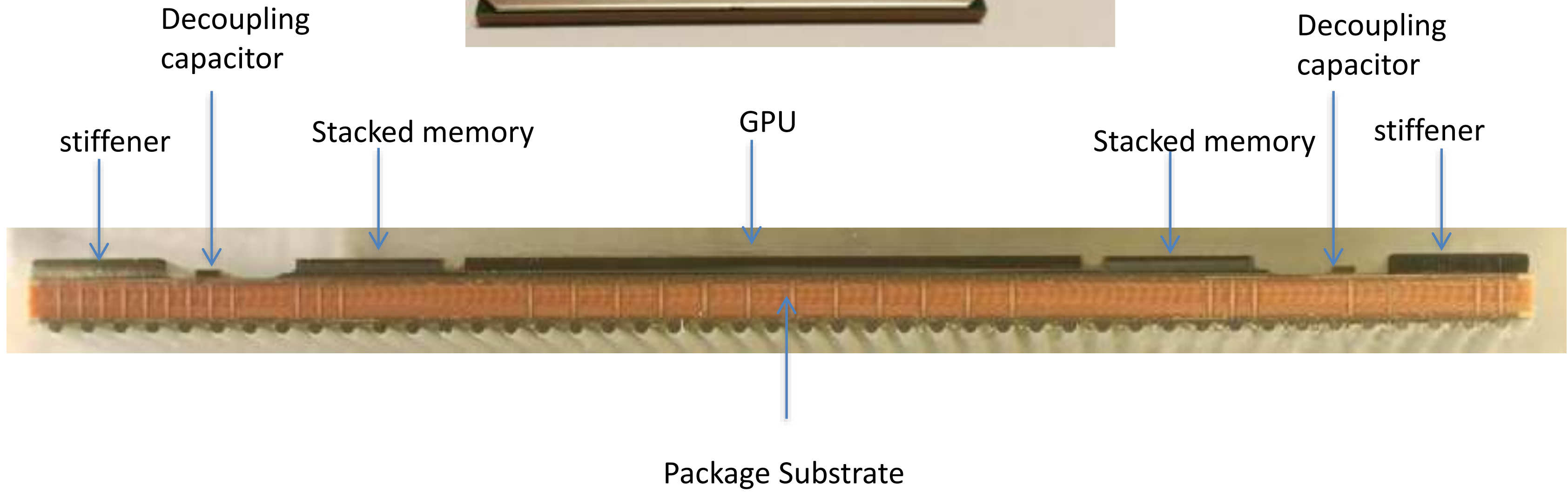
More Complicated Warpage

- As the integrated circuit packaging density increasing, 2.5D packaging and 3D packaging were developed.
- More and more layers are stacked on each other, the CTE mismatches between each layers is becoming more critical.



AMD Fiji Package





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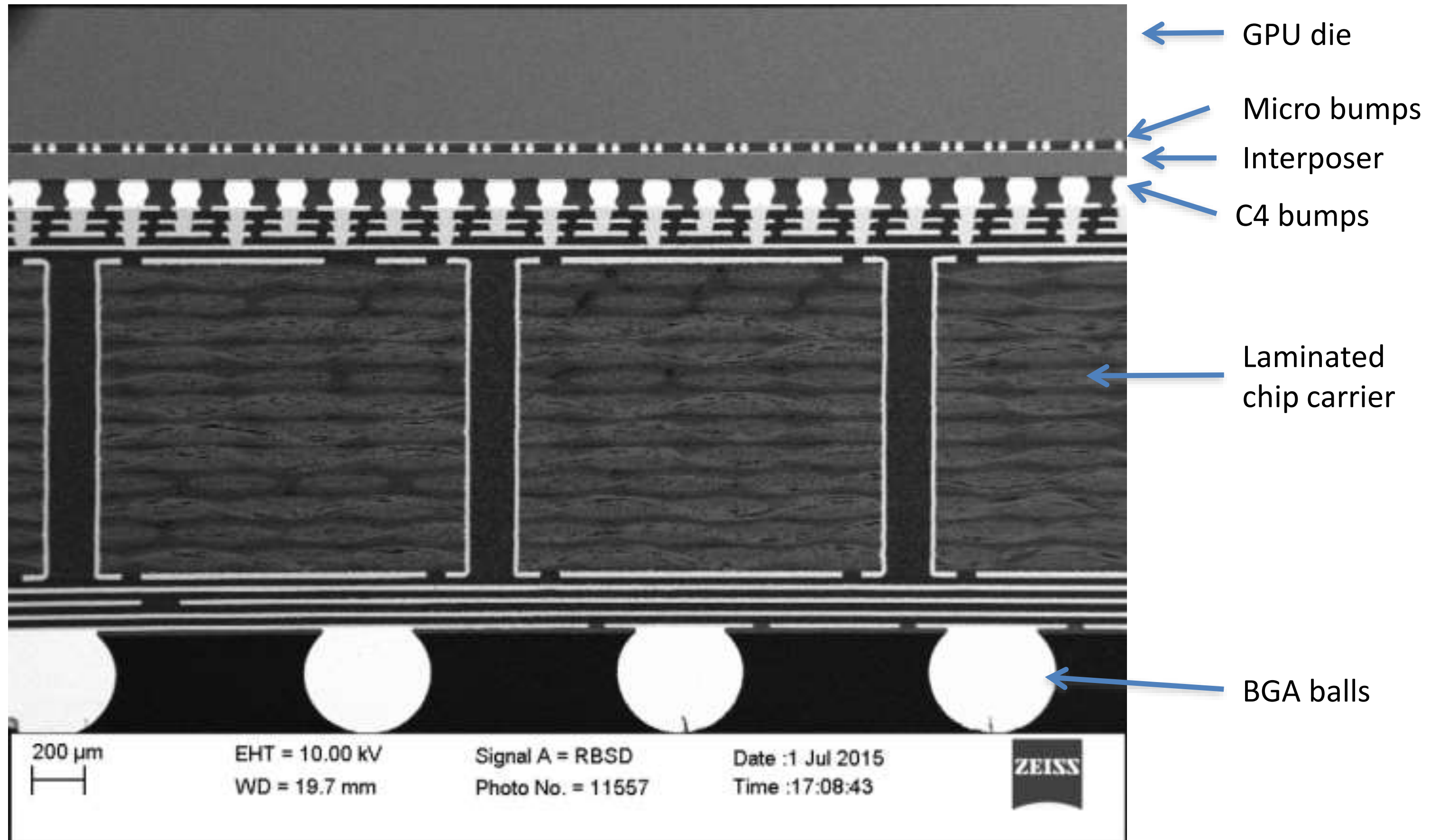
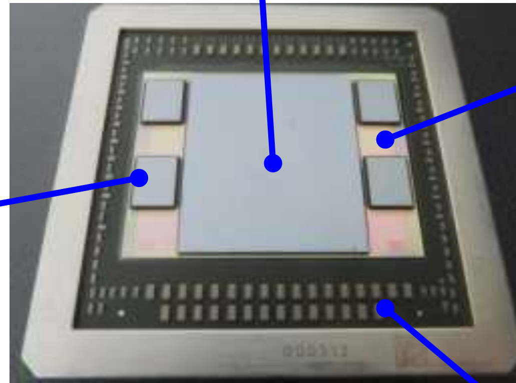
Cross Section of GPU Die



Major Technology Challenges

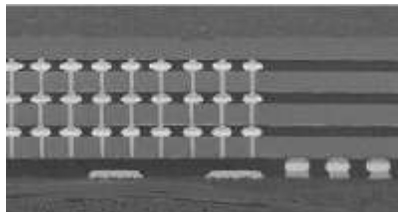
ASIC
- Large die size
- Fine pitch (~40 um)
- High bump count (> 200k)

High Bandwidth Memory (HBM)
- High bump density (~5k)
- Small UBM (25um)
- Inspection thru stacked dies (4 DRAM + 1 Logic inside)



Interposer
- Huge die size
- Double side handling
- High pad count
- High C4 count (> 20k)
- Warpage control

Package
- Package warpage control



(Source: Hynix)

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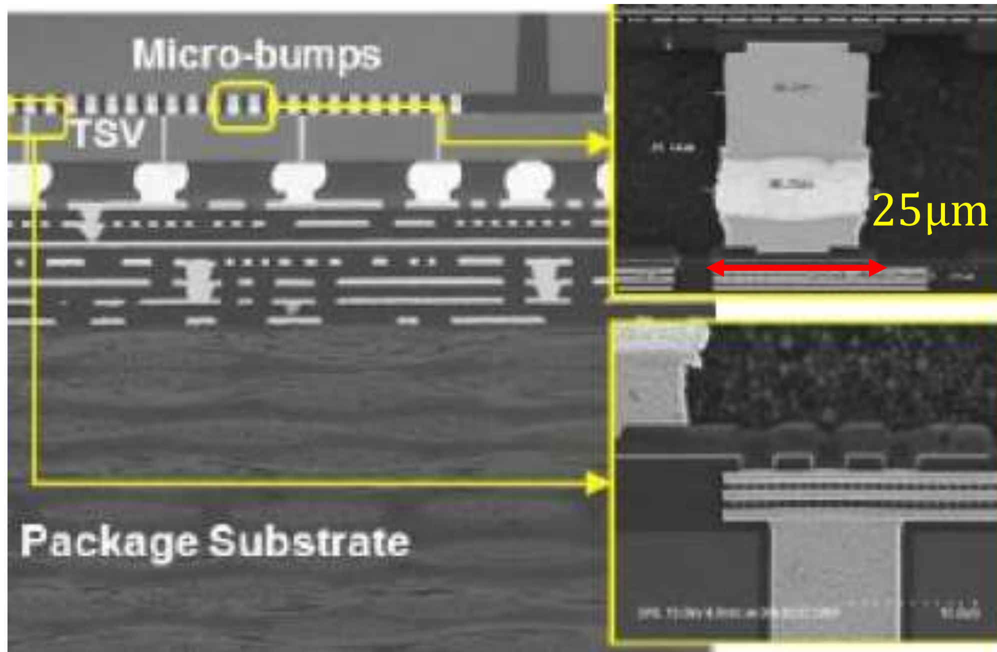
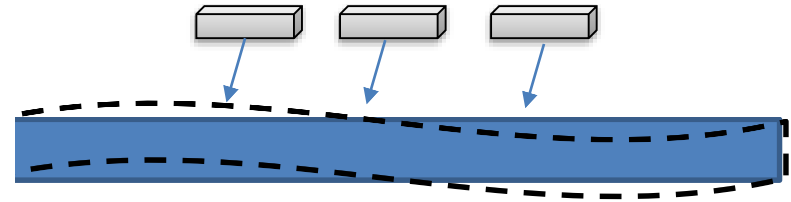
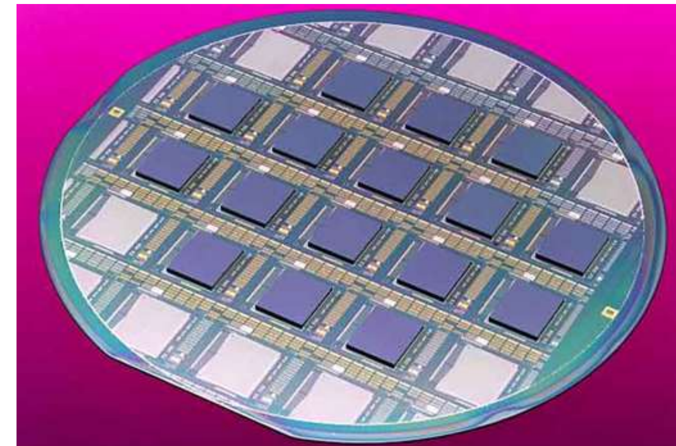
Wafer Warpage

- In chip to wafer or wafer to wafer bonding, the warpage of wafer may lead to serious damage of the devices during thermal compression boning process.







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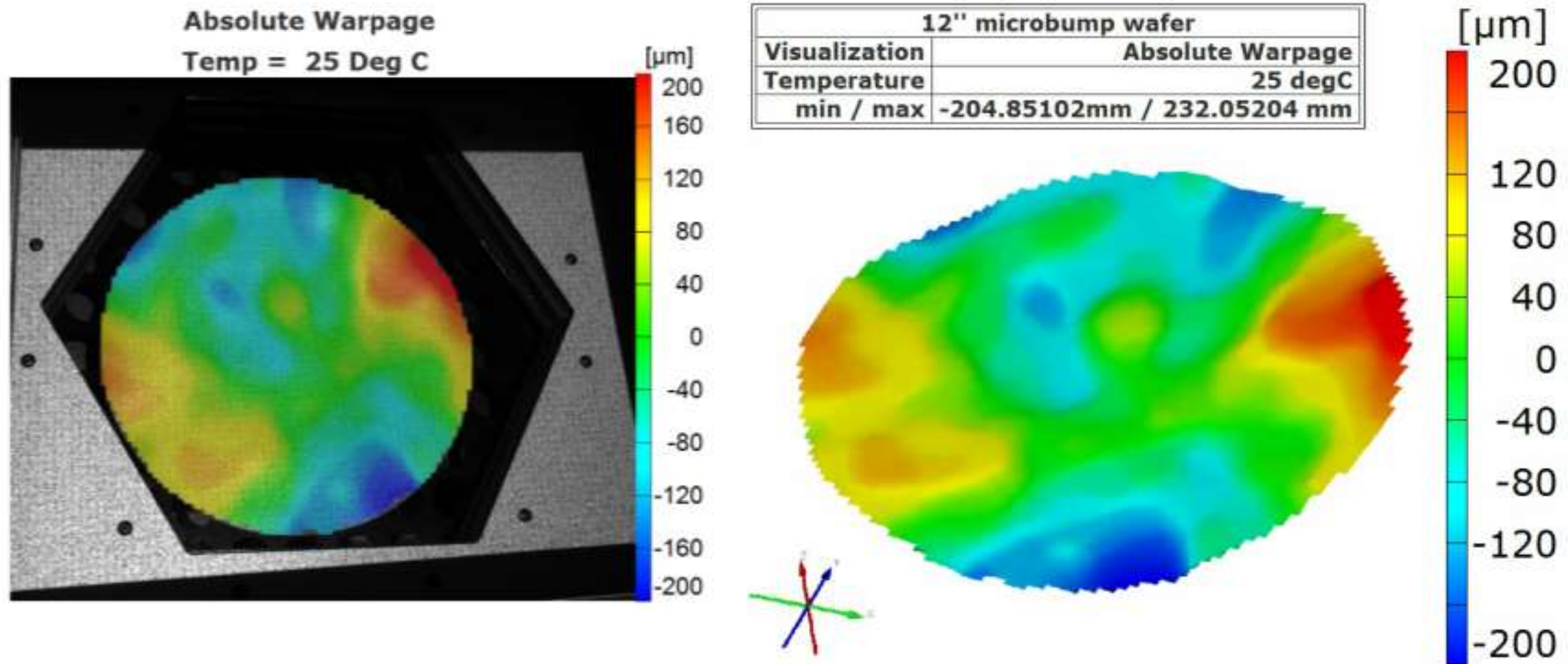
Wafer Warpage During Reflow

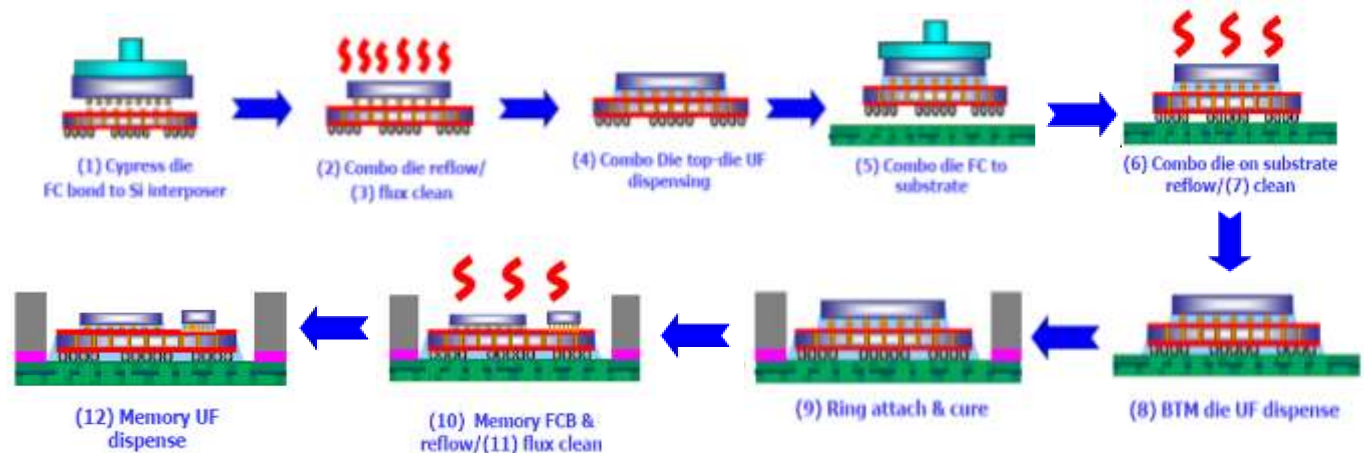
- After solidifying the 3D DIC speckle-free method, a 12 inches fully circuited and back-ground wafer is measured from 25°C to 240°C to demonstrate the method effectiveness.



Warpage

During Assembly Process

- Due to the more and more sophisticated structures, **warpage** has been a main concern during **assembly process.** It is one of the root causes of failures in manufacturing processes causing open interconnect.



Assembly flow of TSV interposer package

- The package undergoes reflow process **three times**. It might lead to the product failure before the final step.
- An in-situ warpage measurement method to monitor the package warpage during assembly process is necessary.

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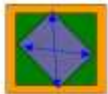
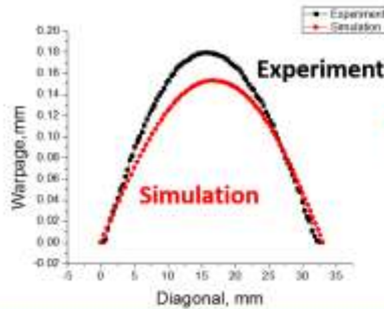
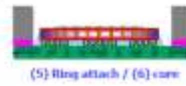
Beyond Traditional Modeling -Assembly Process Modeling

Sim. Vs. Exp. for sample I (substrate+interposer)

Interposer (front side)

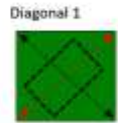




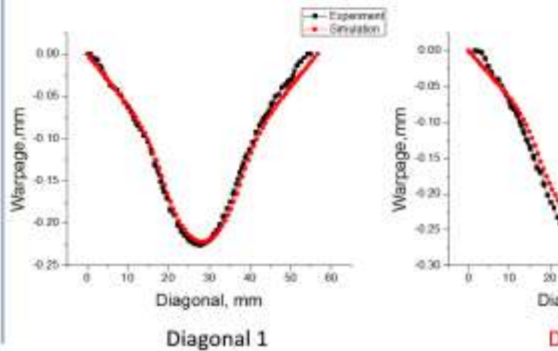


Substrate (backside)

Diagonal 1



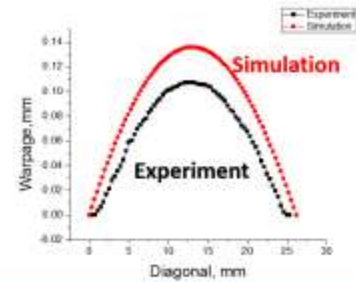
Diagonal 2



Diagonal 1

Sim. Vs. Exp. for sample II (sub.+int.+GPU)

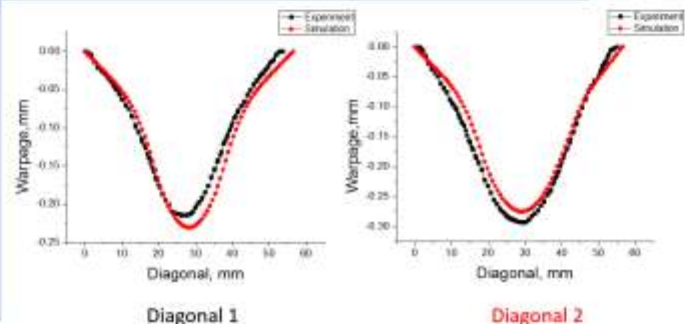
GPU (front side)



Substrate (backside)

Diagonal 1

Diagonal 2



Diagonal 1

Diagonal 2

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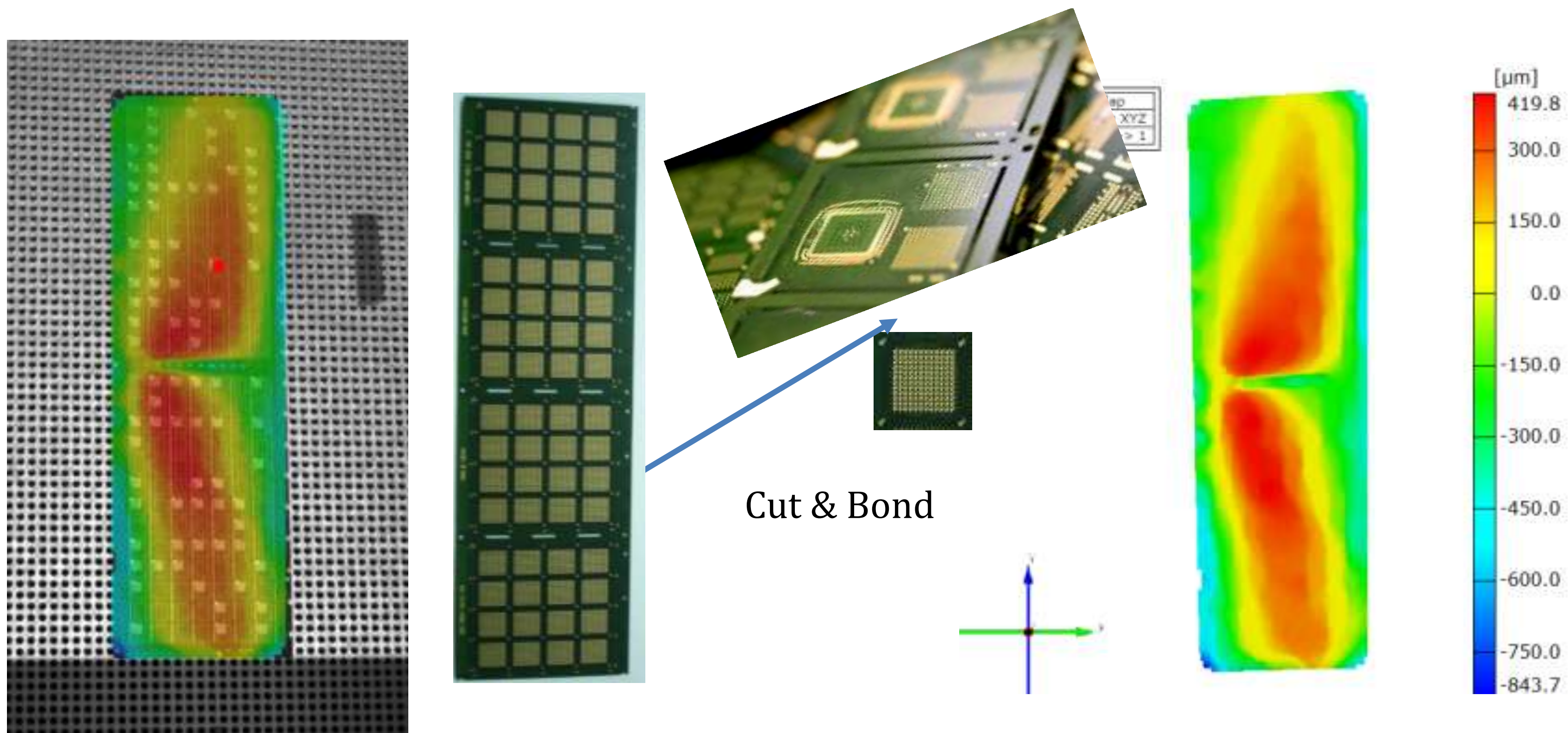
Strip Substrate Warpage Measurement

- Strip substrate is quite thin and light. So it can be warped easily before assembly process. Once it warped, the individual substrate will be affected due to the whole strip warpage.
- It is thin and sensitive, conventional DIC surface treatment will contaminate the specimen and reveal the actual warpage distribution.



Speckle-free 3-D DIC test on a strip substrate

Case 1

µ-bump underfill's isothermal shrinkage and Reliability Impact

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Underfill Material Behavior Under Thermal Aging

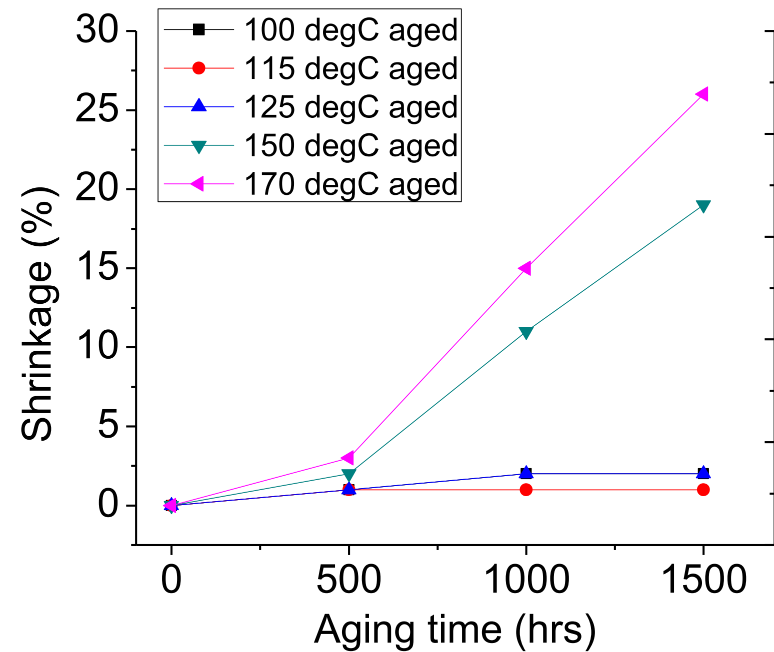
Underfill Fracture Toughness K_{IC} degradation

K1c	100C	115C	125C	150C	170C
0hrs	**2.2**	2.2	**2.2**	**2.2**	2.2
500hrs	**2.1**	2.0	**1.8**	**1.7**	1.5
1000hrs	**2.0**	2.0	**1.5**	**1.4**	1.2
1500hrs	**2.0**	2.0	**1.5**	**1.2**	1.0

(unit: MPa*m^0.5)

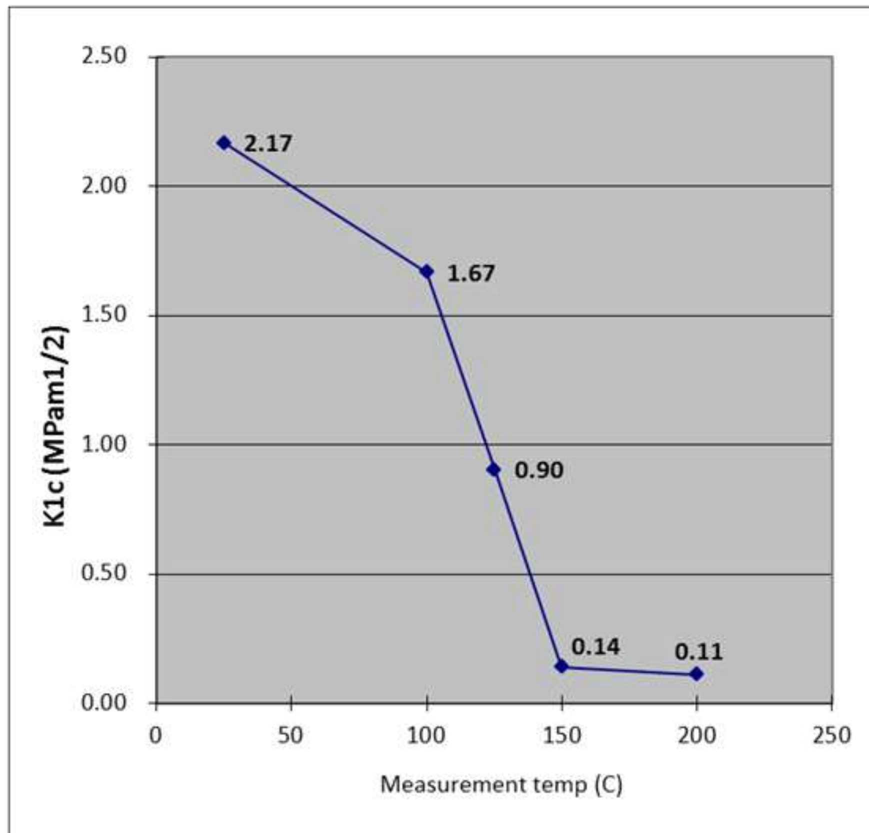
Underfill shrinkage

Shrinkage%	100C	115C	125C	150C	170C
0hrs	**0**	0	**0**	**0**	0
500hrs	**1%**	1%	**1%**	**2%**	3%
1000hrs	**2%**	1%	**2%**	**11%**	15%
1500hrs	**2%**	1%	**2%**	**19%**	26%



Underfill Material Behavior
Fracture toughness temperature dependence

- Fracture toughness is dependent on the in-situ temperature, as seen in the graph, K_{IC} of the μ-bump underfill is decreasing as the temperature gets higher.
- χ_{UF} is to identify the degree of G_{IC} decrease when temperature is elevated from 25°C to 150°C.

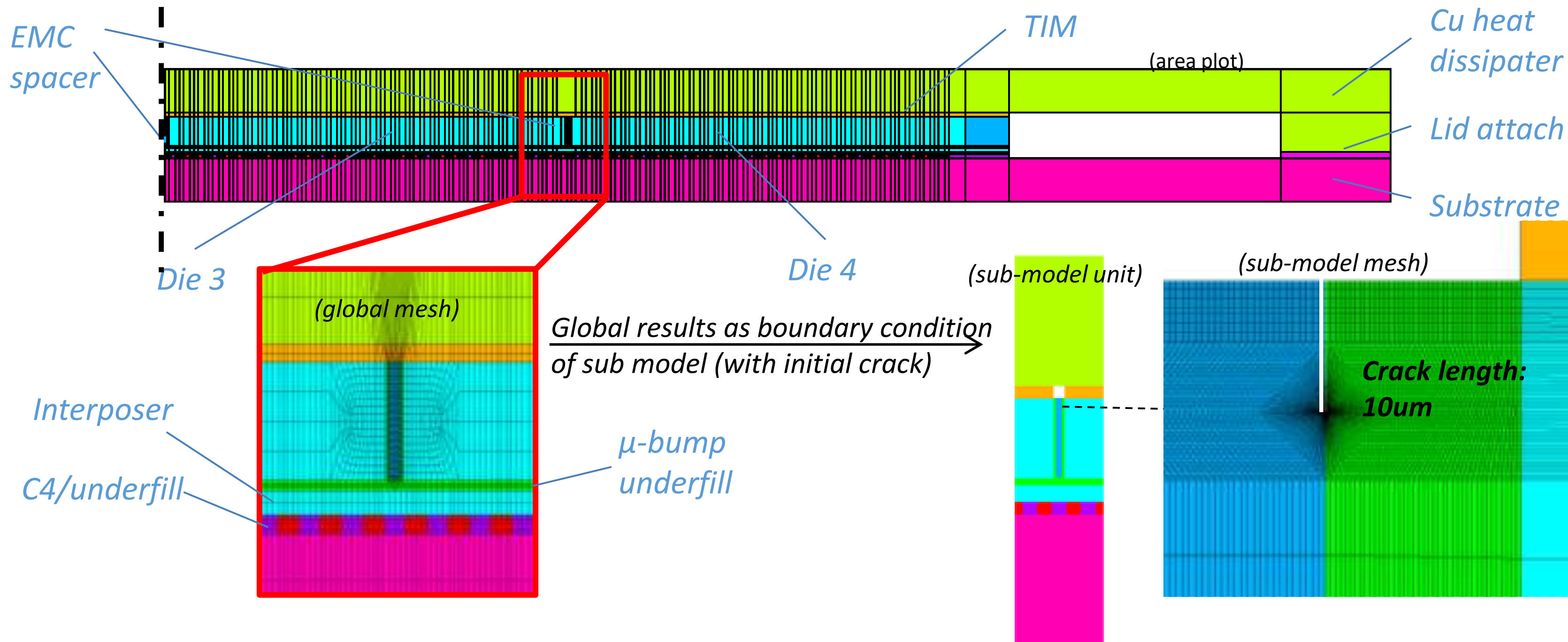


$$G_{IC} = \frac{{K_{IC}}^2}{E}$$

$$\chi_{UF(150°C)} = \frac{G_{IC\ (@150°C)}}{G_{IC\ (@25°C)}} = \frac{6.774\ J/m^2}{556.7434\ J/m^2}$$
$$= 0.012168$$

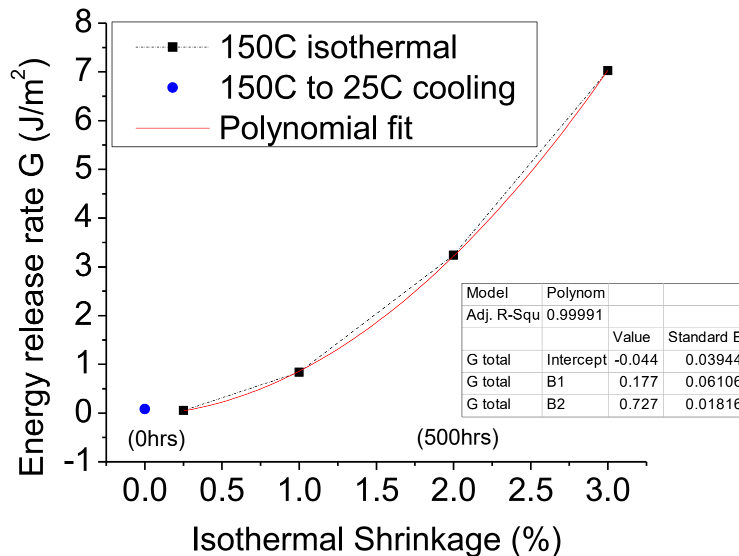
Case1: global & local model

- Use **symmetric** model; dimensions follow actual part size.
- Meshed with all quadrilateral 8-node Plane183 element under **plane strain** condition.
- Assume under isothermal, the deformation is only caused by shrinkage of the μ-bump underfill between the die and interposer.
- Ideal crack (two crack surfaces have identical location) for all sub model cases.
- Converged solution could be obtained in the global model until 20% shrinkage.

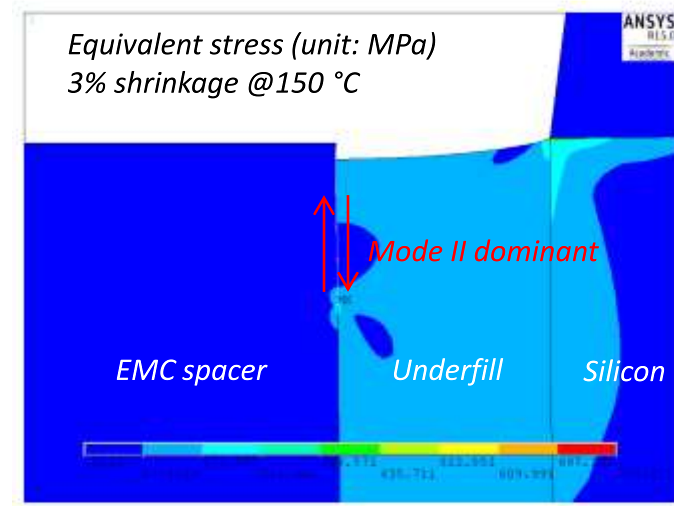


Failure Mode: Interfacial Crack Propagation

- ***Case 1:***
  - EMC/UF interfacial crack;
  - Crack length: ***10um***; crack tip mesh size: 0.0625um
  - Shearing mode (Mode II) crack dominant
  - J integral and virtual crack closure (VCCT)method results are consistent in calculating strain energy release rate (ERR).
  - Polynomial fitting is done for ERR–shrinkage curve, estimate the ERR as shrinkage increases.



Model	Polynom		
Adj. R-Squ	0.99991		
		Value	Standard E
G total	Intercept	-0.044	0.03944
G total	B1	0.177	0.06106
G total	B2	0.727	0.01816



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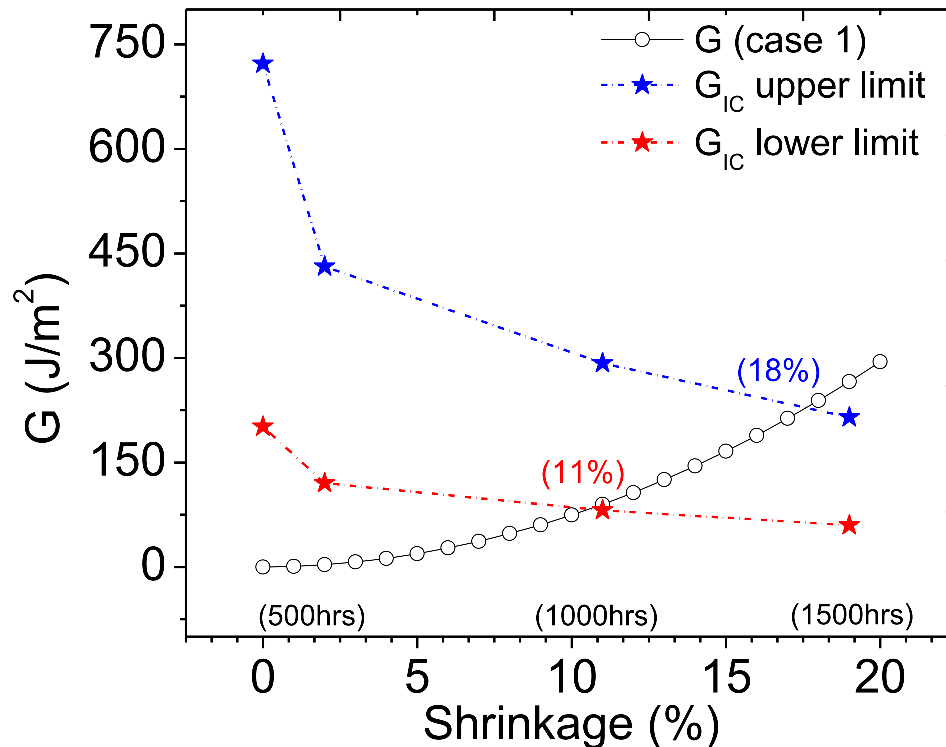
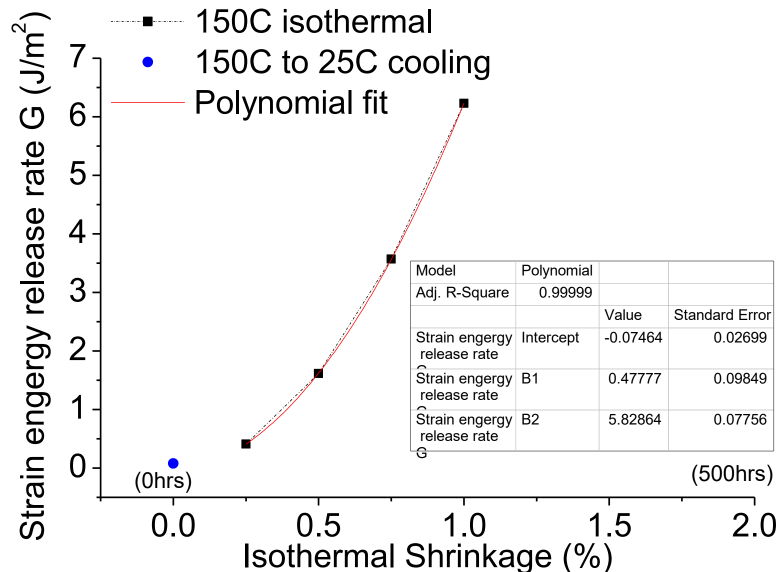
Failure Mode: Interfacial Crack Propagation

- Assume the interfacial critical toughness is the same with the cohesive value.
- Estimated 11% - 18% amount of "threshold shrinkage" could drive the crack into further propagation.
- Crack propagation would occur once the threshold shrinkage was reached.

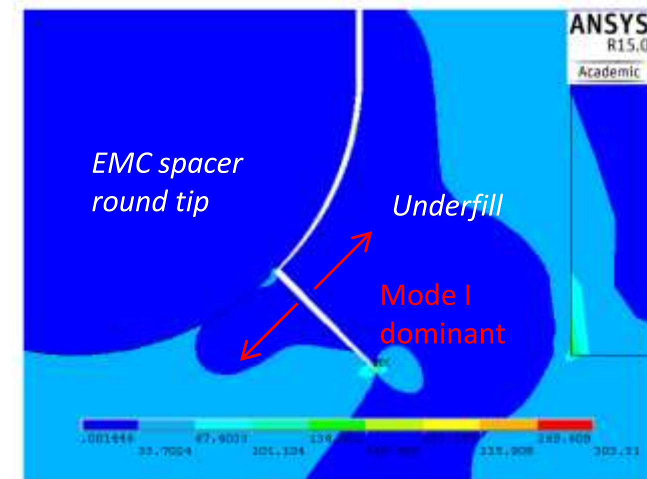


Failure Mode: Cohesive Crack Propagation

- Cohesive crack in underfill
- After delamination of the EMC/underfill interface, a crack tip extends into the underfill.
- Assumed Initial Crack length: *10 um*;
- Opening mode (Mode I) dominant.



Equivalent stress (unit: MPa)
1% shrinkage @150 °C



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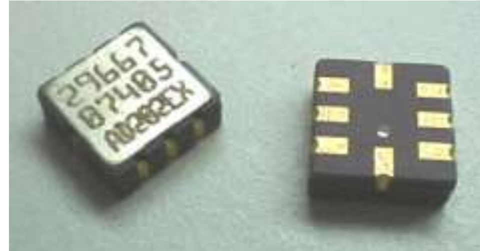
Case 2

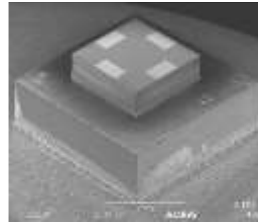
*i*MEMS® Package Modeling

CERPAK

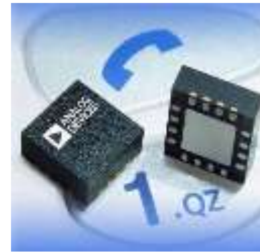


Leadless Chip Carrier
(5x5x2mm)

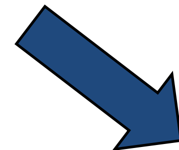
CBGA
(7x7x3mm)



Capped Die



Lead frame chip scale package (LFCSP)
(4x4x1.45mm)



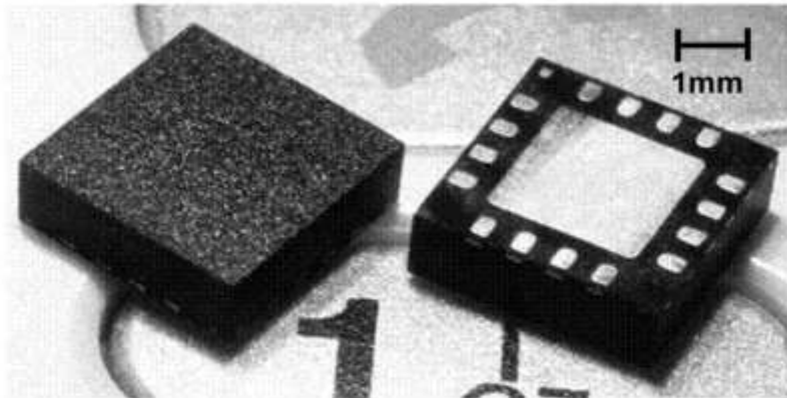
Wafer Scale Package
(2x2x1mm)

This is a Major MEMS Industry Breakthrough – Finally removes the concern of single mass 3-axis sensing

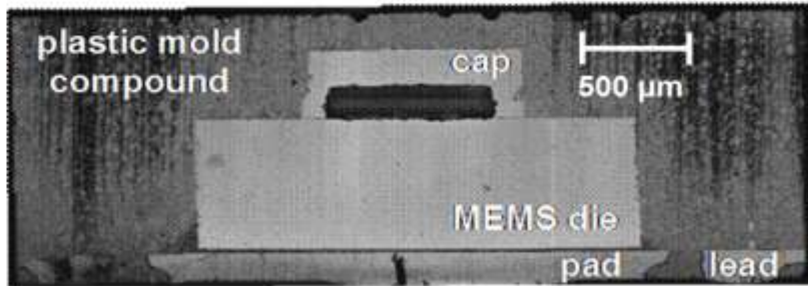
ADXL330 enables Nintendo's Gaming Revolution Wii

and many more applications...

Package study objects: 4 x 4 x 1.45 mm LFCSP



(a)



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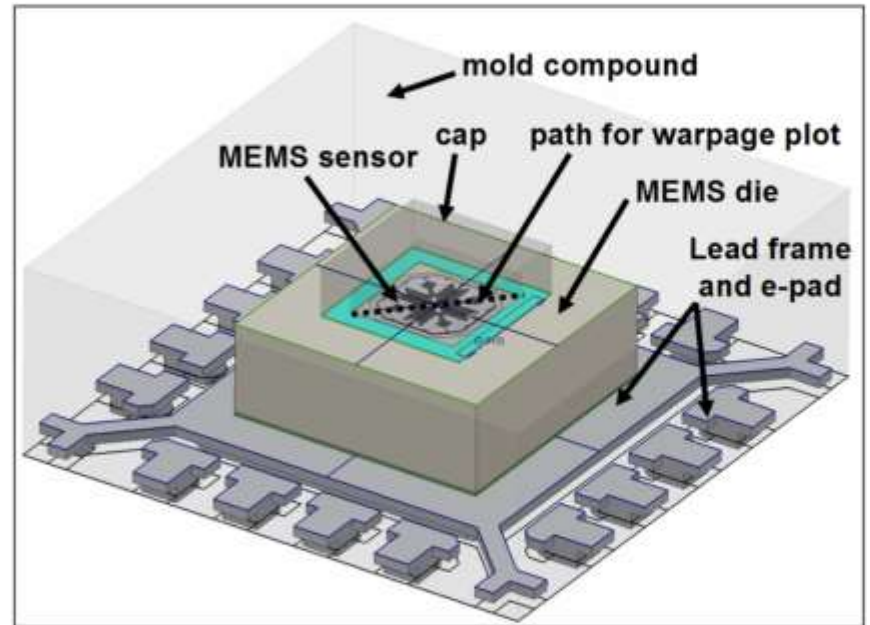

**4 x 4 x 1.45 mm LFCSP
(ADXL330 package)**

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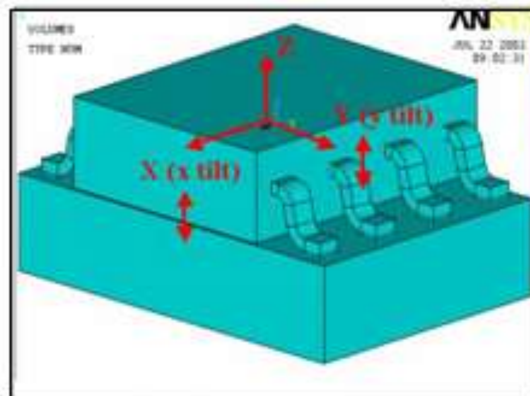
MEMS Packaging

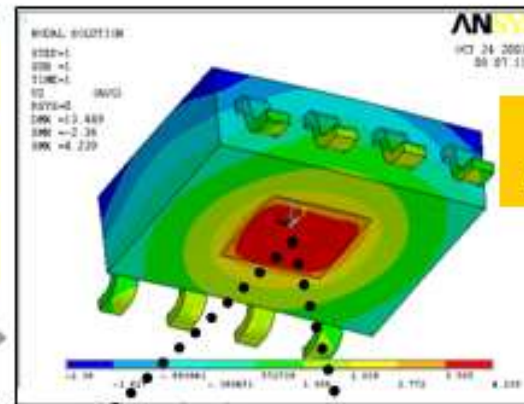
Why model the stress and device interactions?



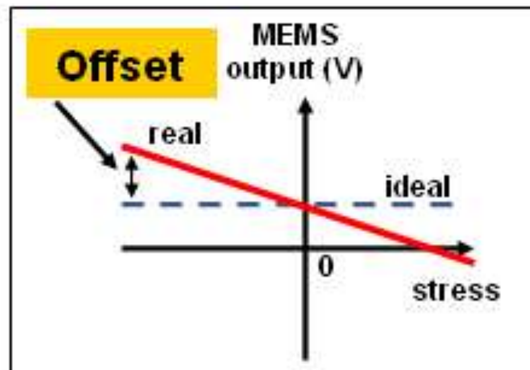
Thermal

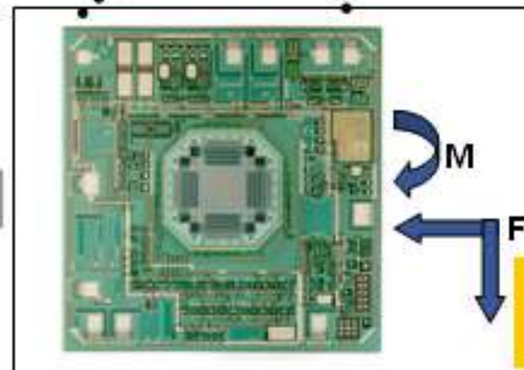
Torque

Force



Package Deformation





Device Deformation

- **Modeling interactions is extremely hard. We take a novel approach:**
  - Finite element package model + Sensor reduced-order model (CoventorWare) ➔ Integrate the two!

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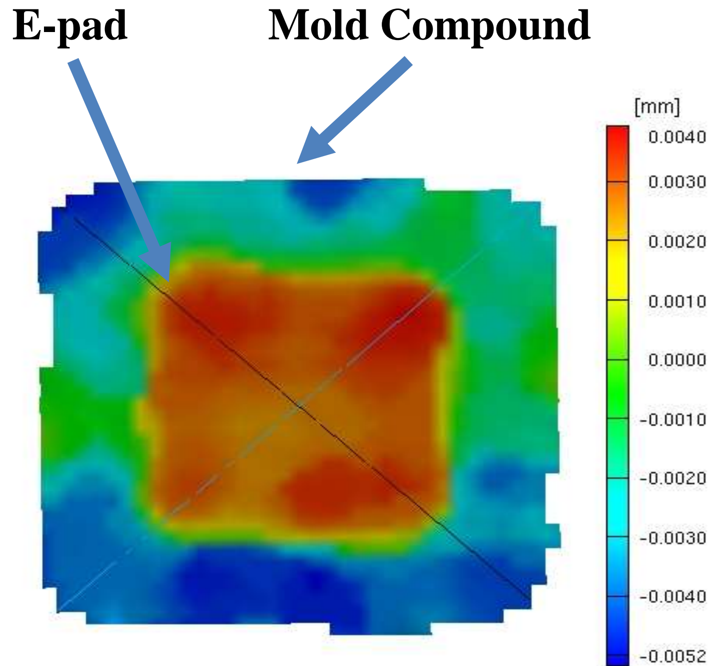
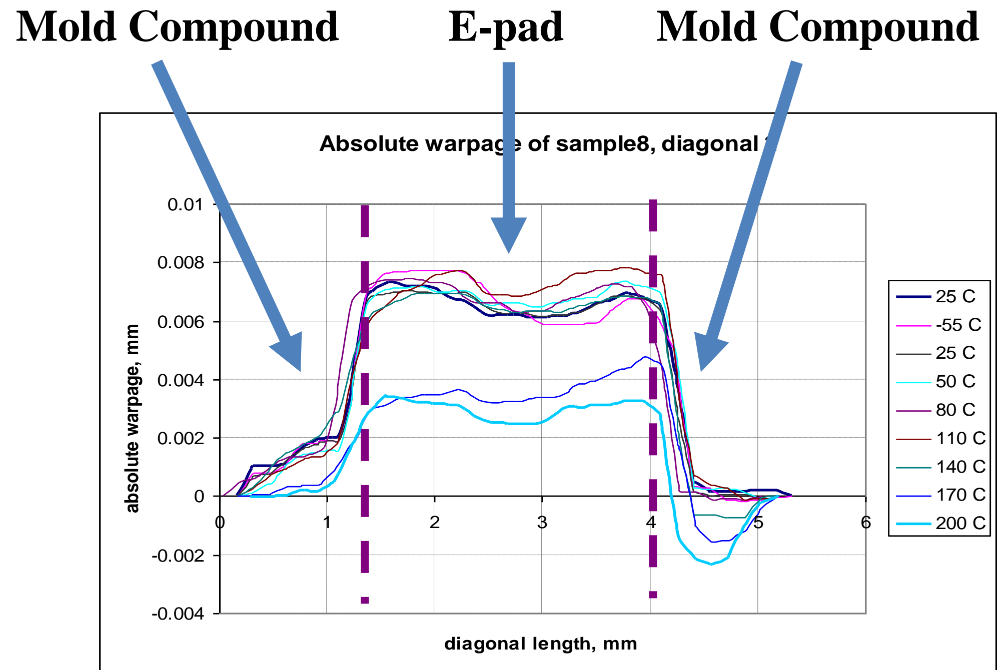
LFCSP Package Warpage Measurement

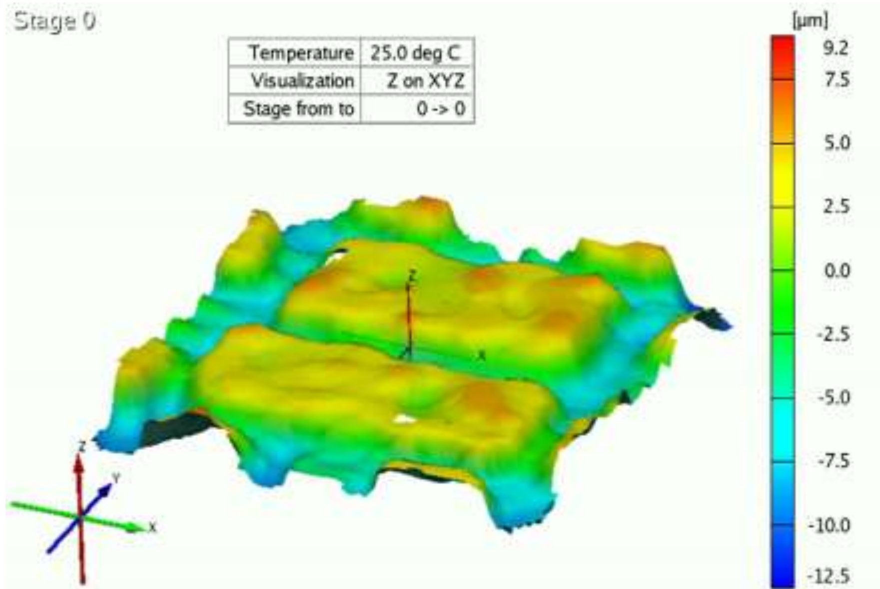


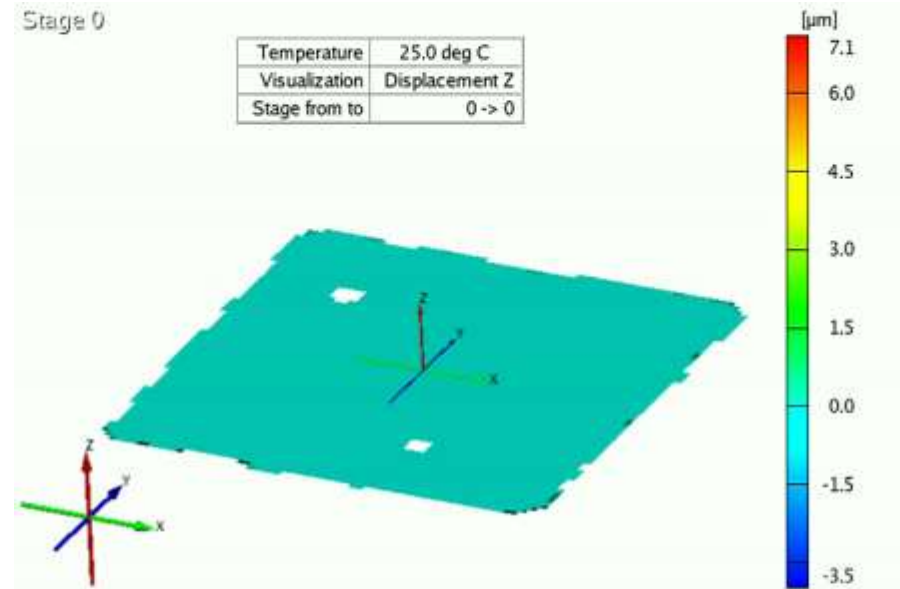
(a) Warpage of the package bottom side (e-pad side) at 20°C.



(b) Warpage plot over -55 ~ 200°C along a diagonal axis.

MEMS Packaging Analysis





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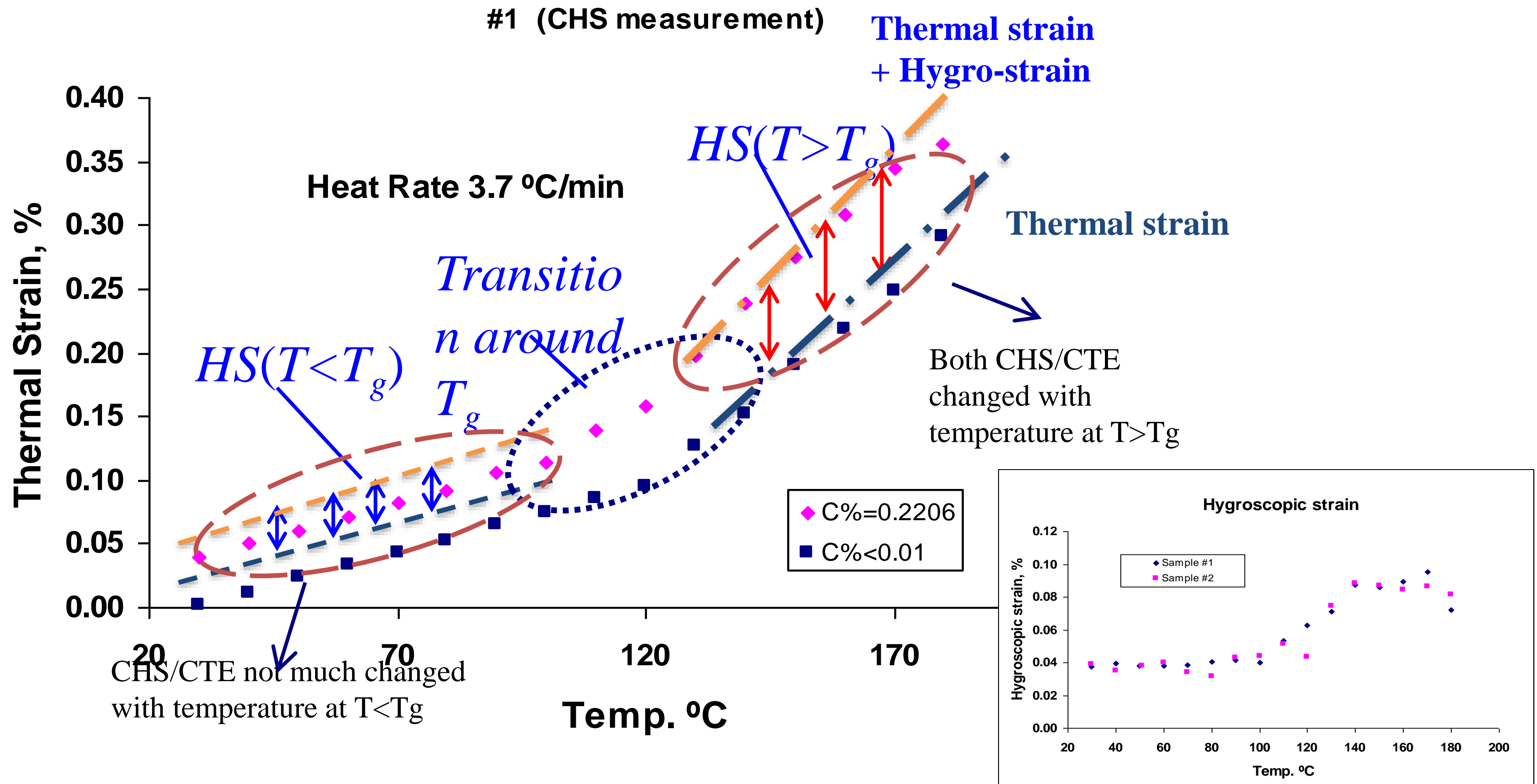
Tg and CTE w.r.t Moisture



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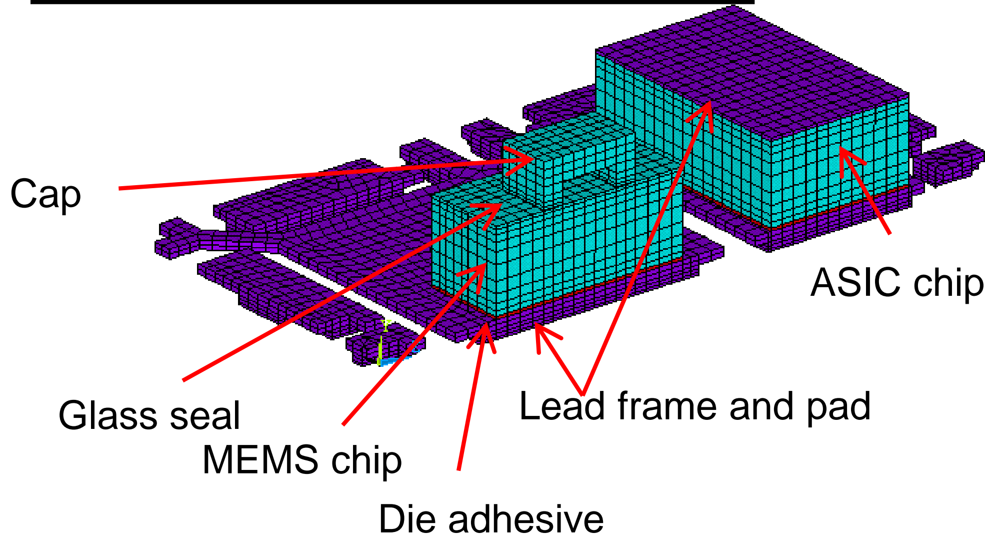
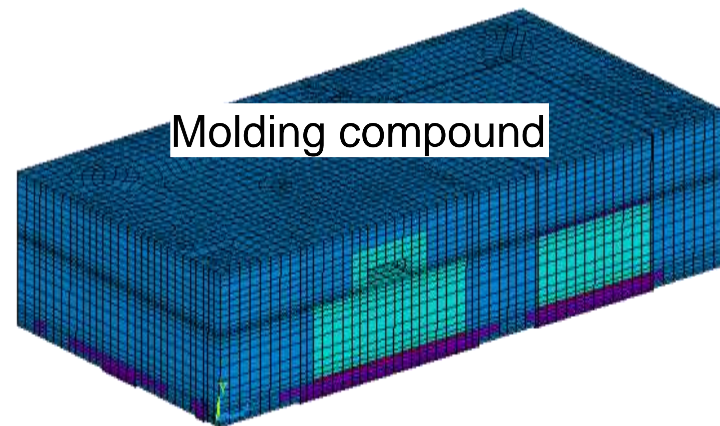
Process Modeling of MEMS (Package Level)

Reference setting
Temperature: 175ºC



Subjected to

1. Curing shrinkage
   (175ºC, 0.24% shrinkage)
2. Cooling down
   (25ºC/50%RH)
3. MSL 3 Preconditioning
4. Reflow (30ºC~260ºC)
5. HAST



CHS = 0.44 %strain/%wt

$\varepsilon_{SW} = 0.44 \times 0.171\%wt_{@60\%RH}$

$= 0.075\%strain$

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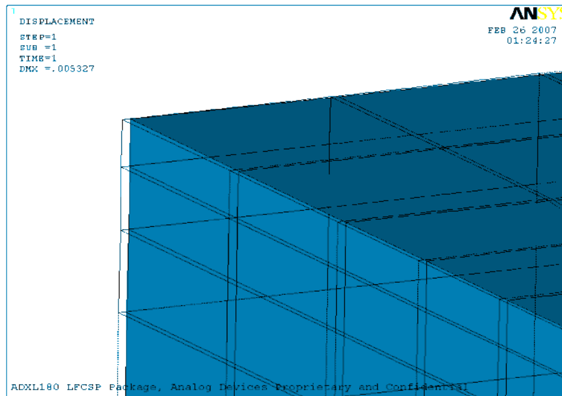
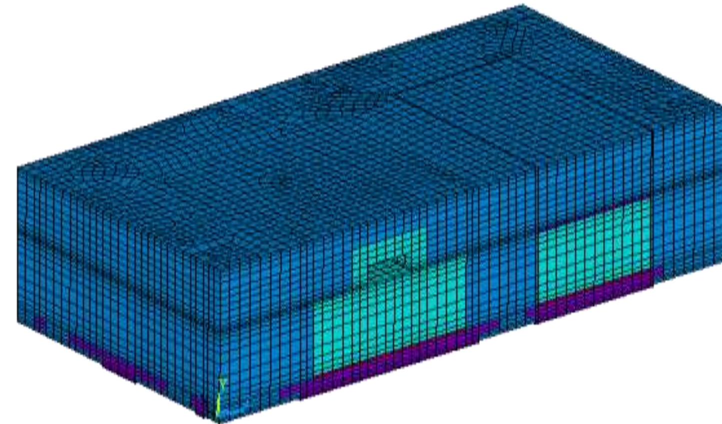
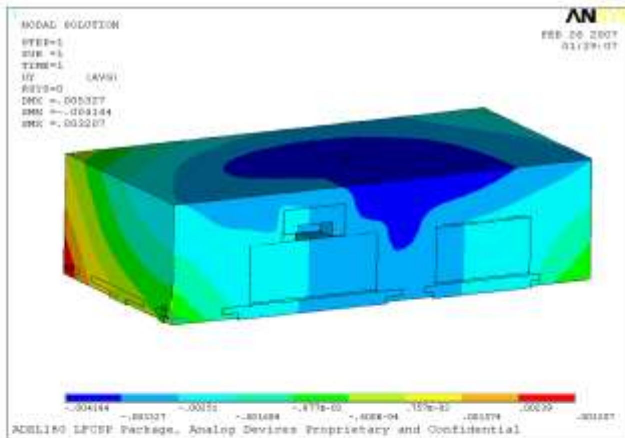
FE Model of MEMS (Package Level)

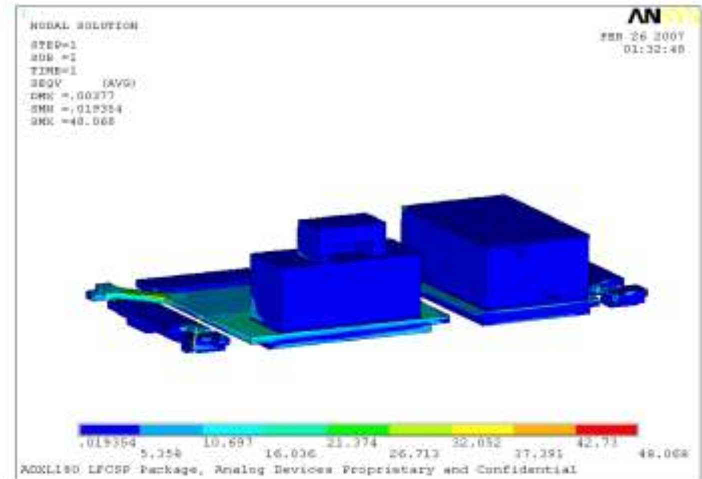
1. 0.24% Curing shrinkage (At 175ºC)







Max. UY 4.144 μm



Max von mises: 48 MPa

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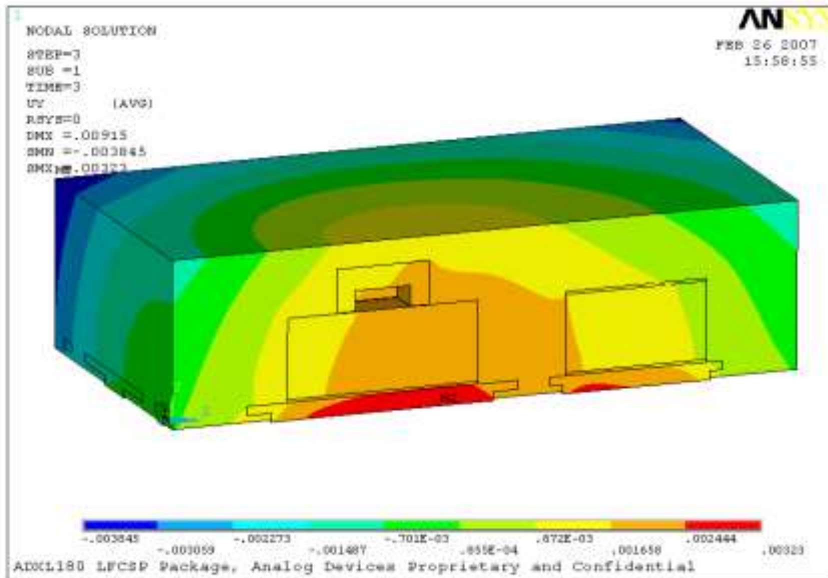
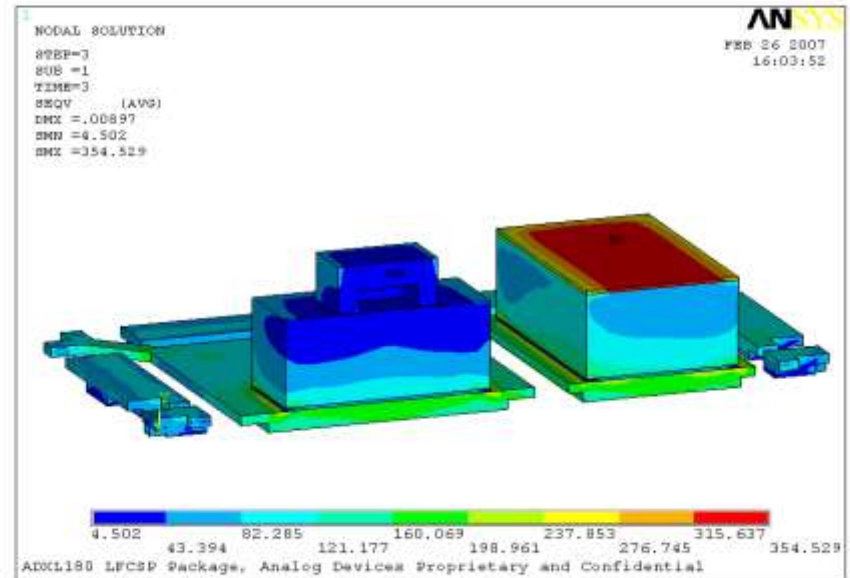
FE Model of MEMS (Package Level)

2. Cooling down from 175ºC to 25ºC and fully saturated at 50% RH





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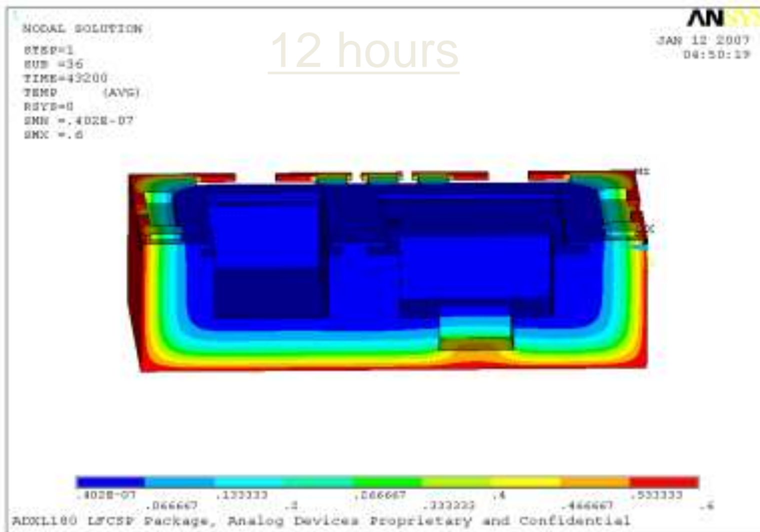
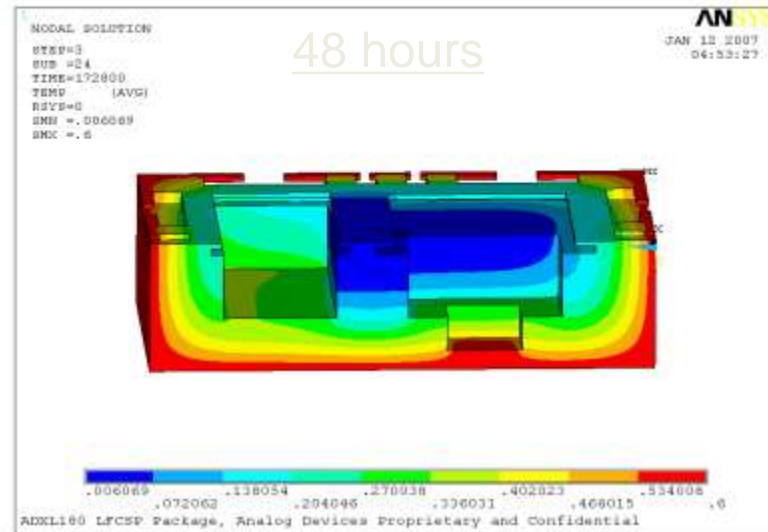
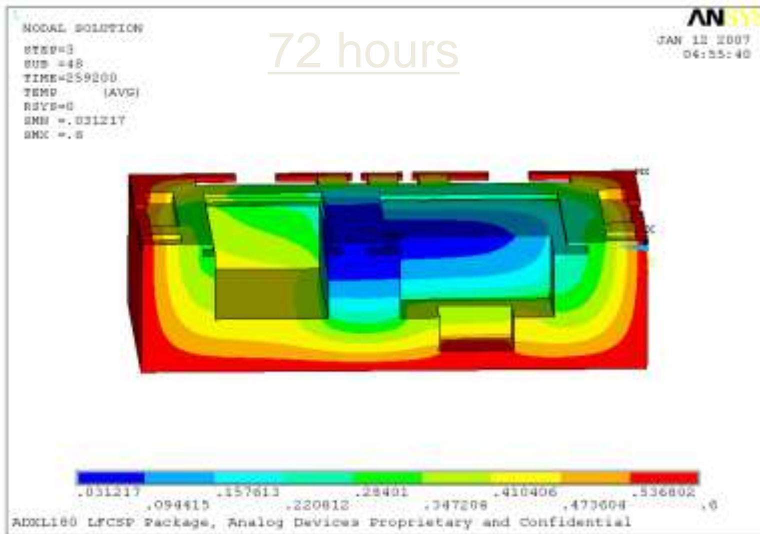
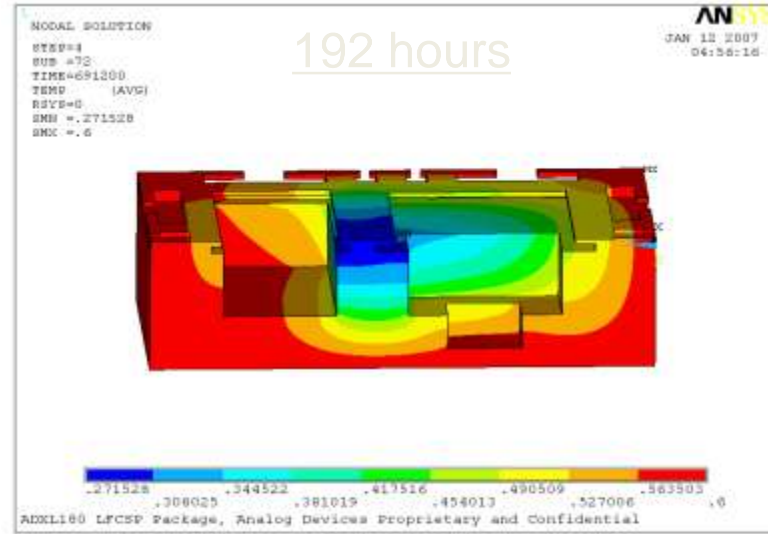
Moisture Concentration Distribution MSL 3



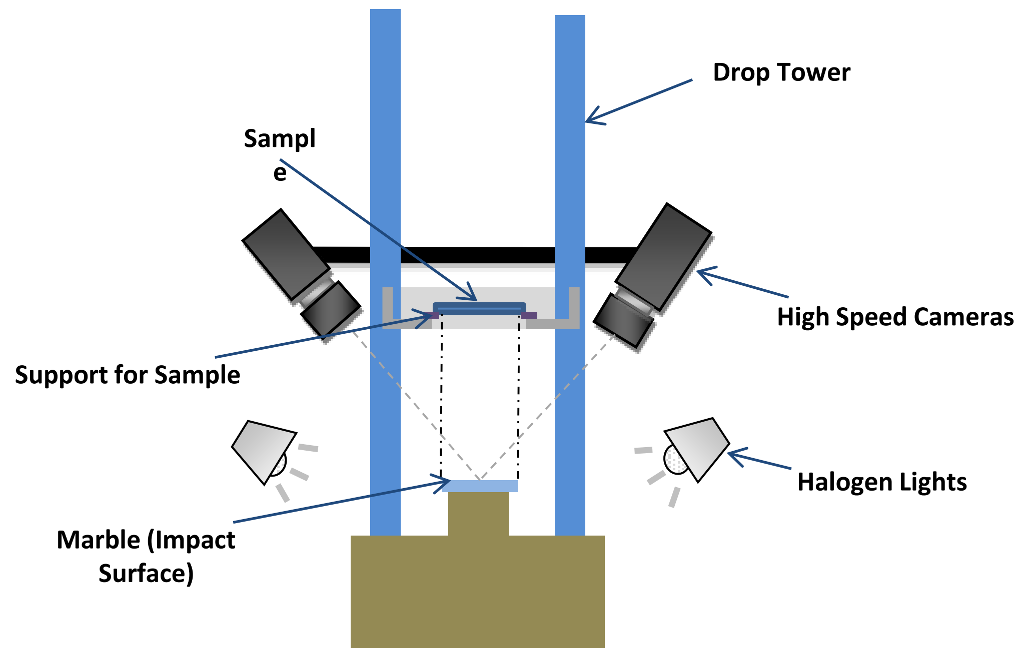


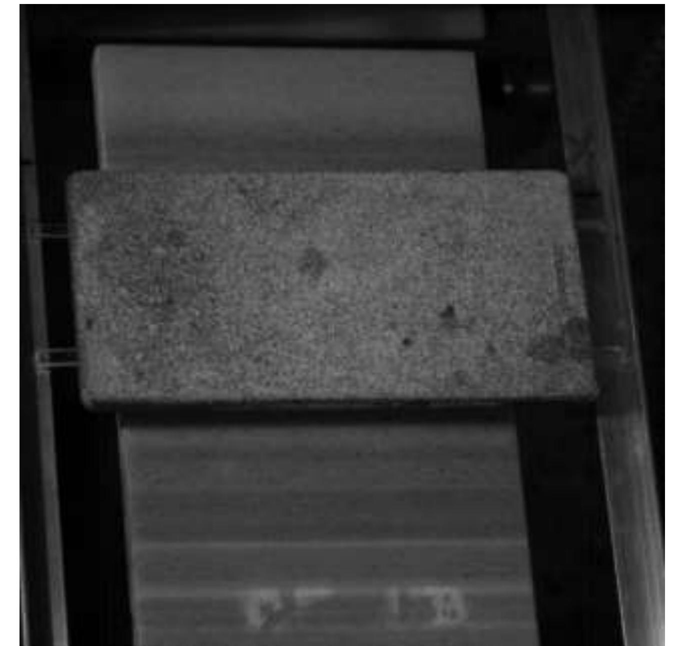




CASE 3
High Speed DIC Drop Test and Modeling

Experimental Set up





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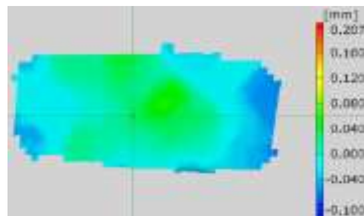
TDM Deformation with Drop height change

- TDM makes first contact with surface at 1.75 msec.
- With increase in drop height the maximum deformation of the center point increases.



First Impact for 30 cm Drop

30 cm Drop
60 cm Drop

Deformation (mm)

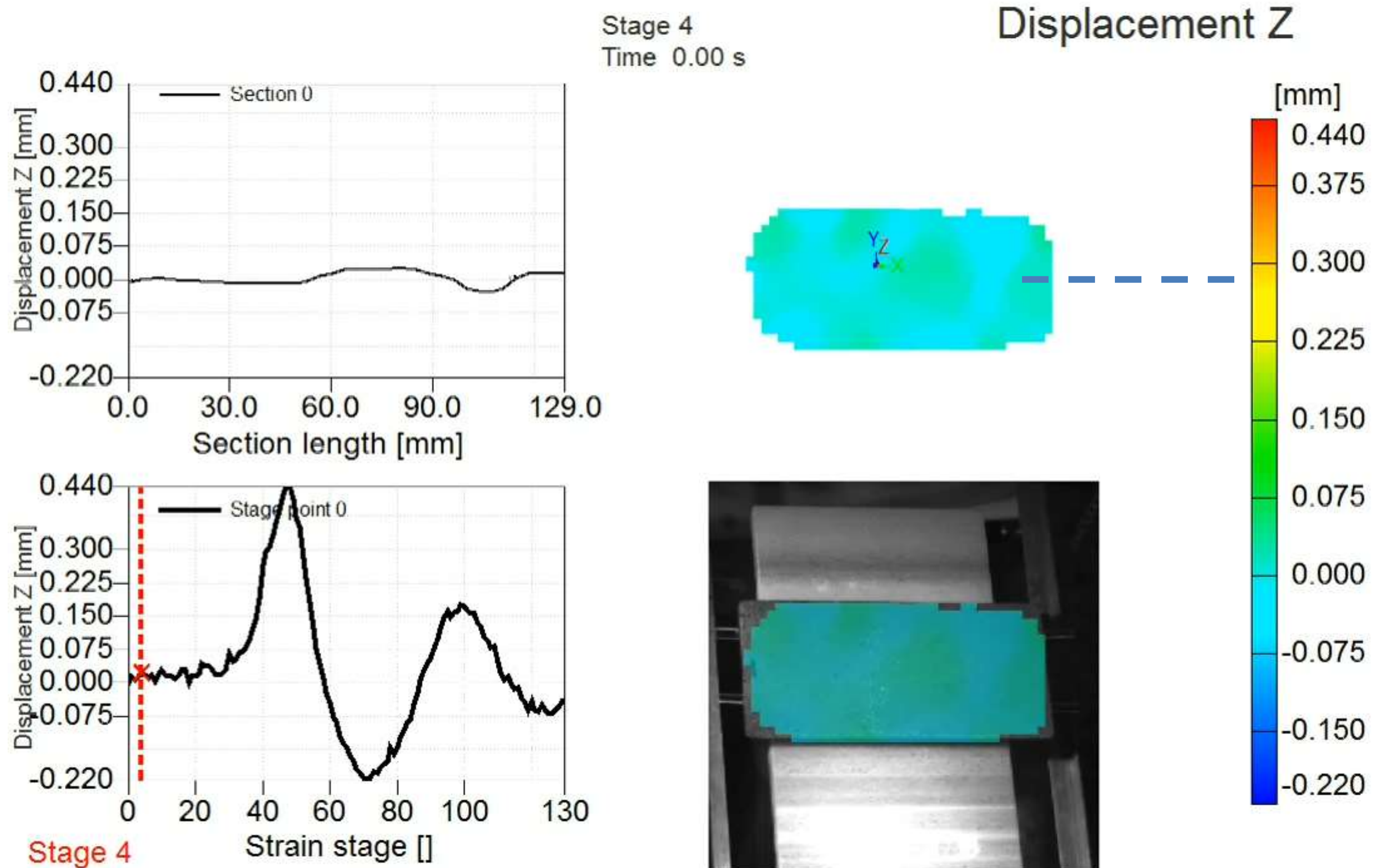
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3

-2 0 2 4 6 8 10 12 14

Time (msec)

Animation for 60 cm TDM Drop

- Video highlights the Deformation of TDM after 60 cm drop.
- Section line runs in horizontal direction passing though center of the module.



CASE 4
2.5D Package Modeling

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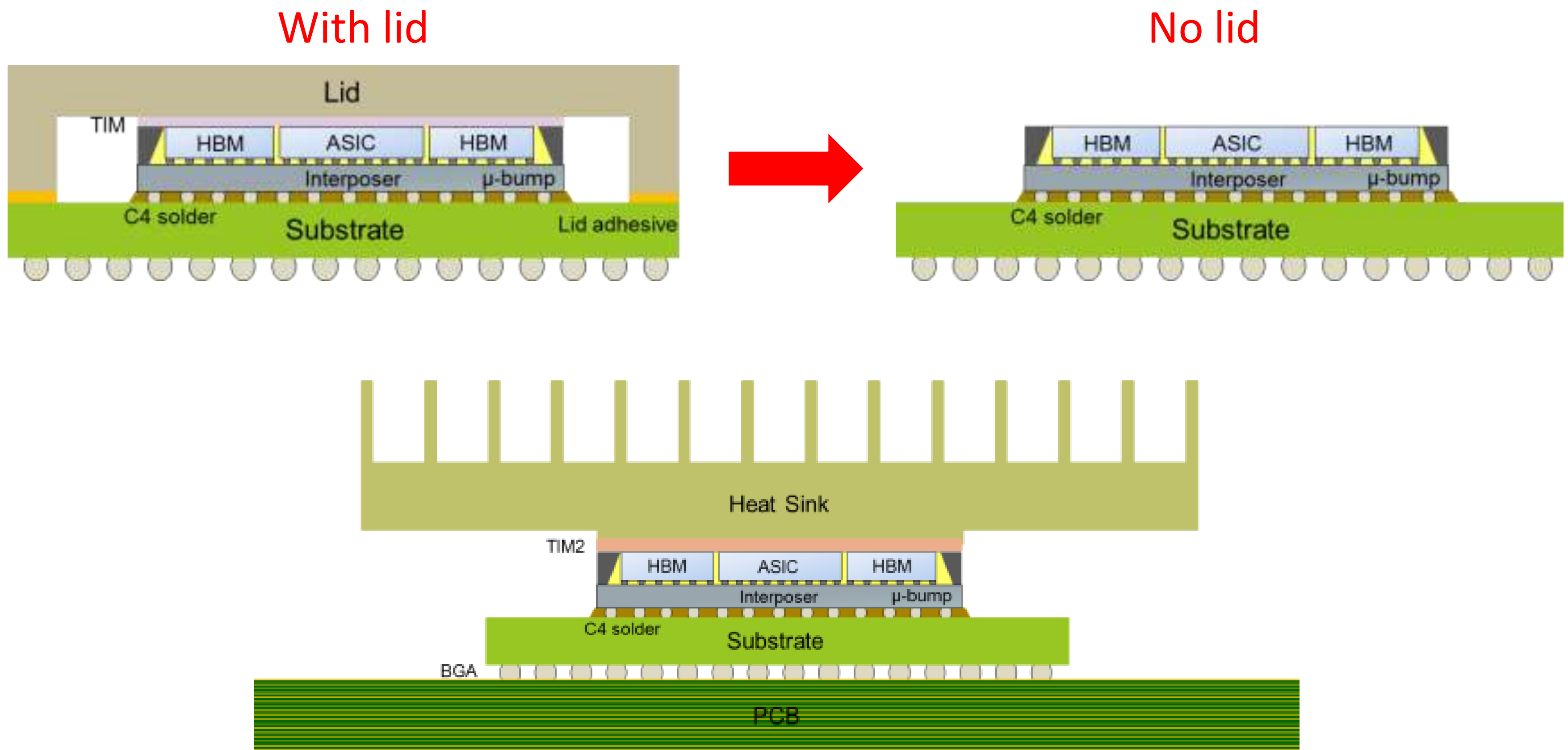
Influence of lid on thermal performance

- Lid is removed from the lidded package
- Heat sink is directly attached on the silicon dies through TIM2



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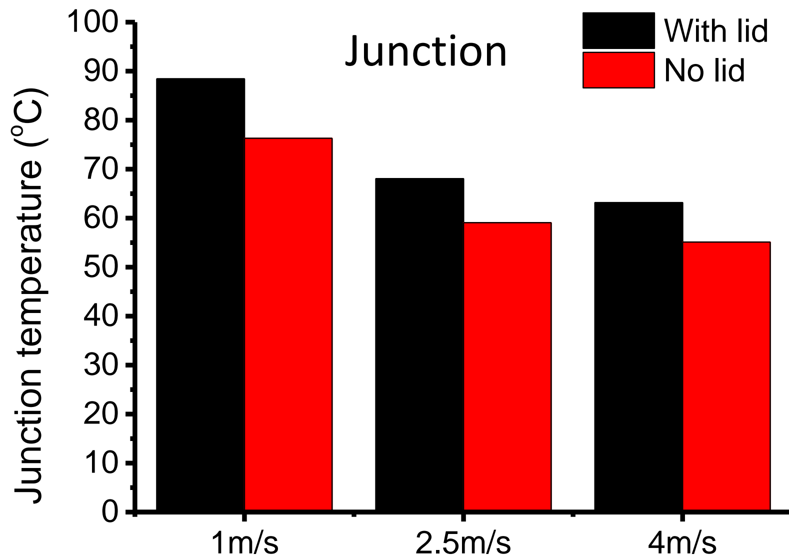
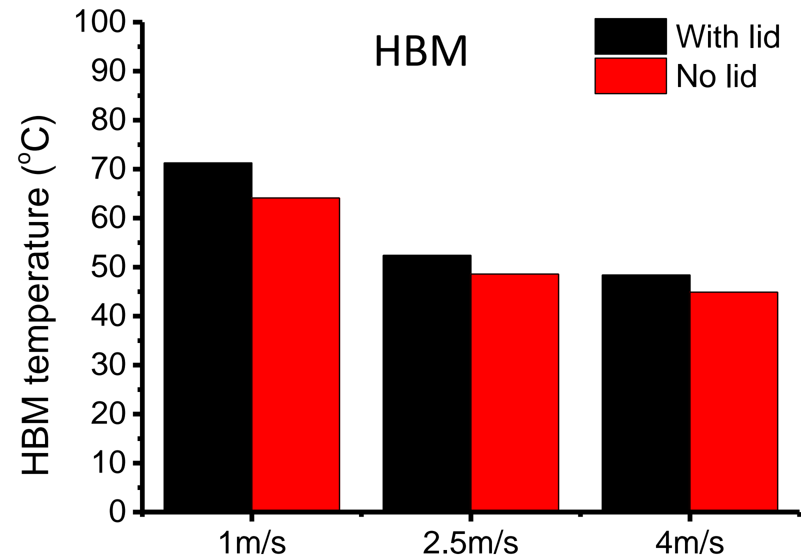
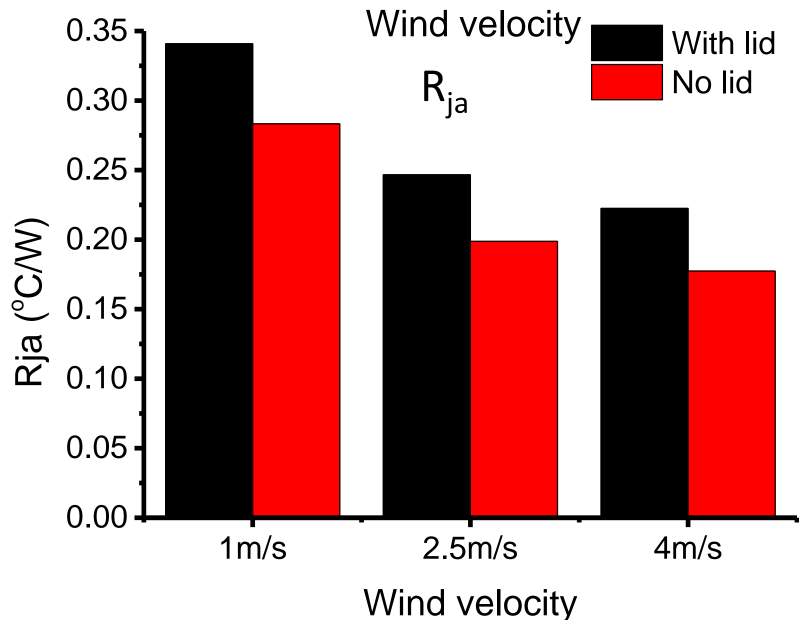
Influence of lid on thermal performance



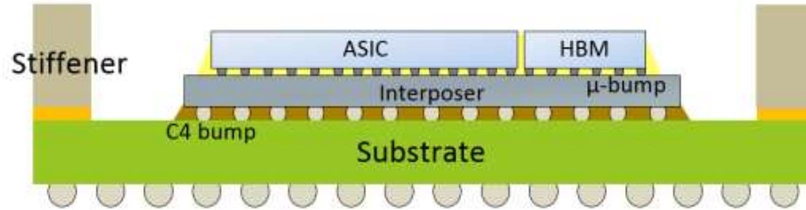


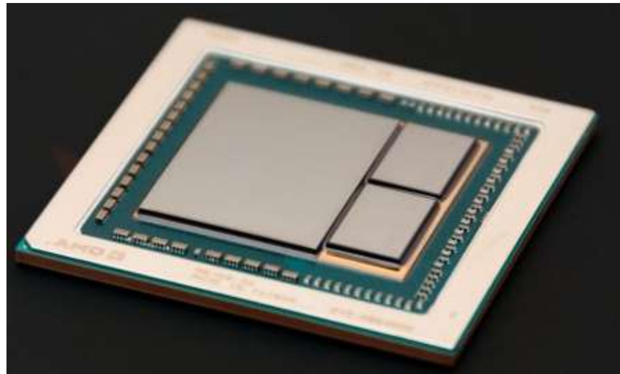


- Removing the lid can effectively reduce the junction and HBM temperature;
- Temperature drop on HBM is less than ASIC;
- R_{ja} decreases by ~ 0.05°C/W.

Thermo-mechanical challenges in lidless package

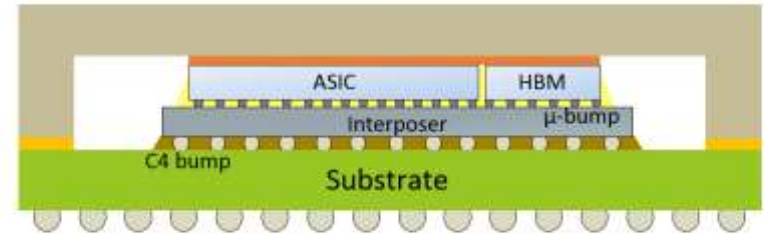
Lidless 2.5D package





- Advantage:
  - better heat dissipation
- Disadvantage:
  - larger warpage
  - moisture penetration
  - risk under mechanical loading

Lidded 2.5D package

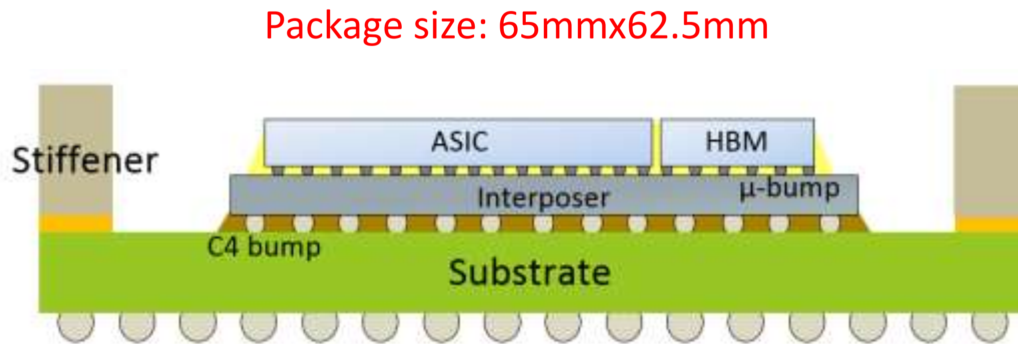


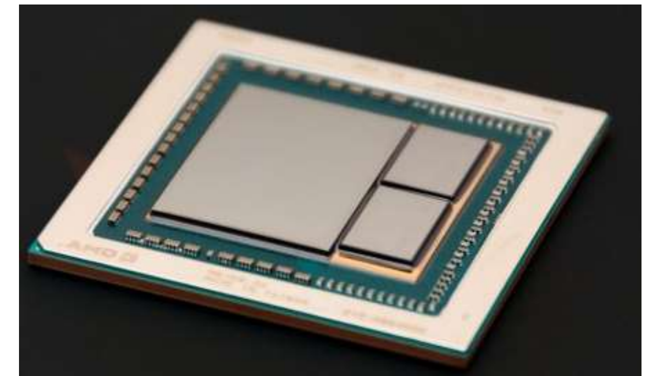
- Advantage:
  - less warpage
  - moisture barrier
  - less risk under mechanical loading
- Disadvantage:
  - worse heat dissipation

Thermo-mechanical reliability assessment

Objective: To investigate the design factors that contribute to the thermal deformation and stress development of the 2.5D package, and to provide design guidelines for building thermo-mechanically reliable 2.5D packages.

Package size: 65mmx62.5mm





Lidless 2.5D package

- Package level reliability
  - warpage and stress
- Board level reliability
  - BGA solder joint reliability under thermal cycling
  - BGA solder joint reliability under power cycling

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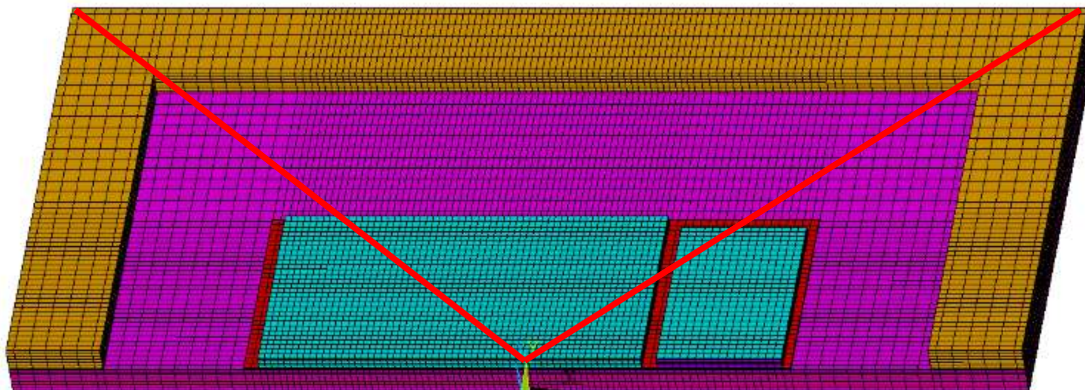
Parametric study on package level model

Material and geometric parameters are considered in parametric study using 3D finite element analysis

Material Parameter	Value
Substrate Core CTE	6, 8, 10 ppm/^{o}C
Substrate Core modulus	25, 30, 35 GPa
C4 underfill modulus	6.8, 10.8, 14.8 GPa
C4 underfill CTE	20, 27, 34 ppm/^{o}C
Microbump underfill modulus	5, 8.5, 12 GPa
Microbump underfill CTE	20, 28, 36 ppm/^{o}C
Stiffener CTE	15.5, 17, 18.5 ppm/^{o}C
Adhesive modulus	0.008-3 GPa

Geometric Parameter	Value
Stiffener thickness	1, 1.5, 2mm
Stiffener foot width	4, 6, 8mm
Adhesive thickness	0.1, 0.185, 0.27mm
Adhesive coverage	67%, 83.5%, 100%
Interposer thickness	0.08, 0.11, 0.14mm

Reference temperature-170°C



Two metrics for comparison:

- Substrate warpage in diagonal at 25°C
- Maximum Von-Mises stress in die at 25°C

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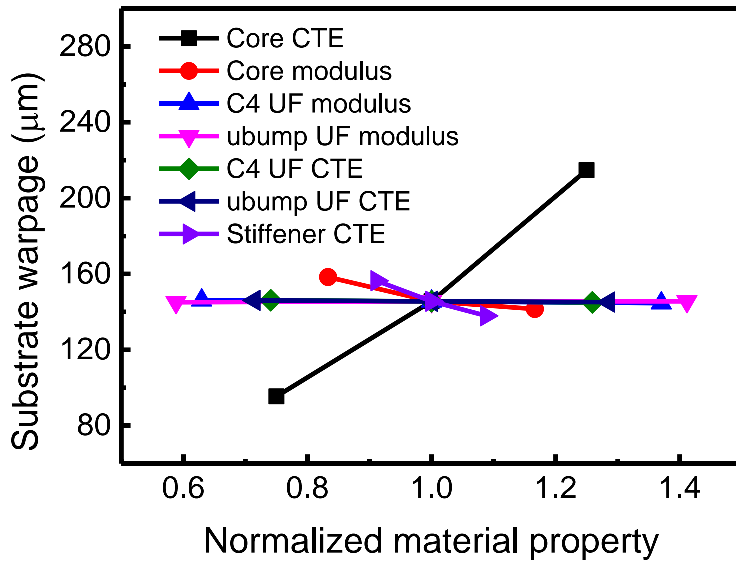
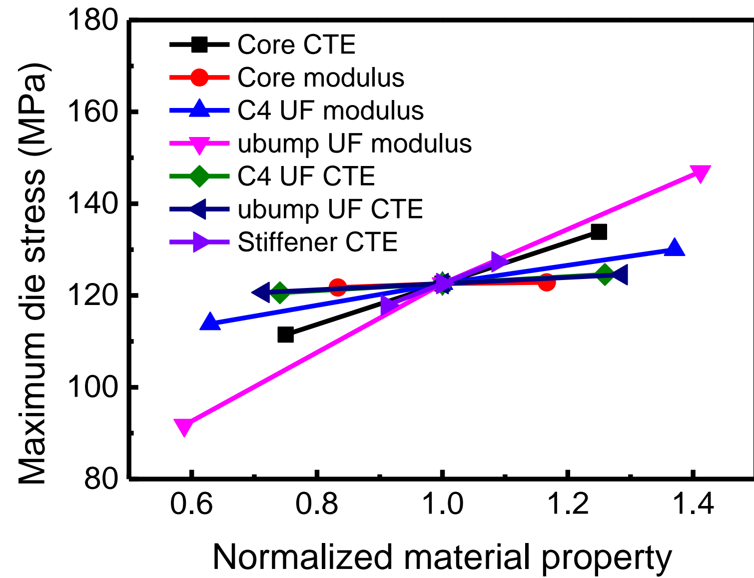
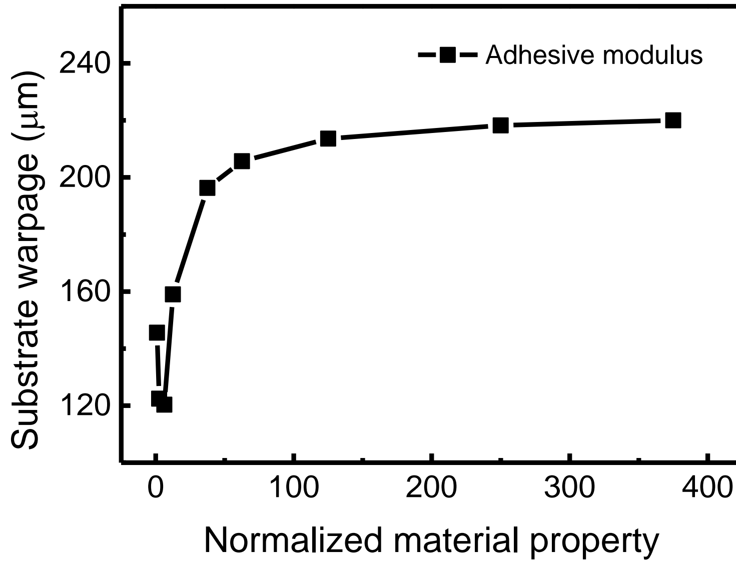
Material effect on substrate warpage and die stress

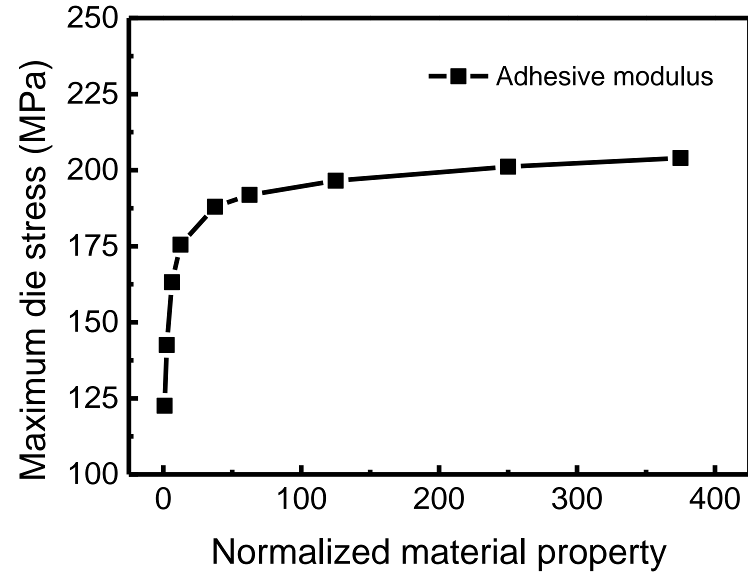


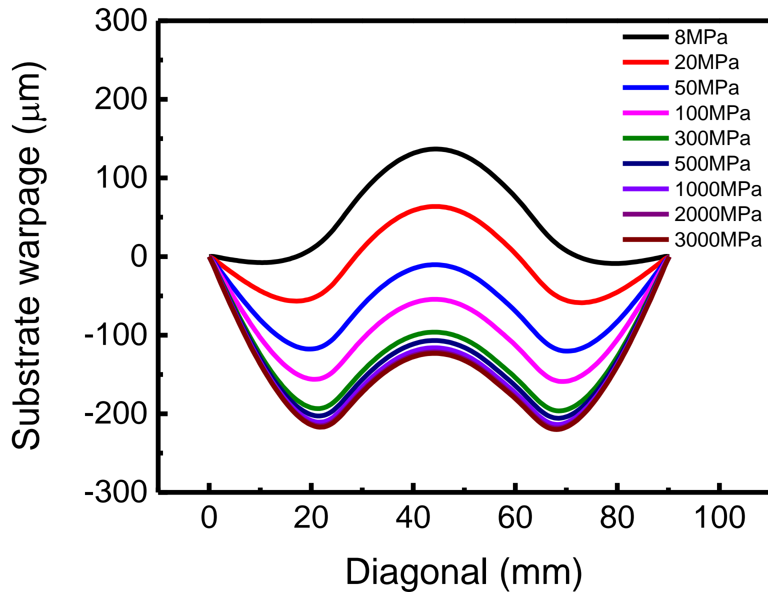


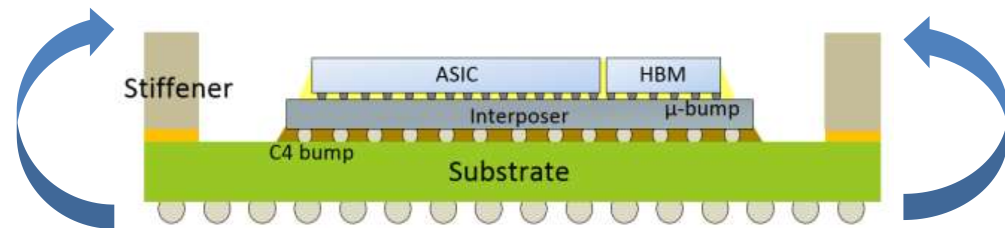
Parameter	Trend (warpage)	P_warp	Trend (stress)	P_stres
Substrate core CTE	↗	0.017	↗	0.67
Substrate core modulus	↘	0.892	→	0.753
C4 UF modulus	→	0.88	↗	0.694
C4 UF CTE	→	0.885	→	0.758
Microbump UF modulus	→	0.879	↗	0.296
Microbump UF CTE	→	0.885	→	0.758
Stiffener CTE	↘	0.84	↗	0.744

Adhesive modulus on substrate warpage and die stress









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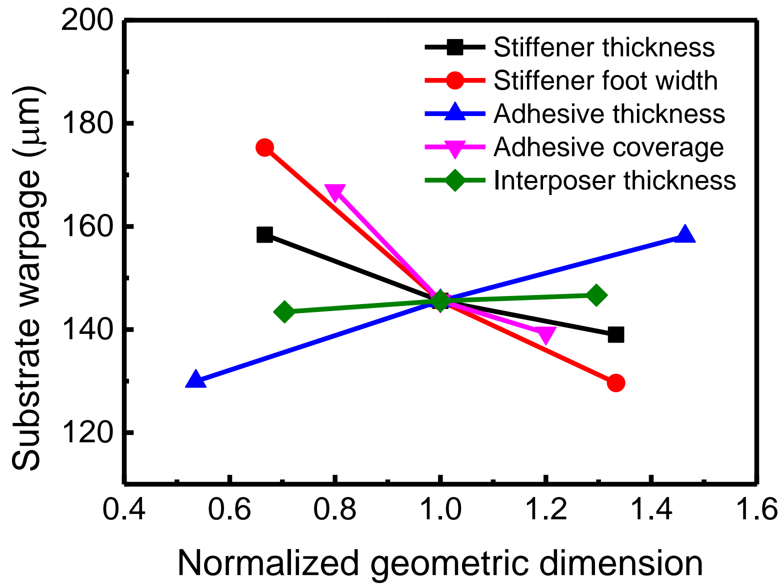
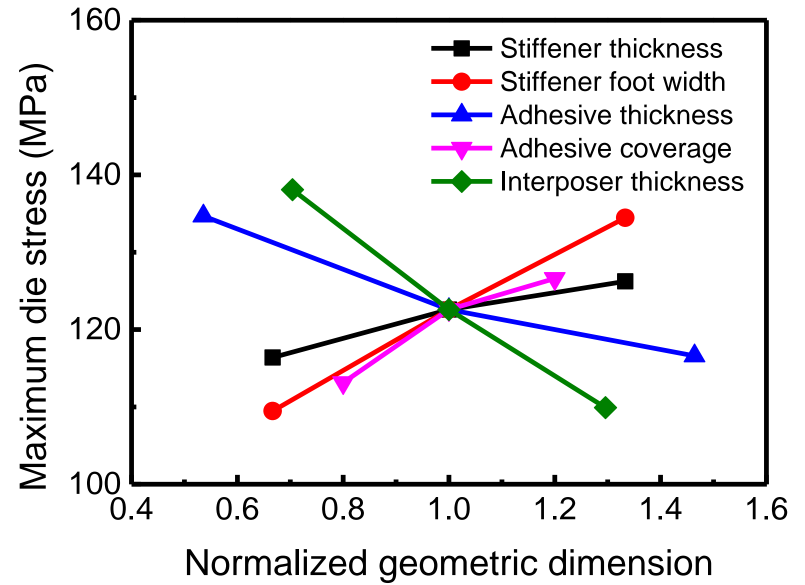
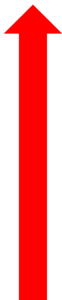
Geometric effect on substrate warpage and die stress







Parameter	Trend in warpage	P_warp	Trend in stress	P_stres
Stiffener thickness	↘	0.578	↗	0.737
Stiffener foot width	↘	0.015	↗	0.121
Adhesive thickness	↗	0.272	↘	0.313
Adhesive coverage	↘	0.249	↗	0.524
Interposer thickness	↗	0.994	↘	0.056

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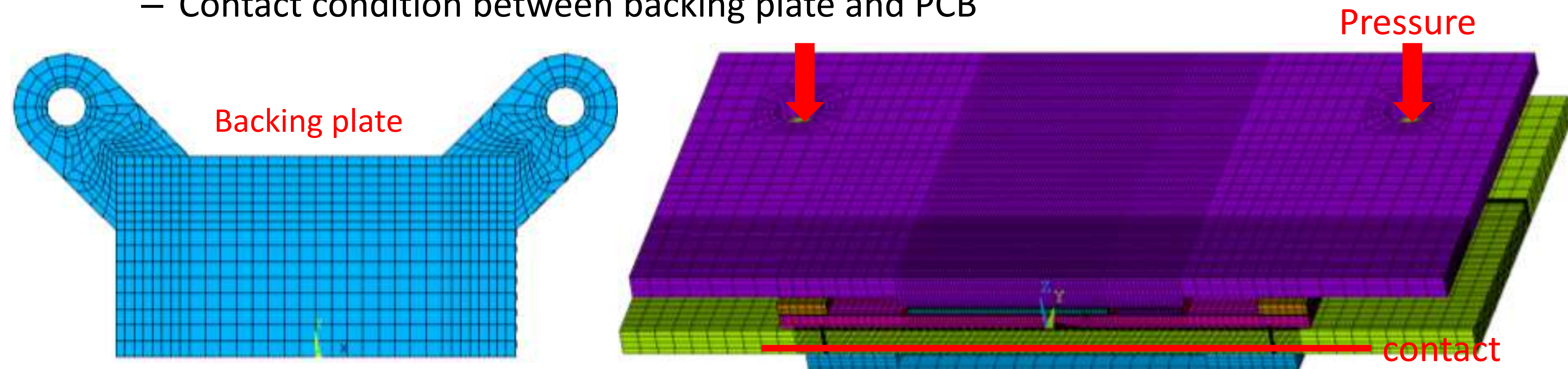
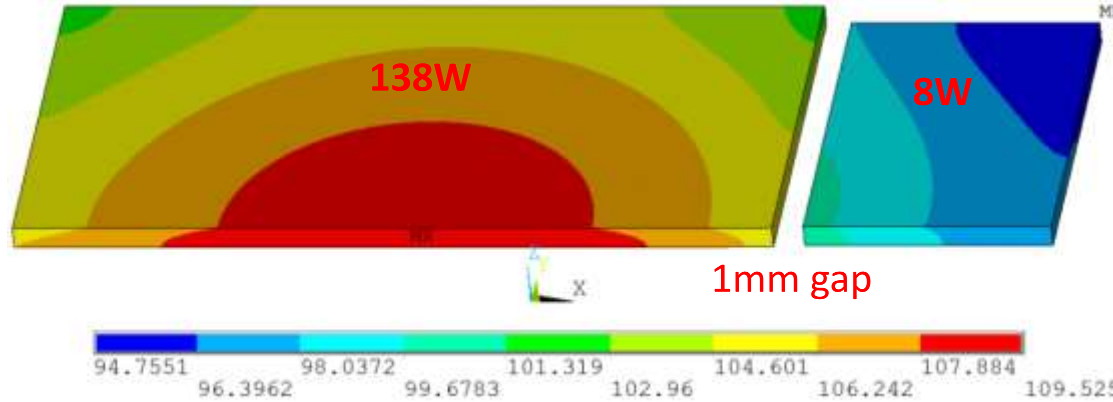
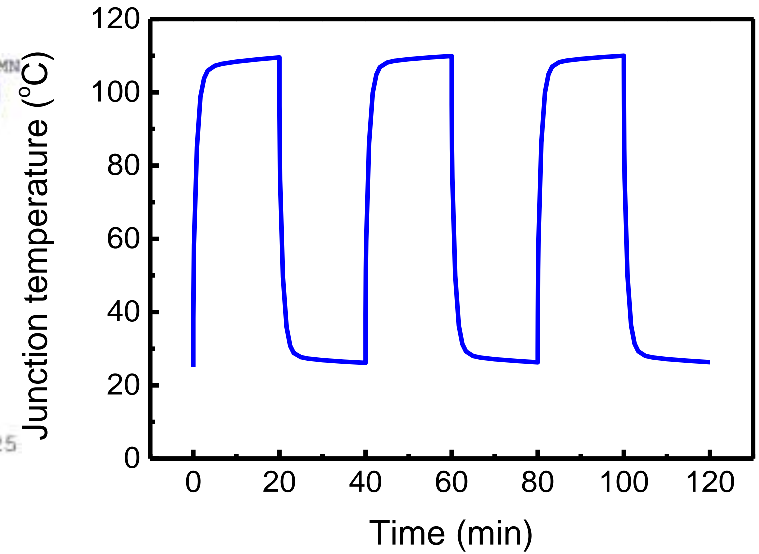
Board level study under power cycling

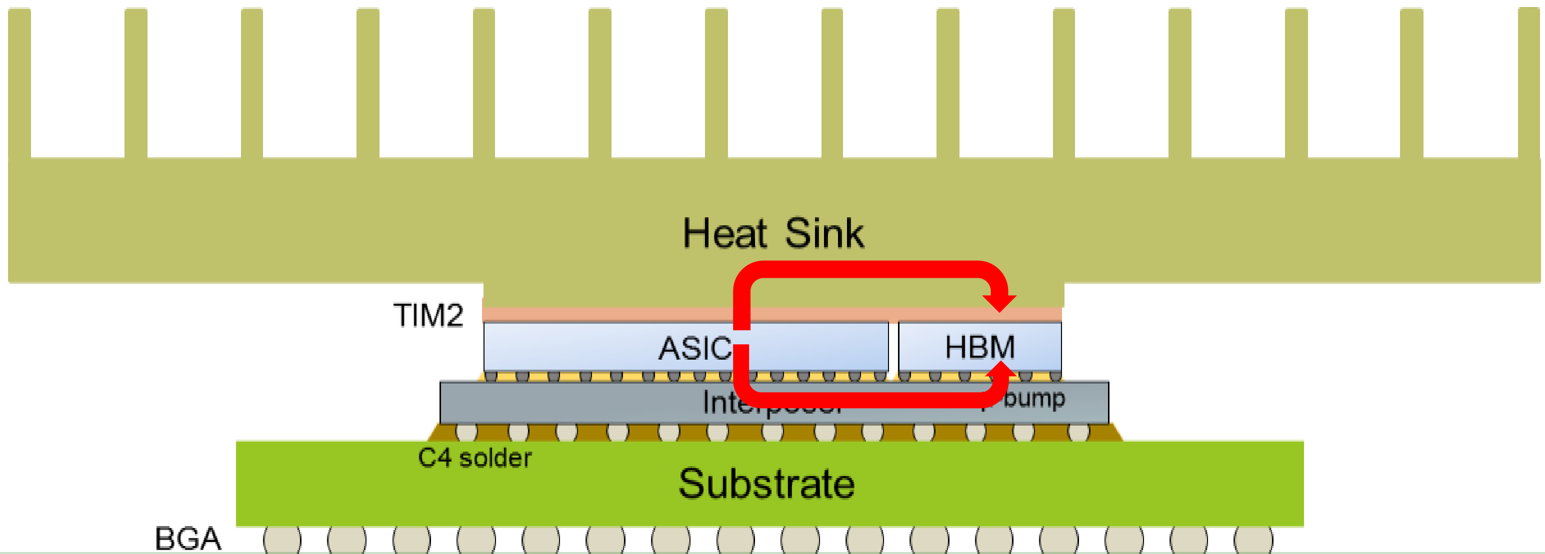
- During real working condition, temperature is non-uniformly distributed, power cycling effect should be considered.
- Thermal analysis
  - 20 min power on, 20 min power off
  - 138W for ASIC and 8 W for each HBM
  - Heat transfer coefficient is applied on heat sink
- Structural analysis
  - Temperature loading
  - Clamping force is applied on heat sink and backing plate
  - Contact condition between backing plate and PCB



Temperature distribution of silicon chips







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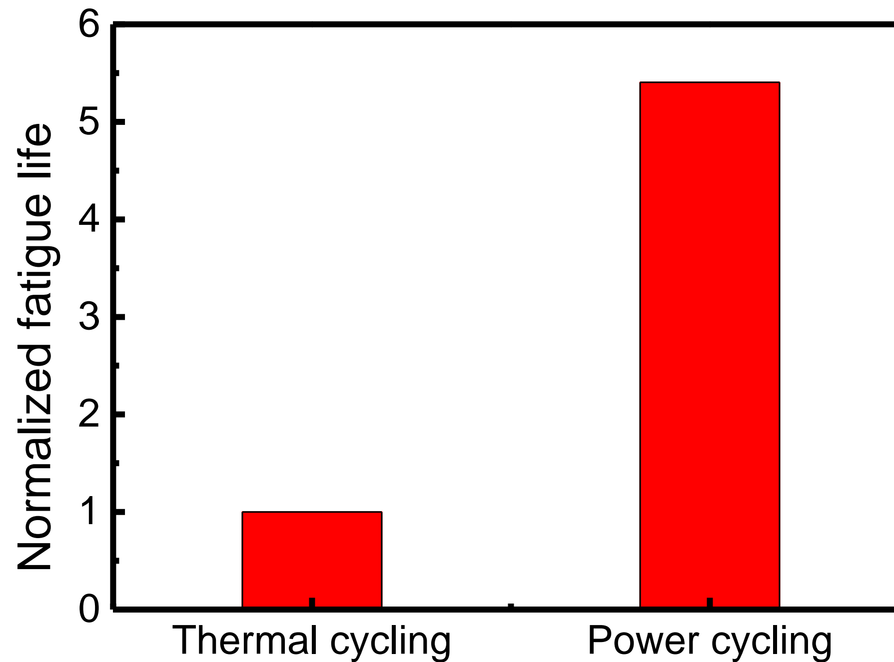
Power cycling vs thermal cycling

- Solder reliability is compared between thermal cycling and power cycling condition.
- Solder fatigue life is much higher in power cycling condition



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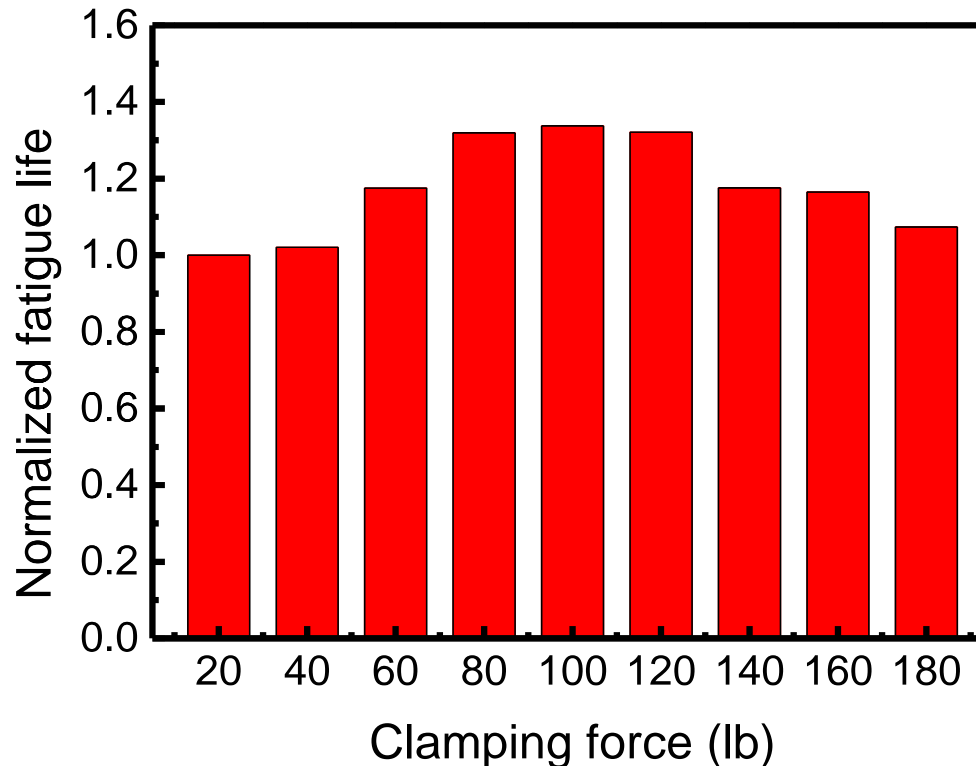
Influence of clamping force

- Different clamping force is considered.
  - 20lb to 180lb
- 100 lb clamping force shows the highest fatigue life



Thank you!

Questions?