Trends and Design Methodologies for 3D Multi-Chip(let) IC Packaging

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Product Management Director – IC Packaging & Cross-Platform Solutions

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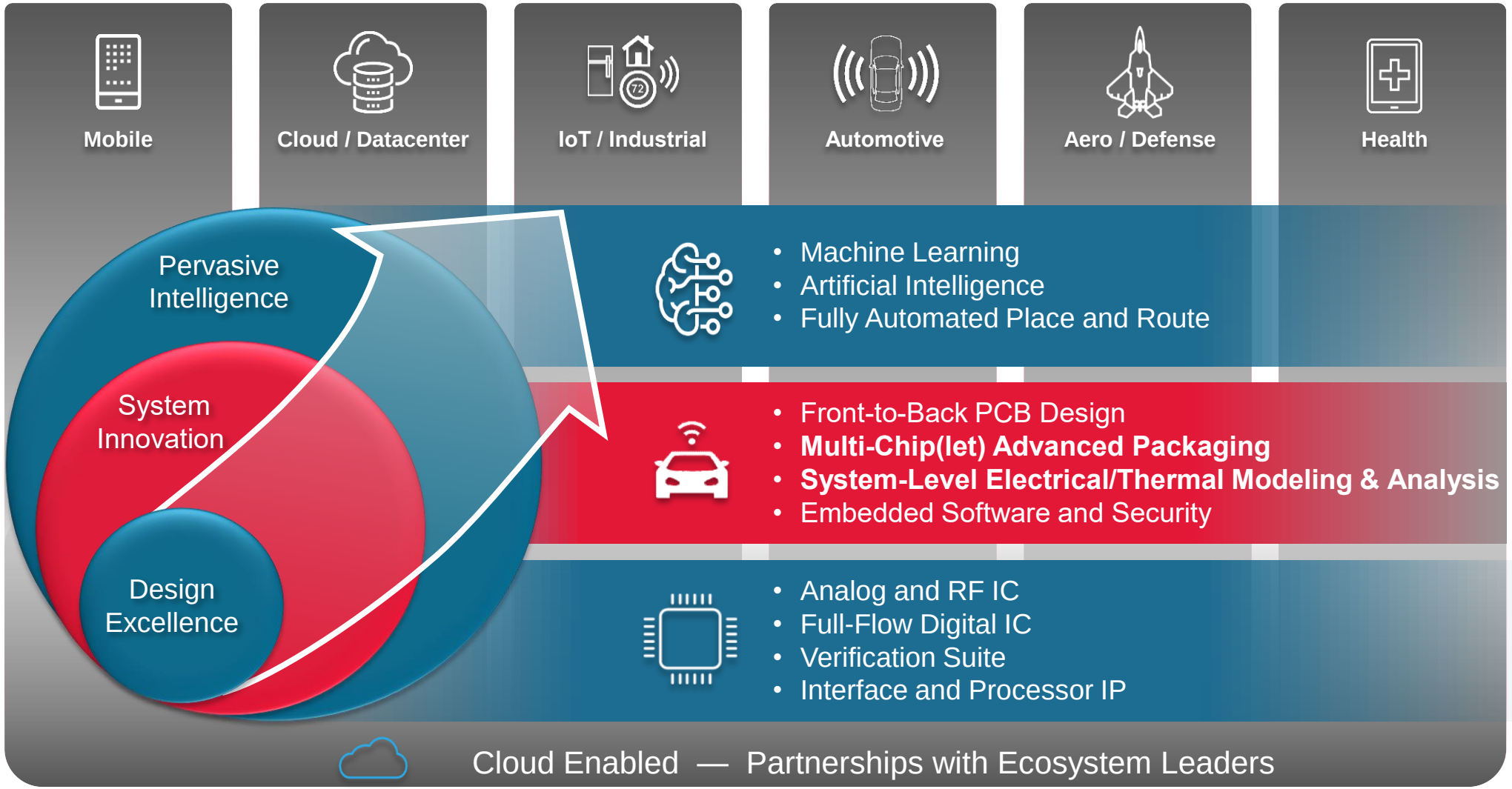
Outline

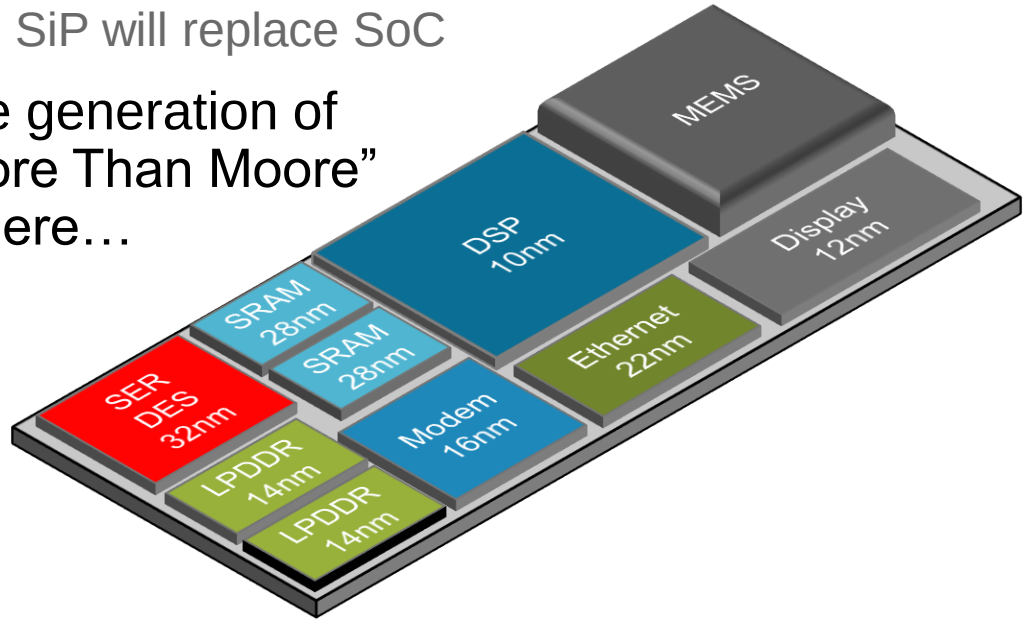
- Advanced Multi-Chip(let) 3D Packaging Technology Trends
- Cadence 3D Multi-Chip(let) Advanced Packaging Solutions
- Reference Flows

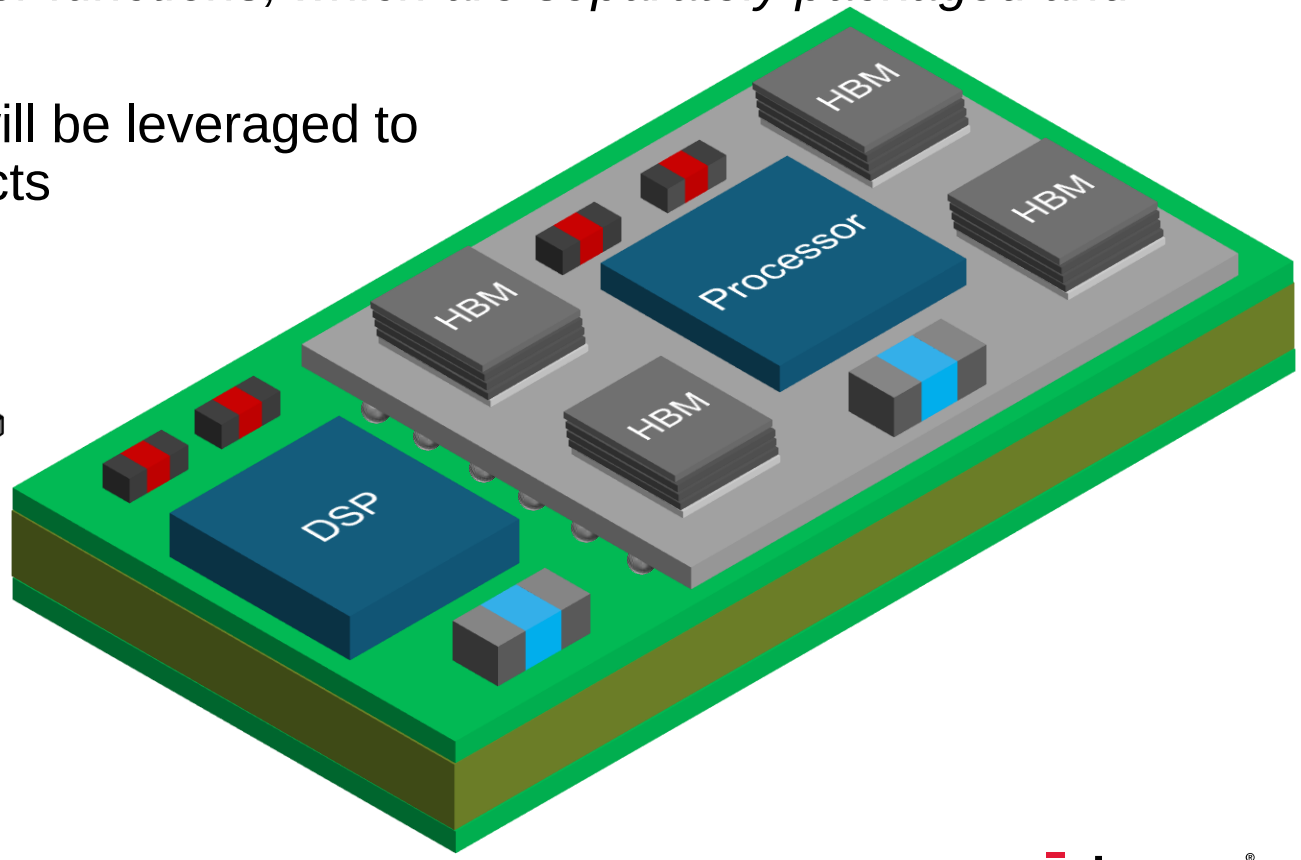
Cadence Intelligent System Design…Thinking Outside The Chip



The Beginning of the “More Than Moore” Era

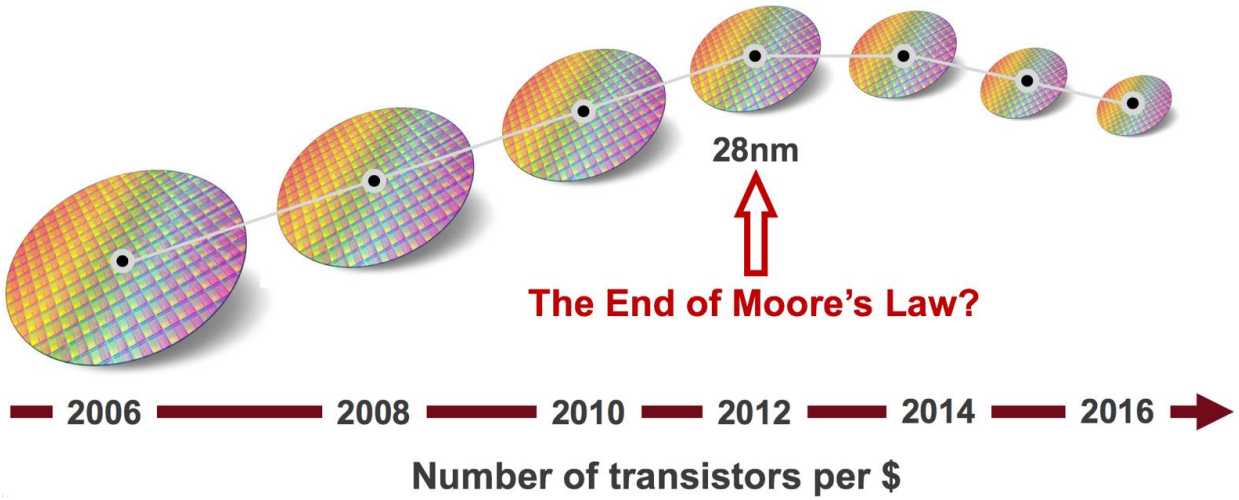
- For the past five decades, the electronic industry has thrived while enjoying the benefits of Moore’s Law. But things are changing…The economics of semiconductor logic scaling are gone
- Gordon Moore knew this day would come. He also predicted that *”It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected”.*
- Heterogeneously integrated packaging (SiP) will be leveraged to design the next generation of electronic products
  - SiP will replace SoC
- The generation of “More Than Moore” is here…

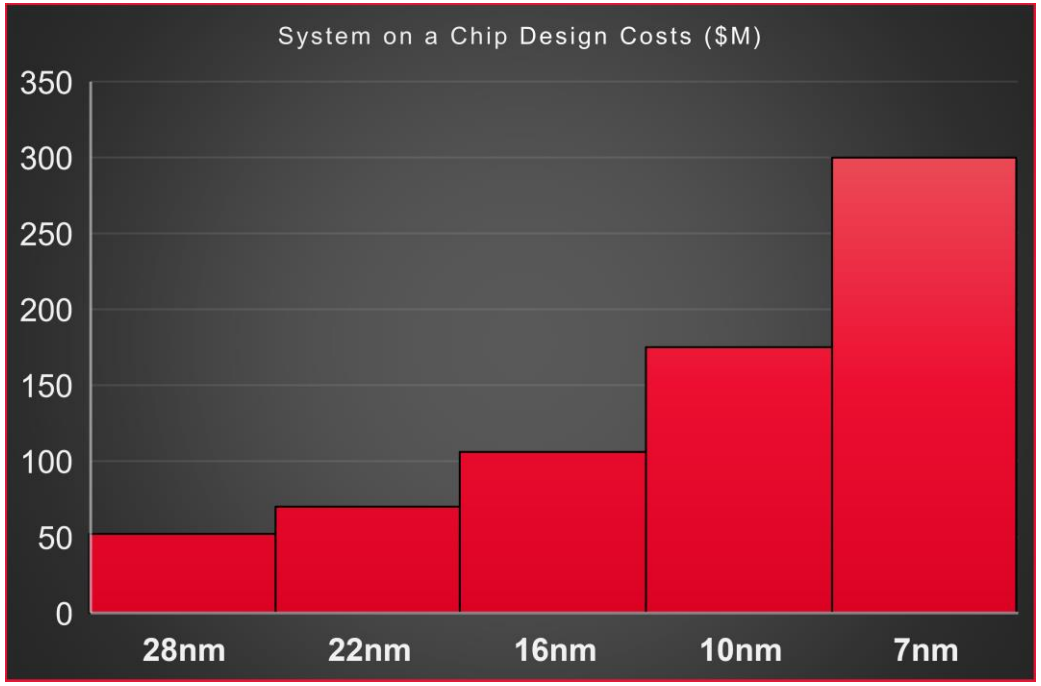




Is Moore's Law Already Dead?

- It's more than the limitations of physics…
- Cost per transistor has steadily increased since 2012/3 (28nm)
- Designing chips at the latest nodes is hard and expensive
  - Low-volume businesses can't justify the NRE costs of designing an SoC at the latest node
  - Requires huge teams of engineering specialists that aren't always easy to find
  - Systems and software companies now designing chips and challenging the status quo of SoC approach
- Todays SoC's are reaching reticle limits…but big chips don't yield anyways
- More Analog/RF content in today's designs.
  - Analog/RF never have benefited from Moore's Law





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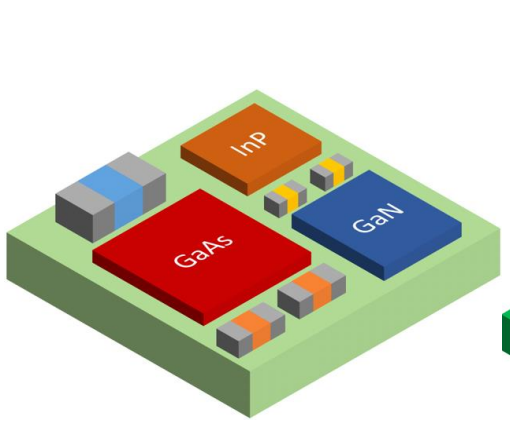
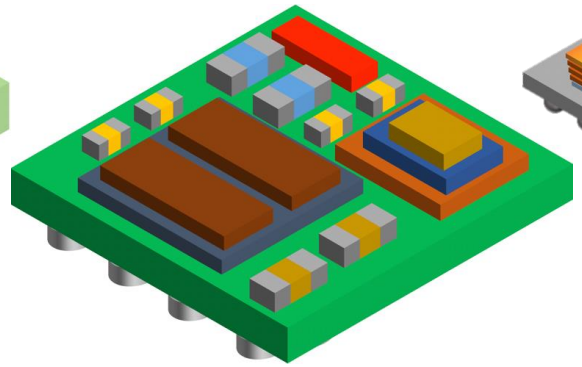
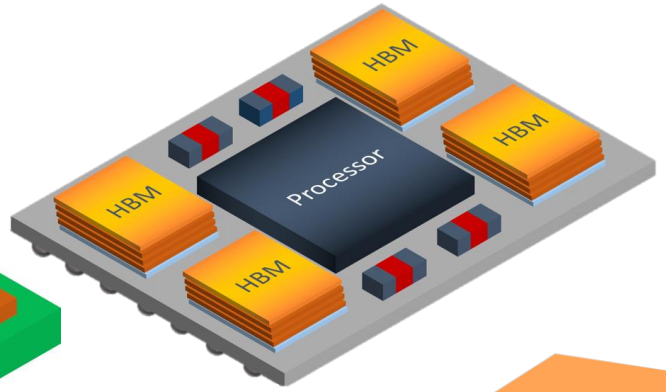
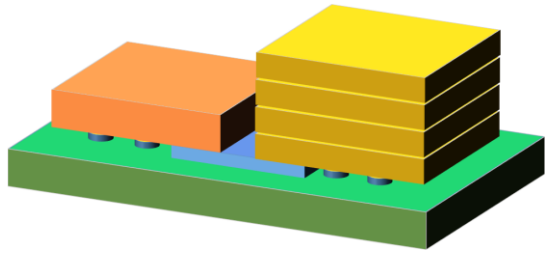
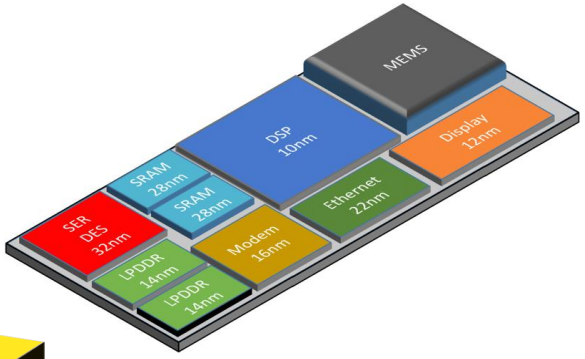
Evolution of Multi-Chip(let) Packaging…











Multi-Chip Module (MCM) — 1970

System in a Package (SiP) — 1998

RF Module — 2005

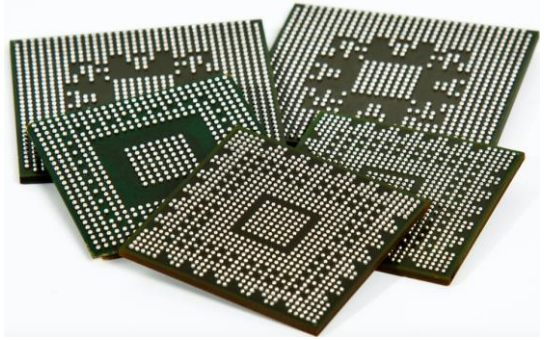
Silicon Interposers 2.5D IC — 2008

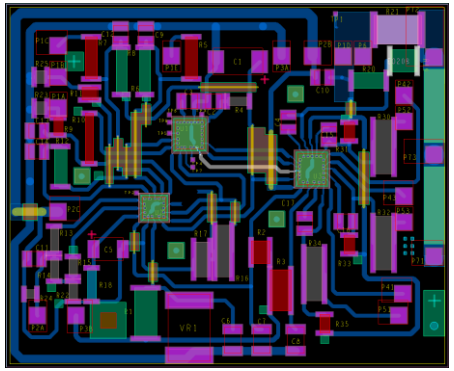
FOWLP 3DIC — 2018

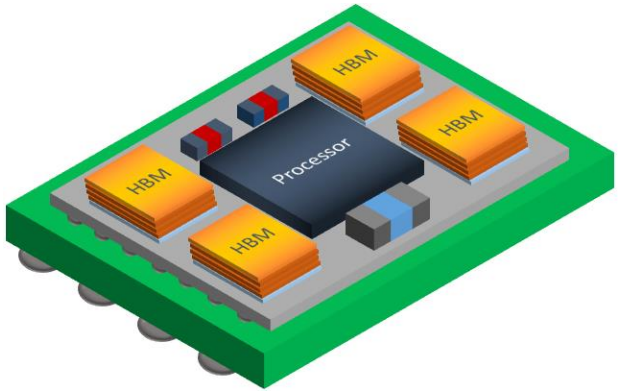
Heterogeneous Integration Disaggregated SoC — Future

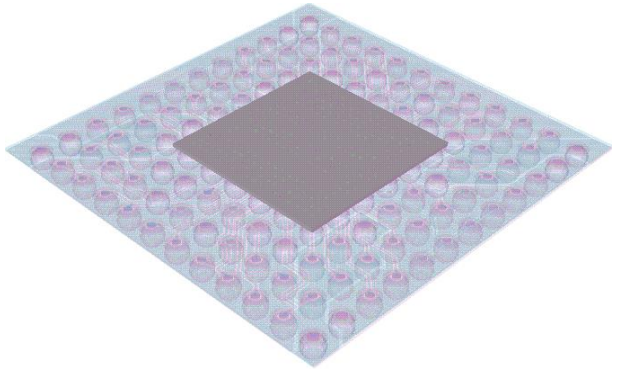
The Next Packaging Paradigm Change is Here…

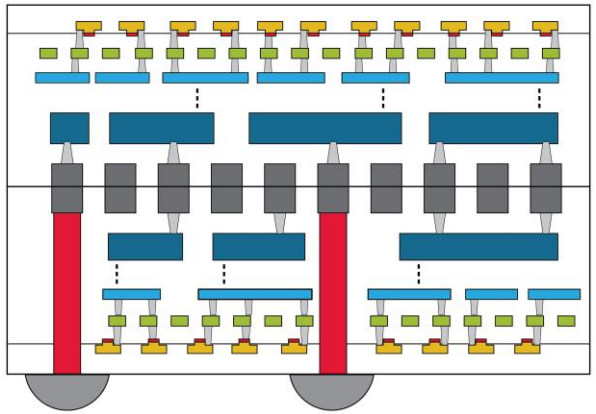
Mechanical Design Tools	PCB-Like Design Flows	Hybrid Design Flows	IC-Like Design Flows
Mechanical Leadframe	Routable Substrates Organic & Ceramic	2.5D-IC/Silicon Interposer, Embedded Bridges & FOWLP	3D-IC

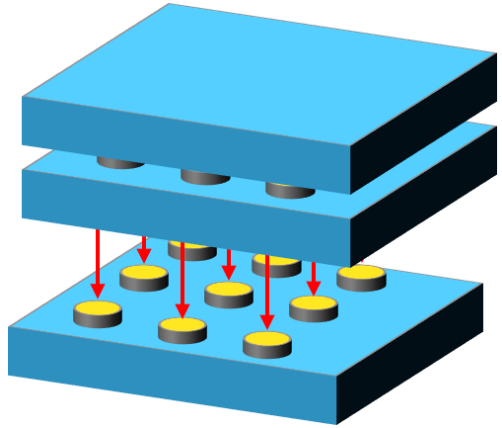












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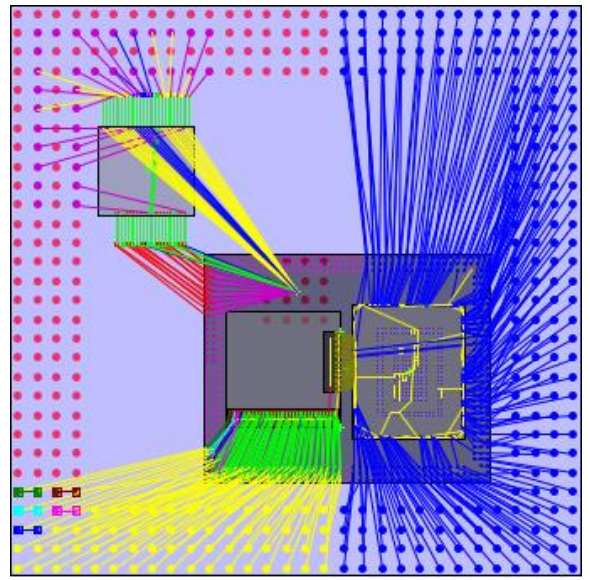
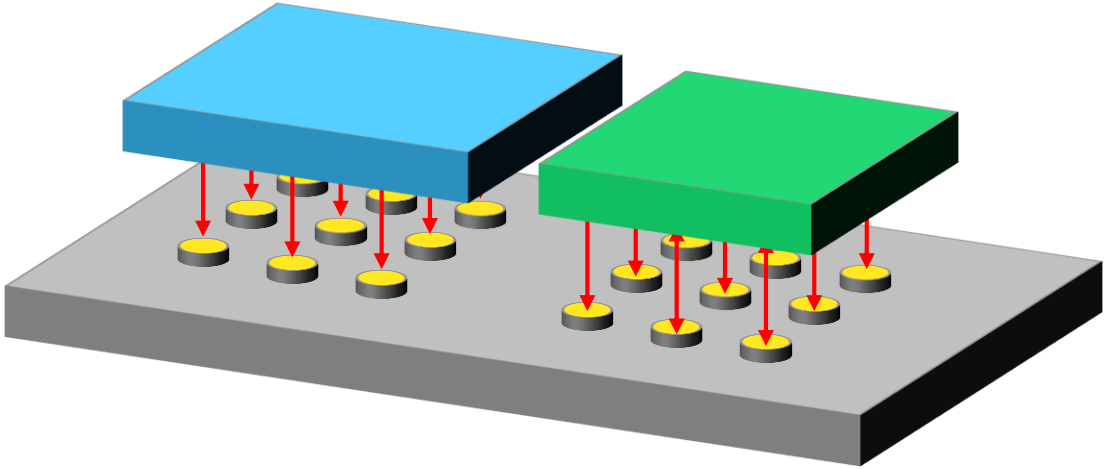
Design Tool/Flow Challenges for Next-Gen Heterogeneously Integrated 2.5-/3D-IC Designs…

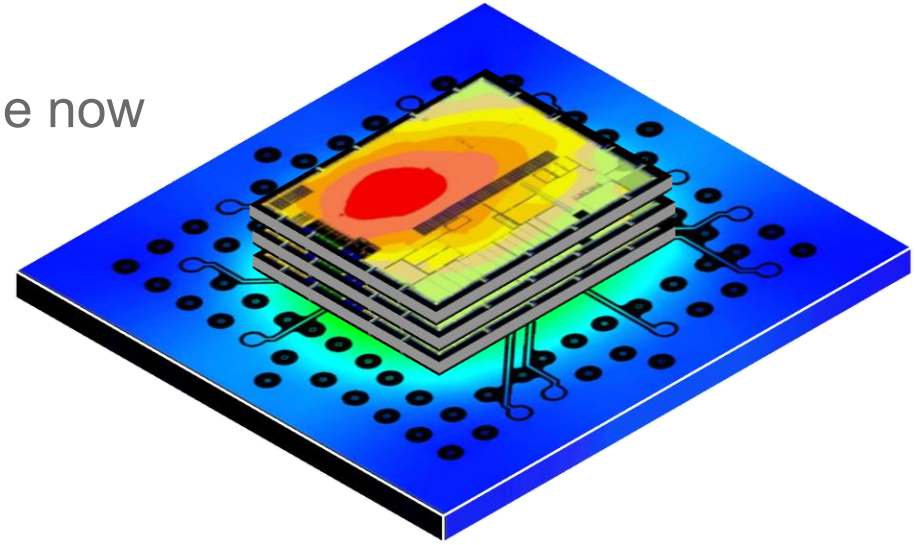
- Top-level design aggregation and management
  - Pre-layout planning
  - Top-level (chip to chip to package to PCB) netlist definition
  - System-level IO optimization
- Understanding the right level of chip(let) abstraction/representation
  - Simple (extents & pin locations), Complex (Full chip(let))
- Advanced multi-chip(let) IC packages require specialized verification
  - Layout vs schematic (LVS) connectivity validation driven by top-level management tool
  - Advanced chip-to-chip alignment checking
  - Silicon substrate design and verification methodology
- Cross-domain electrical/thermal modeling
  - Modeling the coupling effects between domains?
  - Linking different extraction tools for IC, package, and PCB?

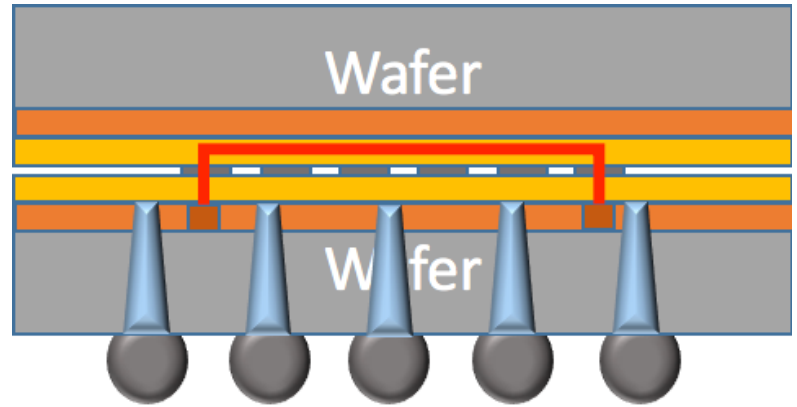




Additional 3D-IC Considerations

- No significant flow/tool challenges when chips designed/verified independently and then bonded
  - Innovus and Allegro implementation platforms are capable now
  - Virtuoso will be later this year (ISR6)
  - Signoff and Test tools are all 3DIC enabled
- Major challenges arise when two or more chips need to be concurrently designed together
  - Huge database sizes
    - Hundreds of millions to billions of instances
  - Cross-chip partitioning and floorplanning
  - Thermal analysis more critical than electrical analysis
  - Route resource sharing between two or more chips
  - Automatic direct copper to copper connectivity
  - STA across two chips stacked face-to-face





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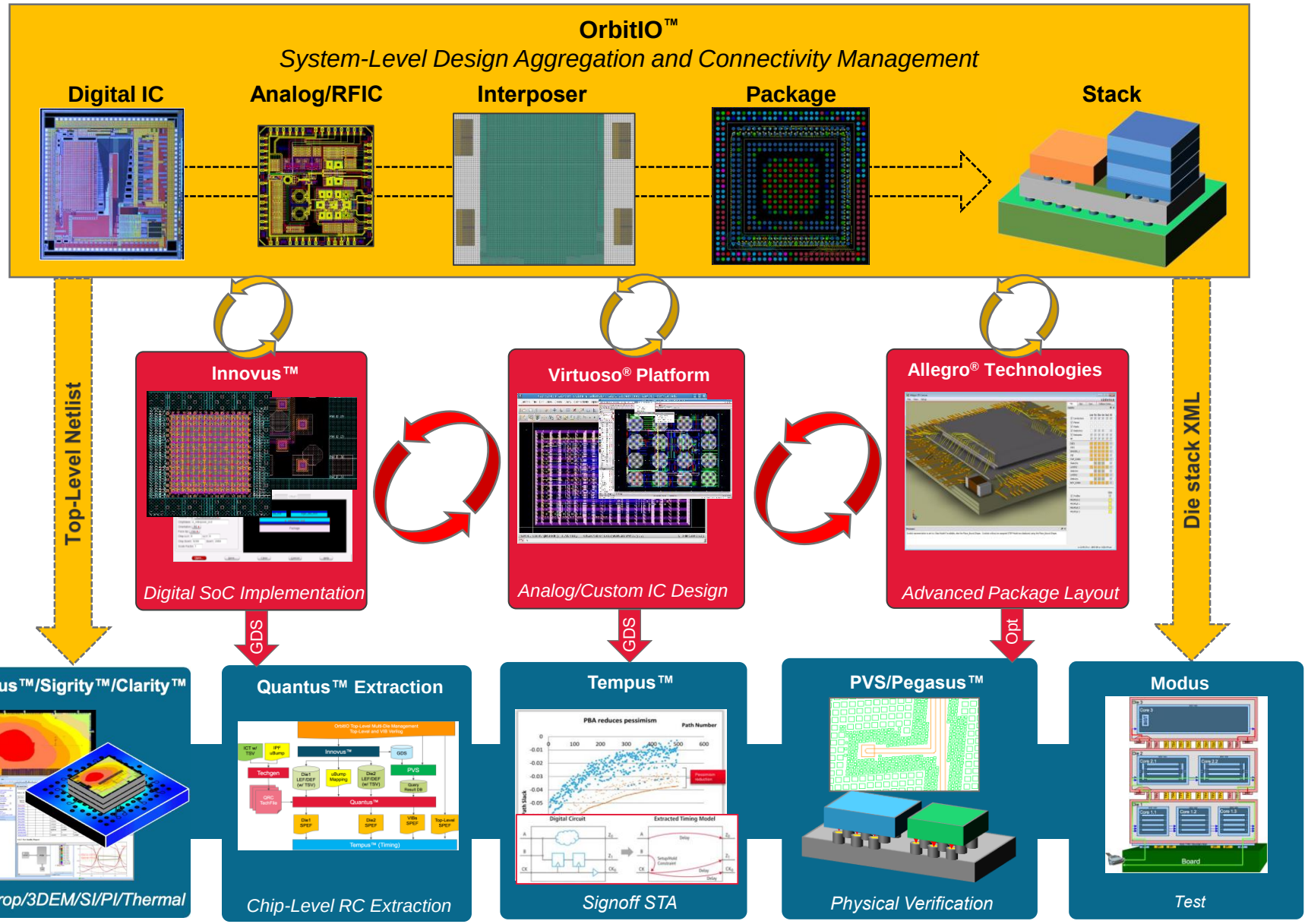
Top-Level Flow

Multi-Chip(let) Design Planning, Optimization and Management

Multi-Chip(let) Design Implementation

Multi-Chip(let) Design Test, Extraction, Analysis, DFM, Verification & Sign-Off



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Implementation Solutions for Multi-Chip(let) Advanced Packaging

- Cadence implementation platforms have been enabled to support next-gen multi-chip(let) advanced packaging
  - Multi-chip(let), TSV, MB and chip tiering aware
  - Each platform has inherent advantages and disadvantages
  - Performance and capacity must be considered
  - Two or more platforms often required to create optimal design
  - Cross-platform solutions improve domain to domain data exchange

	Allegro® Technologies		Virtuoso® Platform		Innovus™ Solutions
Architecture	Flat Layout PCB and BGA	VSDP/VMT/XDA/OA →	Hierarchal Layout Analog/Custom IC	XDA/OA →	Hierarchal Layout Digital SoC
Package Type	Organic, Silicon, ABF, PoP, FOWLP, 2.5D/3DIC		Silicon (Active & Passive), 2.5D/3DIC RF module		Silicon (Active & Passive), 2.5D/3DIC
Routing Styles	Constraint driven 45 degree auto and push/shove		PDK driven, Litho correct, 45 & 90 degree routing		Litho correct, timing driven routing, plus 45 degree RDL routing
Performance	100,000s		1,000,000s		1,000,000,000s
Parasitic Extraction	Clarity™/Sigrity™ + SI/PI Analysis	←	Quantus Extraction Clarity™/Sigrity™	←	Quantus Extraction
Manufacturing Output	IPC2581,Gerber, GDSII		GDSII, OASIS		GDSII, OASIS
Physical Verification	PVS/Pegasus				
OS	Windows, Linux		Linux		Linux

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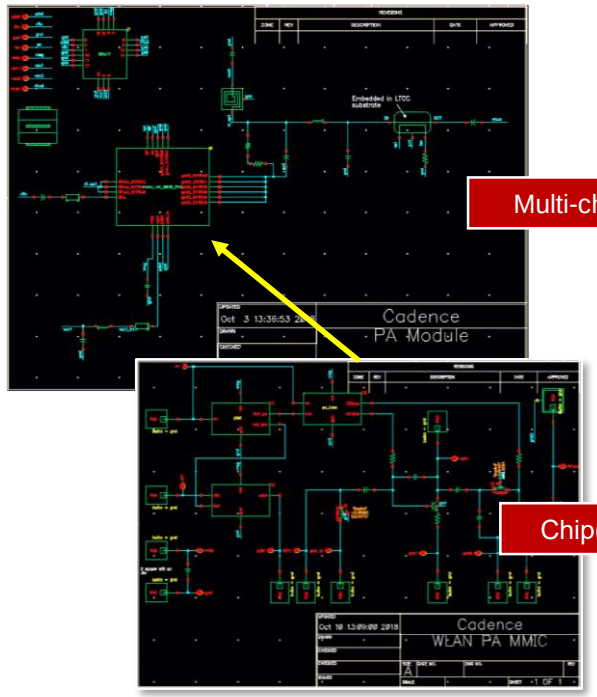
Virtuoso® for Intelligent System Design

- Cross-platform solution that integrates Virtuoso, Allegro and Sigrity technologies
- Industries first multi-chip(let) (multi-PDK) solution that provides system-level connectivity validation, automated layout parasitic feedback loop and true concurrent chip/package co-design

Golden System-Level Schematic

Capture top-level hierarchal schematics for multi-chip(let) designs to drive LVS

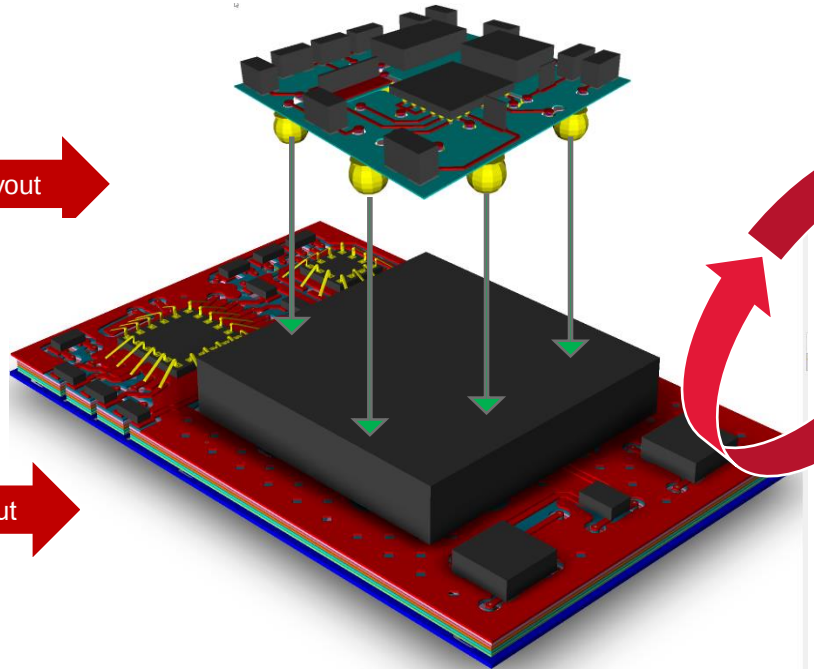


Multi-chip(let)Layout

Chip(let) Layout

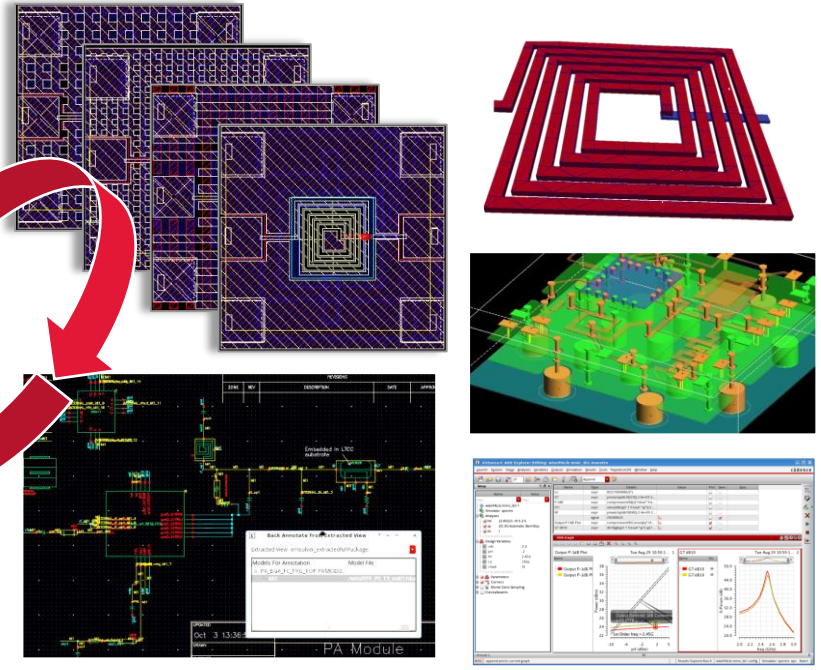
Edit-in-Concert™

Automatically drive multi-domain multi-chip(let) layout with seamless co-design

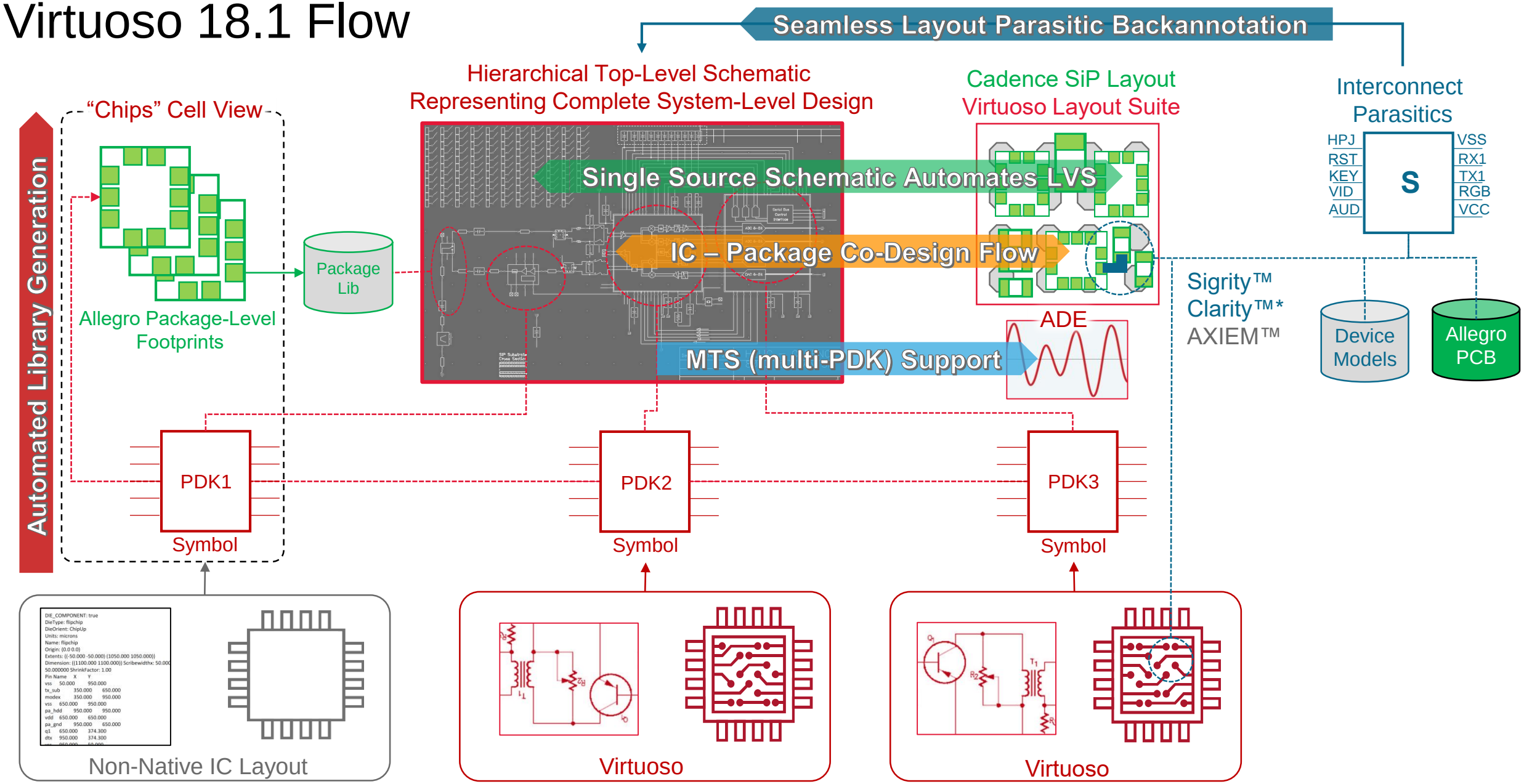


Smart EM Integration

On-chip/off-chip 2.5D/3D EM (extraction) with automated back-annotation & simulation flow

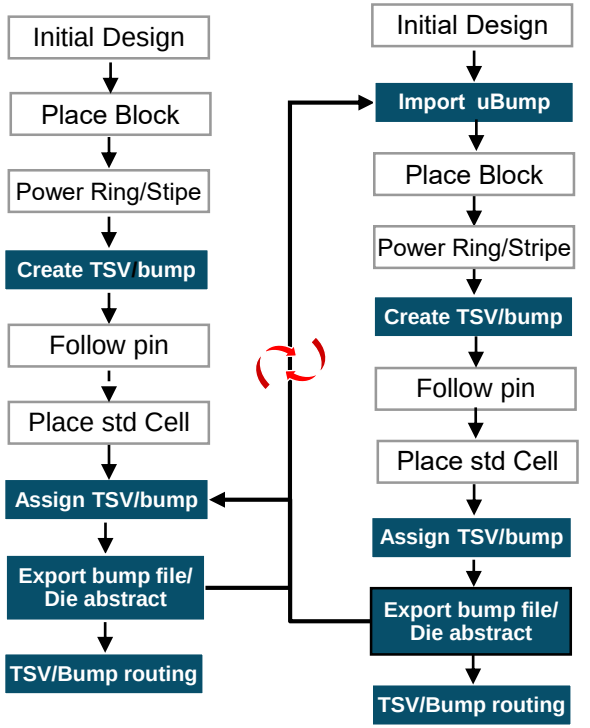


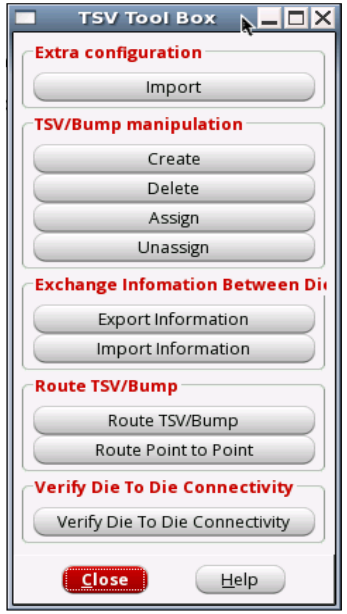
Virtuoso 18.1 Flow

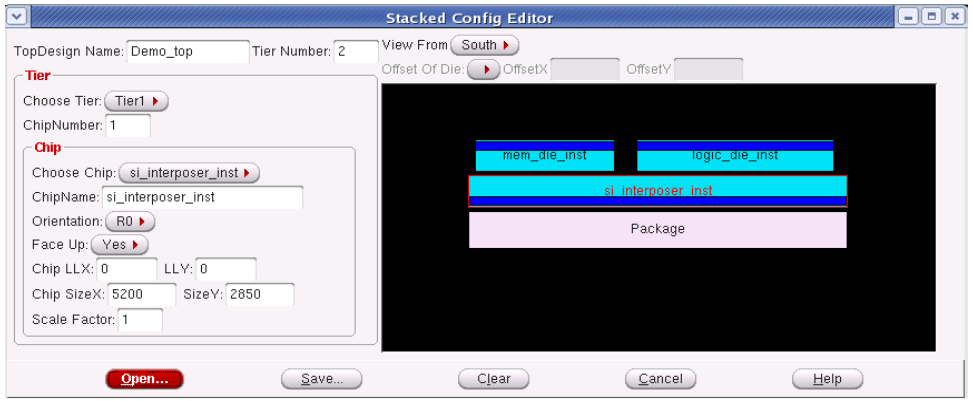


Innovus Multi-Die 2.5D/3D IC Implementation

- Netlist-driven multi-die flow
  - High-capacity implementation for large standard-cell based digital designs
  - Flow Based on die abstraction and bump file
  - GUI-based 3D stacking/tiering
- Basic structure modelling for 3D Implementation
  - Back side Metal – MB as a routing layer
  - Through Silicon Vias modeled as a VIA between M1 and MB
  - uBump modeled as “CLASS COVER BUMP” macro
- Seamless TSV/uBump creation
  - TSV Toolbox
  - Specific 3D IC commands for TSV/uBump creation, net assignment , power and signal routing
  - Built-in alignment checks
- Multi-dies co-design during floorplanning
  - Hard constraints: uBumps with same net on adjacent dies in stack must be aligned
  - Soft constraints: Minimize wire length for die to die

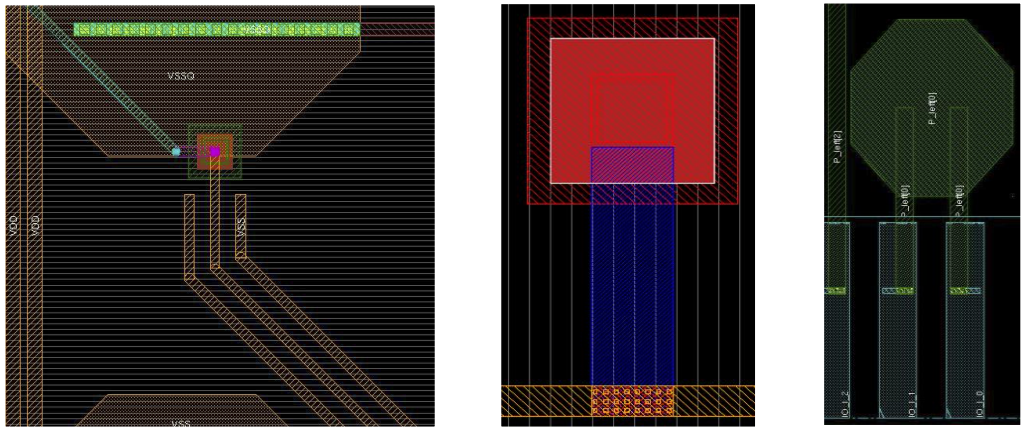


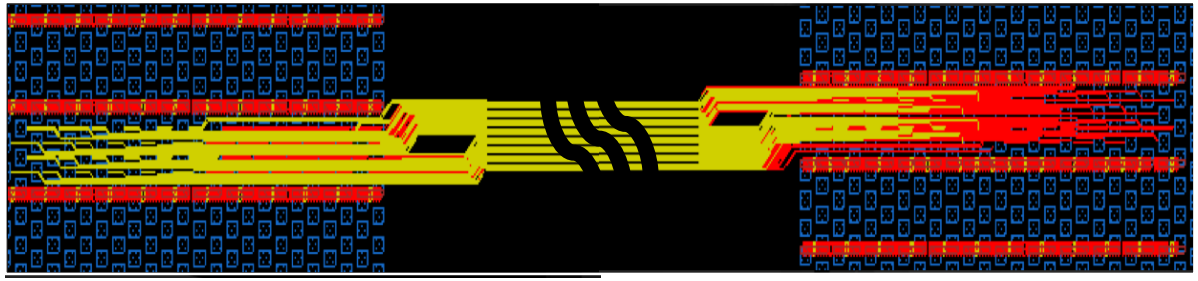


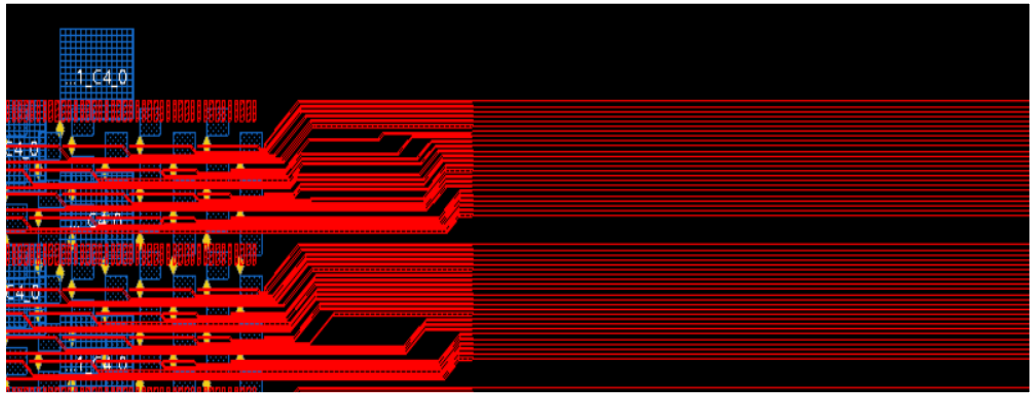


Innovus Multi-Die Routing Capabilities

- Auto Routing using NanoRoute RDL router
  - Complete Stack- 45-Degree or Manhattan
  - Cu Pillars supported
  - Multi-IO to Bump Routing supported
- Auto Bus Routing
  - Uses NanoRoute HF router
  - Maintain Bus ordering
  - Honor spacing/width constraints
- Flip Chip Routings using fcroute
  - Used for PG routing and connections to IO Pads
  - 45-degree routing enabled

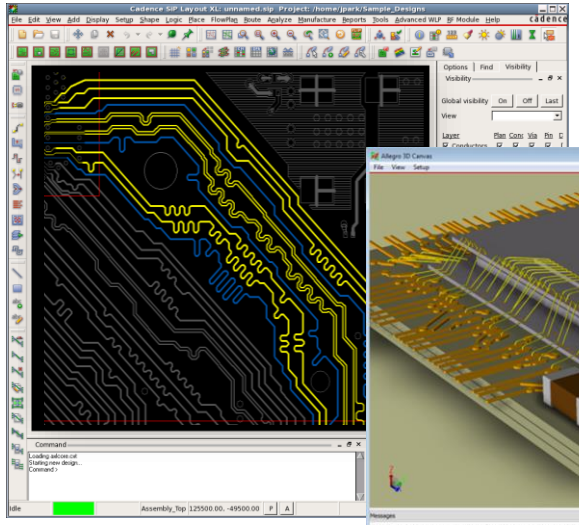


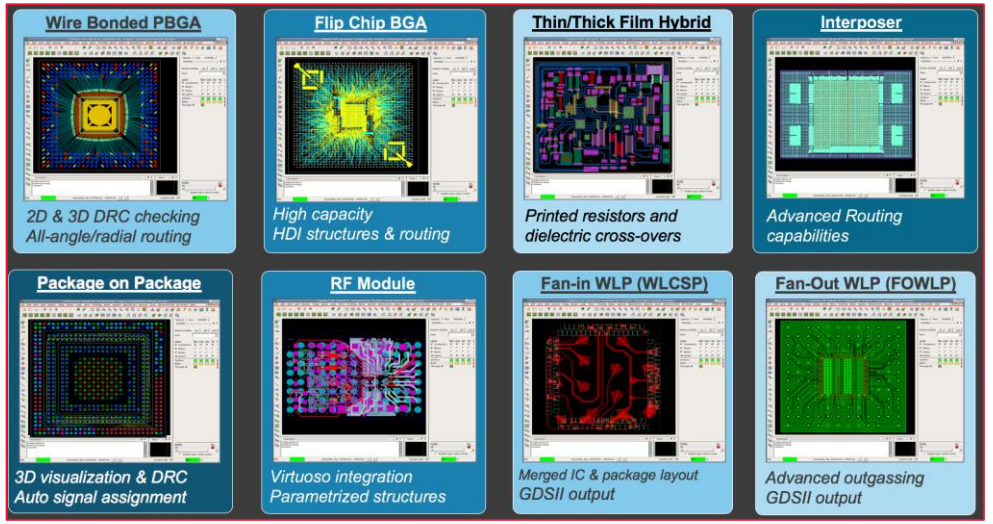




Multi-Chip(let) Capabilities of (Allegro®) Cadence SiP Layout

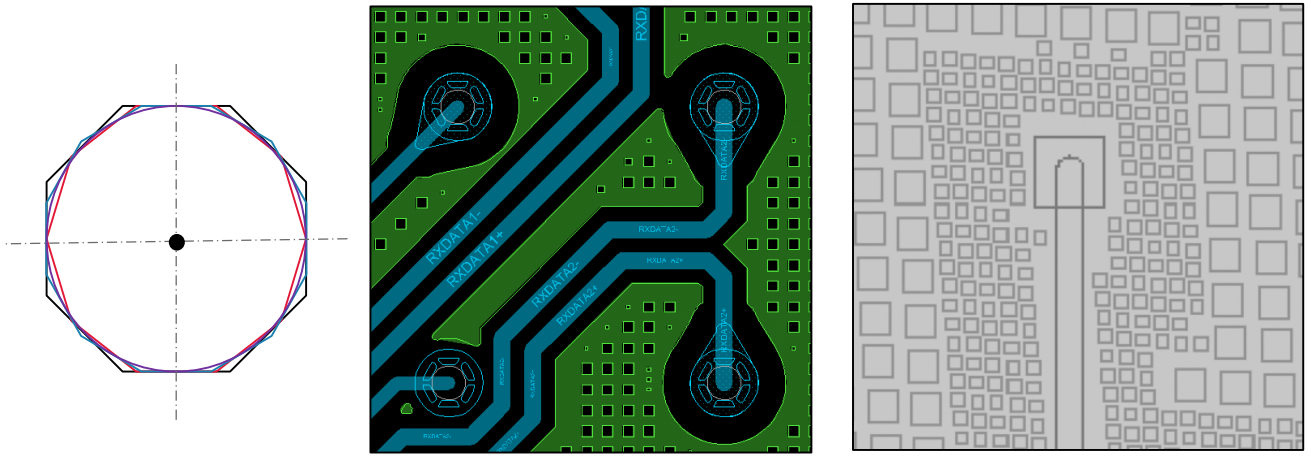
- Architected as a package/module design solution
  - Correct-by-construction with real-time DRC
  - Support for all chip(let) attach methods
    - Bond wire, flip-chip, stacked, embedded, etc.
  - Incredibly flexible connectivity use model
    - Schematic and/or table and/or spreadsheet
    - Connectivity on-the-fly
  - Technology file-driven package substrate style stack-up
    - Unlimited substrate material types
      - Laminates, Ceramics, Glass, Flex, etc.
  - Advanced package-specific push/shove and automatic routing styles
    - Radial, all angle, flip-chip
  - Package-specific manufacturing outputs
    - BGA ball-maps, bond wire diagrams
  - Integration with IC-level DRC, LVS and metal fill tools
  - PCB and IC manufacturing outputs
    - IPC-2581, Gerber, GDSII, etc.

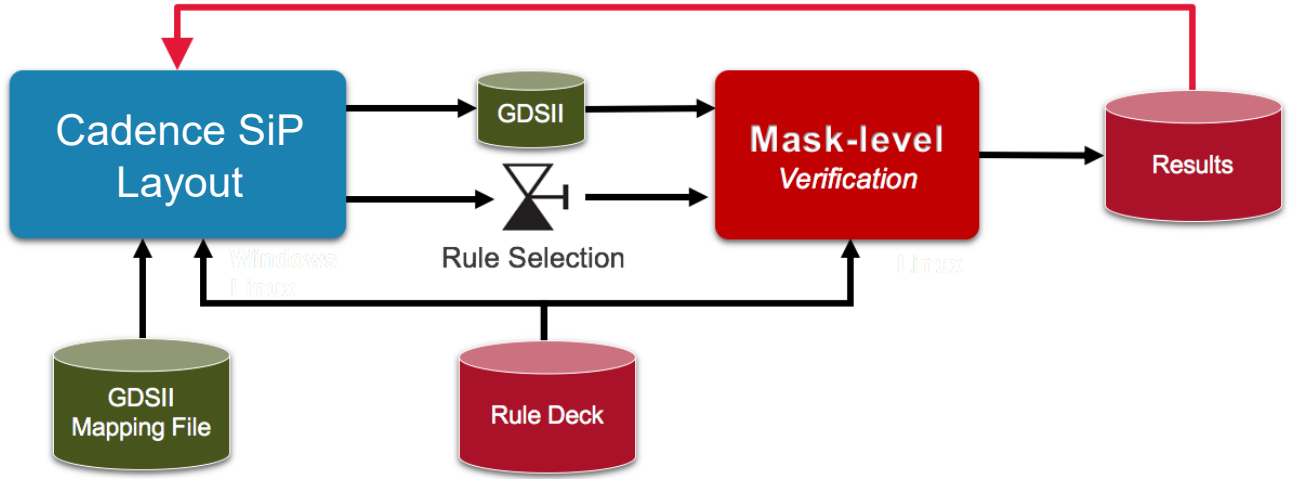




Cadence SiP Advanced WLP Option

- Layout features specific to silicon substrate designs
  - Advanced filleting and acute angle identification with automatic coverage
  - Automatic pad degassing
  - Progressive metal degassing algorithm
- Mask-level accurate output data (GDSII)
  - Advanced arc vectorization
- Cross-OS (Windows/LINUX) integration with Cadence PVS™ verification tool for:
  - Mask-level DRC
    - Rule deck integration with SiP layout eases rule selection
    - DRC results file integrated with SiP Layout provides closed loop signoff flow
  - Connectivity verification (LVS) of multi-chip(let) designs
    - CDL netlist export with option to included pseudo resistors to support non-CDNS verification tools
  - Region specific advanced metal fill (balancing)

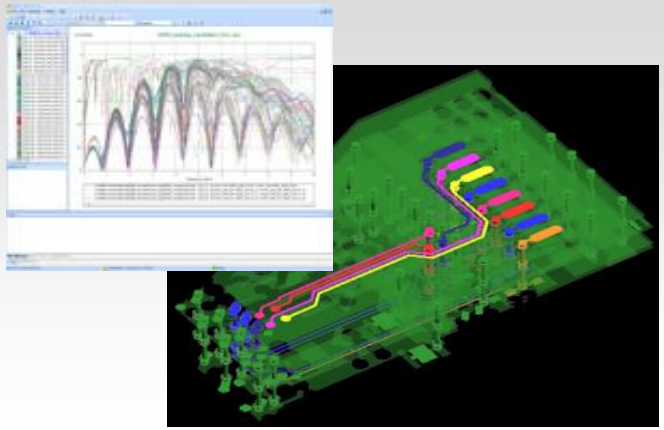




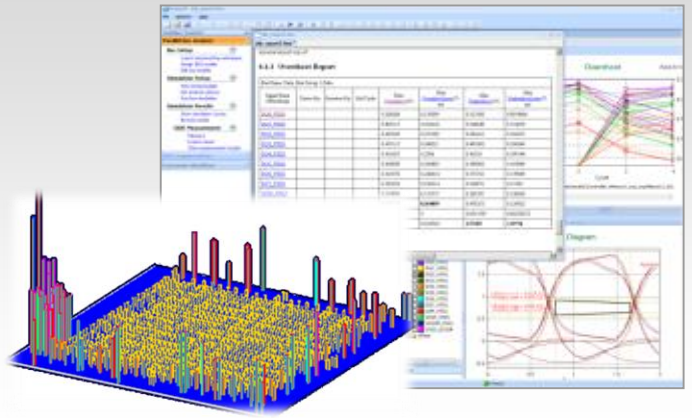
Sigrity™/Clarity™ Technologies for Electrical/Thermal Modeling

- Technologies for 3D EM, signal integrity and power delivery modeling
  - Multiple full-wave (Clarity™) and quasi-static solver/extraction technologies
  - Coupled power (PDN) and signal integrity analysis
  - Robust frequency- and time-domain simulation technology can be combined with statistical techniques for advanced multi-gigabit channel analysis
  - Industry-leading IBIS-AMI modeling support
  - Compliance validation kits for multiple high speed interfaces

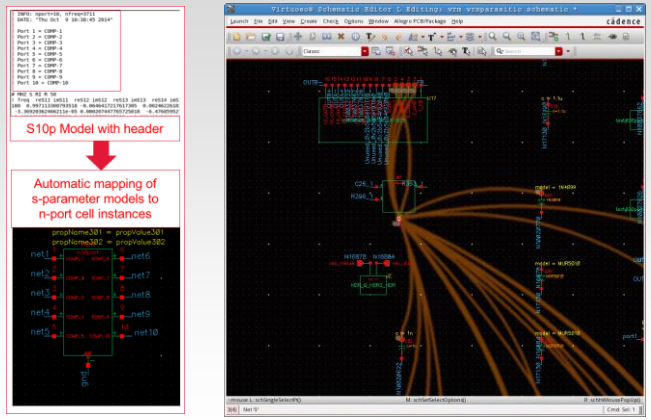
3D EM Extraction



Signal & Power Integrity

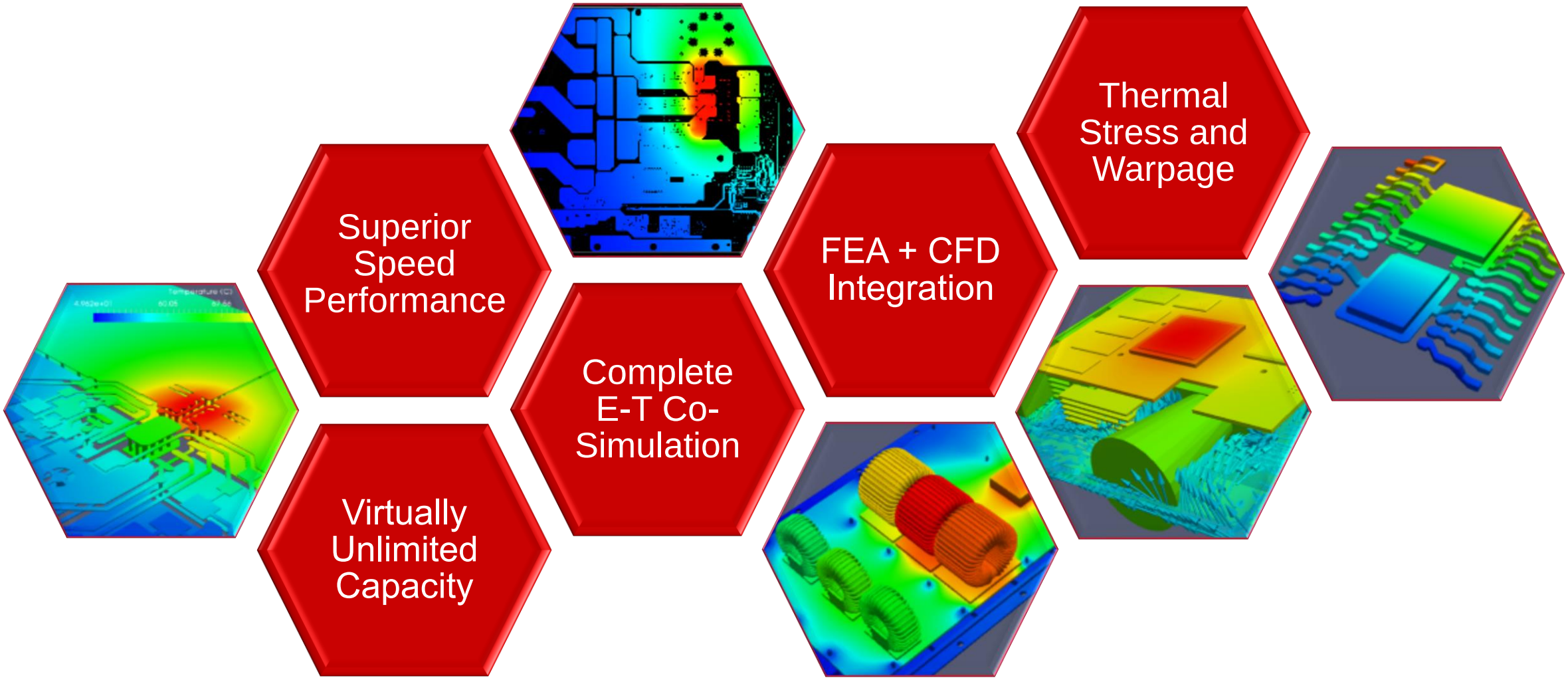


Direct Schematic Integration



Celsius Thermal Solver: 3D Multi-Physics E-T Co-Simulation

Advanced computational capabilities and features to improve productivity



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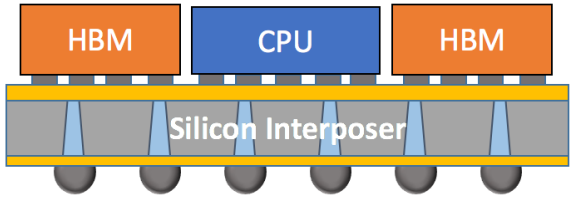
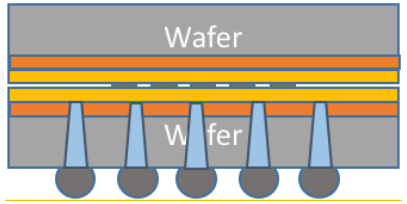
TSMC “Certified” Flows for 3D Advanced Packaging

InFO_MS +PoP (FOWLP)

CoWoS (2.5D IC)

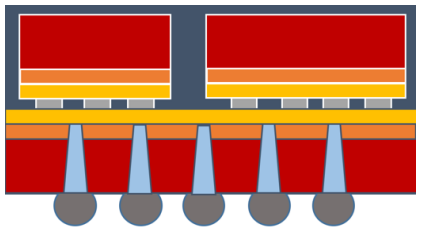


WoW (3D IC)



NEW

SoIC (3D IC)



Cadence Delivers Design and Ana Enhancements for TSMC InFO an 3D Packaging Technologies
SAN JOSE, Calif., 13 Sept 2017

Highlights:

- Completed InFO flow provides custo holistic experience from planning an

Cadence Supports New T Packaging Technology
SAN JOSE, Calif., 01 May 2018

Cadence Design Systems, Inc. (NASDAC suite of Cadence® digital, signoff and cus advanced IC packaging design solutions, (WoW) stacking technology.
For more information on the Cadence sol

Cadence Delivers Support for TSMC InFO_MS Advanced Packaging Technologies
Cadence signoff and packaging solutions optimized for TSMC InFO_MS packaging technology

SAN JOSE, Calif., 02 Oct 2018
Cadence Design Systems, Inc. (NASDAQ: CDNS) today announced that its digital tools and advanced IC packaging

PRESS RELEASE: Paid content from Business Wire

Cadence Design Solutions Certified for TSMC-SoIC™ Advanced 3D Chip Stacking Technology

yesterday

Press release content from Business Wire. The AP news staff was not involved in its creation.

Click to copy

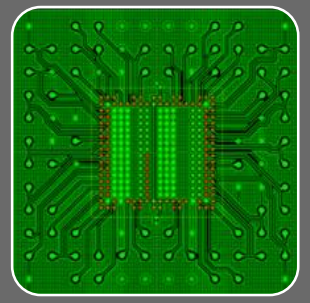
SAN JOSE, Calif.--(BUSINESS WIRE)--Apr 23, 2019--Cadence Design Systems, Inc. (NASDAQ: CDNS) today announced TSMC certified Cadence’s design solutions for the new TSMC System-on-Integrated-Chips (TSMC-SoIC ™) 3D advanced chip stacking technology, which integrates heterogeneous chips—including logic ICs and memory—that are fabricated on different process nodes onto a single chip stack for a subsequent packaging process. A full suite of Cadence ® digital and signoff, custom/analog, and IC package and PCB analysis tools have been optimized for TSMC’s SoIC chip stacking technology, enabling mutual customers that require heterogeneous chipset integration capabilities to create complex designs more

- Complete reference flows from early planning to tape-out
  - OrbitIO for top-level management of all multi-chip(let) flows
  - Virtuoso, Innovus and Allegro implementation platforms for 2.5D/3D IC flows
  - Sigrity for chip & substrate-level electrical/thermal analysis
  - Cross-platform FOWLP flow including SiP Layout (Allegro), Sigrity and PVS

cadence®

Summary

Cadence Cross-Platform Solutions for Advanced Packaging

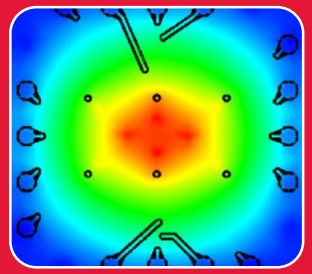


Complete Implementation Platforms

Support flexible entry point and seamless cross-platform co-design

Allegro®, Innovus™, and Virtuoso® technologies Each platform has unique and dedicated functionality and cross-platform capability for multi-chip(let) advanced packaging

Early-stage system-level exploration and top-level connectivity management with OrbitIO™



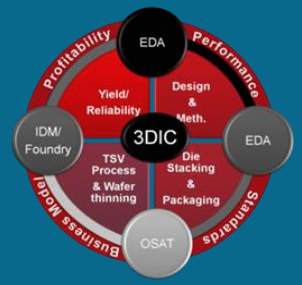
Robust Signoff Capabilities

Modus™ DFT and ATPG for 3D IC

Voltus™/Tempus™/Quantus™ digital analysis tools

Sigrity and Voltus for chip/package thermal analysis
Clarity™ 3D EM Extraction, SI, and PI provides system-level analysis

PVS/Pegasus™ for LVS, DRC and metal-fill



Ecosystem Partnership and Real Tape-out Experiences

Cadence has been working with ecosystem partners since 2007 on 3D IC

Over 10 test chips completed and multiple production chip tape-outs

Several ongoing projects