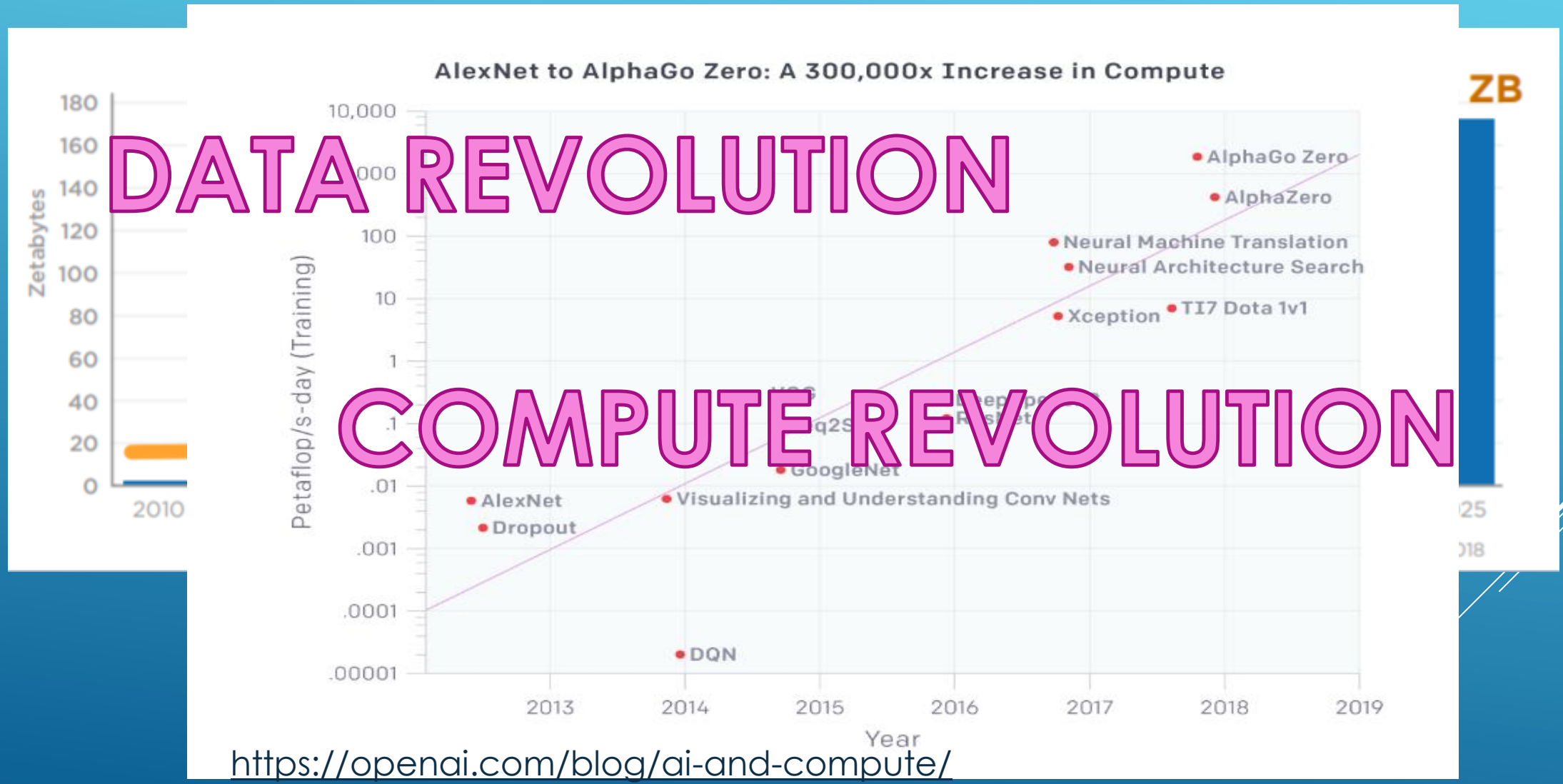
AI CHIPS EVERYWHERE, WHERE IS AI IN DESIGN

Srinivas Bodapati

Intel Corporation

AI/ML REVOLUTION

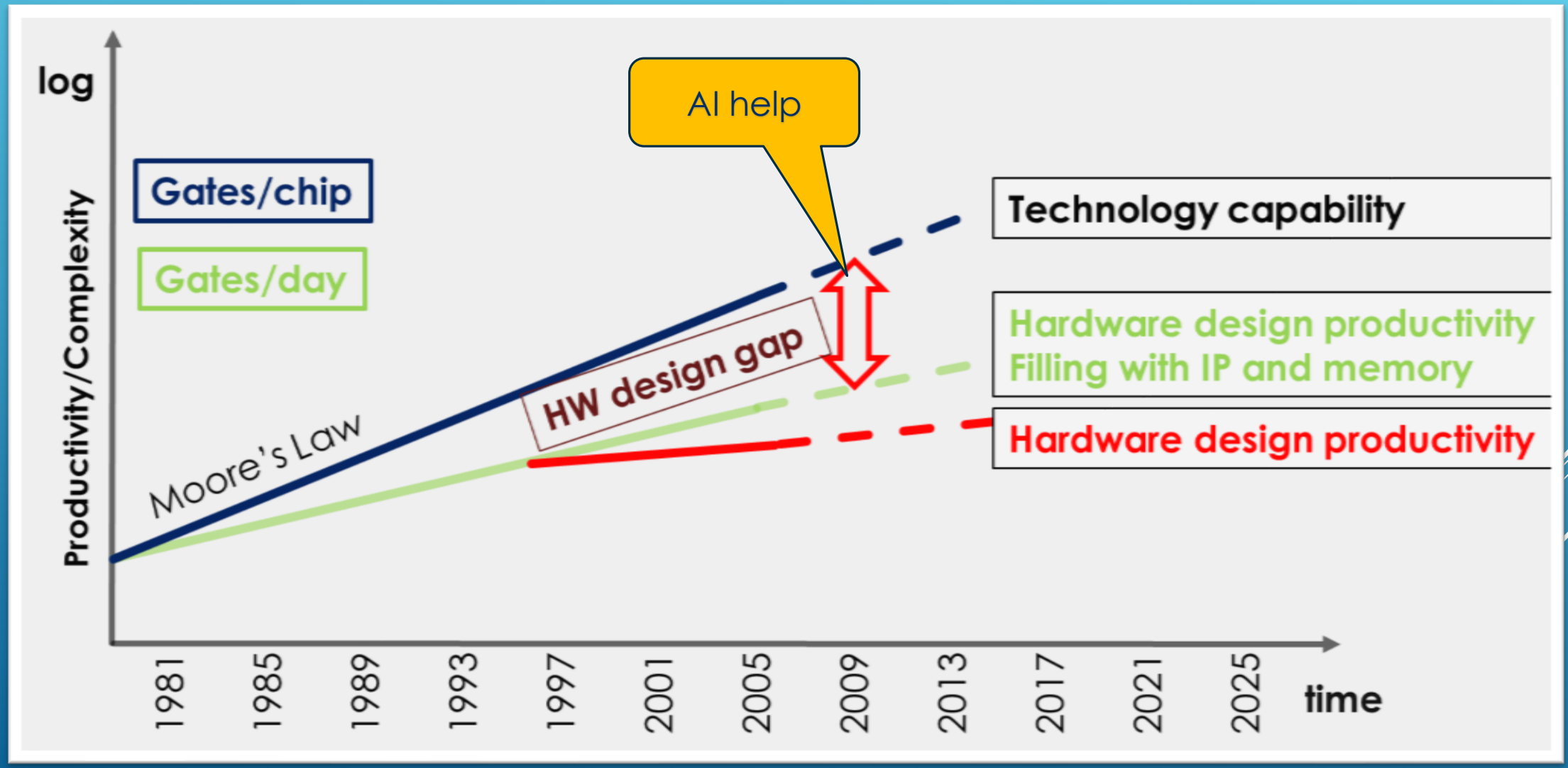


DATA REVOLUTION

COMPUTE REVOLUTION

https://openai.com/blog/ai-and-compute/

DESIGN PRODUCTIVITY GAP



ITRS 2011, Design

RECENT CONFIRMATION

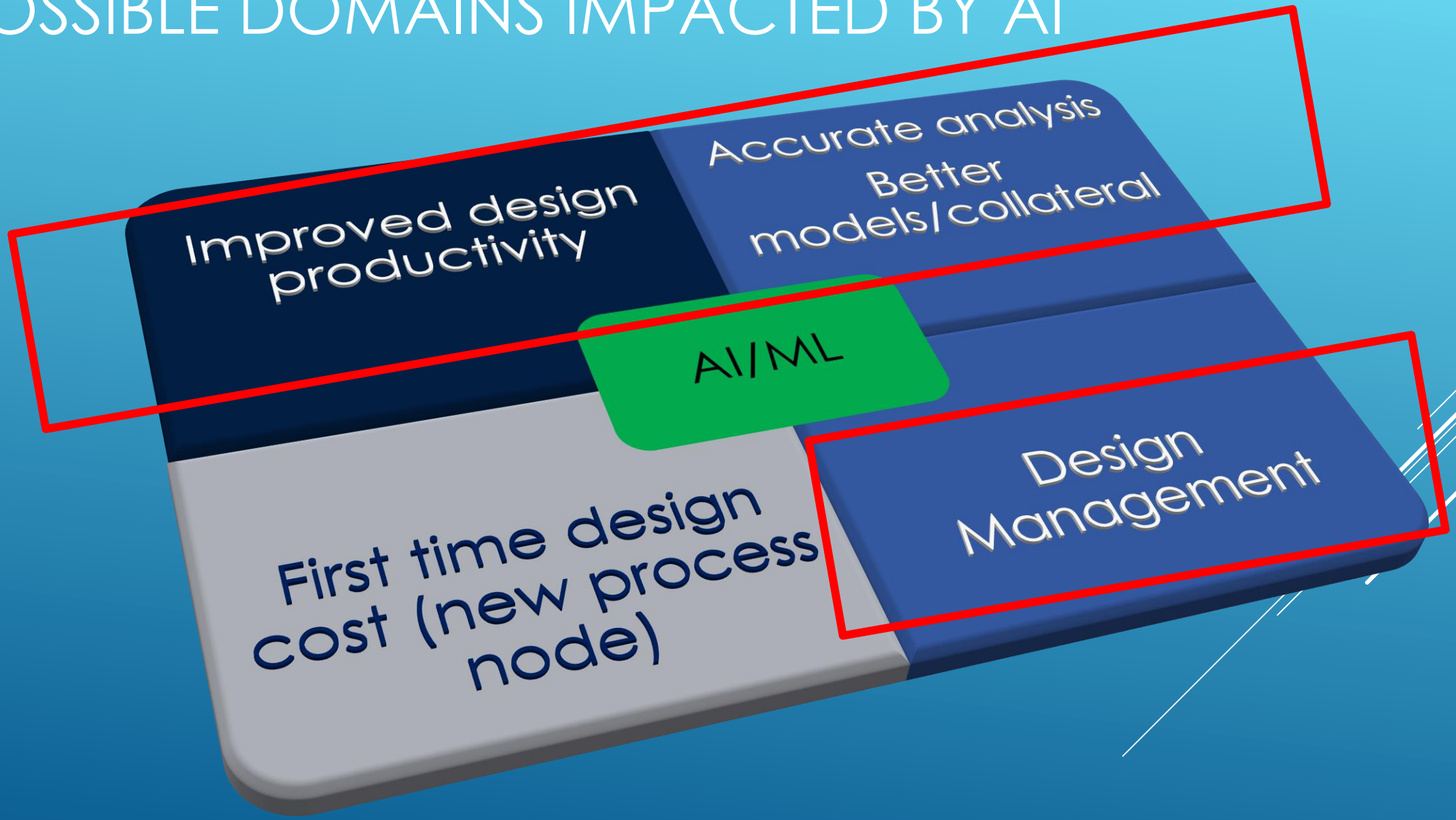
- https://semiwiki.com/eda/cadence/7622-an-update-on-the-design-productivity-gap/
- DAC 2018 Panel Discussion Quote
  - "Monster Chips – Scaling Digital Design Into The Decade

'Design implementation capacity must be improved. The Quality of Results (QoR) for blocks greater than 2 million instances tends to degrade substantially."

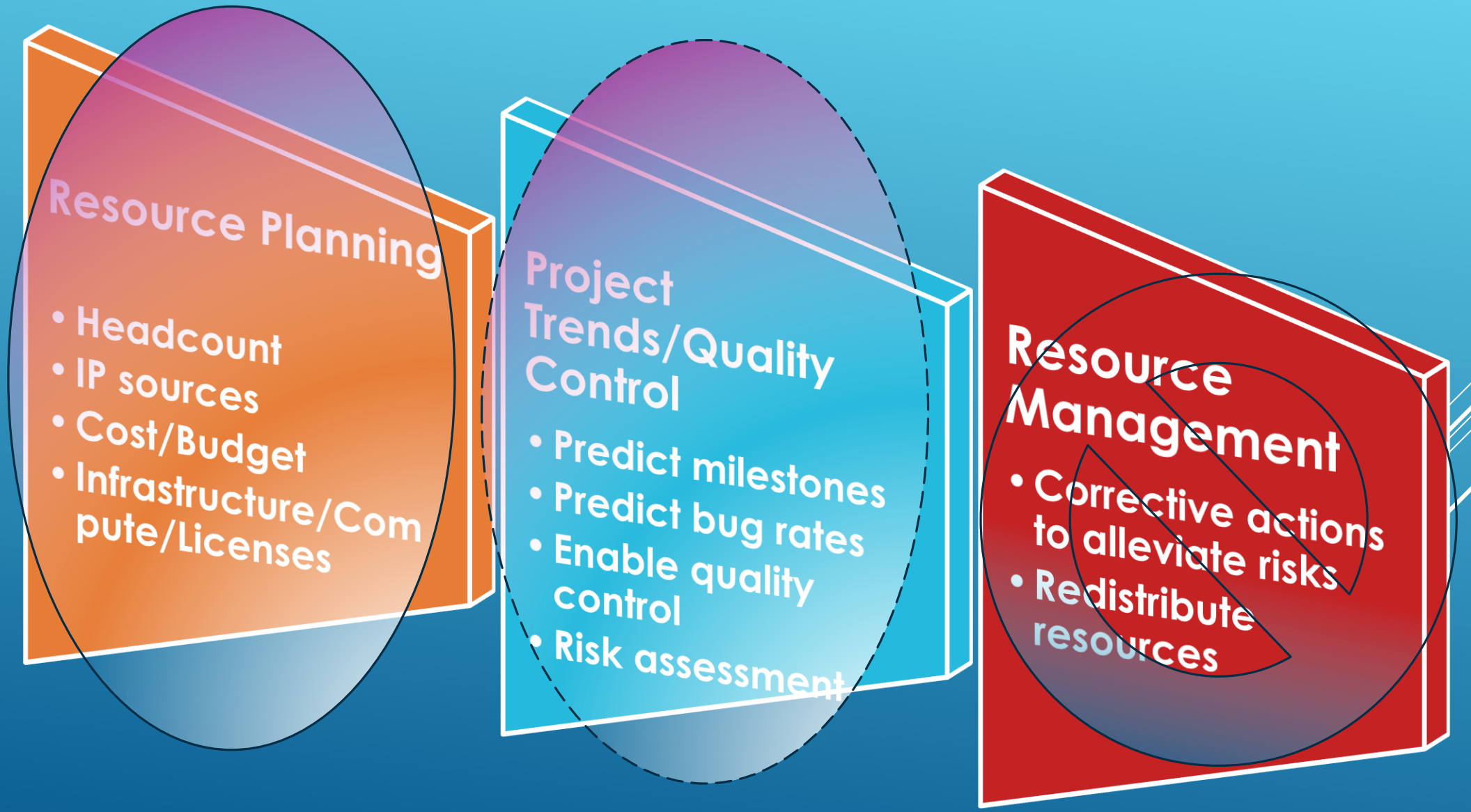
'Agreed. We are constrained to block sizes of 1M-3M instances to achieve suitable turnaround time and QoR. The design partitioning overhead in floorplanning and constraint management is cumbersome. We need to be able to support ***block sizes of 20M-30M Instances*** *to keep pace with the technology."*

https://semiengineering.com/can-ai-alter-the-burgeoning-design-cost-trend/

POSSIBLE DOMAINS IMPACTED BY AI



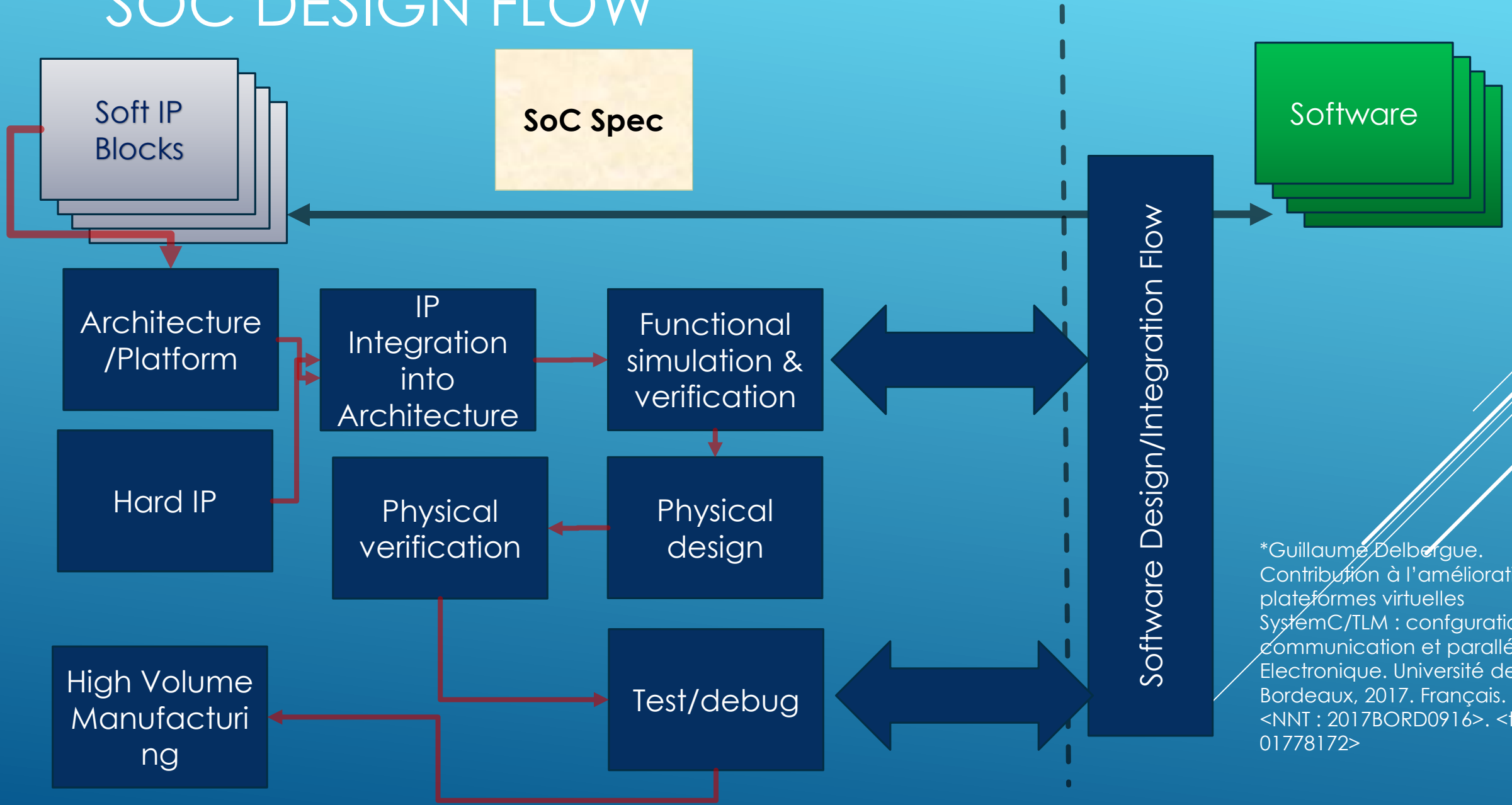
DESIGN/PROGRAM MANAGEMENT



DESIGN/PROGRAM MANAGEMENT EXAMPLES

Quality Control	• RTL turn-in controls for integration • Predict the probability that RTL turn-in is of good quality
Milestone Prediction	• Predict RTL bug rate trend for tape-in prediction • Huge struggle for data • Predict DRC/APR closure time
Infrastructure/Resource Management	• Assign/manage resources based on schedule risks or other costs • https://vlsicad.ucsd.edu/Publications/Journals/j121.pdf

SOC DESIGN FLOW*

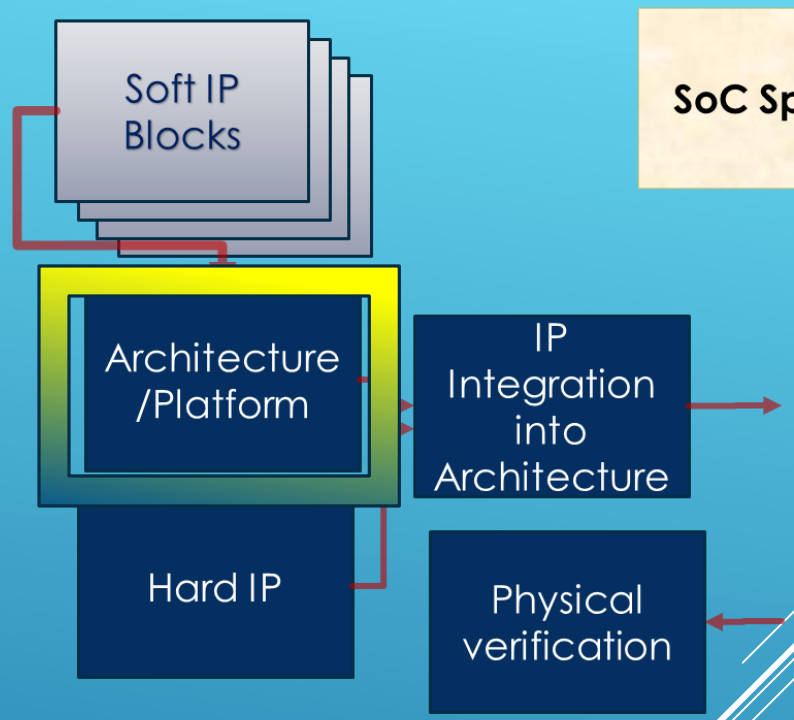


*Guillaume Delbergue. Contribution à l'amélioration des plateformes virtuelles SystemC/TLM : confguration, communication et parallélisme. Electronique. Université de Bordeaux, 2017. Français. <NNT : 2017BORD0916>. <tel-01778172>

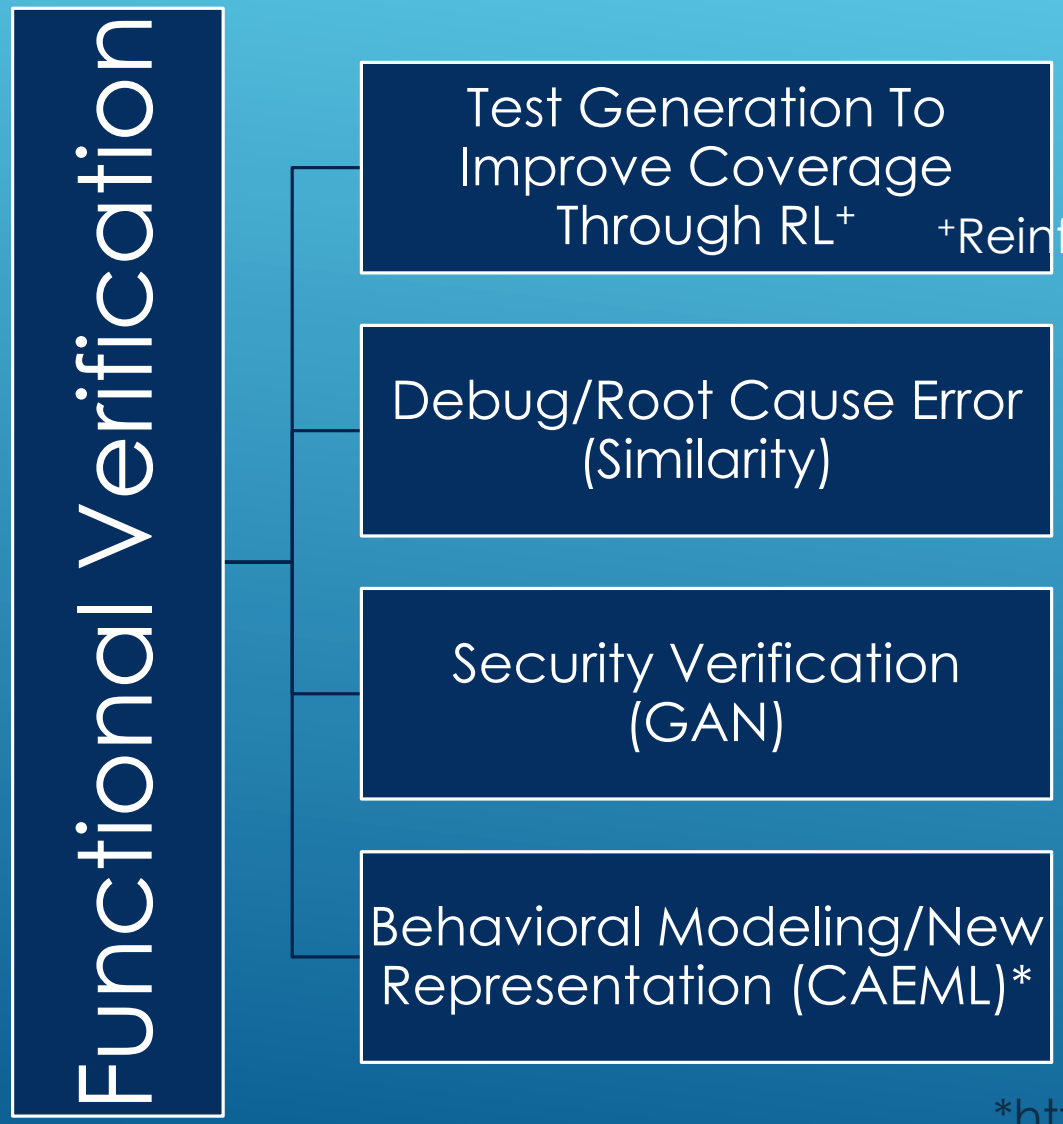
ARCHIECTURE/PLATFORM: AI EXAMPLES

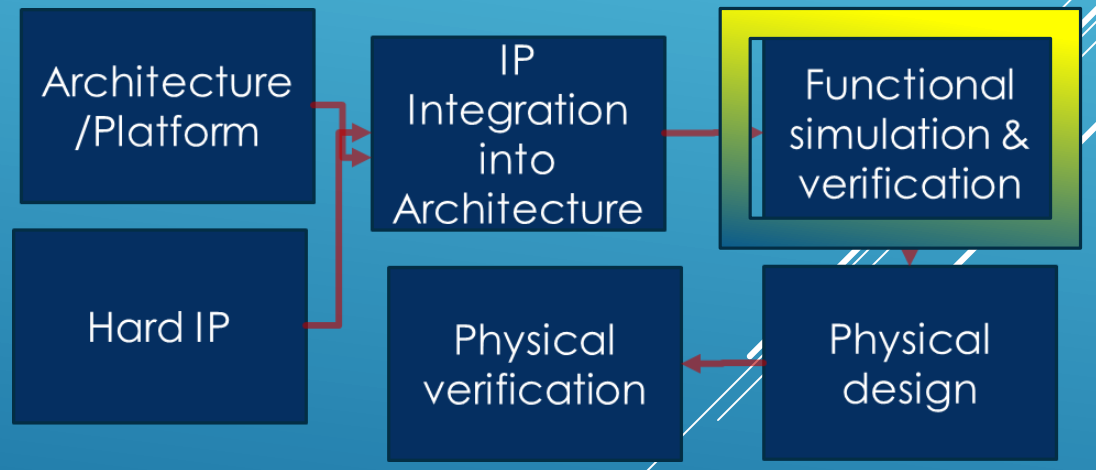
Architecture/Platform

- Accurate Component Models for Performance Modeling
- Power Modeling/ISA Sequence Power Model
- Cost Modeling



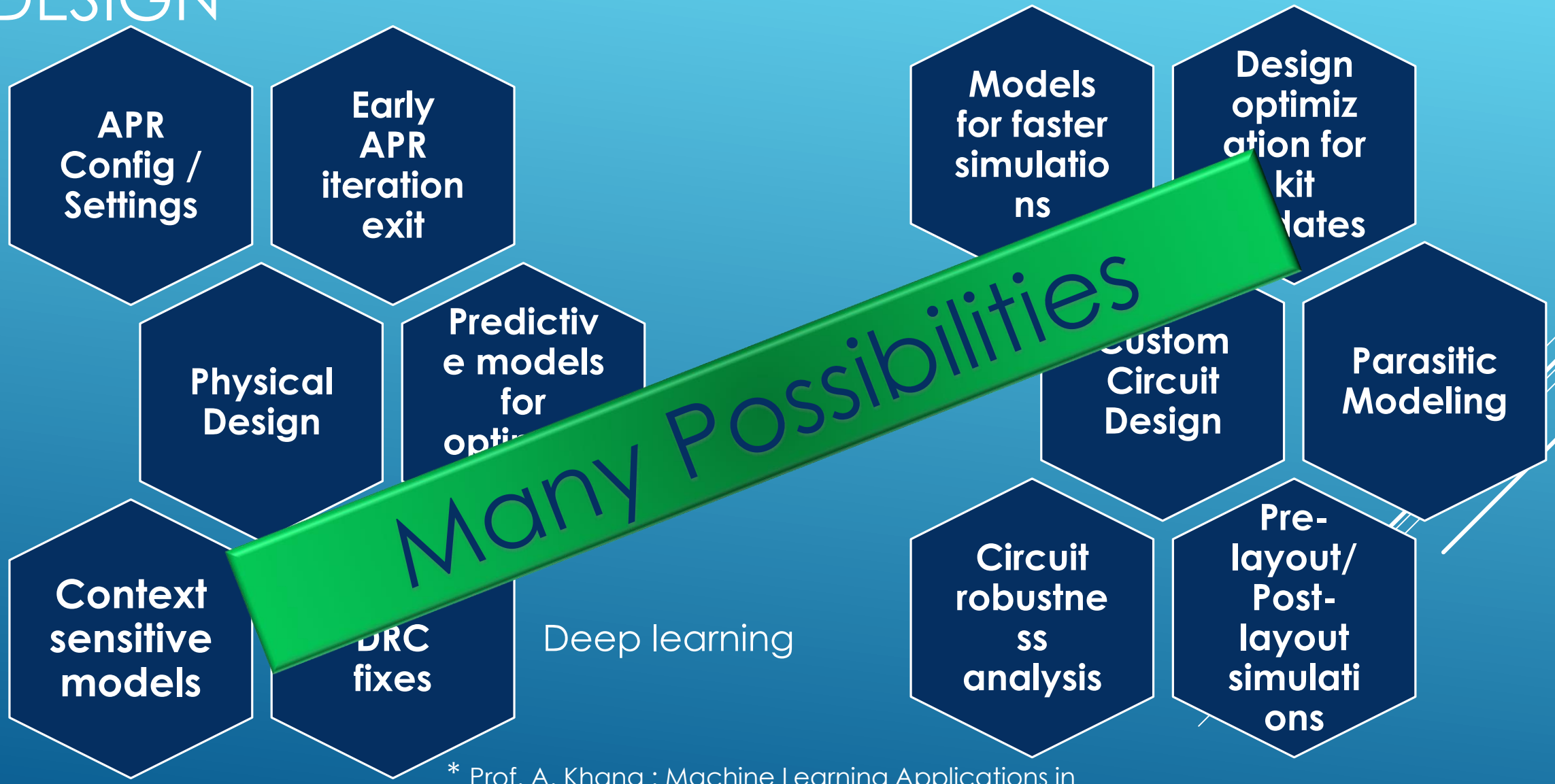
FUNCTIONAL VERIFICATION: AI EXAMPLES





*https://publish.illinois.edu/advancedelectronics/

CORNUCOPIA OF AI APPLICATIONS IN DESIGN

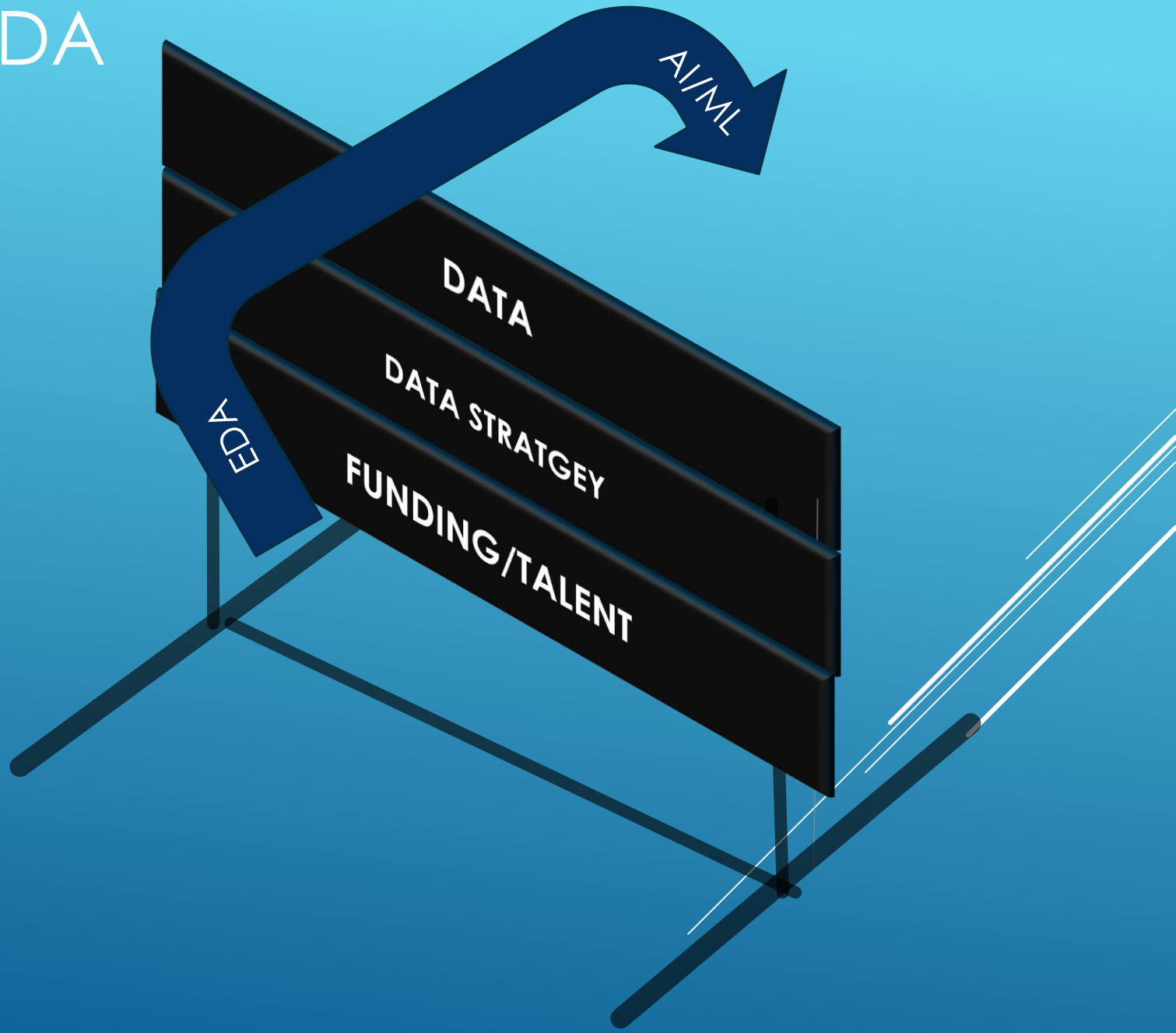


* Prof. A. Khang : Machine Learning Applications in Physical Design: Recent Results and Directions

AI/ML HURDLES IN EDA

Secondary Issues

- AI/ML interpretability problem (XAI)[+]/ transparency
- Unknown errors
  - Difficult to detect errors across the state space
- Bias in the models
- Problem definition



[+] Explainable AI

DATA TYPE FOR AI/ML

With-in design data

- Training based on in-context data
  - Surrogate models for circuits
  - Debug/root cause analysis
  - Power/Performance models for various components

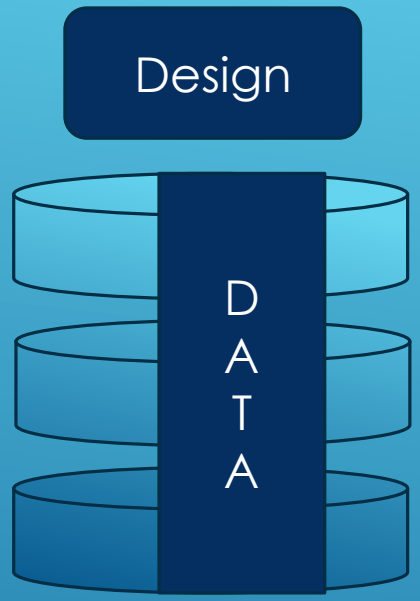
Across design data

- Training based on data across designs
  - Early exit in APR
  - Predictive models for optimization across APR stages
  - Milestone predictions
  - Parasitic estimation

DATA HURDLE

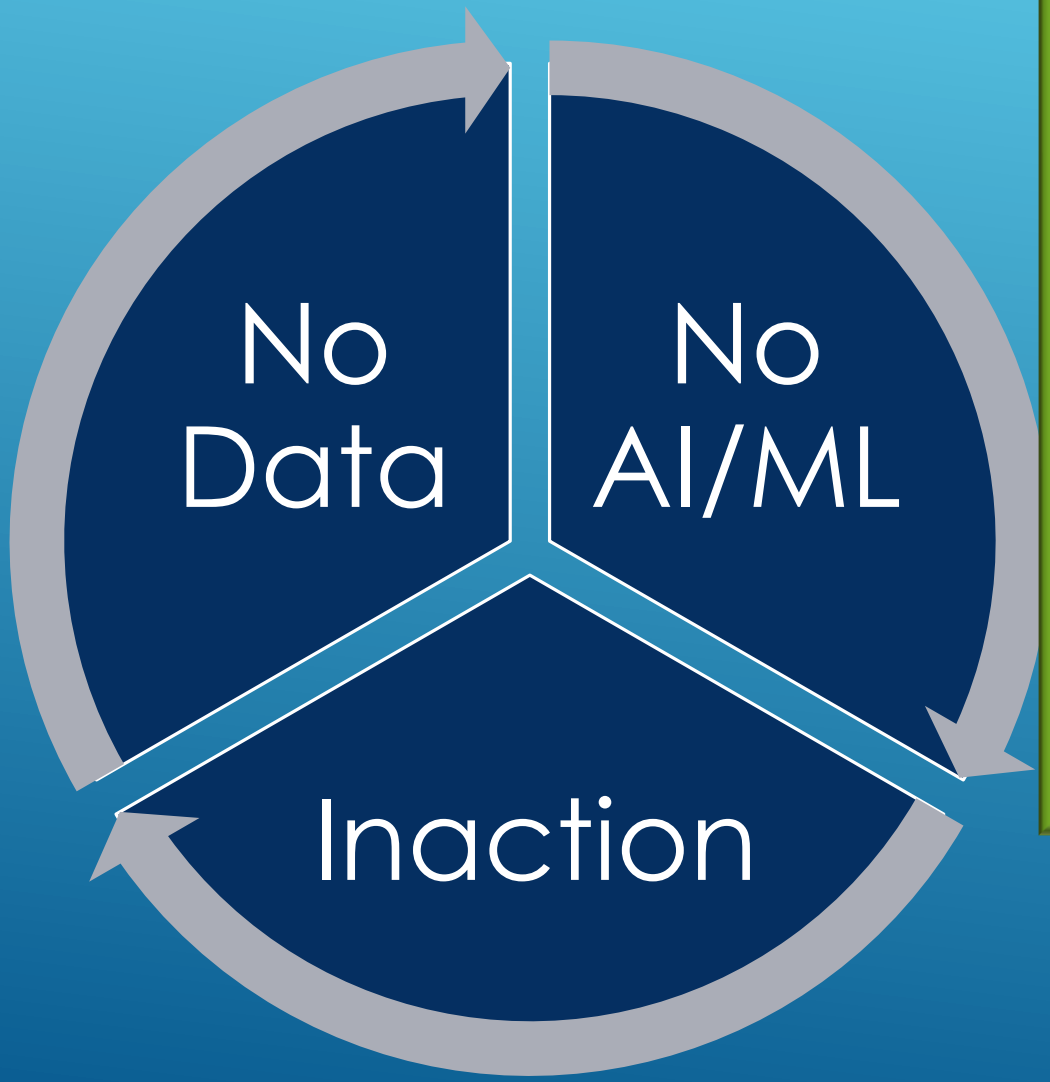
Lack of Data

EDA TOOL VENDORS



- **With-in design data manageable**
- **Across design data no clear strategy**
- **AI/ML revolution in segments driven by cloud**
  - **May be in EDA-in-cloud would help**

DATA STRATGEY



- Lack of data strategy
  - Don't know what data to store / needed
- Data quality
- Lack of easy data storage APIs in tools
  - No standards
- Do not have abstract representation of data
  - E.g Word2Vec/embeddings for NLP
- Data augmentation strategy
  - Different for different applications

AI/ML EFFORTS ROI

- Lack of clear value proposition
- Good models difficult with limited POC hence no investment
- Challenge to solve difficult problems
- Mostly reliant on EDA vendors for ML
- Lack of transparency on model accuracy

AI/ML TALENT/FUNDING IN EDA

- *Lack of research/talent coming into EDA*
  - *CAEML good start*
  - *Still hampered by data*
- *Challenge to acquire talent from research to development*

CONCLUSION

- Vendor tools enabling AI/ML solutions primarily within an execution/design cycle
- Across design learning is difficult
  - Design teams need to own it or may be some collaboration across academia/industry
  - Figure out what, why and how to centrally archive data
    - Waiting for problem definition is too late
- Vendors need to enable easier/standard data access capabilities
  - Parsing log files is not easy and time consuming
  - Enables design organizations to pursue ML along with vendors
- EDA in cloud may enable larger breakthroughs if data sharing strategy is resolved