Design For Thermal Reliability in 7nm

Jae-Gyung Ahn
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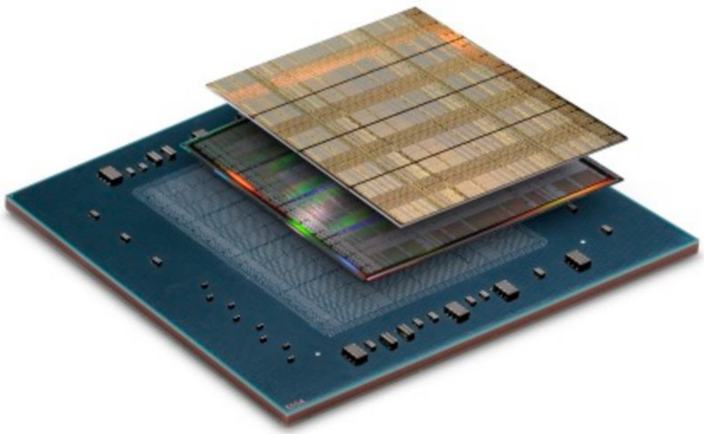
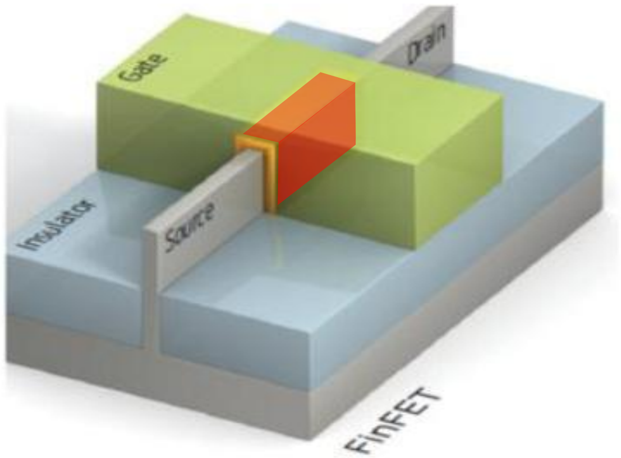
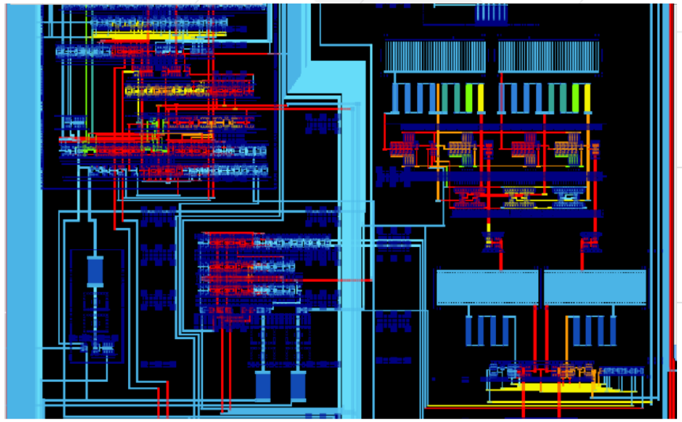
Introduction

- Reliability of SoC Product: *Weakest Link* or *Series System Model*
  - Mix of Digital, Analog, & Memory
  - Multiple Mechanisms(TDDB, EM, BTI, HCI, etc.) & Components (FEOL, BEOL, & PKG)

- High Power in Data Center & High Temp in Automotive
- Thermal Issues: Local Heating & Temperature Gradient







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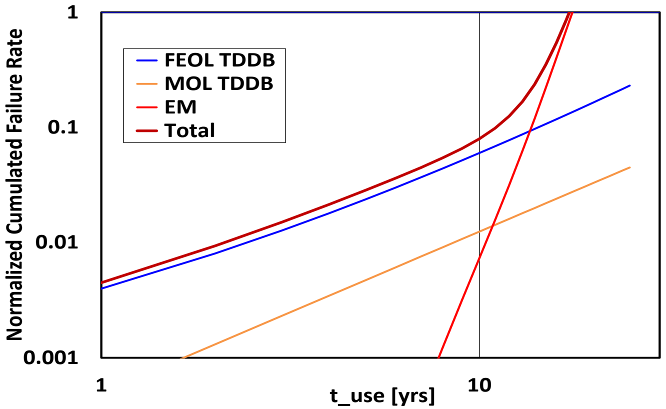
Product Reliability

- Lifetime is defined as the time @CFR (Cumulative Failure Rate) = F_0
  - F_0 = 0.1% ~ 1ppm
  - CFR vs. time relation is required to get lifetime
- Weakest link ➔ $F_{chip} = 1 - S_{chip} = 1 - \Pi\, S_i = 1 - \Pi\,(1\text{-}F_i) \sim \Sigma\, F_i$ if $F_i << 1$
  - Each fail event is independent
  - Failure of any device or metal is considered as failure of chip
  - Pessimistic approach with redundant elements
- Target failure rate of each block is assigned: “Reliability Budget”
  - Make sure failure rate of whole product meets the spec
  - Gives flexibility to Design since budget is transferrable



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Budget-Based Reliability Management

> Budget-Based vs. Rule-Based Reliability Check

> Rule violation (Vmax, Imax, ΔTmax) can be allowed as long as total FR is less than target

	Budget Based	Rule Based
Goals	Total $A_{TDDB,eff}$ <= Area_max?	Vg <= Vmax?
	Total EM FR <= EM FR Budget?	Iavg <= Imax?
	Meet Performance and Functionality @EOL	ΔBTI+HCI <= Criteria?
ΔT Criteria	Can be relaxed	5°C ~ 10°C
Benefit	Guarantee Product Reliability	
	Quantify Product Failure Rate	

> Ref [7] J. Ahn, et al. 2015 IRPS

Local Heating Effects

> Self-Heating Effect (SHE) in FinFET ➔ $T_{channel}$ higher than T_{junc}

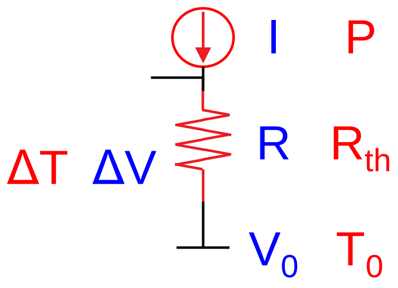
$$\Delta T_{channel} \sim R_{TH} \times Power_{channel}$$

> Joule-Heating Effect (JHE) from high current and resistance: ➔ RMS rule for EM

$$\Delta T_{metal} \sim i^2 R$$

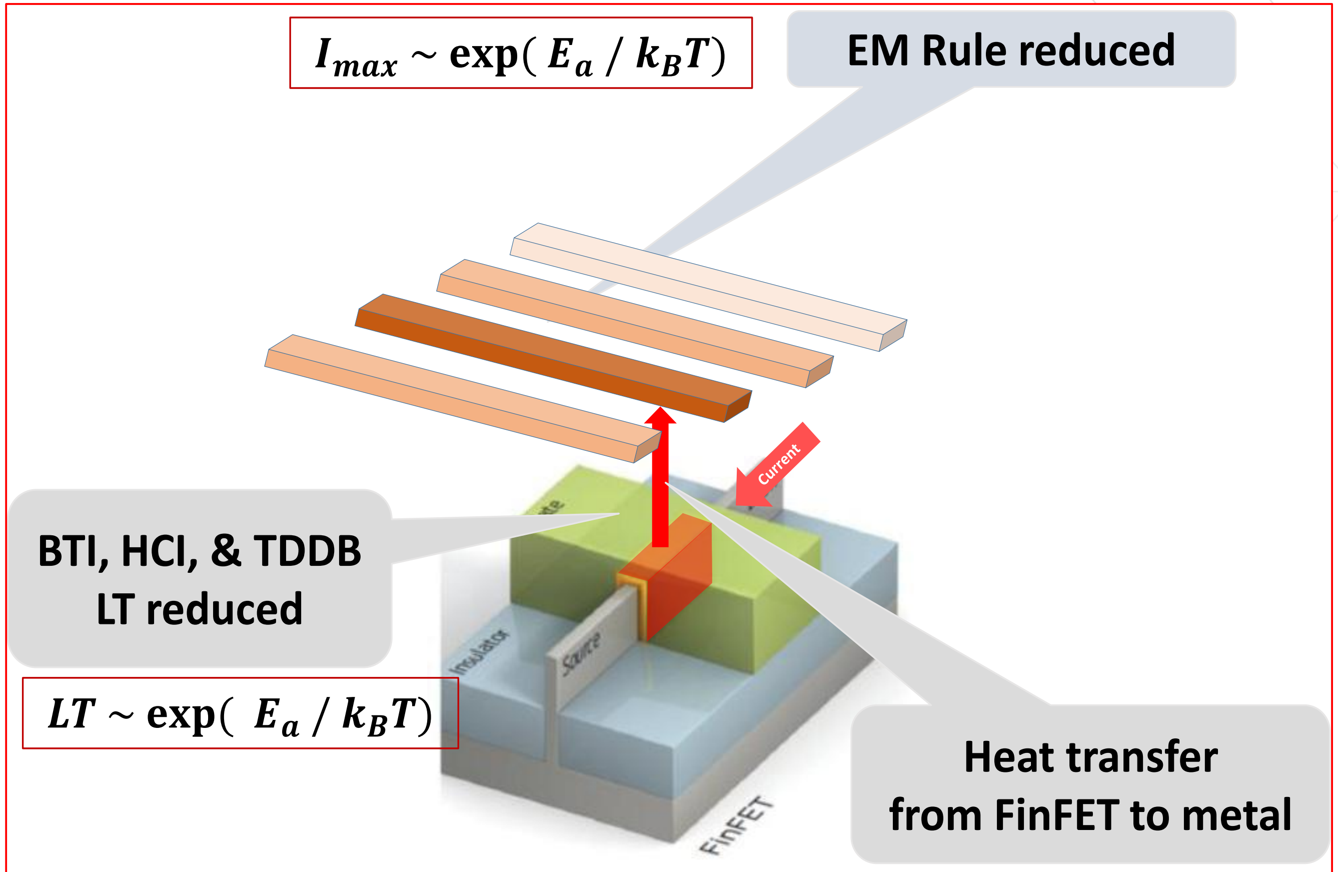
> "Local": $\Delta T = T(local) - Tjunc$:

Does not mean Tjunc is increased



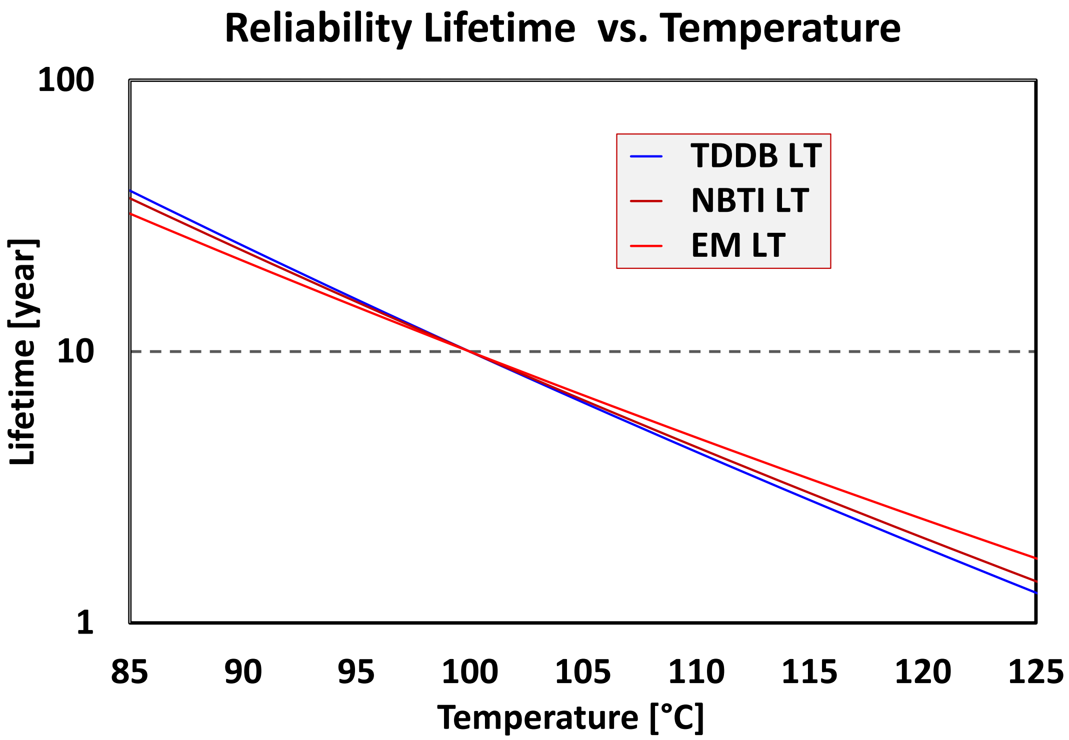
$\Delta V = R \times I$

$\Delta T = Rth \times Power$



Impact of Thermal on Reliability

- Reliability lifetimes are strong functions of temperature
- LT ~ 0.7x with ΔT = 5°C or LT ~ 0.5x with ΔT = 10°C
- Rule of maximum ΔT is hard to meet in advanced technology
- Impact to the product reliability (Impact to Reliability Budget) ?



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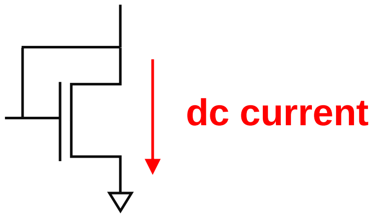
Aging Simulation with SHE

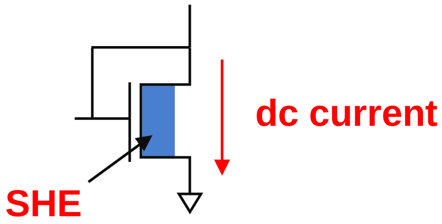
- ΔT_{ch} from SHE enhances Δ of Aging Effect (BTI & HCI)
- Δ (Device degradation) should degrade performance @EOL
- Pass criteria is not amount of Δ, but perf@EOL

Aging Simul w/o SHE



$\Delta Idsat_{HCI+BTI}$ = 8.2%

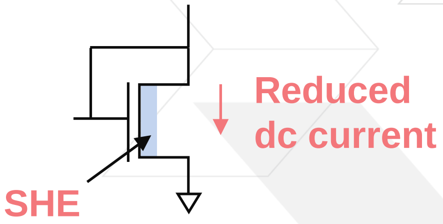
Aging Simul w/ SHE



SHE_DTEMP = 42°C
$\Delta Idsat_{HCI+BTI}$ = 16%

Δvoffset = 22mV

Aging Simul after Circuit modified



SHE_DTEMP = 9.1°C
ΔIdsat = 3.7%

Δvoffset = 3.3mV

Impact of SHE to TDDB

> TDDB impact by checking $A_{TDDB,eff}$ (Effective TDDB Area)

Time-varying bias ➔ one effective value of V_{eff}

High V_{eff} ➔ Shorter LT or higher risk ➔ expressed by Larger $A_{TDDB,eff}$

Example when V_{g0} spec = 0.9V

- **V_{eff} = 0.93V ➔ $A_{eff} = A_{phy}$ x 12 :**
  The device has the same TDDB risk as 12 x the device w/ V_{gs}=0.90V

- **V_{eff} = 0.93V & ΔT = 20C ➔ $A_{eff} = A_{phy}$ x 154 :**
  The device has the same TDDB risk as 154 x the device w/ V_{gs}=0.90V and ΔT = 0C

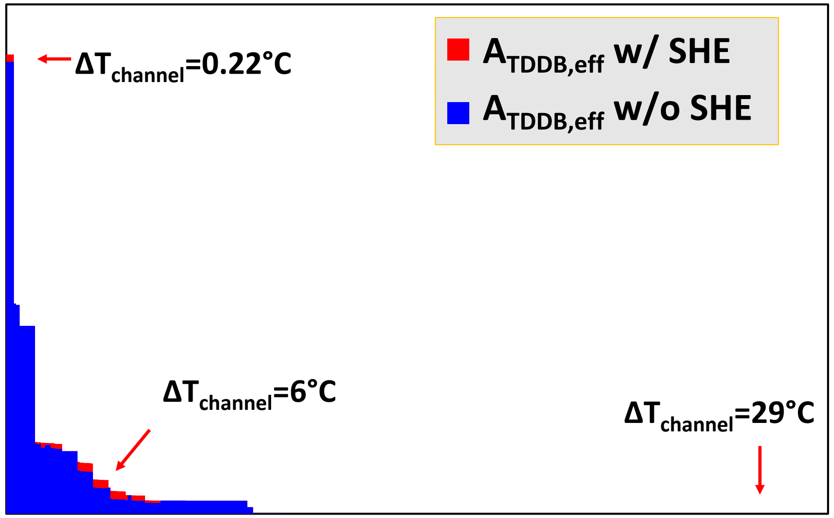
ΔT_{ch} from SHE ➔ Shorter LT ➔ Lower V_{g0} (Reference TDDB Vmax) ➔ Increase of $A_{TDDB,eff}$

Impact of SHE to TDDB is quantified by Aging simulation flow

Impact of SHE to TDDB

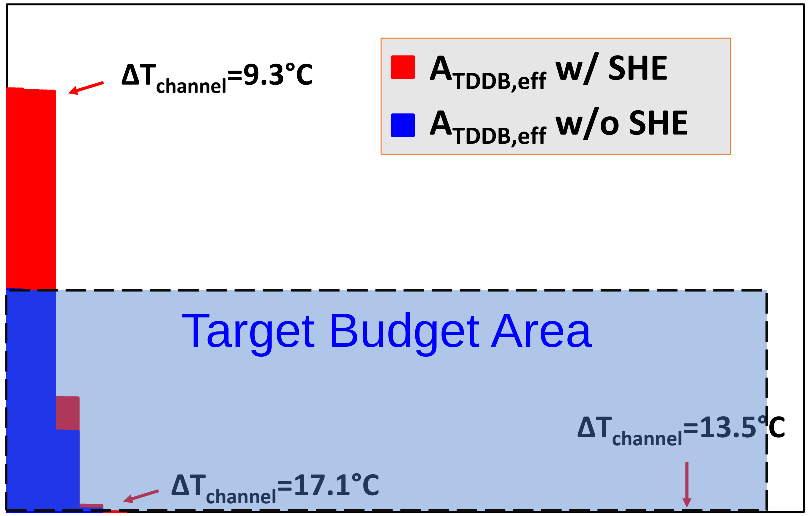
- Highest ΔT_{ch} may not be coincident with highest V_{eff}
  - Case 1: No impact to $A_{TDDB,eff}$ even with ΔT_{ch} = 29°C
  - Case 2: $A_{TDDB,eff}$ doubled due to ΔT_{ch} = 9.3°C
    - Acceptable if $A_{TDDB,eff}$ is within the ***budget***

Distribution of $A_{TDDB,eff}$ [arb. unit]



Case 1

Distribution of $A_{TDDB,eff}$ [arb. unit]

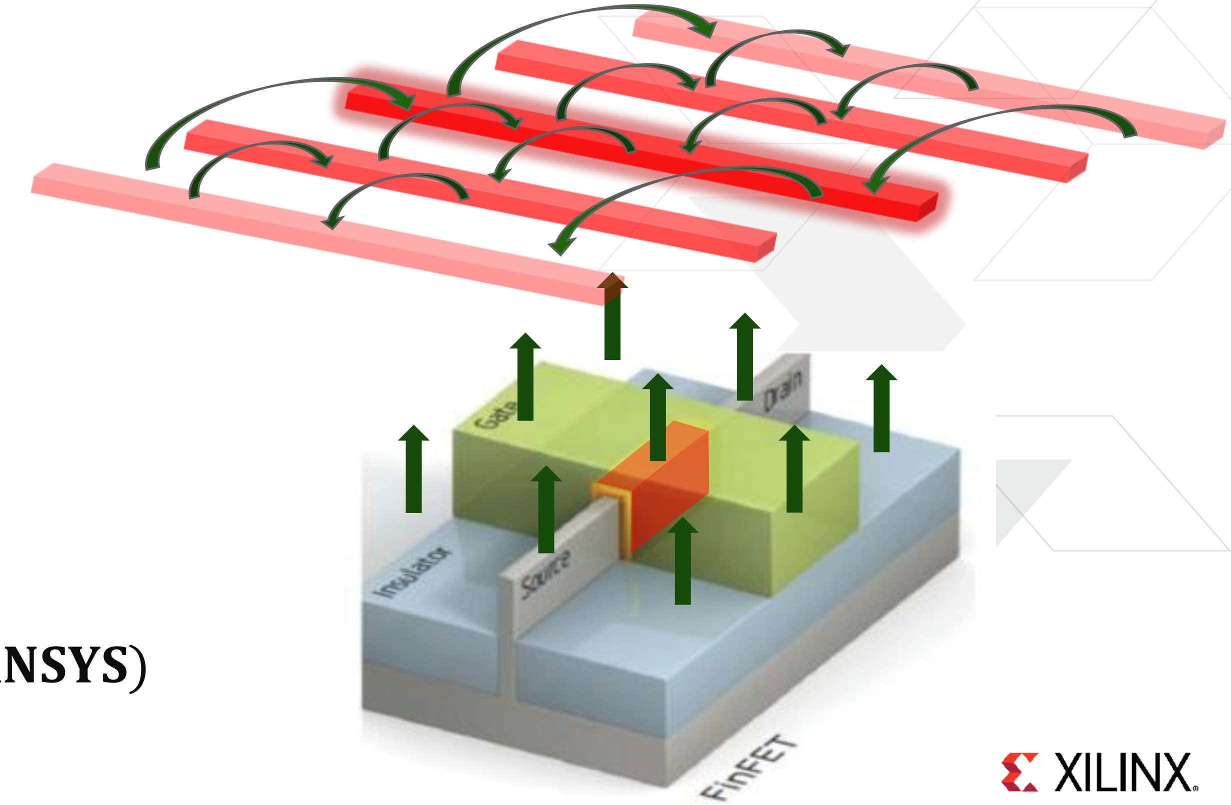


Case 2

Thermal-Aware EM Flow

- Estimate impact of local heating on EM of wires and vias
- FinFET Self-Heating Effect (SHE) & Wire Joule-Heating Effect (JHE)
- *Superposition* of Thermal Coupling from all the neighboring wire aggressors

$$\Delta T_i = \sum c_{ij} \Delta T_j$$



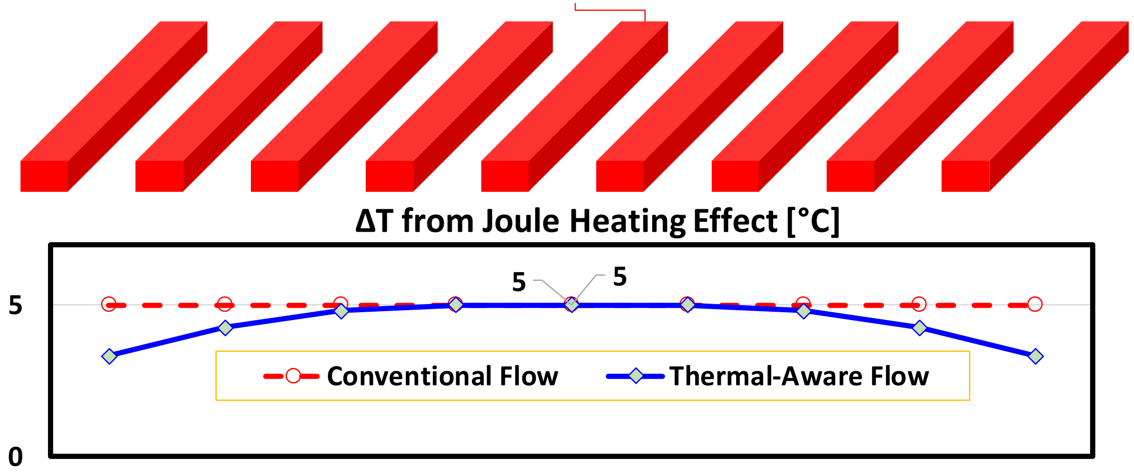
- Coupling coeff. is a function of distance
- Both in horizontal and vertical direction

[4] Stephen H. and Norman C. ECTC 2015 (ANSYS)

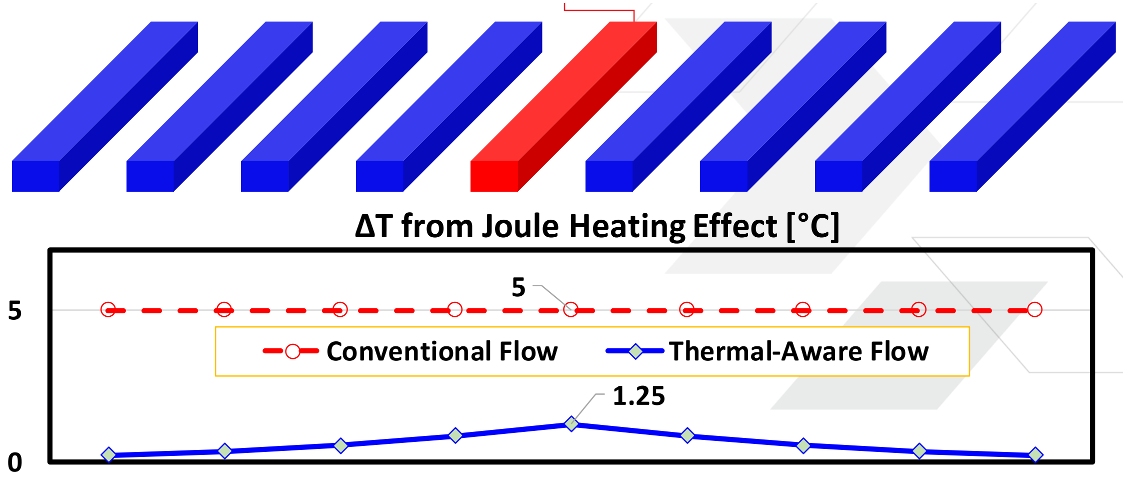
Thermal-Aware EM Flow

- Superposition may result in very high ΔT when there are many aggressors
- Applied Clamping value for ΔT
  - Use the Maximum possible ΔT value (based on rms_ratio values)
  - Within influence range
- Resulted ΔT value for two example cases
  - Isolated heat source has lower ΔT than dense ➔ Additional benefit to Design

rms_ratio = 100% for 9 dense lines



rms_ratio = 100% for center line only



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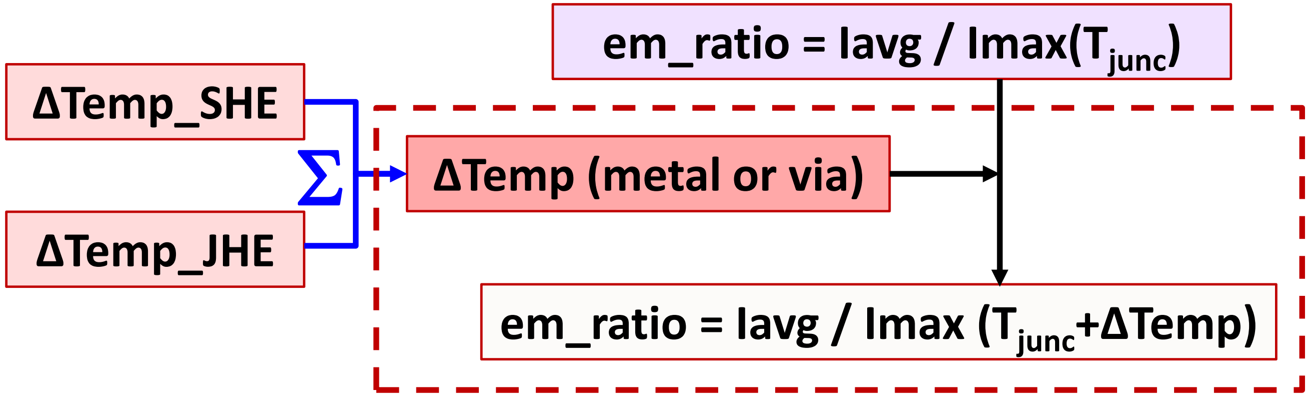
Flow for EM with Thermal

- $\Delta T_{metal\ or\ via} = \Delta T\_SHE + \Delta T\_JHE$
- Imax reduced by $\Delta T_{metal\ or\ via}$ ➔ em_ratio increased ➔ EM Failure Rate increased
- ΔT assumed to be Additive



Example

em_ratio = 80%

Iavg = 0.8mA

$Imax(T_{junc})$ = 1mA

ΔTemp = 13C

ΔTemp_SHE = 8C

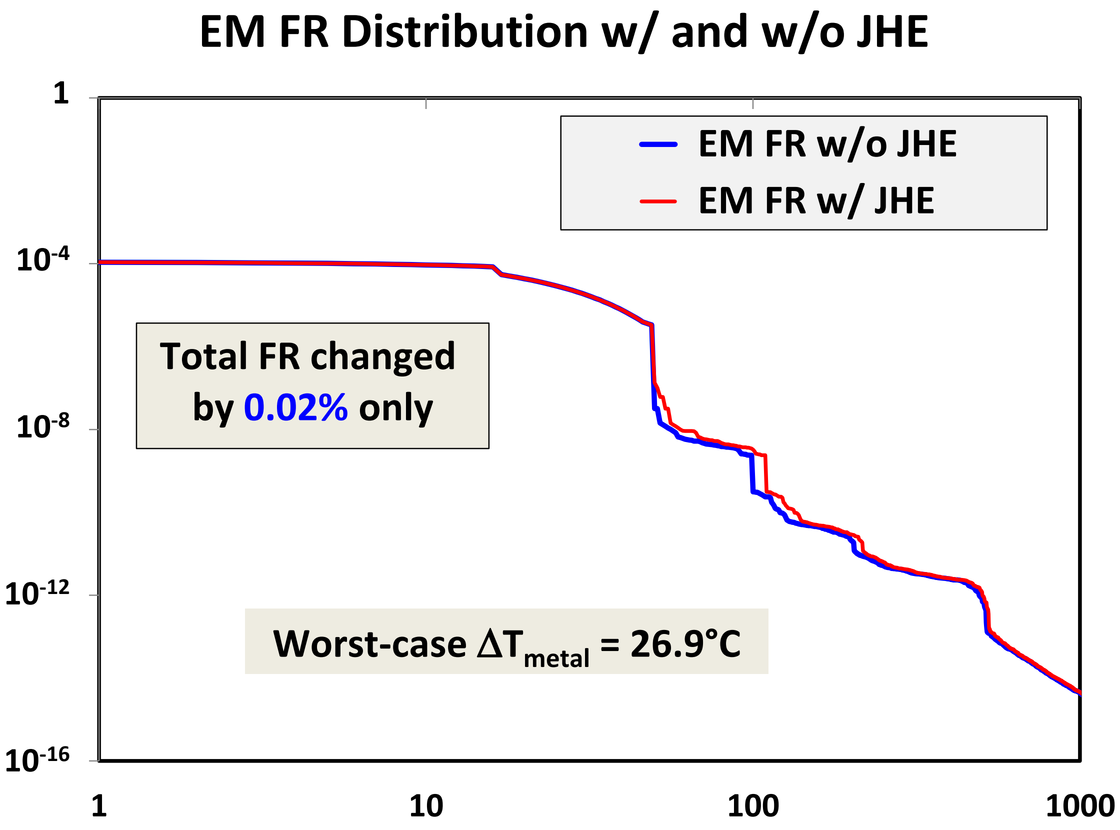
ΔTemp_JHE = 5C

$Imax(T_{junc} + \Delta Temp)$ = 0.39mA

em_ratio w/ Thermal = 205%

Case1 of JHE to EM

- ΔT_{metal} = 26.9°C / Total EM FR increased by ~0.02% ➔ No risk
  - Highest ΔT_{metal} occurs at metals of low em_ratio
  - Modified em_ratio is still at lower level



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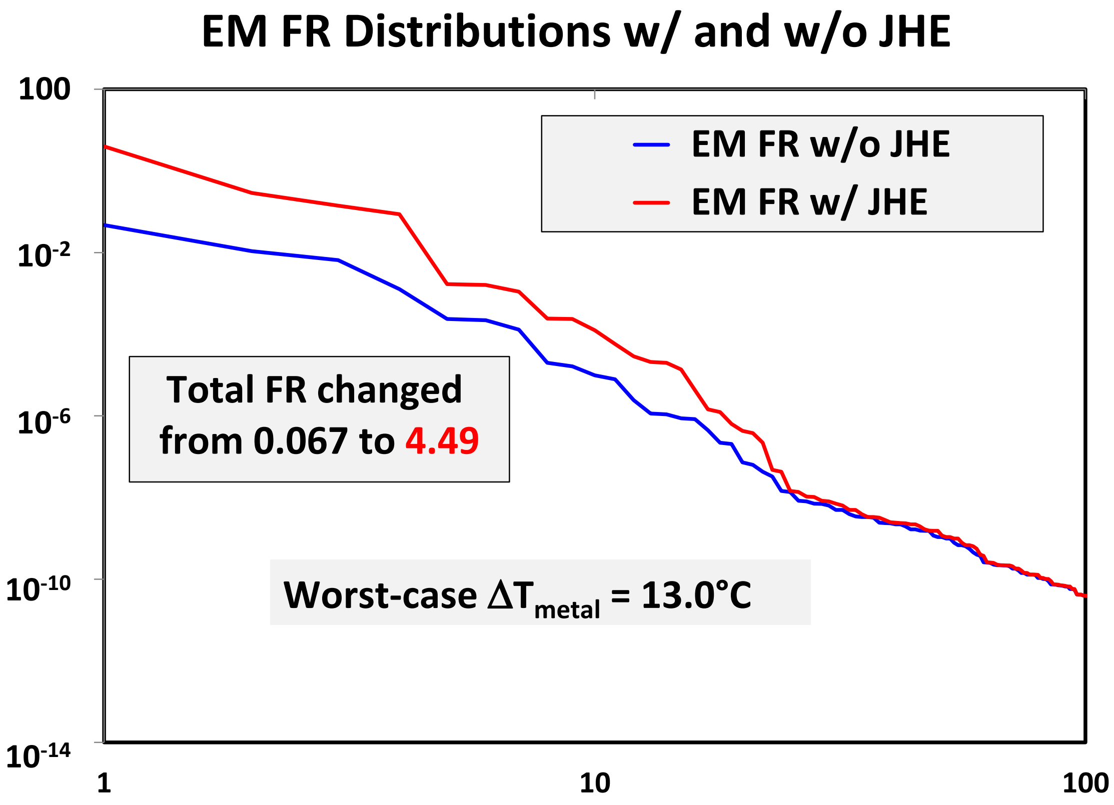
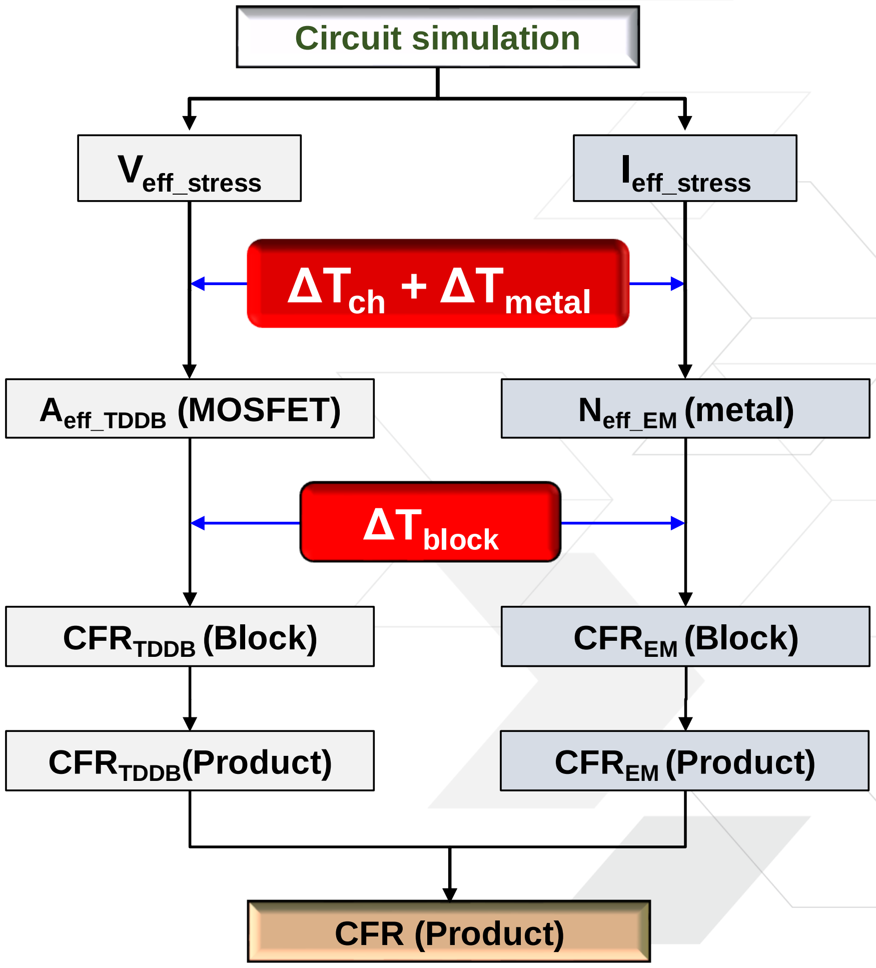
Case2 of JHE to EM

- ΔT_{metal} = 13.0°C / Total EM FR increased to 67x
  - Fail to meet EM FR budget ➔ Design Change Required



Design Flow for Product CFR (Cumulative Failure Rate)

- Transient simulation
  - V_{eff} and I_{eff}
  - Self-Heating Effect + Joule-Heating Effect
  - A_{eff} and N_{eff} --- Proportional to CFR
- A_{eff} and N_{eff} vs. REL Budget
- Use Cond: Vcc & Temp profile
  - ΔT_{block} ➔ Lifetime modulated
  - CFR_{TDDB} and CFR_{EM} vs. time
  - CFR(Product) vs. time
    ➔ Gives *Lifetime of the Product*



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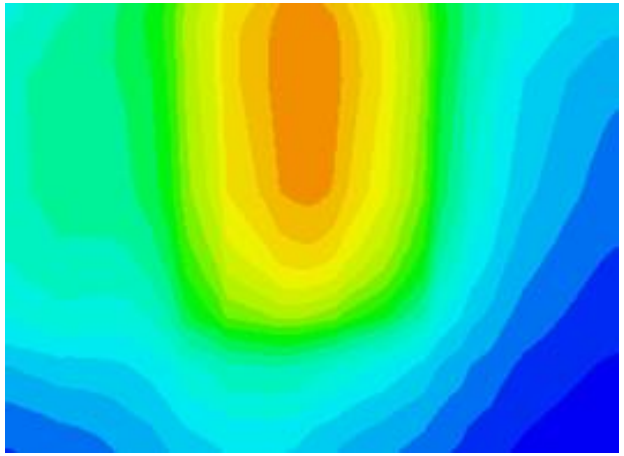
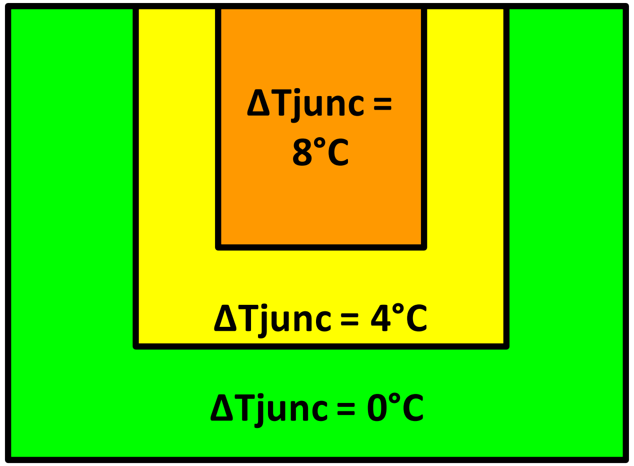
Temperature Gradient within Chip

- Thermal Simulation with Power Density to get Temperature Profile
- Higher T_{junc} in high power circuit block
- Simplified ΔT_{junc} to estimate CFR vs. time and get product Lifetime

$$F_{Chip} = \sum F_{TDDB,i}(\Delta T_{junc,i}) + \sum F_{EM,i}(\Delta T_{junc,i})$$

- High EM CFR w/ high ΔT_{junc} ➔ Threat to the product lifetime





Budget-based check enables us to increase FR of the block with high ΔT_{junc} only.

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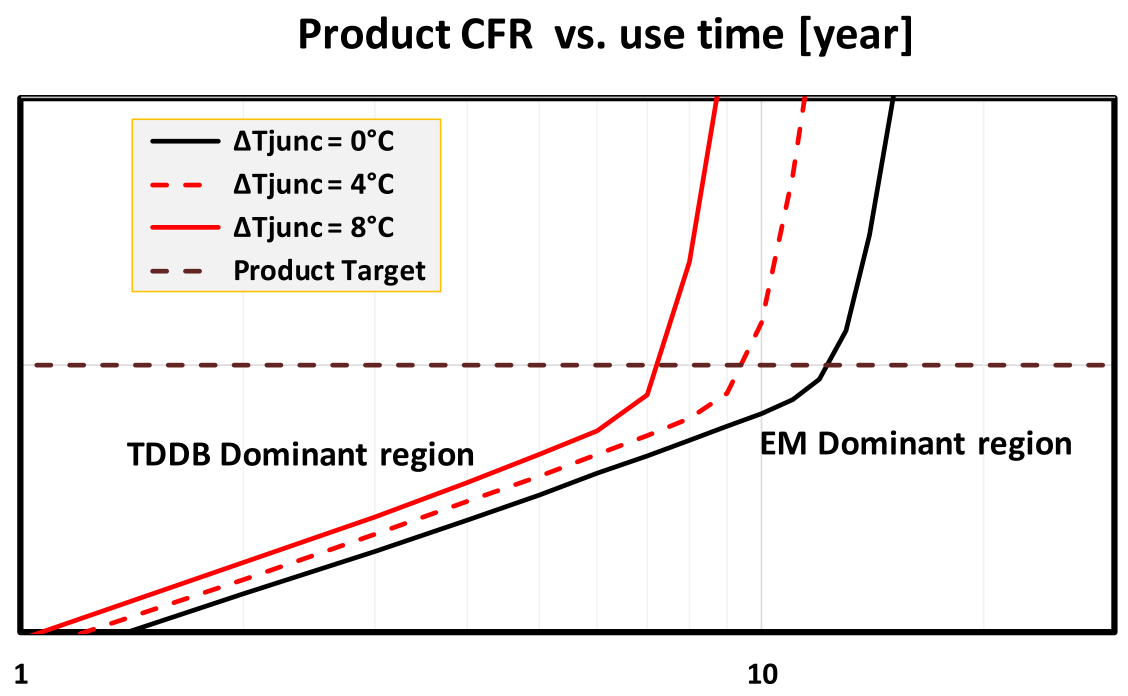
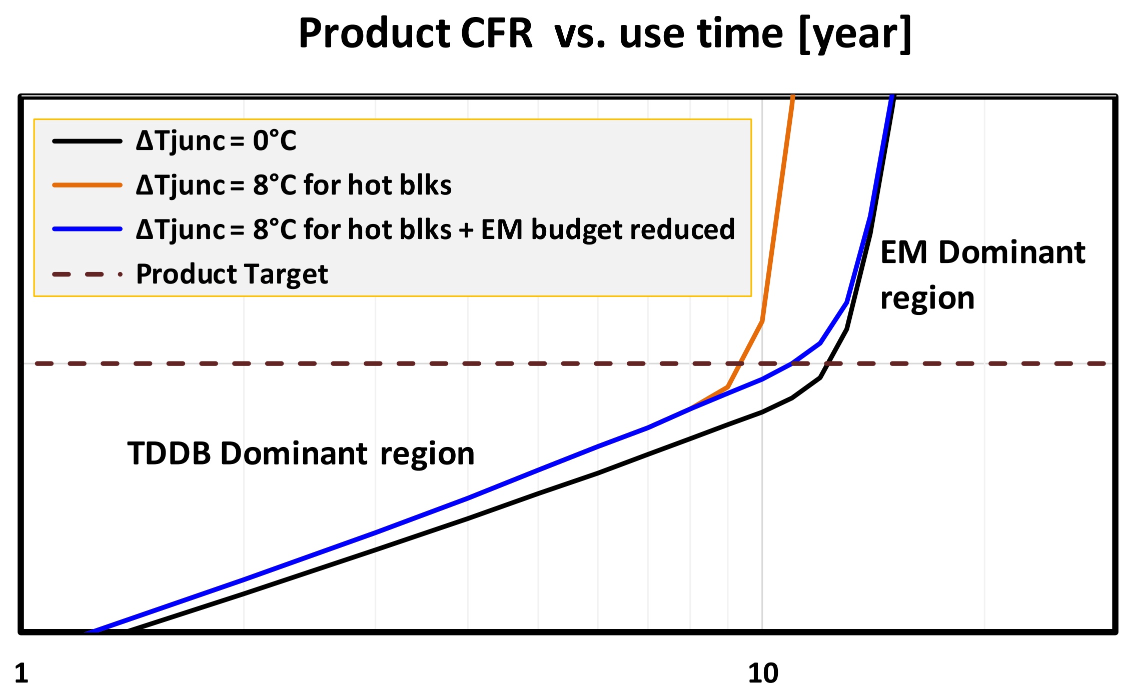
Temperature Gradient within Chip

- ΔT_{junc} = 8°C obtained for a high power block
- CFR increased from EM risk increase ➔ LT=12.4yr reduced to 7.3yr
- Budget-based check and special care for high ΔT_{junc} block ➔ Final LT becomes 12.0yr





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Conclusions

- > Design For Reliability in 7nm node explained

- > CAD Flow enhanced to consider thermal issues
  - >> FinFET Self-Heating Effect impact to BTI / HCI / TDDB / EM
  - >> Metal Joule Heating Effect impact to EM
  - >> Temperature Gradient impact to Product Failure Rate

- > Budget-Based Reliability Flow gives flexibility to handle thermal issues.

Adaptable.

Intelligent.

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