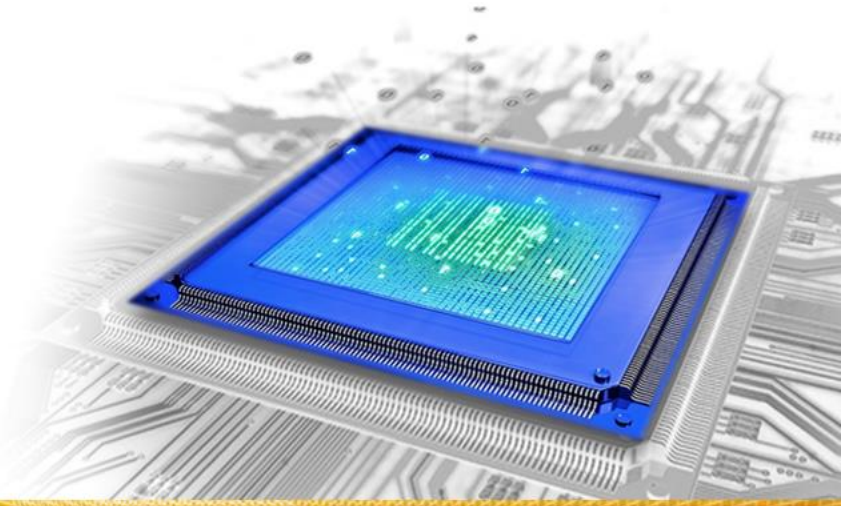
Achieving 5G/ADAS/AI/Photonics System Reliability for Advanced FinFET Designs

Norman Chang

Chief Technologist

Semiconductor BU, ANSYS Inc.

EDPS, Sept. 13, 2018



Semiconductor – Observed Trends and Challenge

Key Growth Drivers

Design Trends

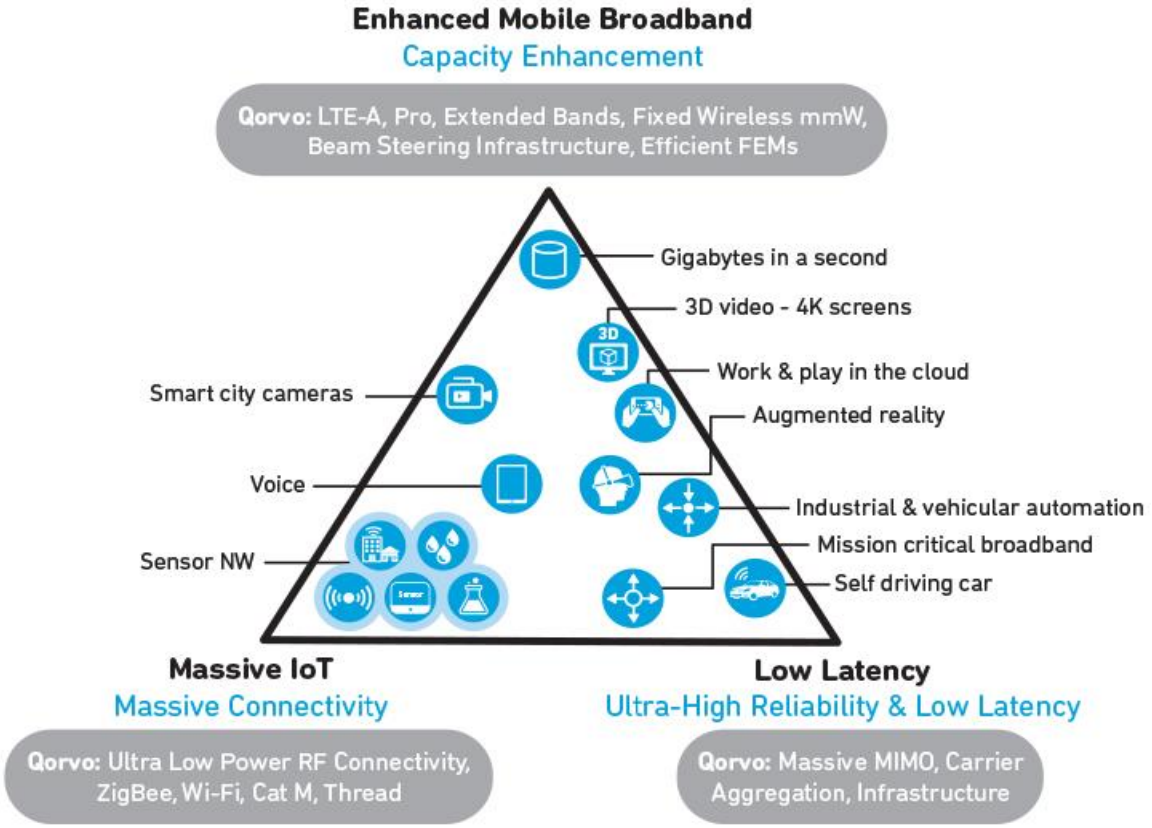
Integration
- Increasing IP content
- 2.5/3DIC

Technology Migration
- FinFET
- More than Moore

Power/Performance
- 100G SerDes , Wide IO
- 5G mmWave high-freq
- Fan-less cooling

- **5G/ADAS/AI are key growth drivers**
  - 7nm/5nm, advanced packaging, aggressive PPA
- **System reliability an emerging challenge**
  - >15 year lifetime, harsh environment, thermal/EM and ESD/EMI/EMS reliability, aging (NBTI/TDDB/HCI)
- **Post-silicon failures, related to voltage, timing, and process variability**
  - Sub 500mV, fast Monte Carlo, LDE, DvD impact on Timing

Emerging Needs of Chip-sets and Systems for 5G Market



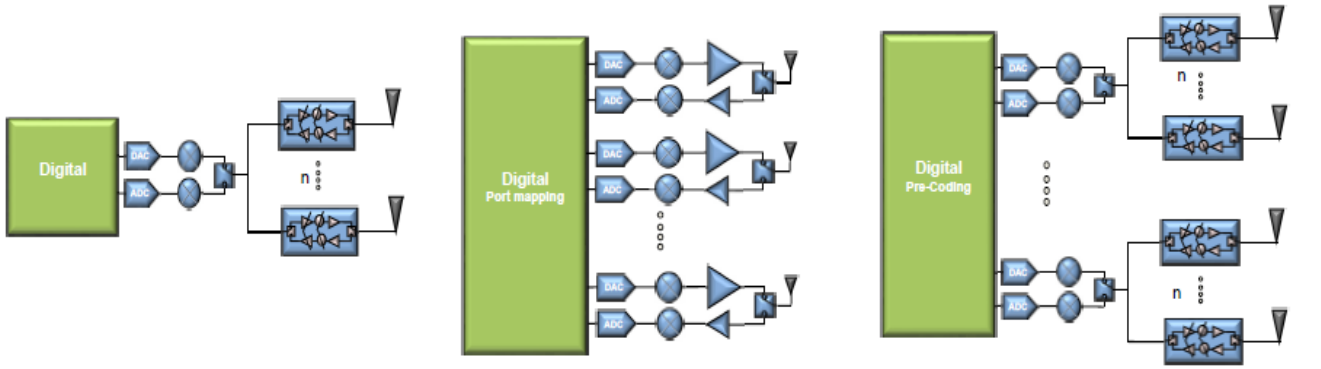
- Frequency increases tremendously covering sub-6G to 28G/39G with larger number of antenna arrays on massive MIMO and beam forming functionality on mobile chips
- Challenges in Power & Reliability Analysis including thermal/ESD/EMC
- Substrate noise from digital to analog or vice versa
- RFI noise analysis
- Accurate electrical models needed for on chip components such as spiral inductor and clock-tree/transmission lines

Source: Quorvo, Inc, from ITU-R IMT 2020 requirements

Increased complexity due to performance needs of 5G infrastructure

5G mmWave Massive MIMO with High-power Consumption

Beamforming Architectures



Analog Beamforming	Digital Beamforming	Hybrid Beamforming
Beam formed by weighting RF paths	Beam formed by weighting digital paths	Beamforming a combination of analog and digital
Low power/complexity	Highest power / complexity	Moderate power/complexity
Good for coverage	Highest capacity / flexibility	Compromise between analog and digital
Single beam – single data stream	Frequency selective beamforming	Best choice with existing technology

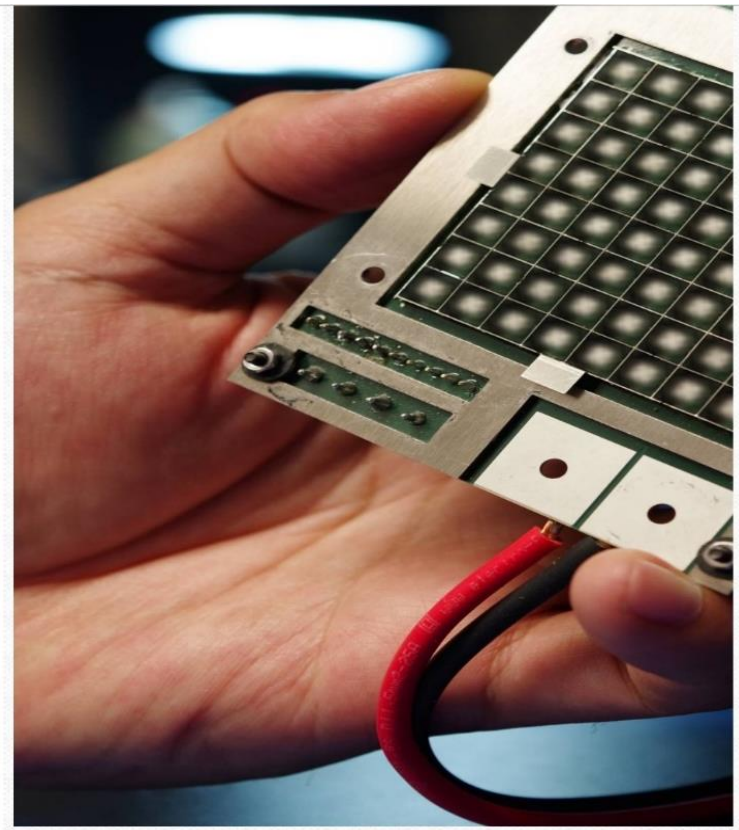


Figure 4 The original Movandi BeamX prototype is a 64-element phased array antenna based on bulk CMOS processes. Image courtesy of Movandi Corporation.

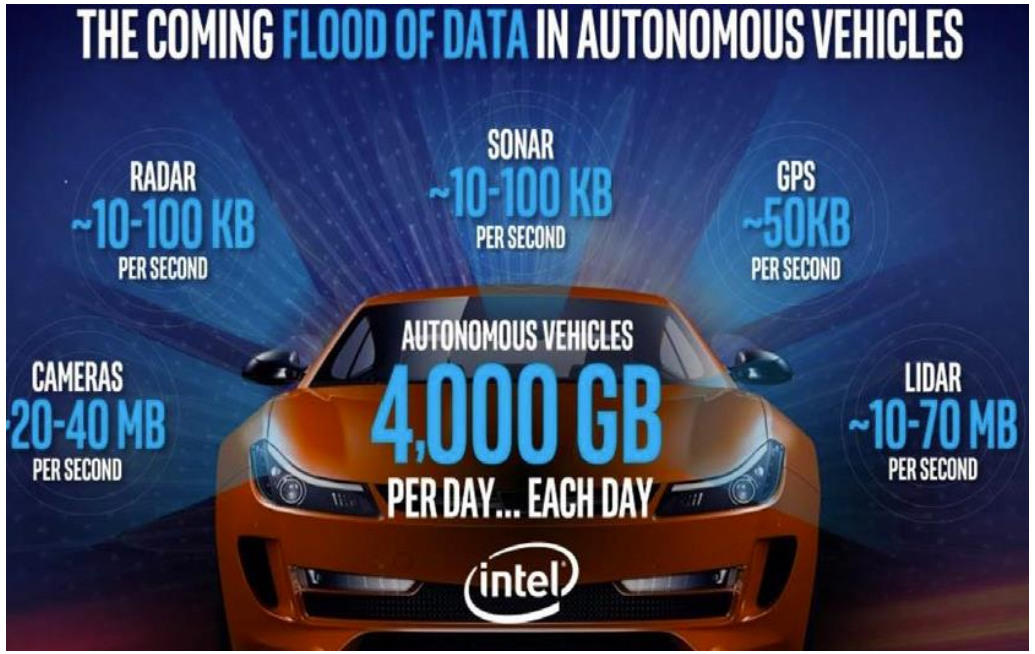
Courtesy: edn.com

Complex CMOS beamforming arrays consume > 160 watts of RF power

(Movandi, Blue Danue, etc.)

Courtesy: Analog Devices, ISSCC 2018

Computing and Reliability Requirements for Next Generation SoC



Source: Intel

Reliability Constraints

- ✓ **Wide range of operating conditions**
- ✓ **Reliability: up to 150°C ambient, 15+ years Life Cycle**
- ✓ **ADAS: Real time data processing w/ AI chips**

Sensor Fusion

- ✓ **16nm FinFET**
- ✓ **500 Watts**
- ✓ **Liquid Cooling**
- ✓ **CoWos with HBM2**

	DRIVE PX Pegasus
SoCs	2x Xavier
Discrete GPUs	2x Post-Volta
CPU Cores	16x NVIDIA Custom ARM
GPU Cores	2x Xavier Volta iGPU & 2x Post-Volta dGPUs
DL TOPS	320 TOPS

source: Nvidia

MCU/ECUs

16nm 800MHz NXP S32S microcontroller

"When we started the development of the S32S it was clear that just building another incremental microcontroller was not what customers needed to handle the safety and performance requirements of next-generation and autonomous vehicles"

- Ray Cornyn, VP & GM, Vehicle Dynamic products, NXP

New opportunities for highest growth potential

- Image sensors, High frequency RADARs, LiDARs with signal/image processing
- Graphics/AI cores for big-data analytics and Sensor Fusion
- End-to-end security

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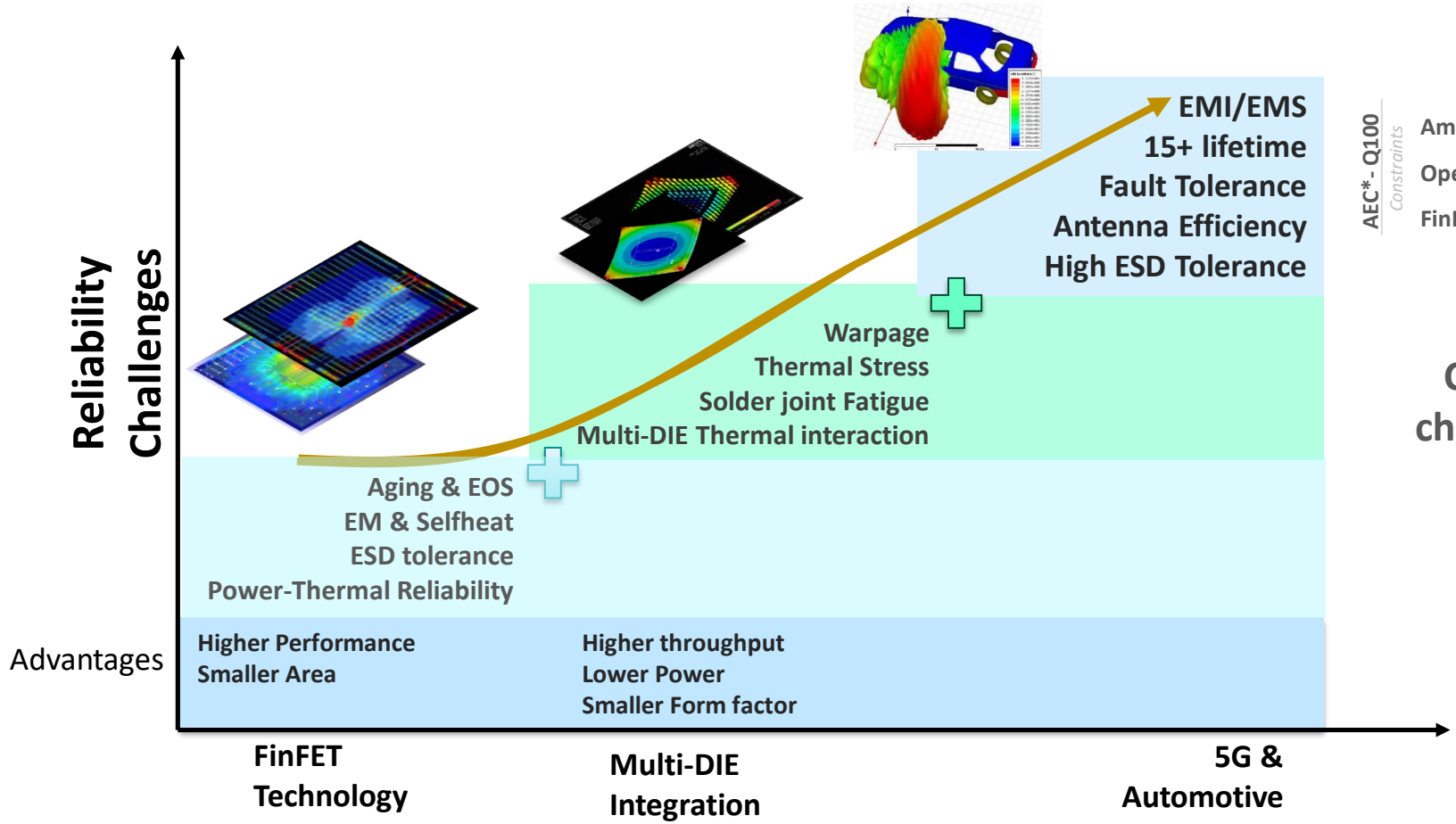
System Reliability for Automotive and 5G Chip-Package-System

Reliability Challenges



AEC*- Q100 Constraints

Ambient Temperature: Grade0 = -55°C / +150°C

Operating Lifetime: 15+ years

FinFET Technology! Heat Dissipation vs. MTTF

Compounding Reliability challenges in Electronics for Automotive & 5G

Multidomain and Multiphysics simulations are critical for Reliable 5G and Automotive Electronics

Si Photonics to Enable Next Generation Data Centers

- **Si Photonics leveraging CMOS process can be the next major growth segment**
  - **Automated large scale integration**
  - **High yield and reliability, and low cost**

- **Advantages for the next generation data center**
  - **Single-mode -> multi-kilometer links**
  - **Wavelength-division multiplexing (WDM) for high BW/fiber**
  - **High freq transceiver and receiver, and reliable waveguides**

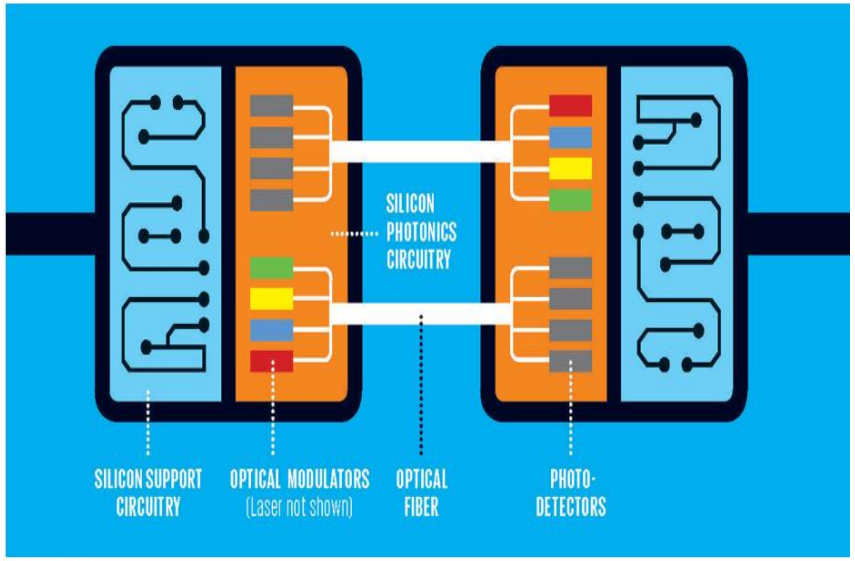


Photo: Luxtera

Luxtera Achieves Record Breaking Optical Performance with New TSV-Enabled Silicon Photonics Platform at TSMC

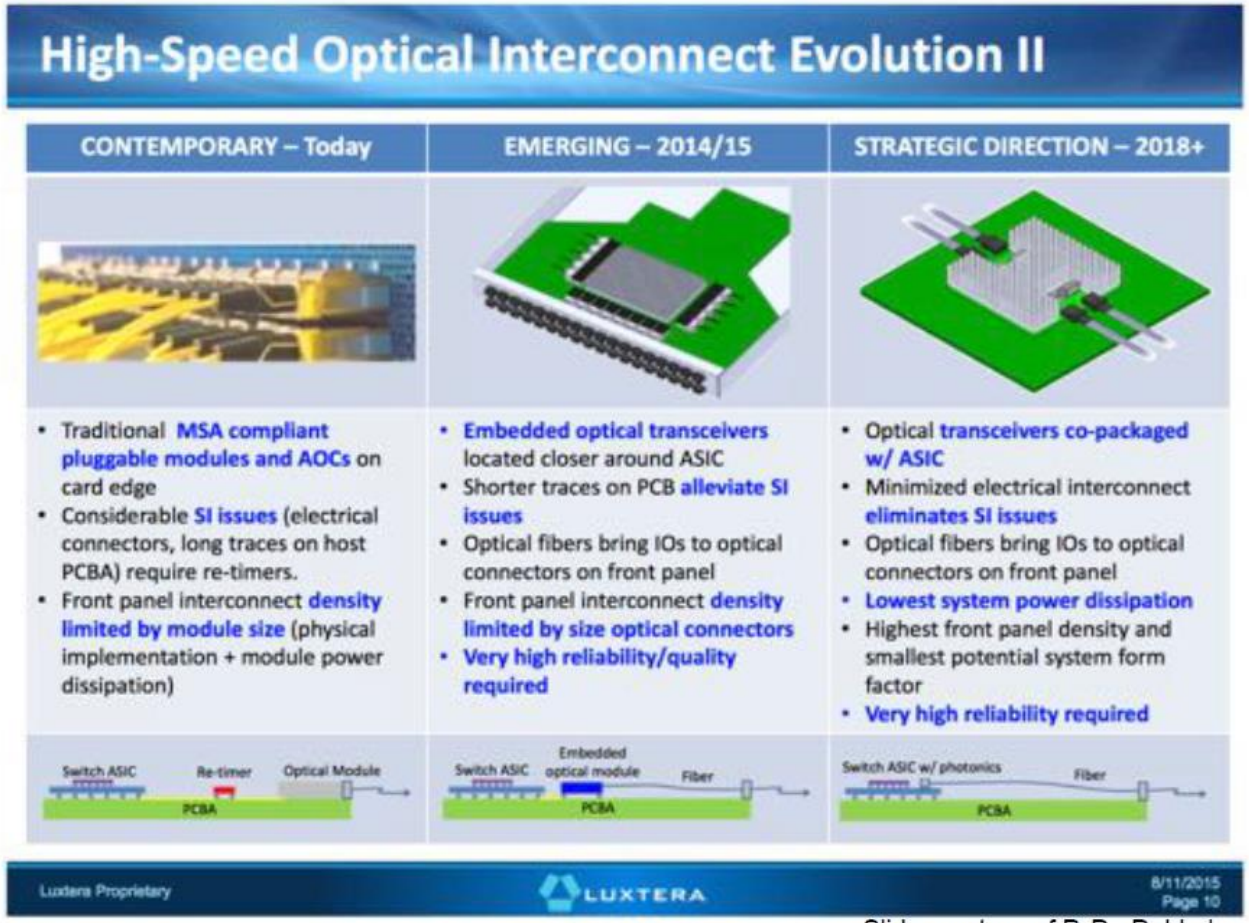
- On TSMC 300nm SOI wafer
- TIAs, CDRs, MZI modulator drivers and advanced DSPs that achieve world-class levels of performance and power efficiency. These advancements are crucial in providing customers with a differentiated portfolio of high performance optical transceiver products starting with next generation PAM4 100G/λ single wavelength and multi-wavelength transceivers which commence shipments in 2019

http://www.luxtera.com/2018/03/13/luxtera-achieves-record-breaking-optical-performance-with-new-tsv-enabled-silicon-photonics-platform-at-tsmc/

Potential Simulation Needs of Upcoming Photonic ICs

UCSB

From Discrete Modules to Integrated Chip I/O (Luxtera)



Slide courtesy of P. De Dobbelaere, Luxtera

October 22, 2015 C. Schow, UCSB 26

- **High reliability simulation needs**
  - Thermal/stress simulation
  - PI/SI of High-freq transceiver and receiver Chip-Package-System
  - Waveguide S-parameter 3D EM simulation

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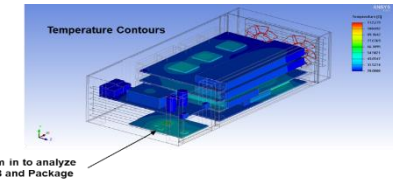
Chip-Package-System Thermal Reliability Workflow

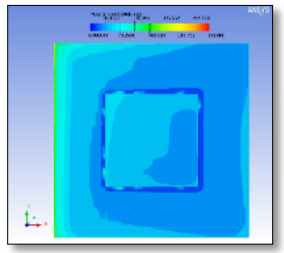


- ✓ Fluid flow (Laminar and Turbulent)
- ✓ Conjugate heat transfer(Conduction, Convection, Radiation, Joule Heating)
- ✓ Steady state and transient thermal analysis

Chip-Aware System Thermal Analysis

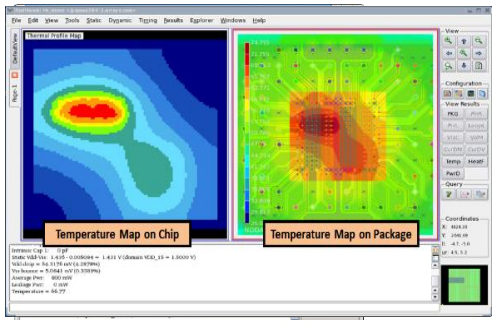
System Thermal Simulation

Chip Thermal Model (CTM)



HTC BC

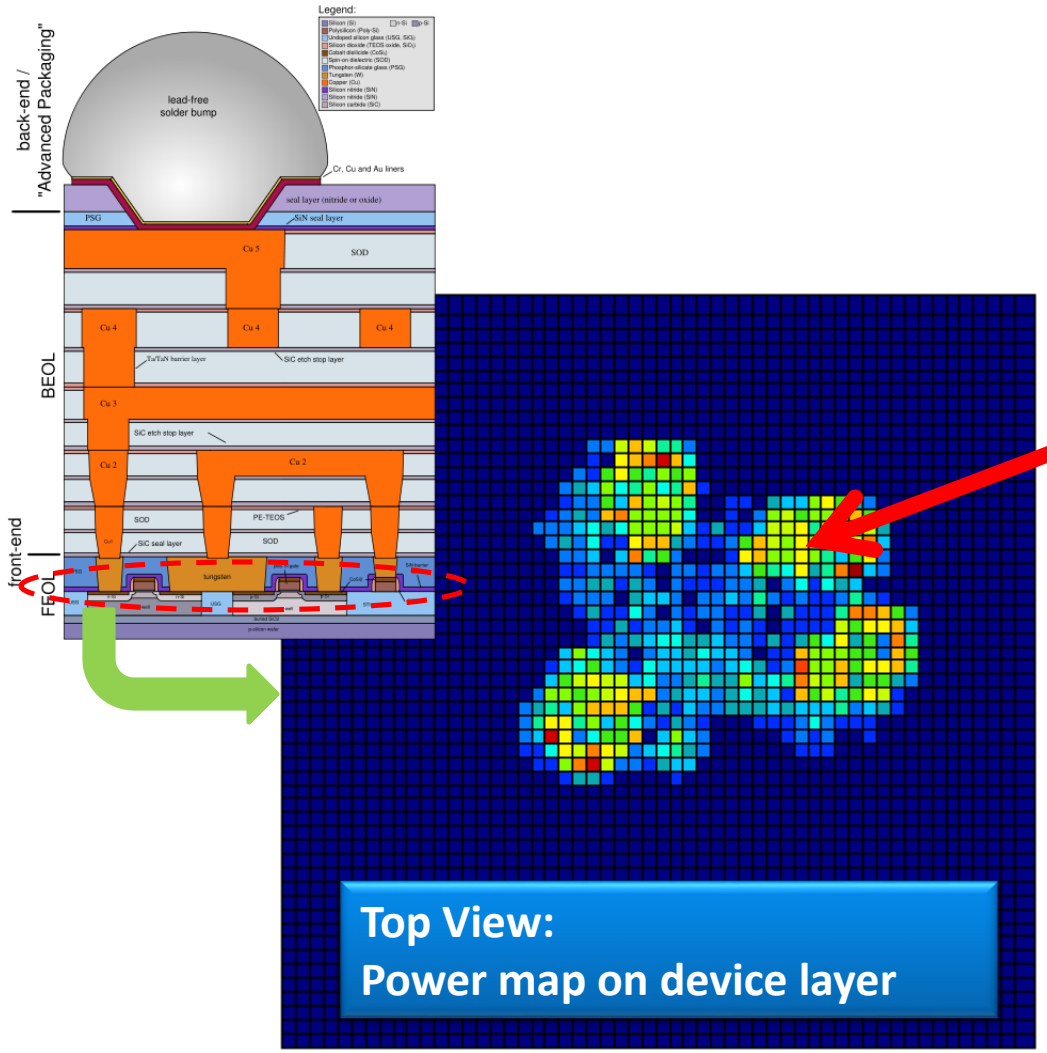
IC Simulation for Thermal-aware EM



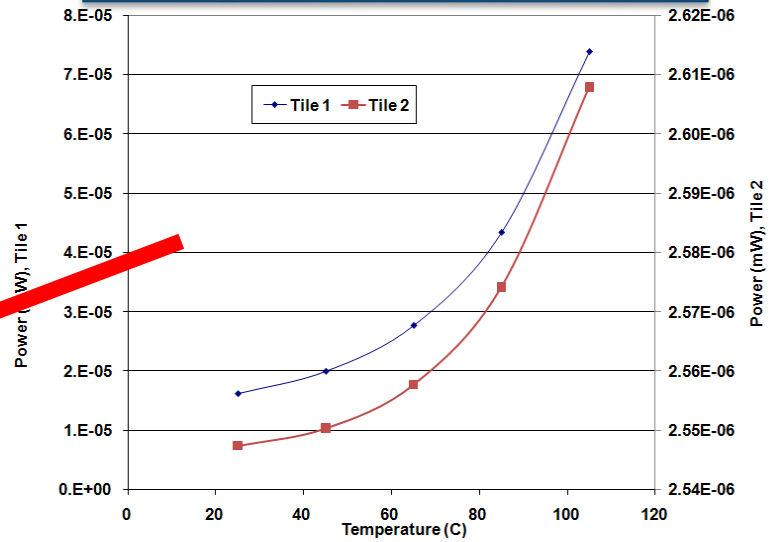
- ✓ Power-Thermal loop convergence
- ✓ FEM w/ adaptive mesh
- ✓ 2.5/3D IC support
- ✓ Thermal aware EM analysis

System-Aware Chip Thermal EM Analysis

Thermal Run-away Power/Thermal Convergence Flow



Temperature dependency of leakage power on tiles



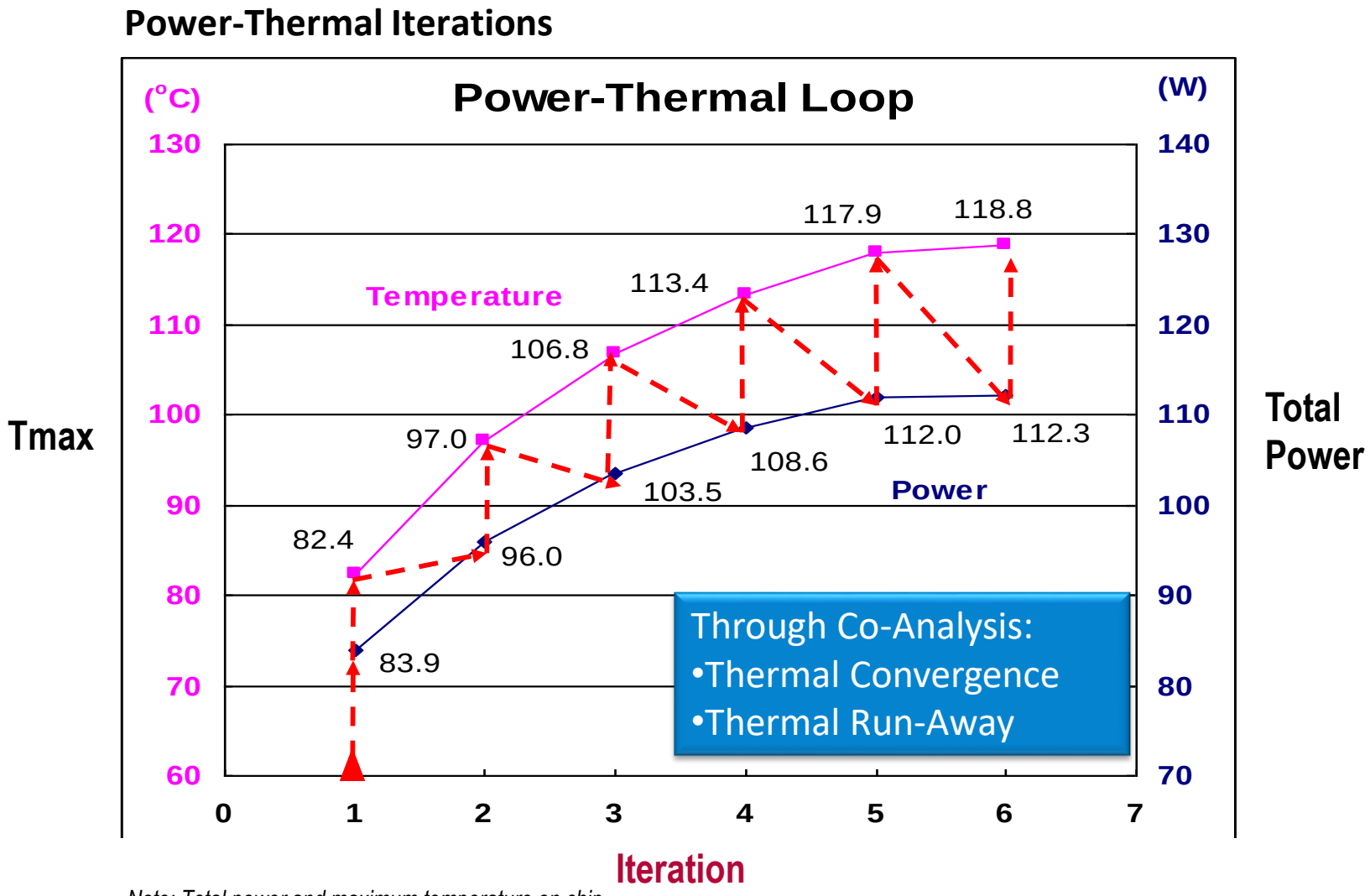
ΔV_T = −4 mV/°C to −2 mV/°C

$P_{static} = V_{CC}\, I_{leak} \sim exp\,(-V_T)$

Temperature dependent leakage power equation per cell from foundry or SPICE simulation

Local temperature rise has significant impact to P_{static} due to temperature dependent leakage power, and vice versa

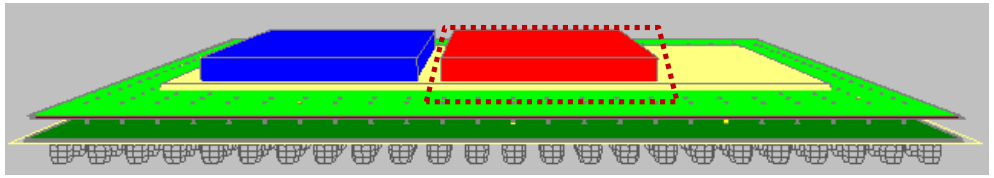
Power/Thermal Convergence Example



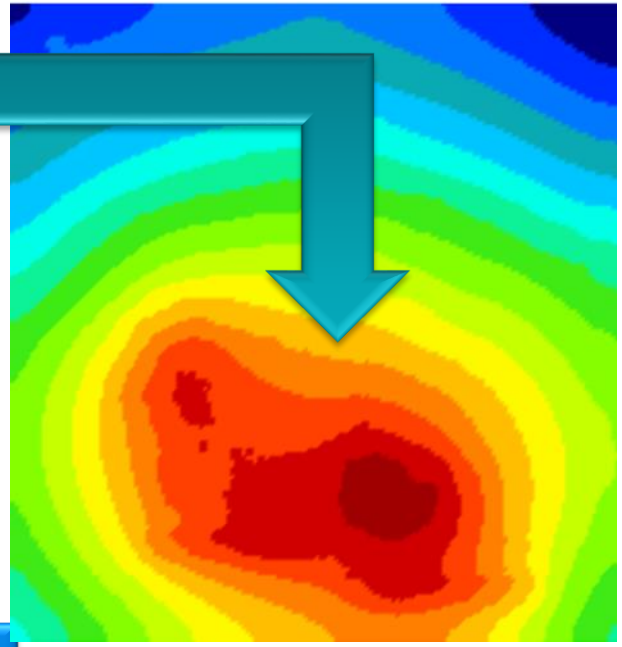
Note: Total power and maximum temperature on chip

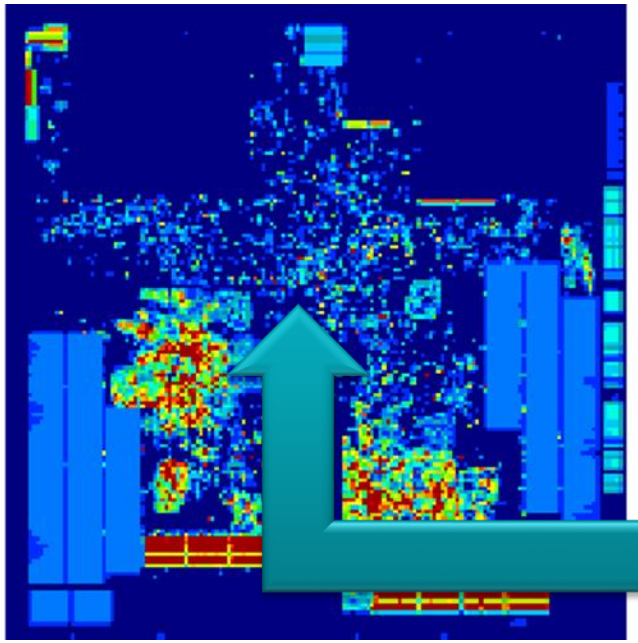
3DIC Thermal Run-away Power/Thermal Convergence Flow

3D IC Model



Updated Temperature in 3D IC

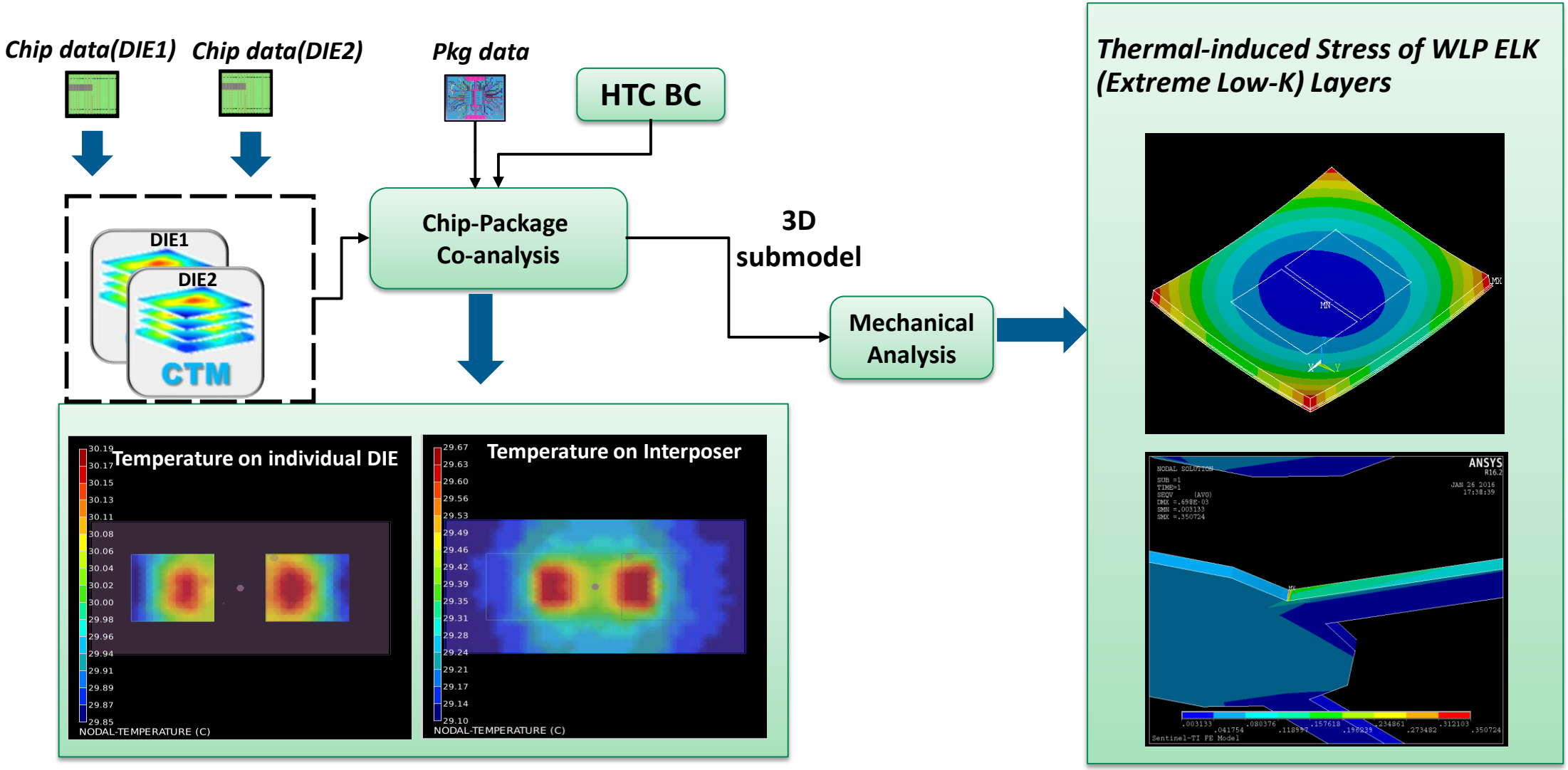




Updated Power in 3D IC

CTM for each chip in 3D IC : Lookup power map from temperature map

Multiphysics Simulations for Fanout Wafer Level Packaging (FOWLP) Designs

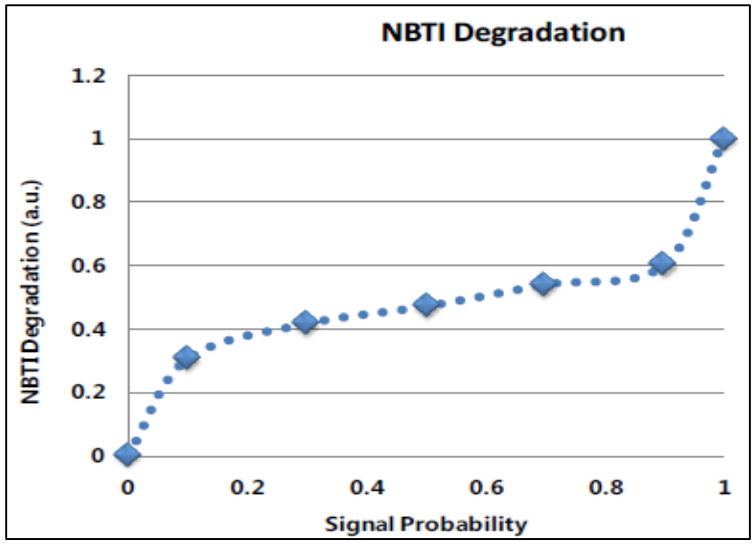


Emerging ADAS Thermal Reliability Needs and Solutions, N. Chang, et al., IEEE Micro Magazine, April, 2018

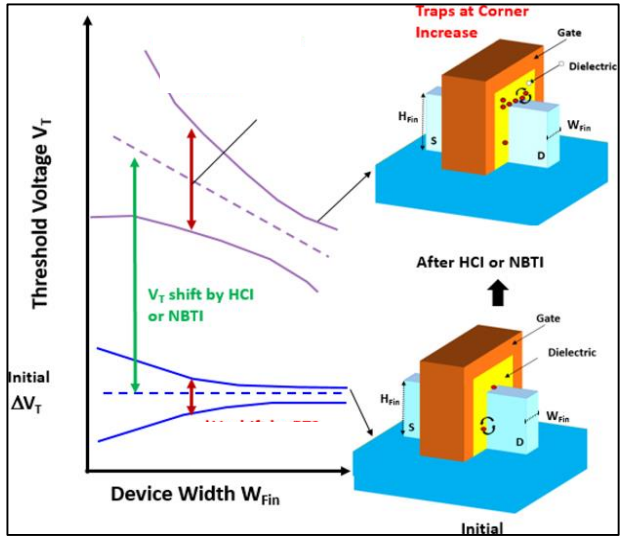
Aging Reliability in FinFET Technologies

Aging in FinFET accelerated by two major device degradation mechanisms:

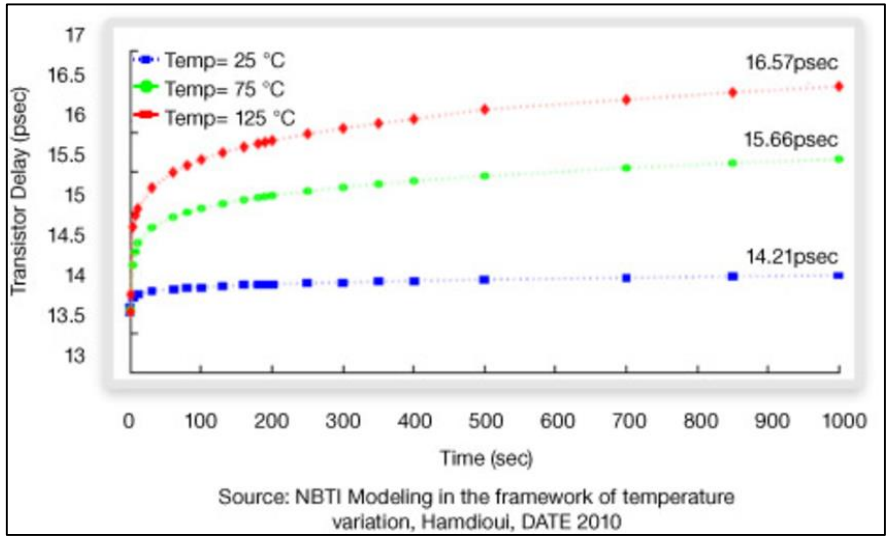
- Negative Bias Temperature Instability (NBTI)
- Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB)



NBTI degradation & Signal Probability



Shift in Vth due to Aging effect



Aging impact on transistor delay

Aging aware SOC Timing closure is necessary to ensure long term reliability for FinFET designs

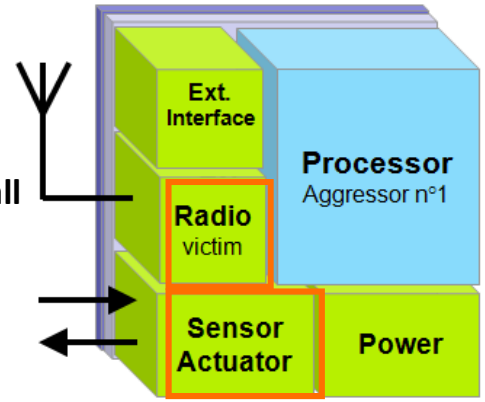
SoC Chip Level Aging Timing Sign-off in Advanced FinFET Technologies, Y. Sun, C. Zhan, HiSlicon, DAC, 2017

Substrate Noise among Analog/Digital Sections

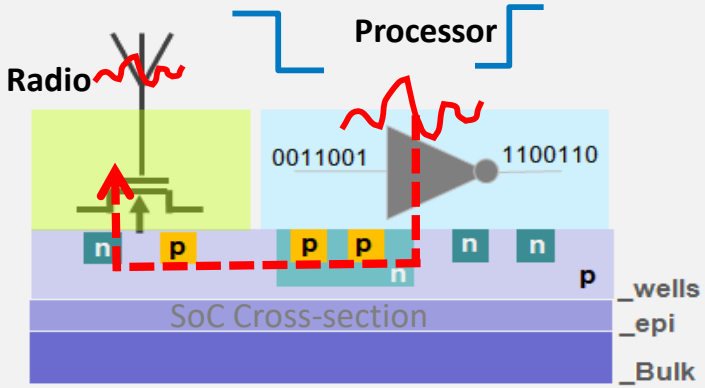
Applications for 5G / ADAS SoC Development

Case study: NXP (Saturn SAF360X)

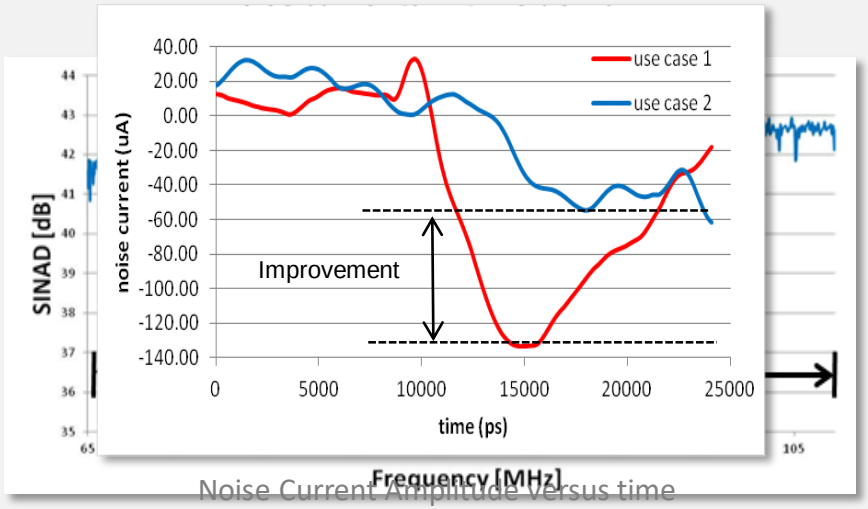
- **Multi-standard software-defined** radio co-processor capable of decoding **all three major digital** terrestrial radio standards
- **6 separate IC functions** in one chip == 75% size reduction



Coupling Noise from switching digital to sensitive analog through the silicon



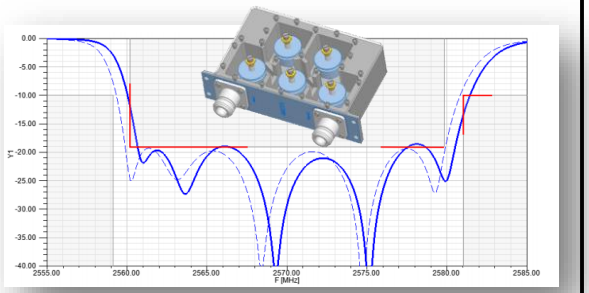
Noise coupling → Spikes in FM Spectrum
Impacts audio quality and performance

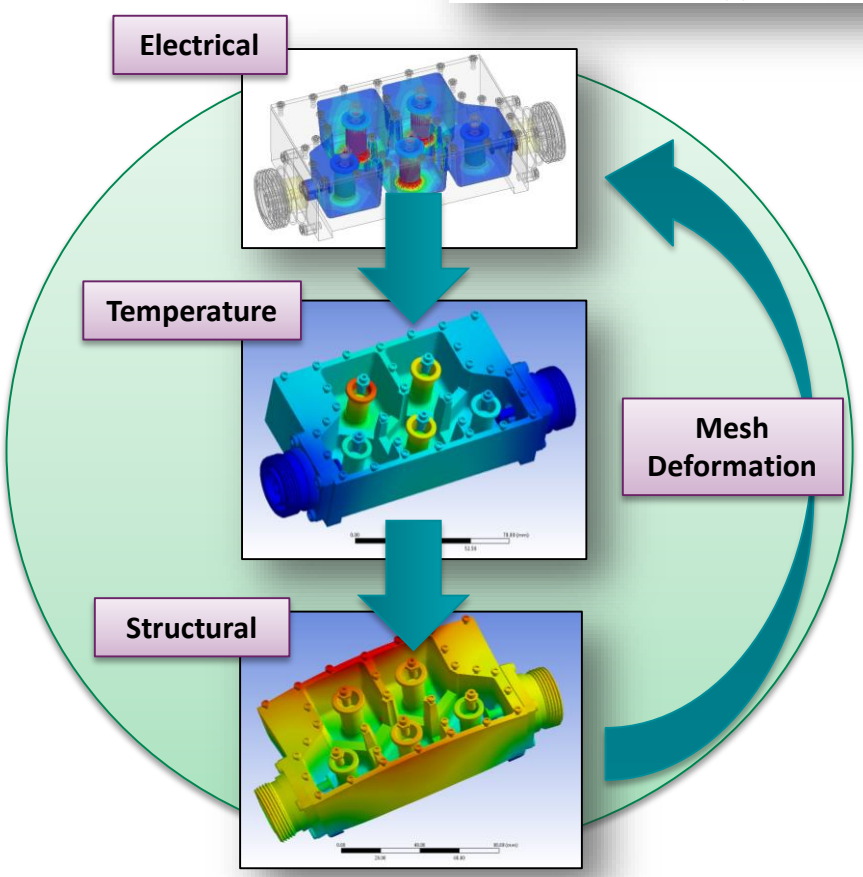


Noise Current Amplitude versus time

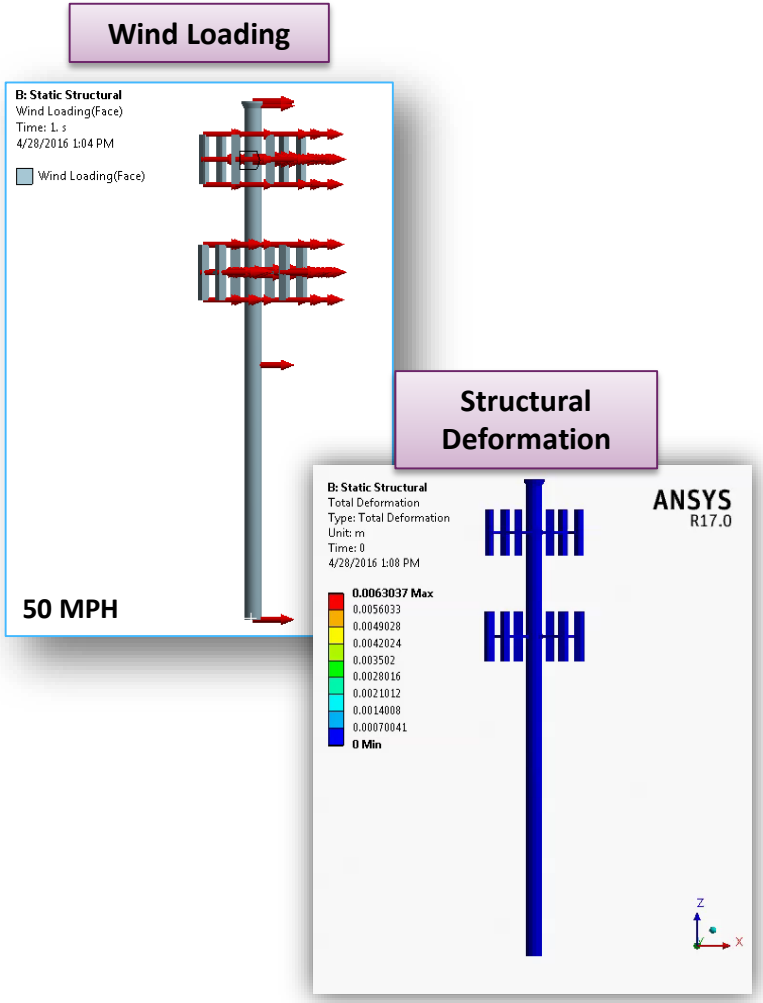
Multiphysics Reliability Simulation: Full 5G System

Coupled EM/Thermal/Structural Analysis: High Power Filter Detuning

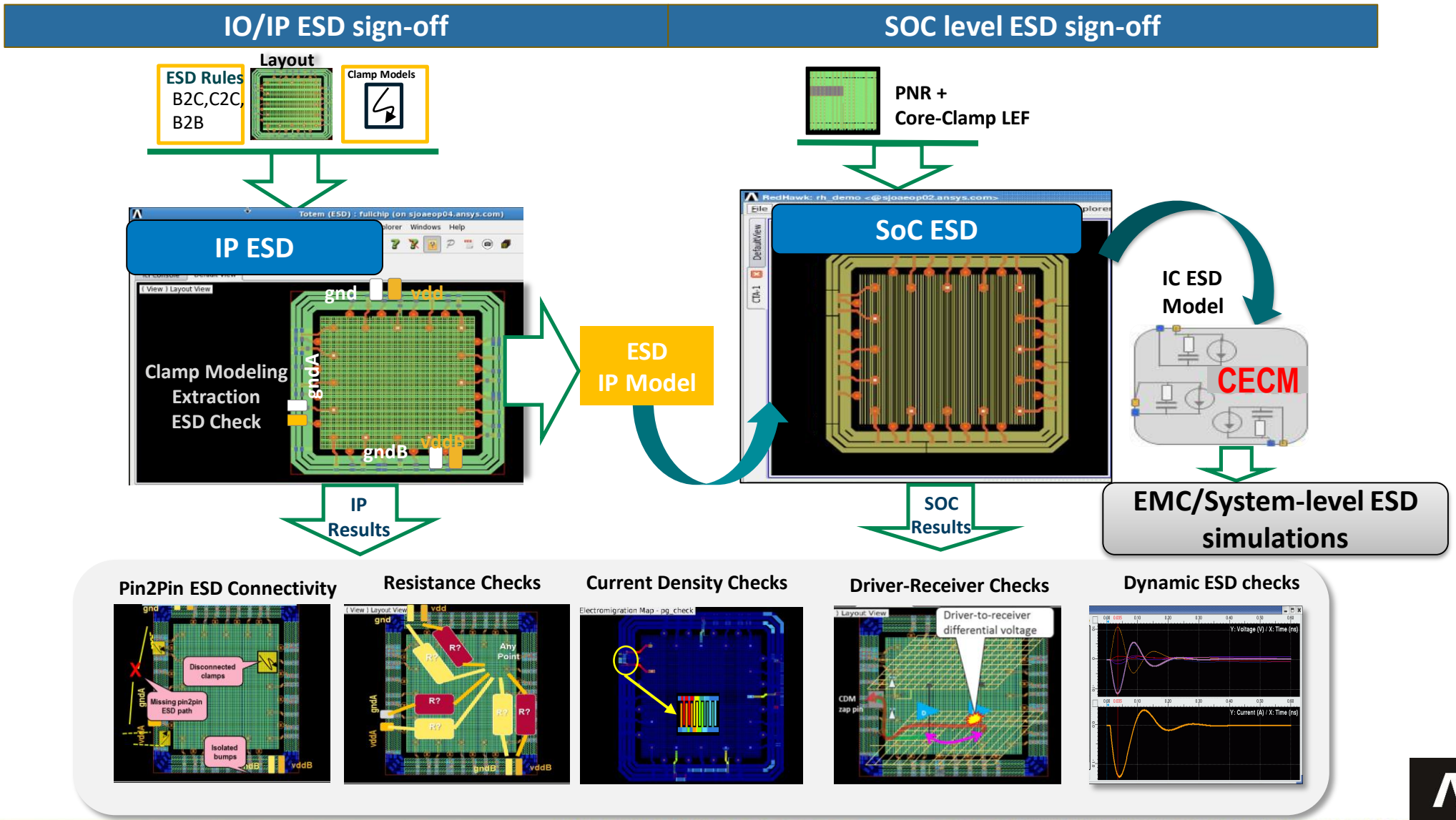




Structural Analysis: Wind Loading on Cell Tower



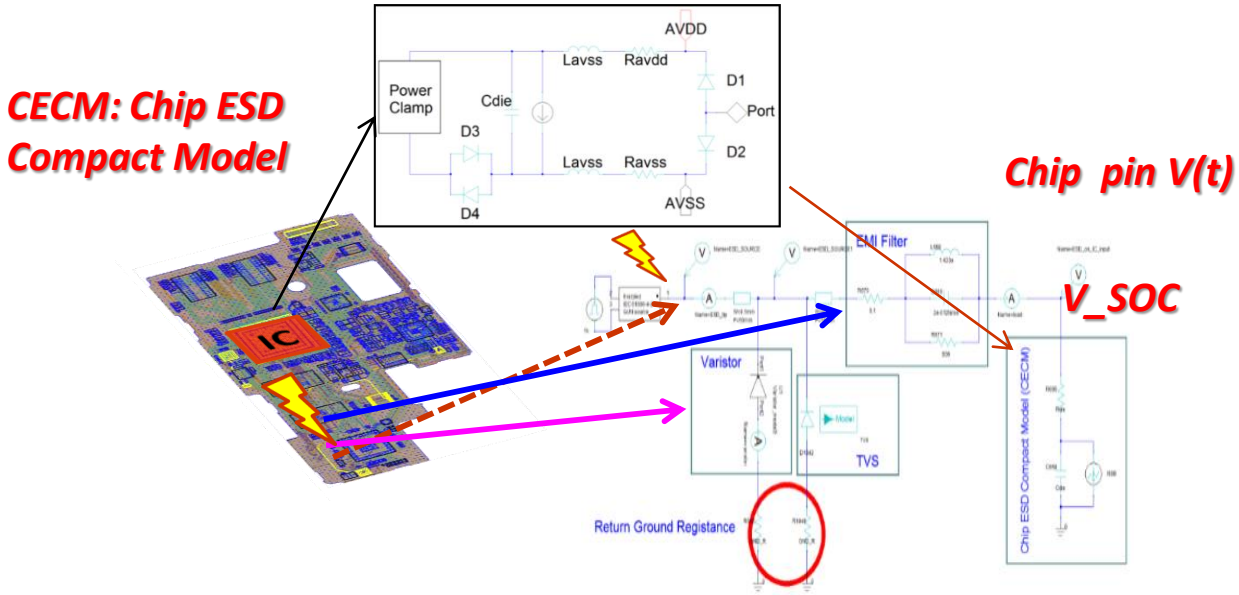
Chip-Package-System ESD/EMC Simulation Needs



System Level ESD Simulations Demanded for Upcoming 5G/ADAS Systems

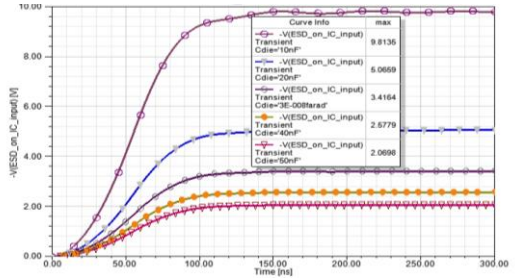
Target: System level ESD Sign-off with CECM for IEC61000-4-2 testing

- What-if Analysis for system level ESD optimization
- Improve ESD protection from chip all the way to PCB



Solutions needed:

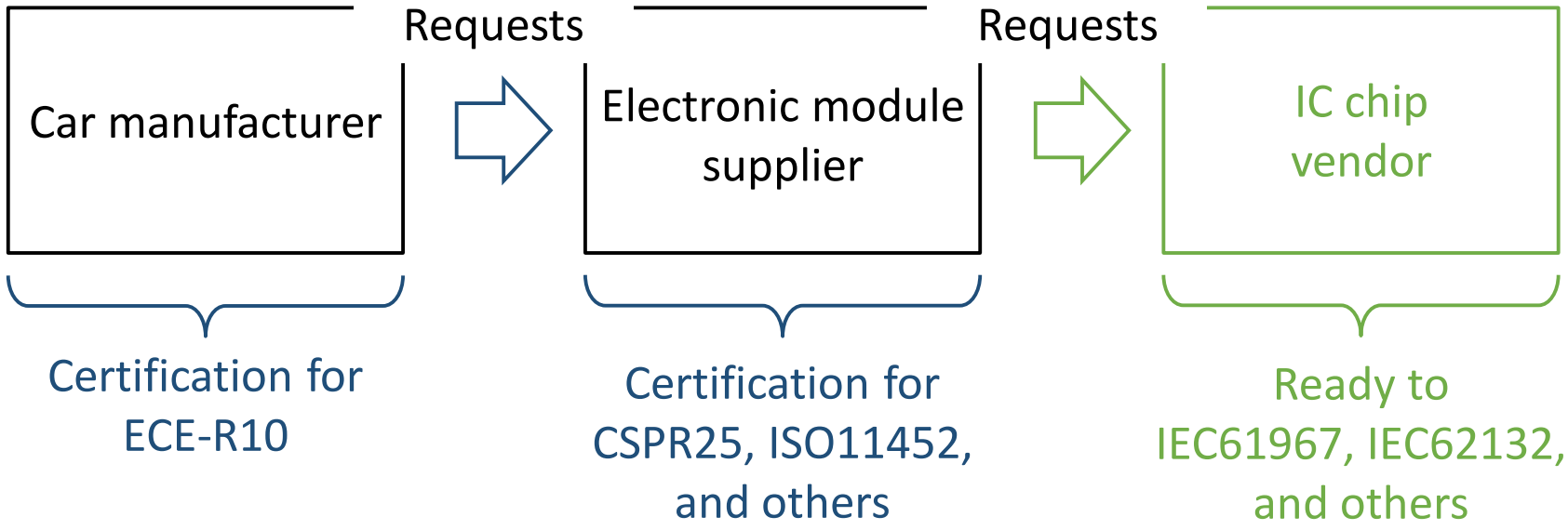
- ✓ IO/IO Ring Modeling
- ✓ Fullchip Layout modeling and PG extraction
- ✓ ESD device modeling, Chip ESD Model
- ✓ System level ESD analysis with CECM



Chip pin V(t) for different CECM. Higher Cdie results in lower pin residual voltage

"System-level ESD Failure Diagnosis with Chip-Package-System Dynamic ESD Simulation"
R. Myoung, B. Seol, N. Chang, Samsung/Ansys, EOS/ESD Symposium 2014

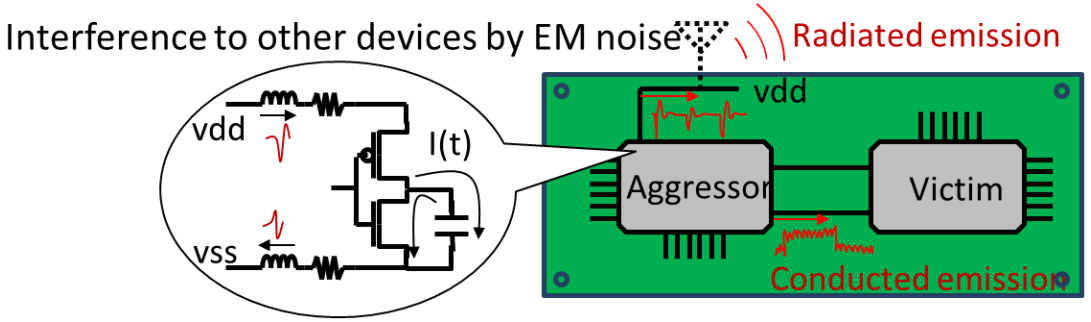
EMC Compliance on Automotive IC's



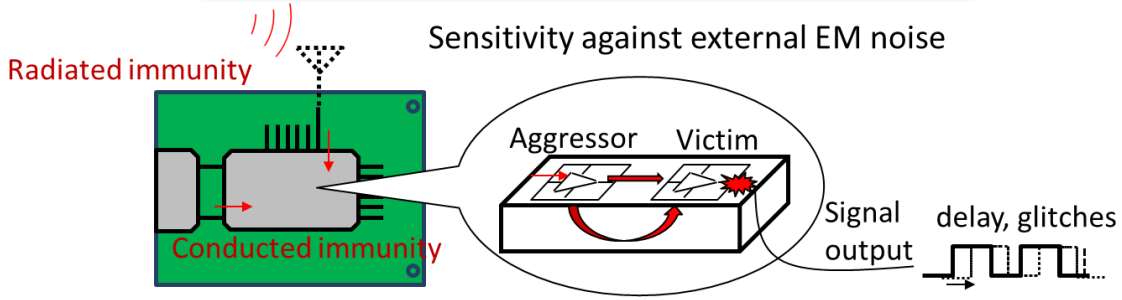
- **EMC compliance covers automotive supply chain at different levels**
- **ECE-R10 ⇒ General EMC regulation for car manufacturers**
- **CSPR25, ISO11452 ⇒ Component-level EMC tests against radio disturbance**
- **IEC61967,IEC62132 ⇒ IC chip-level emission and immunity tests**

EMI/EMS CPS Reliability

Electromagnetic Interference(EMI)



Electromagnetic Susceptibility(EMS)

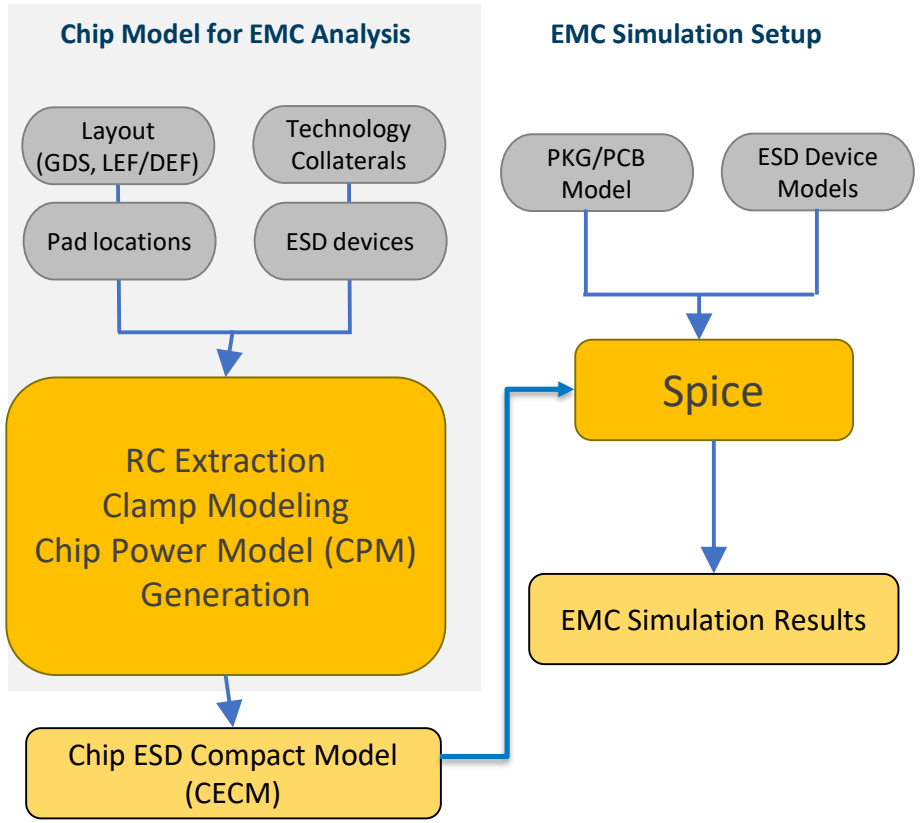


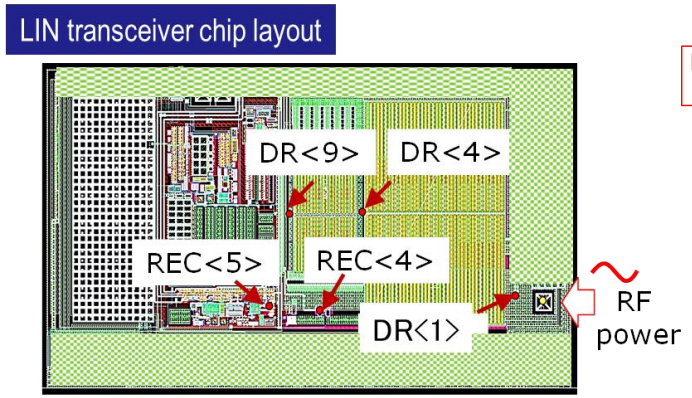
Electromagnetic Compatibility(EMC) **EMC = EMI + EMS**

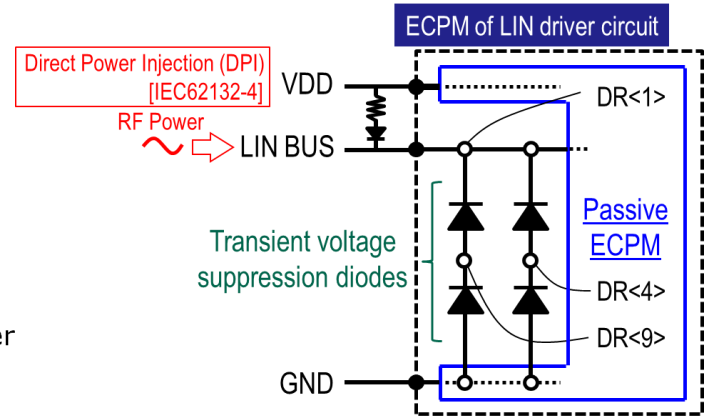
- The legal requirements to limit the generation or vulnerability due to Electromagnetic disturbance
- The automotive products need to comply with the requirements
- Achieving EMC compliance is a time-consuming task

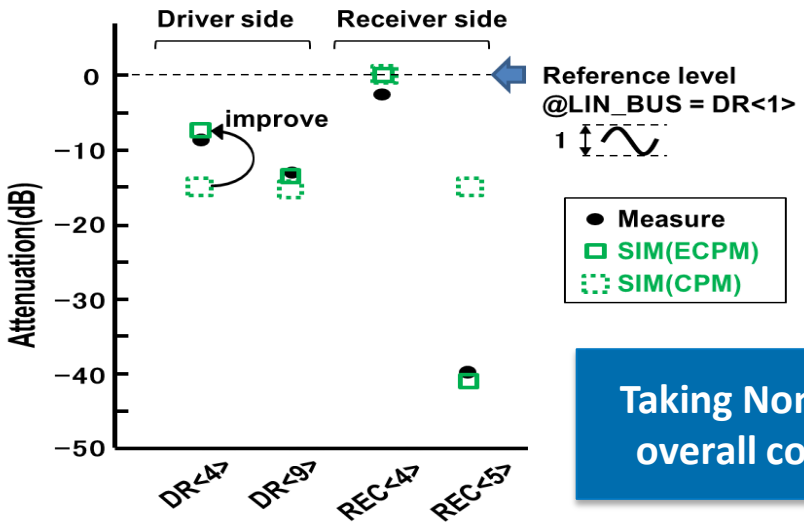
Multiphysics simulations combining Chip-Package-System are required to avoid costly redesign during manufacturing

EMI/EMS System Reliability







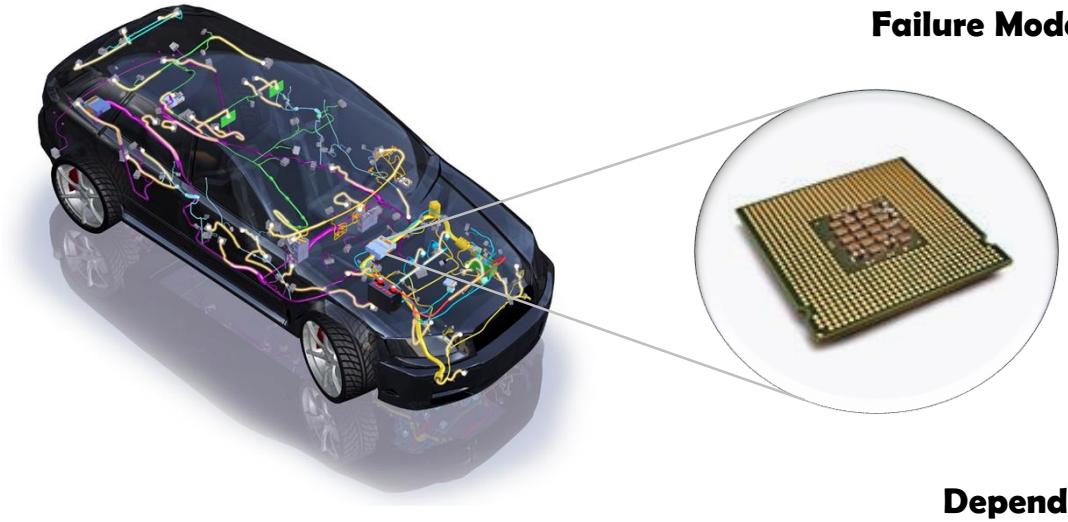


Taking Non-linear ESD devices improves overall correlation with measurement

"Integration of RF DPI on ESD Protection Devices in EMS Testing of IC Chips", M. Nagata, N. Chang, et al, Kobe Univ , ANSYS, EMC Europe, 2018

Meeting the Challenge of 2nd Edition of ISO26262 for ADAS Reliability

Revision of the international standard dedicated to product development processes for safety-related electrical and/or electronic systems (E/E system) comes with new challenges for Semiconductors



Safety Requirements

Failure Mode and Effects Analysis (FMEA)

Hardware Diagnostic Coverage Metrics (FMEDA)

Safety Mechanism Design

Fault Injection & Simulation

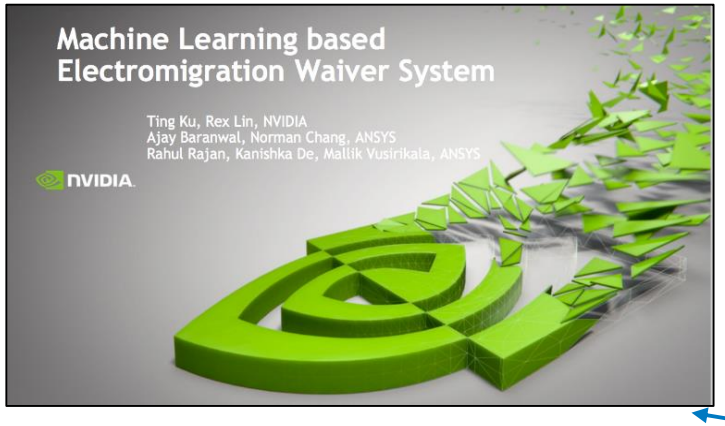
Fault Tree Analysis (FTA)

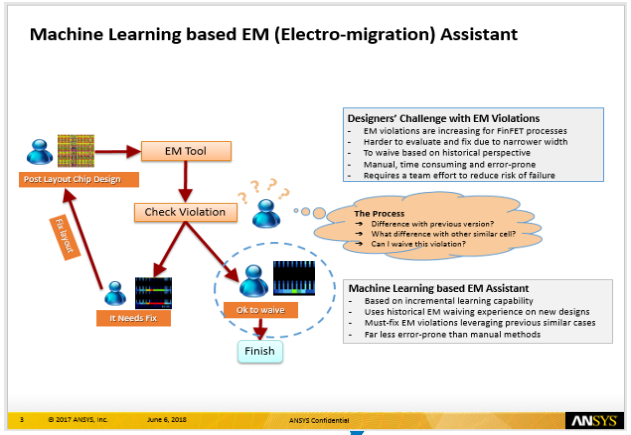
Dependent Failure Analysis

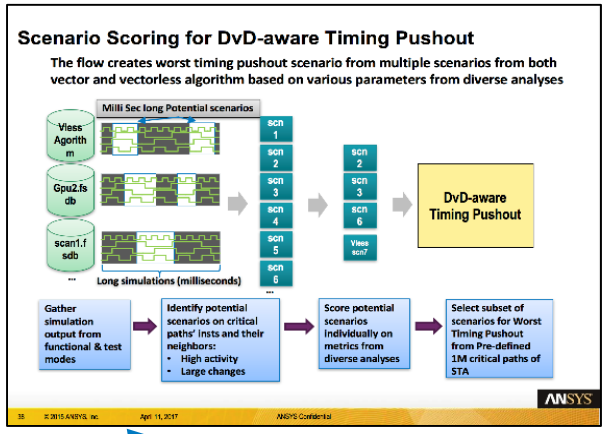
Change Management & Impact Analysis

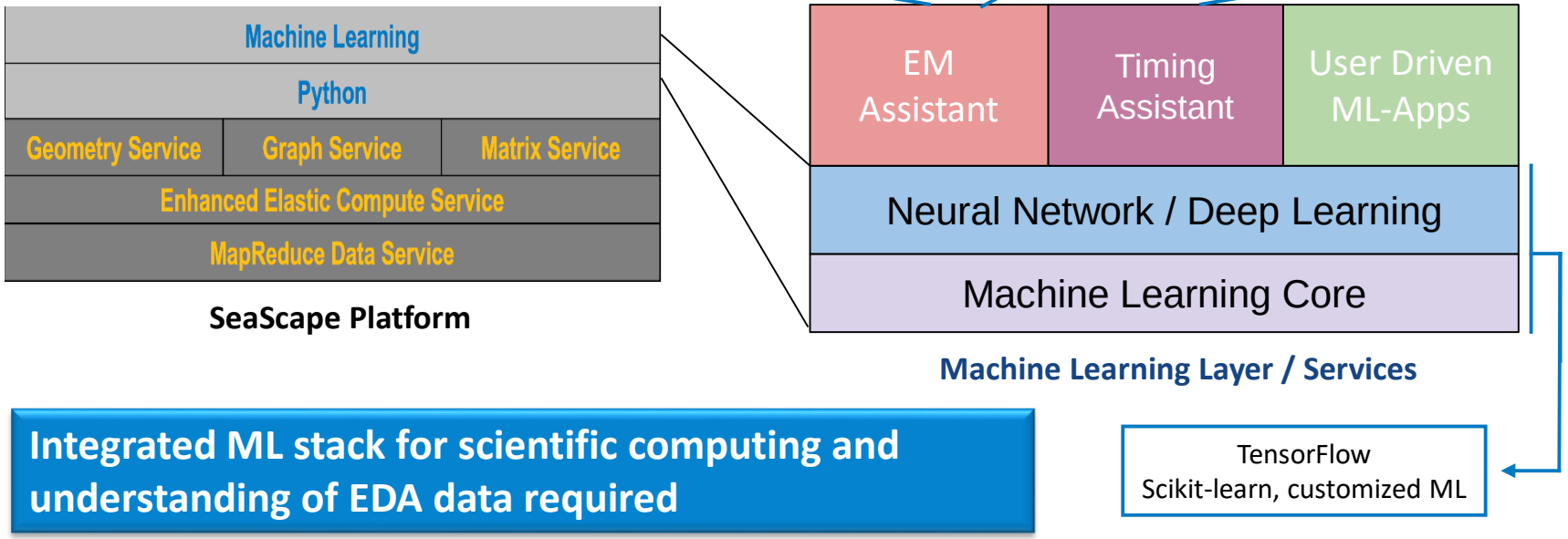
Chip data and reliability info should be part of System Reliability Calculation

System Reliability Checks can be Greatly Augmented with ML/DL









Integrated ML stack for scientific computing and understanding of EDA data required

Example Application: "Machine Learning based Generic Violation Waiver System with Application on Electromigration Sign-off, N. Chang, T. Ku (Nvidia), et al, ASP-DAC, 2018

Upcoming Challenges for System Reliability Analysis Flow

- **Comprehensive system reliability flows needed to cover unique demands from high-frequency, high-power 5G systems**
  - High-frequency effects need to be considered for 5G CPS
  - System-level thermal/ESD presents a new challenge

- **ADAS/AI ramping up very quickly with many new start-ups in this area targeting a complete Level-4/5 Autonomous Driving system**
  - Electronics needed to survive >15 years under harsh environment and with smaller margin
  - Thermal and aging become an immediate reliability threat
  - EMI/EMS become part of standard compliance

- **Si Photonics leveraging CMOS process can be the next major growth segment**
  - Automated large scale integration
  - System reliability analysis flow required