

Device Manufacturing in an Era of Neural Networks

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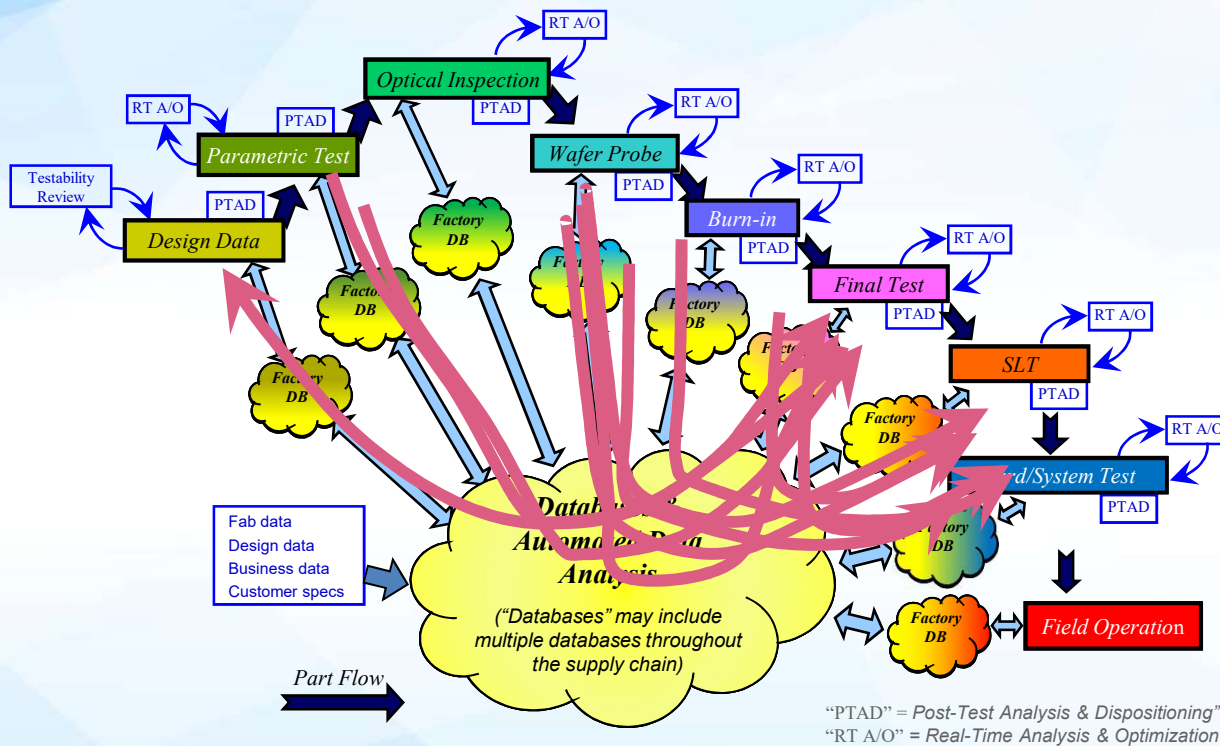
and

Heterogeneous Integration Roadmap, Chairman, Test Working Group

Agenda

1. What is Adaptive Test?
2. What are Convolutional Neural Networks?
3. How can these techniques be combined to improve the semiconductor manufacturing process?

Adaptive Test – The Vision



In Practice....

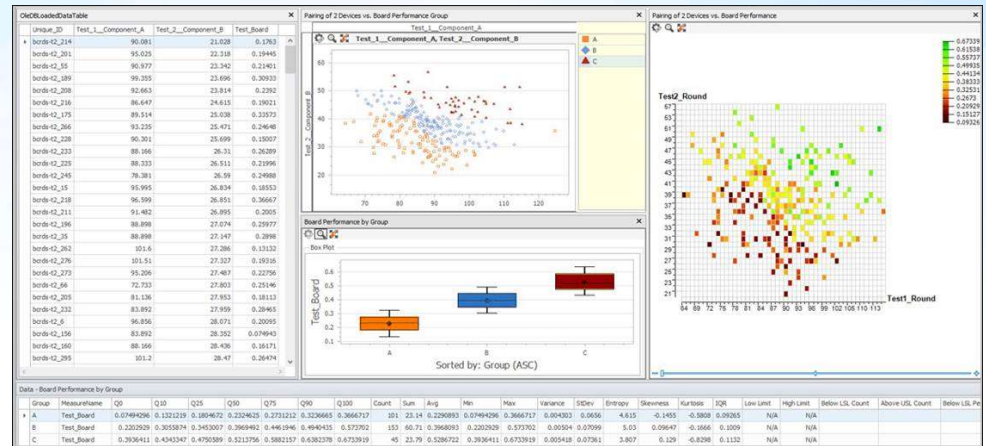
Why do a partial database search today. Wafer Probe data being used for wafer to wafer tests would provide the most value for least cost.

- All adaptive test today is feedforward in nature.
- Feedback data only helpful on future designs.

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Adaptive Test – Today

- Data analysis today requires an expert data system and an expert data analyst.



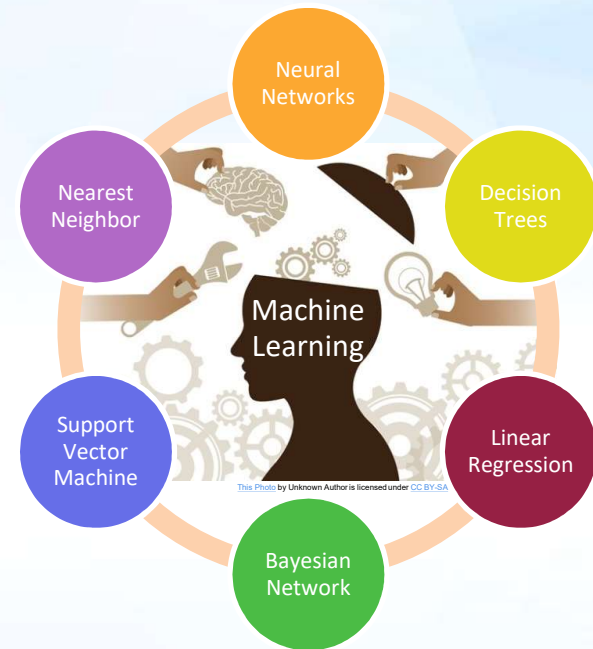
TestVision 2020: “SQN Shared Quality Network” by Dan Sebban of OptimalPlus

In the future AI systems will do the analysis and the entire manufacturing flow will be tracked and optimized automatically.

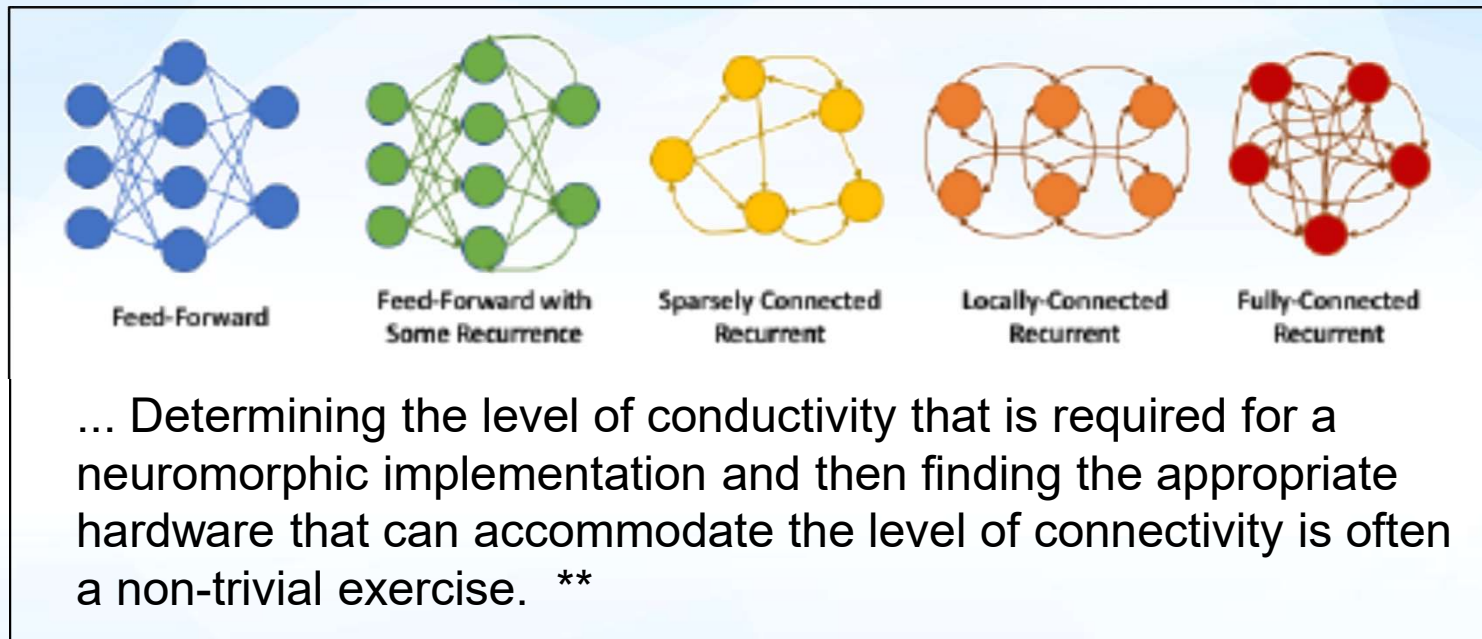
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The Machine Learning Toolbox

- Rich library of Machine Learning algorithms available
- Each algorithm is best for specific applications – no “one size fits all”
- Choosing the right algorithm is a mix of art and science – many factors must be considered
- Neural Network algorithms are particularly useful for recognizing patterns/relationships in complex data



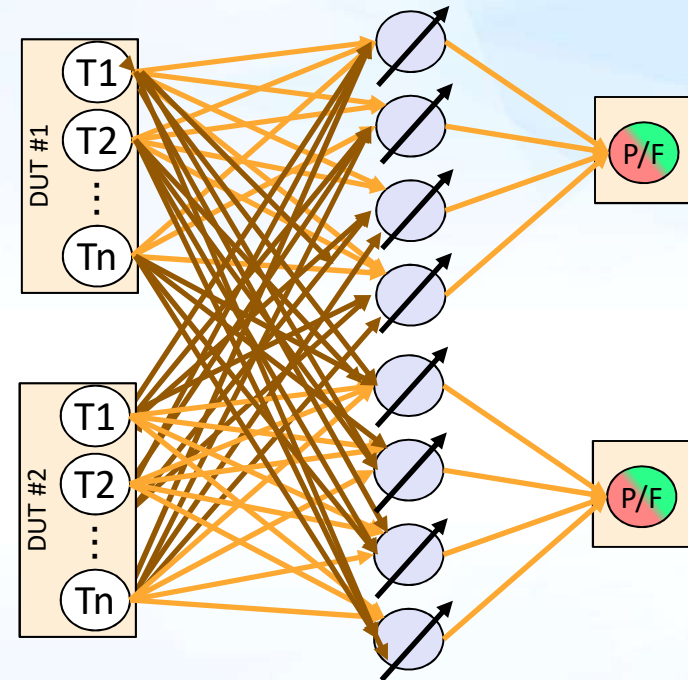
Types of Convolutional Neuromorphic Networks



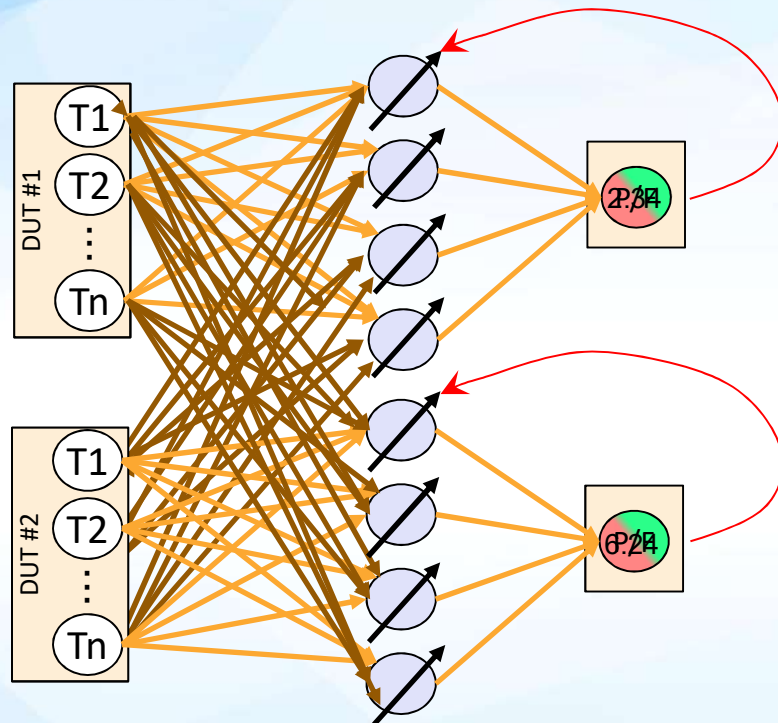
** A Survey of Neuromorphic Computing and Neural Networks in Hardware; Catherine Schuman et al; arXiv:1705/006963v1

What is a Convolutional Neural Network?

- A neural network takes test data, remaps it through one (or more) computational layers in order to determine pass/fail.
- Of course we have data for many devices per wafer/lot.
 - Which gives us possibility for many more relationships.
- The convolutional step learns the feedforward coefficients over time. This is called “training”.



Training



- Training is going to be the hardest part of setting up a Neural Network for semiconductor devices.
- What constitutes a “good” test result?
 - One with the most margin to spec?
 - One which help achieve the best yield?
 - One which meets spec with the minimum power consumption?
- Neural Networks today are typically trained with subjective (human) classifications.
- Once we have automatic loop training is we will truly have an artificially intelligent manufacturing environment.

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Neural Networks are Good at Picture Recognition

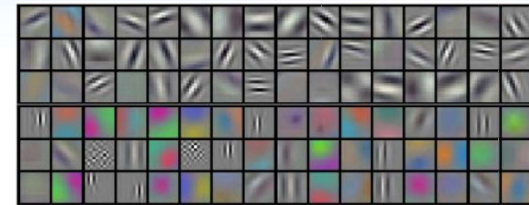
- Training requires a lot of data (something the semiconductor industry is not short of).

Input a bunch of Chihuahuas



Machine Learns to recognize Chihuahua patterns

MODEL = Set of Coefficients



“hmm, ok I learned what Chihuahuas look like”

- Pointed ears
- Small typically dark nose
- Little beady eyes
- ...

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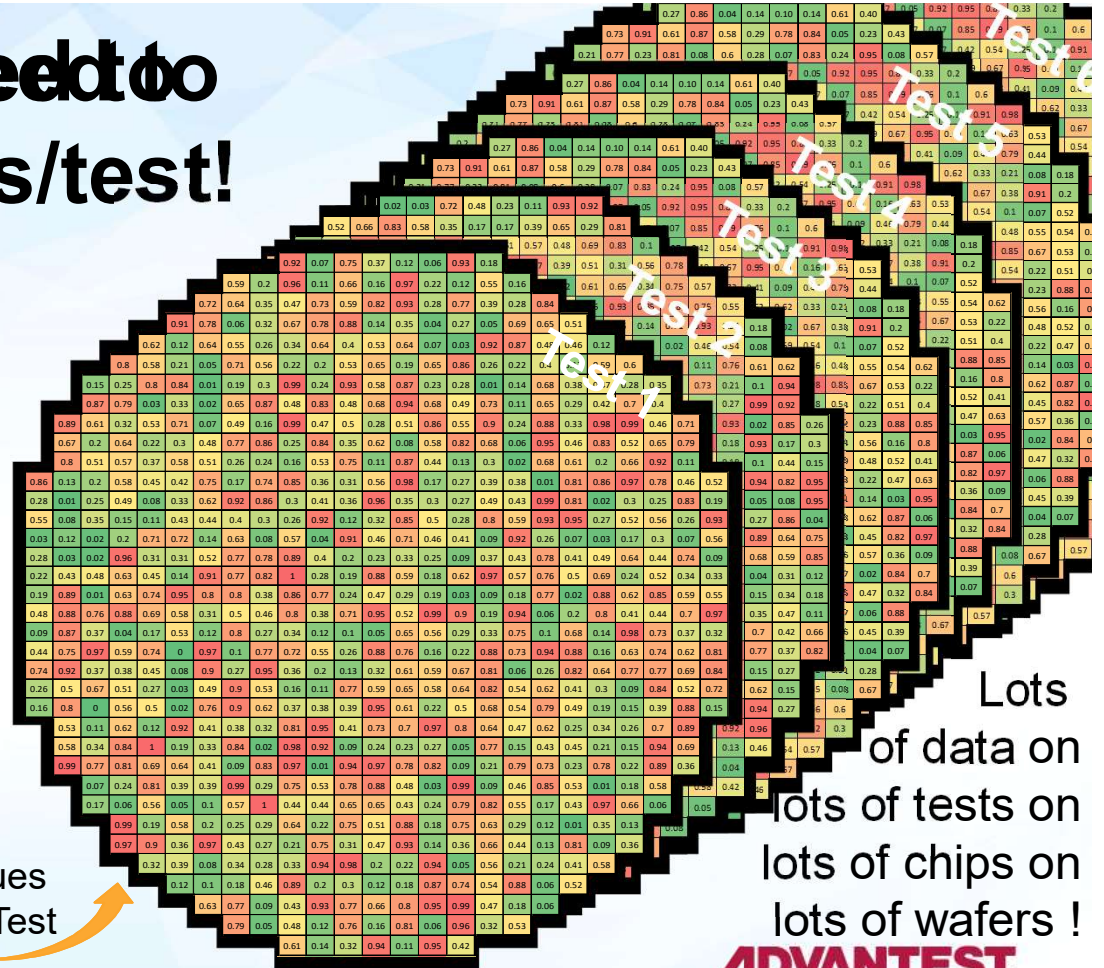
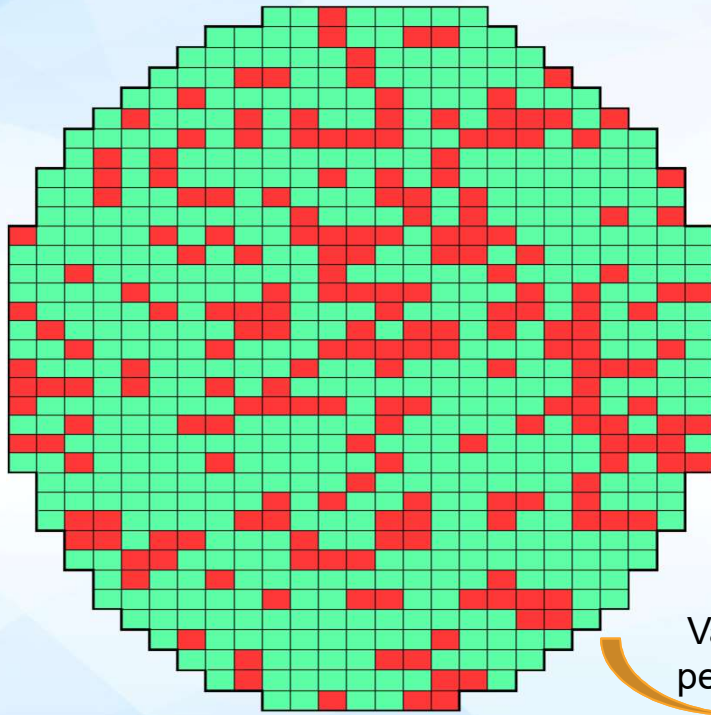
Training a Self-Driving Car



- Since the beginning, autonomous vehicle programs have analyzed videos of ~ 1 million traffic miles.
- But, statistics suggest ~ 770 accidents per billion miles driven. (0.8 per million miles!)
- Training these networks with real-world is both expensive, deadly, and slow.
- The industry is moving to simulated driving situations to get the vast quantity of data that's needed to adequately train.

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The Pictures We Need to Work With – Results/test!



Values per Test

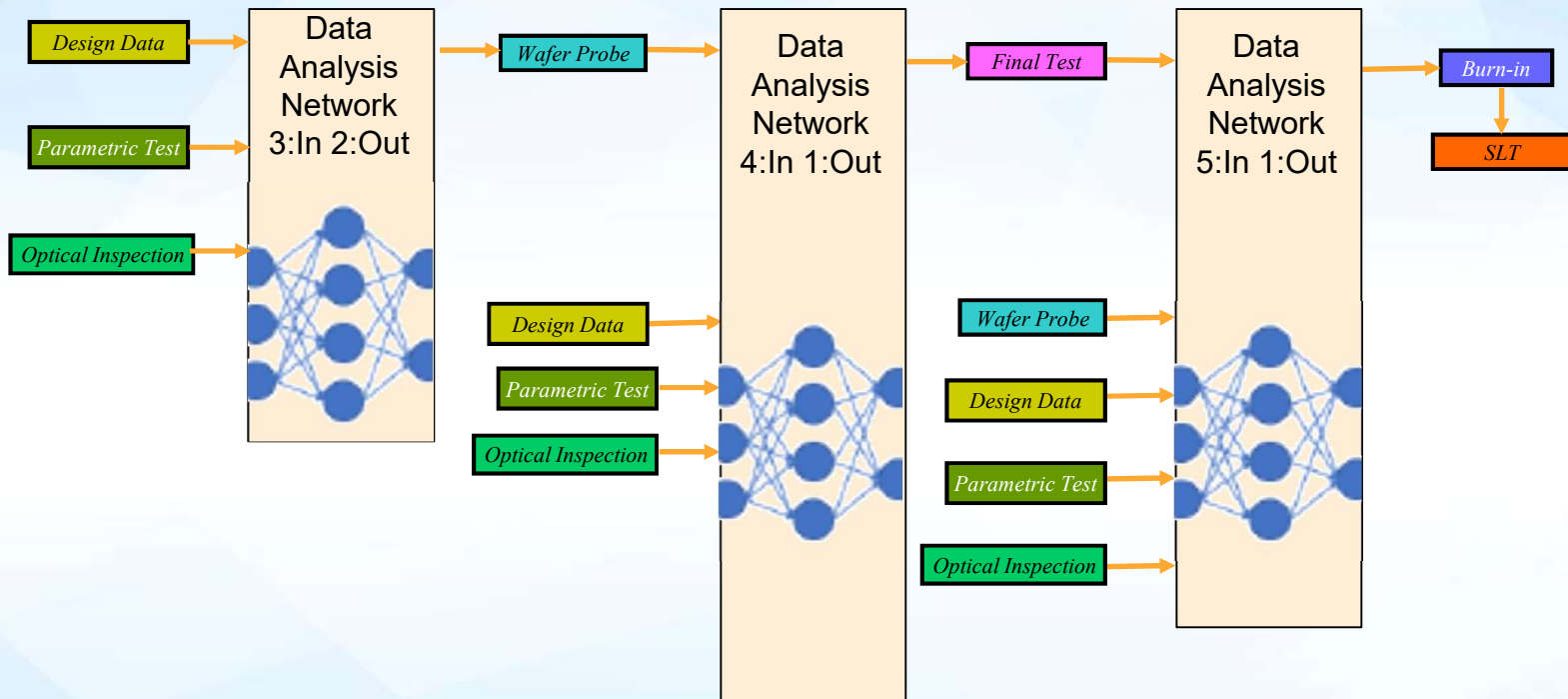
Lots of data on lots of tests on lots of chips on lots of wafers !

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Key Advantages of Applying NN to Semiconductor Manufacturing

1. Lots of data available:
 - TSMC capacity is > 2M wafers/month
 - Each device likely has > 1K test data points (manufacturing & E-test data is in addition)
 - 500-10,000 devices per wafer
2. Semiconductor “images” don’t move around.
 - Unlike cars & dogs, correlations are always done in a fixed location.
3. Semiconductor industry models everything
4. Target to train against is fairly well understood.
 - Test results.
 - High yield.
 - Low cost.

Feed Forward Possibilities in Test



What are Some of the Neural Networks Inputs Which Might Make Sense?

- Let's look just at an Fmax Test . . .

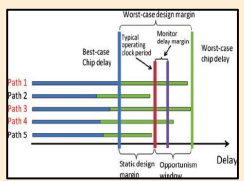
Design Data

Parametric Test

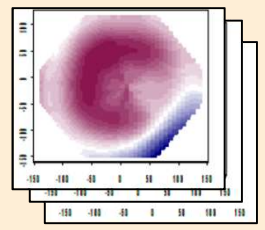
Wafer Probe

Final Test

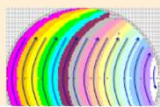
Critical Path Analysis



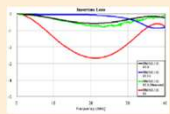
Gate-CD Meas.



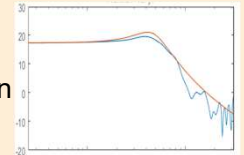
Stepping Patterns



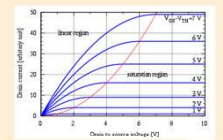
Probe BW



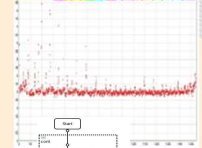
Signal Transmission



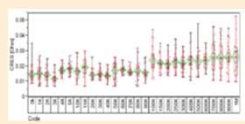
Transistor Curves



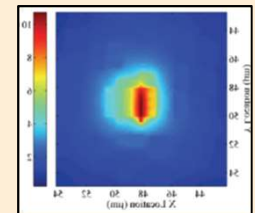
CRES Per pin



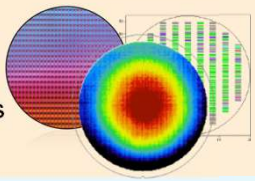
Probe Life



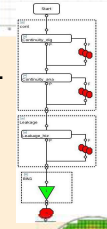
Thermal Simulations



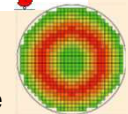
Typical Process Parameters



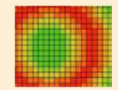
Test Prog. & Setup Param.



Chuck Thermal Resistance



Package Thermal Resistance



Per-Test Results

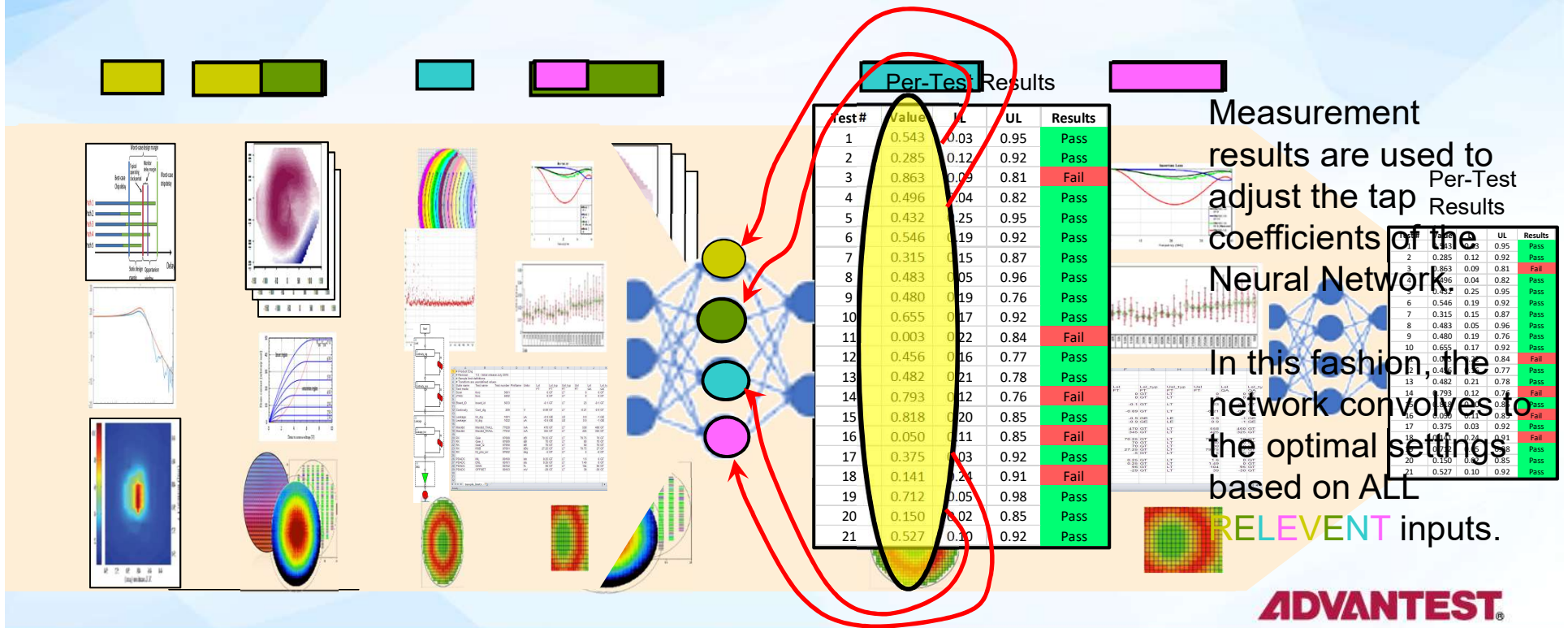
Test #	Value	LL	UL	Results
1	0.543	0.03	0.95	Pass
2	0.285	0.12	0.92	Pass
3	0.863	0.09	0.81	Fail
4	0.496	0.04	0.82	Pass
5	0.432	0.25	0.95	Pass
6	0.546	0.19	0.92	Pass
7	0.315	0.15	0.87	Pass
8	0.483	0.05	0.96	Pass
9	0.480	0.19	0.76	Pass
10	0.655	0.17	0.92	Pass
11	0.003	0.22	0.84	Fail
12	0.456	0.16	0.77	Pass
13	0.482	0.21	0.78	Pass
14	0.793	0.12	0.76	Fail
15	0.818	0.20	0.85	Pass
16	0.050	0.11	0.85	Fail
17	0.375	0.03	0.92	Pass
18	0.141	0.24	0.91	Fail
19	0.712	0.05	0.98	Pass
20	0.150	0.02	0.85	Pass
21	0.527	0.10	0.92	Pass



Note: Data shown for example only. Likely bears no resemblance to actual distributions.

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How Will We Train this Neural Network?



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What is Required To Implement This?

1. Test measurement values are critical → ATE needs an efficient way to gather and transmit large volumes of data.
2. Infrastructure needs to be upgraded to support big-data → Data bandwidth improvements, elimination of data-silos, improved encryption with easy access for those who need the data.
3. Data analysts need to monitor and help direct the convolutional efforts → Speed convergence, avoid instabilities.
4. Eventually, ATE will need to use Neural Network analysis to pinpoint good and bad devices → “Low hanging” gains likely in both yield and device reliability.

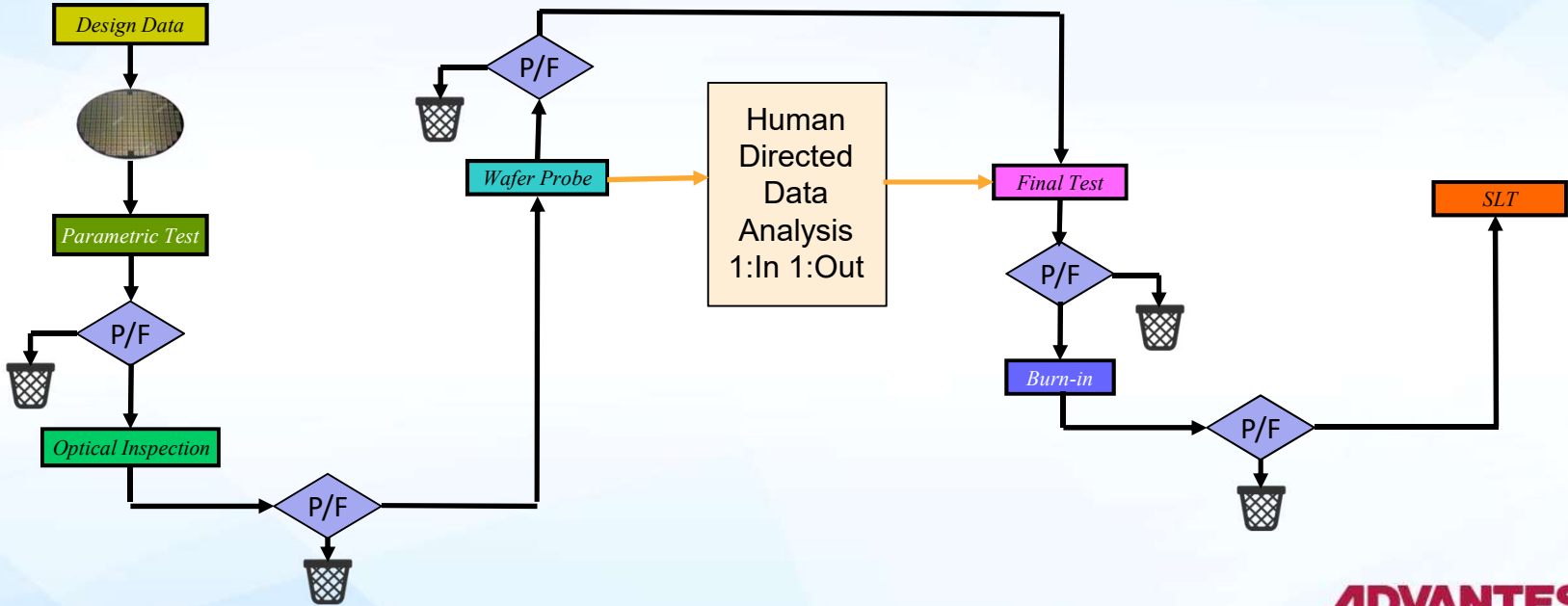
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Conclusions

- The potential gains associated with Machine Learning Algorithms such as Convolutional Neural Networks are considerable.
- The tools which support deploying this in semiconductor manufacturing are just arriving on the market.
- It will take some work to make this happen but the fruits of this labor will (in my opinion) revolutionize the semiconductor industry.

Backup

Adaptive Testing Today is Most Often Only Used Between Wafer & Final Test



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