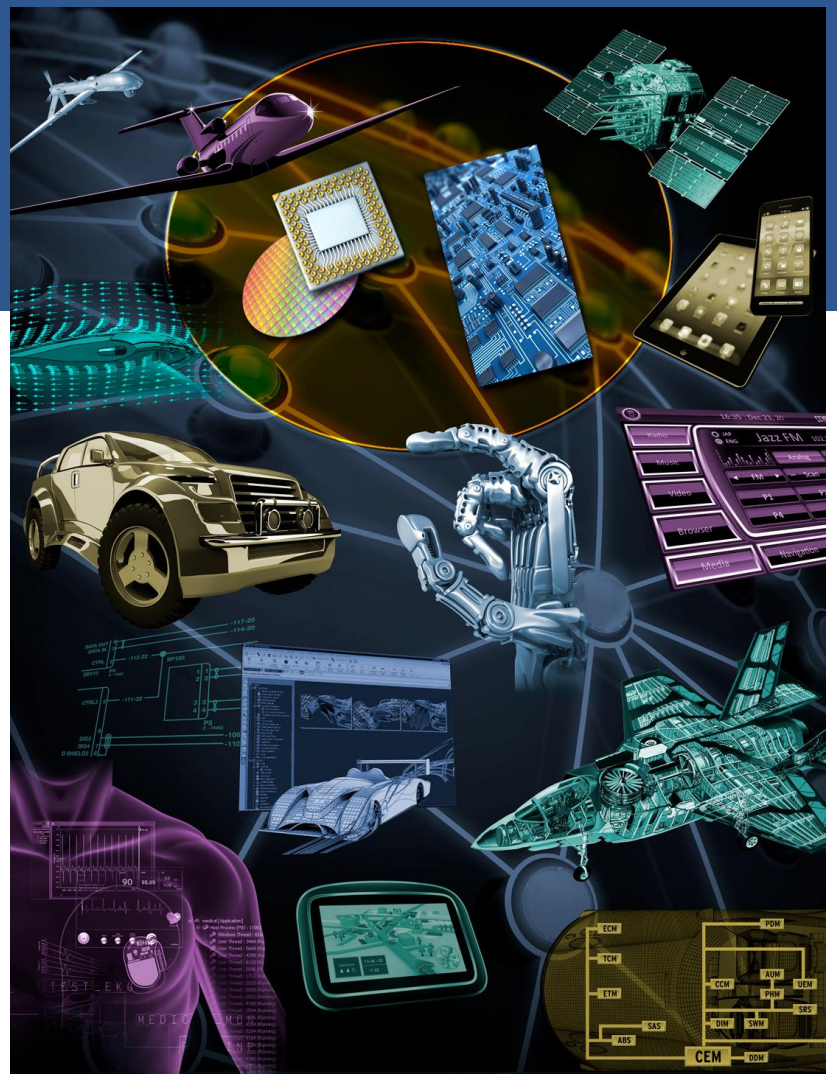


Connecting Advanced Manufacturing Test To Design, Fab And Final Product Yield For Complex FinFET Defect Challenges

Matthew Knowles, Ph. D.
Product Marketing Manager
Tessent Silicon Learning
Mentor, A Siemens Business

September 2018

Mentor®
A Siemens Business

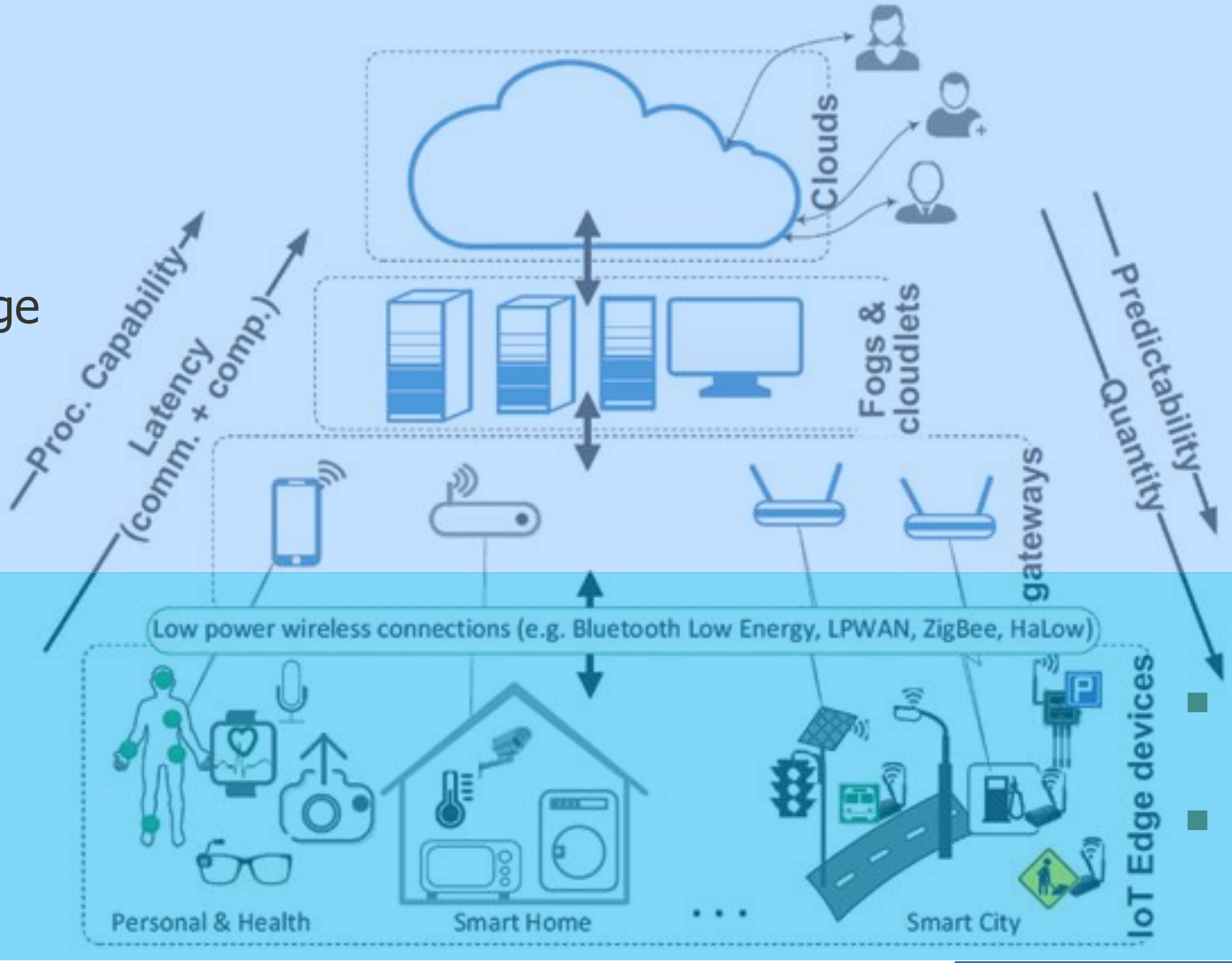
Outline

- Yield Challenges
- Scan Diagnosis Basics
- Data Sharing Fabless / Foundry
- Conclusions

Market Landscape and Challenges

Leading Edge

- Advanced nodes yield ramp (7nm-16nm), 300mm
- Challenged by large designs, in-cell complexity and defects



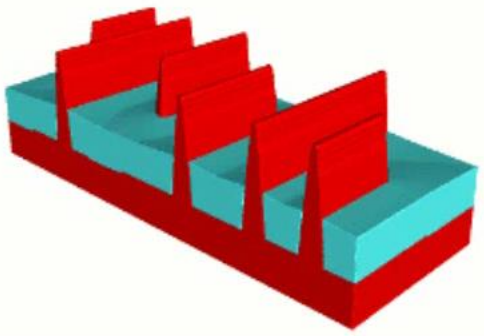
Mature

- Established nodes (≥28nm), 300mm/**200mm**
- Challenged by low cost, high volume, limited capacity

Figure 1: The layers of IoT computing and the communication between them. (Image: F. Samie, L. Bauer, and J. Henkel, "IoT Technologies for Embedded Computing: A Survey", in CODES+ISSS, 2016.)

Leading Edge Challenges: Complexity

- Big increase in transistor processing complexity 7/10/14nm nodes
  - "Myriads of systematic defects" for 10nm
  - "With 10nm the number of multi-patterning steps makes things much more complex"
  - "7nm is a disaster (because of the number of steps)"
    - "With 7nm it takes 21 days to go from M0 to M1, compared to 3-4 days in 14nm"
  - "90% of defects are inside cells"



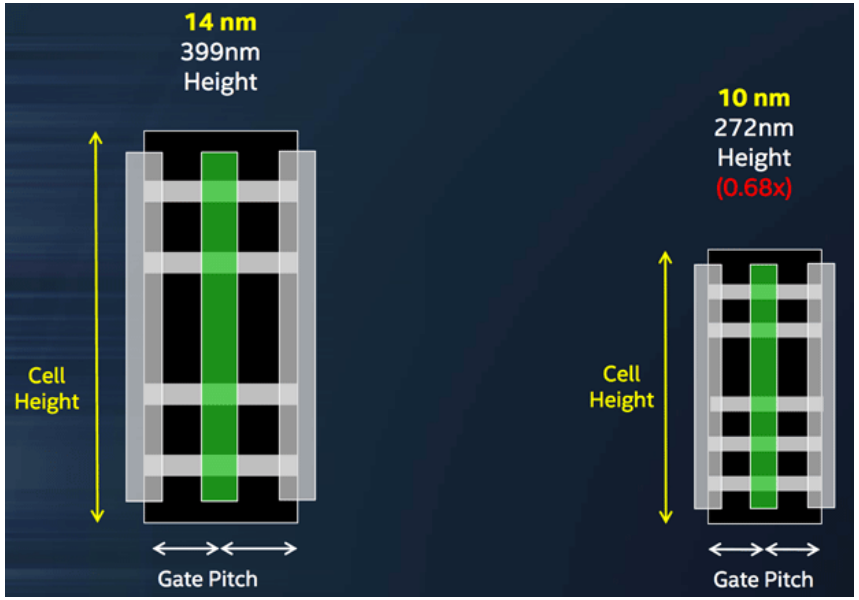
from Coventor Semulator3D

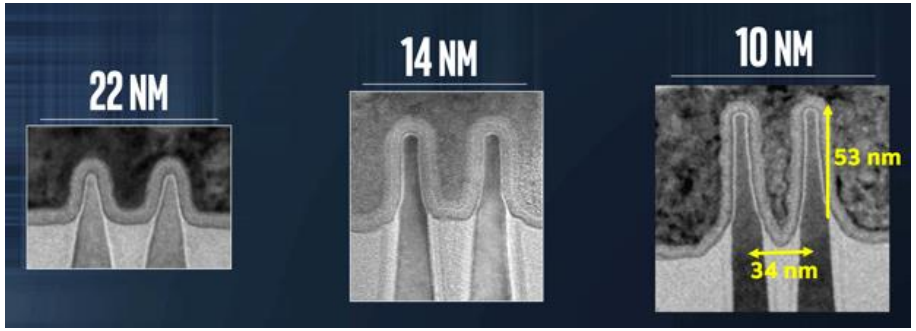
Advanced cells now have multiple layers included

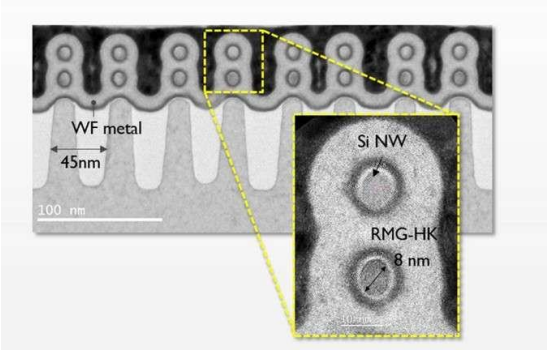
Old cell was only very first layers of the transistor

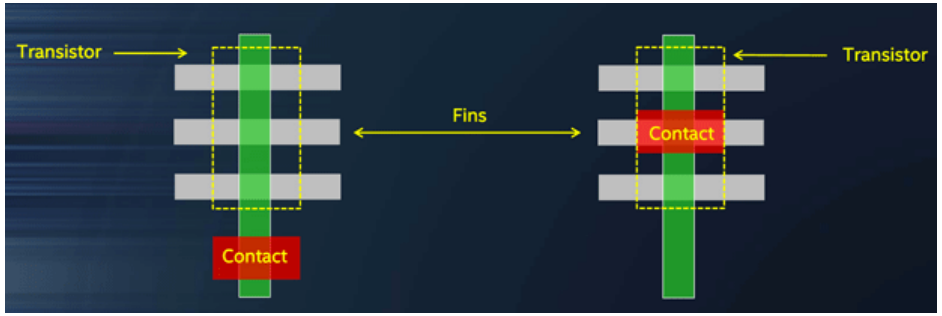
Leading Edge Challenges: Complexity

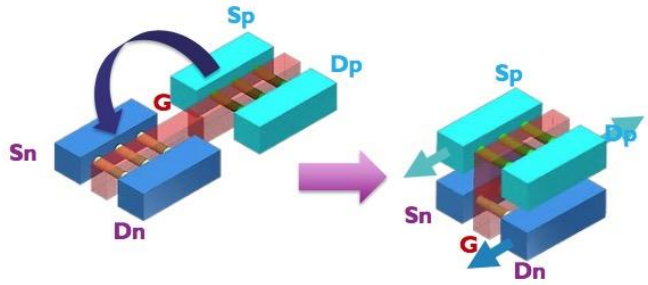
- Trend continues with future 5nm/3nm nodes
  - — Further scaling requires density increase in addition to pitch scaling











https://techreport.com/review/31660/intel-defends-its-process-technology-leadership-at-14nm-and-10nm/2

How to Solve Systematic Yield Issues?

Traditional Approach

Yield Monitoring

Selection

Physical Failure Analysis (PFA)

Diagnosis

Electrical and Physical Fault Isolation

Construction Analysis

Volume Diagnosis

Diagnosis Sampling

Low Yield (Scan)

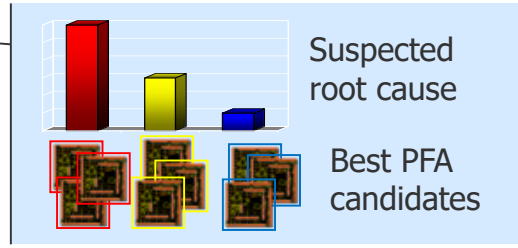
Diagnosis-Driven Yield Analysis

Layout-Aware Diagnosis

Statistical Analysis

PFA

Construction Analysis



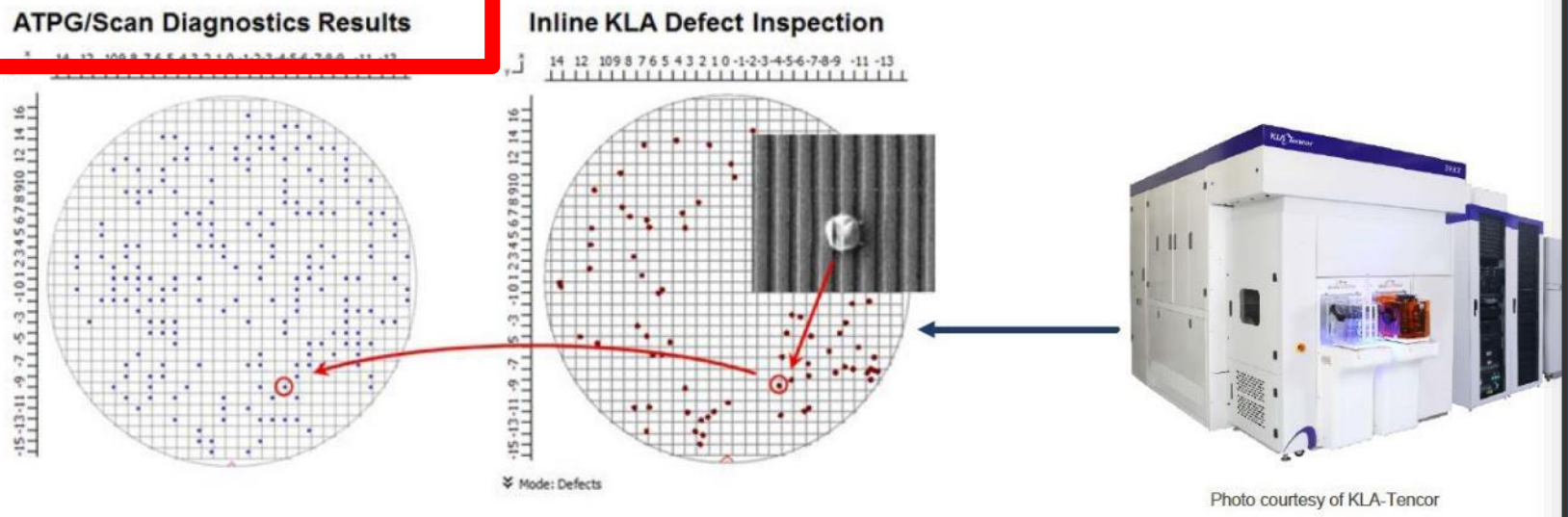
- Focus PFA on biggest yield hitters
- Increase PFA success rate
- Eliminate costly physical localization

Can we eliminate PFA altogether?

Data Sharing

Fabless-Foundry Information Exchange

- Beyond WAT data → Open sharing of more IN LINE data including KLARF



- Overlay of fab defect data to identify origin of mapped failing nets/cells.
- Eliminate need to PFA defects with a known source in fab
- Improves signal-to-noise ratio to identify outlier systematic defects thru PWQ's

W.J.Miller – ASMC 2017

Q: Why Volume Diagnosis?

A: Eliminate PFA altogether!

A: Reduce costs.

William Miller, VP Engineering, Qualcomm
ASMC 2017

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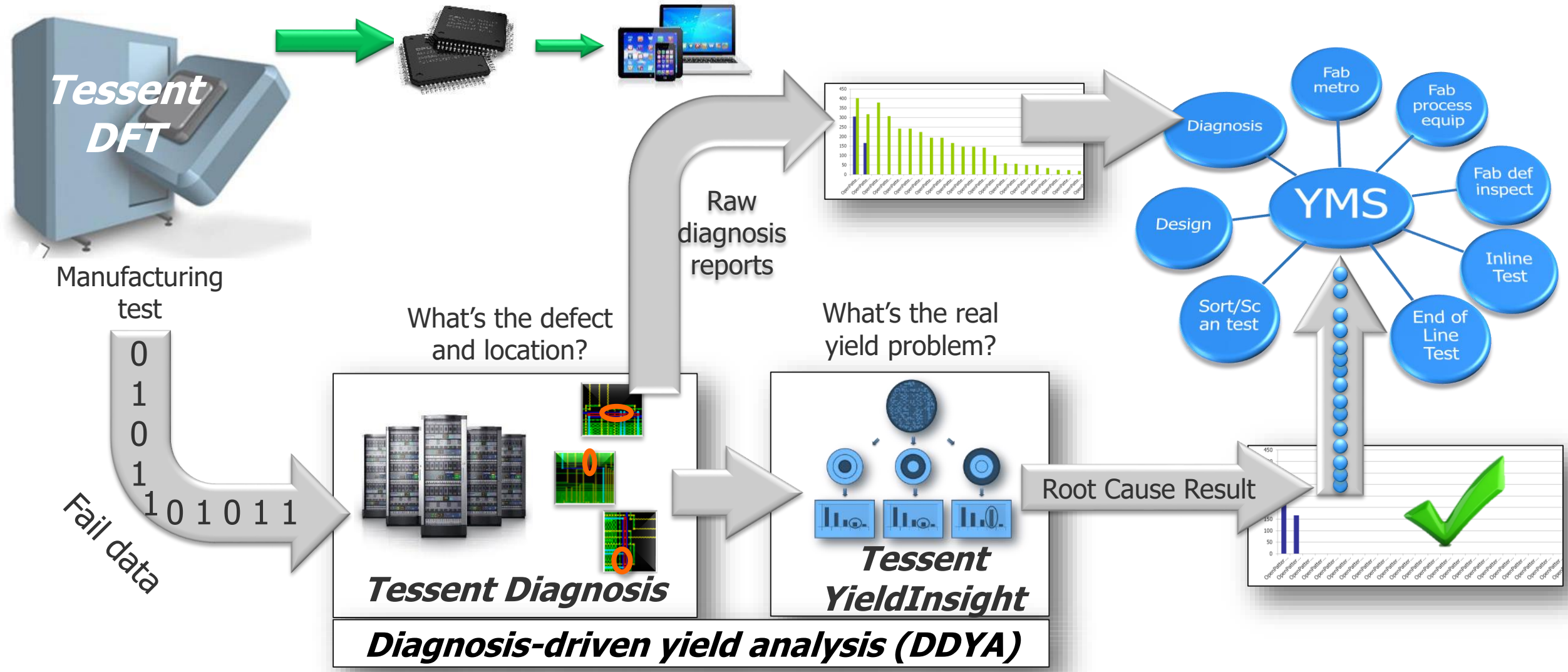
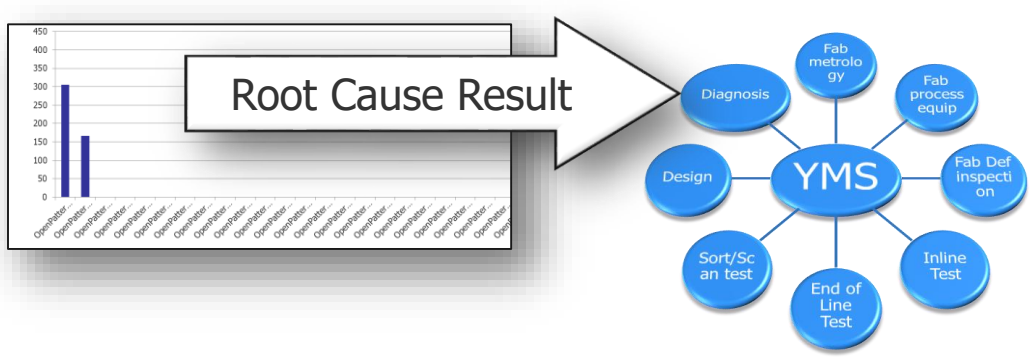
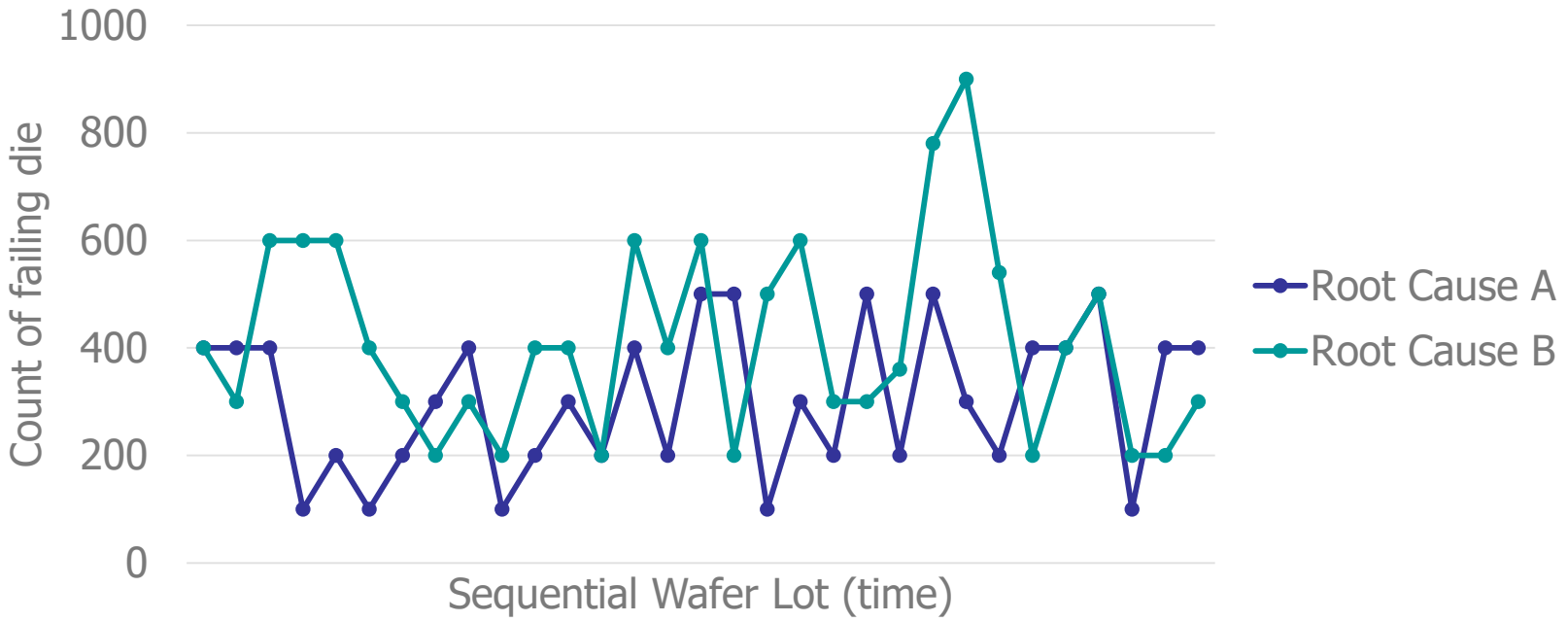
Leveraging Scan Test for Yield Learning



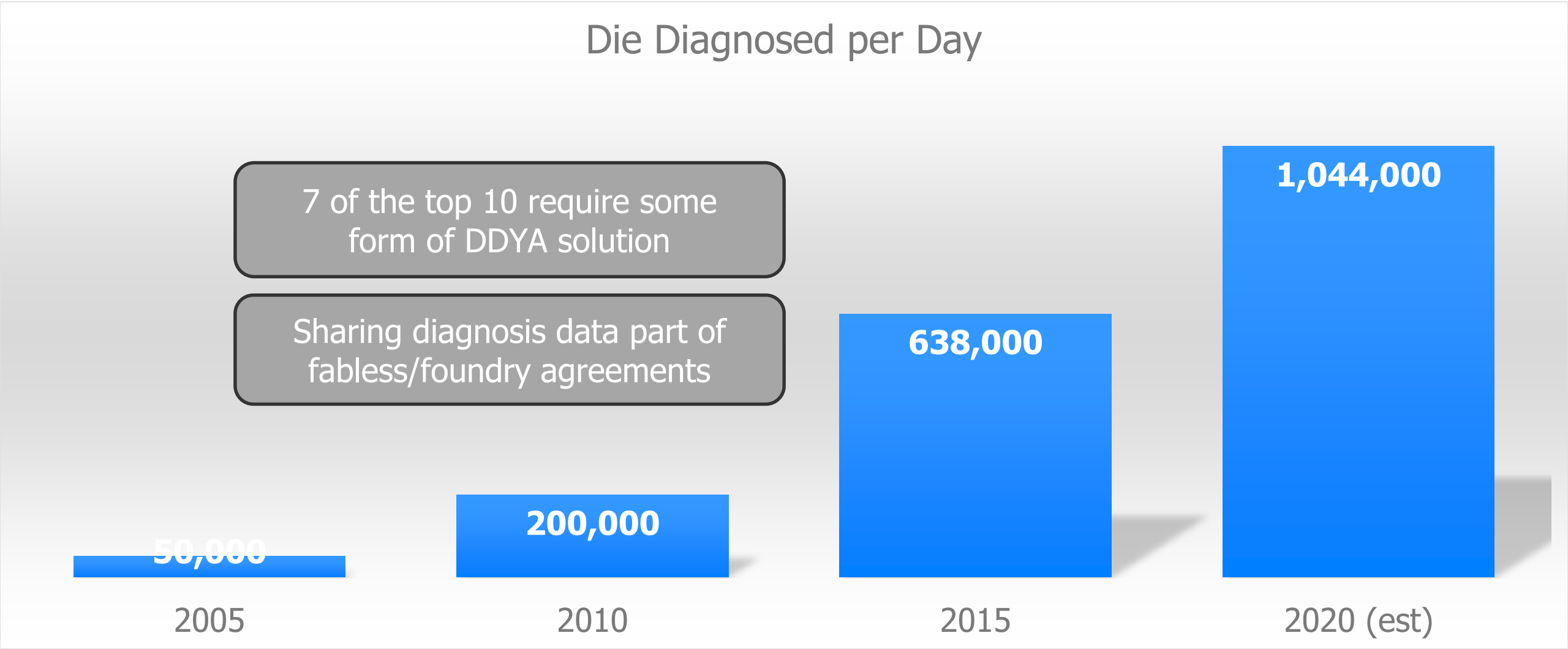
Why Diagnose All Fails?

- Monitor specific root causes over time to understand variability
- Accelerated excursion response
- Trigger outliers will drive response
  - Root Cause A→ etch equipment issue
  - Root Cause B→ pattern design marginality
- …Prevent excursions



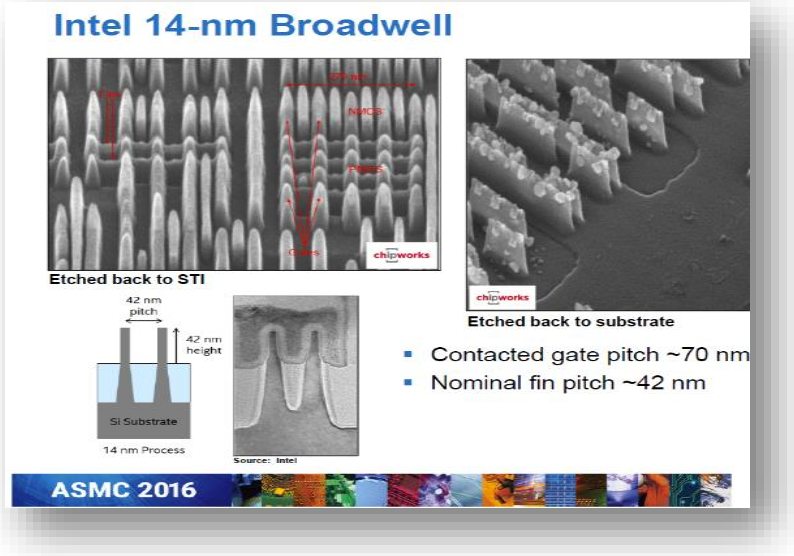


Industry Moving→100% Analysis of All Failed Die



Source: ITC 2016 plenary keynote: Dr. Wally Rhines https://youtu.be/A0K3rkWiXJo

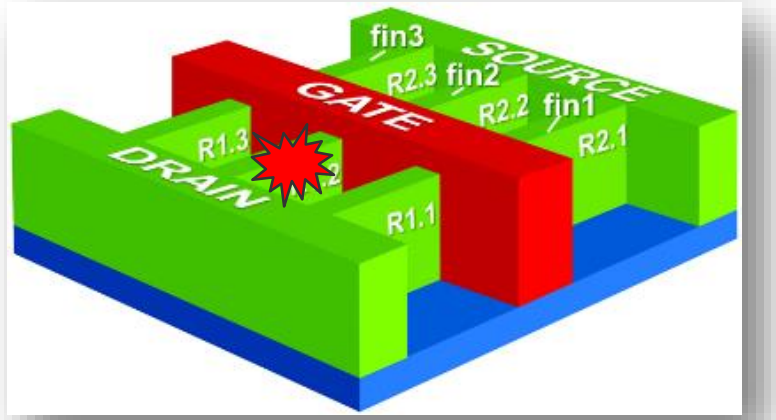
FinFET Requires More from Diagnosis than Planar



Accelerated critical dimensions

↓

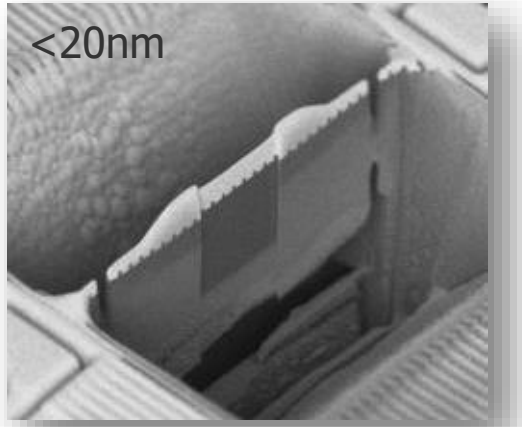
Increased number of cell related failures



Defects cause timing failures

↓

Diagnosis must consider intra-cell transition faults



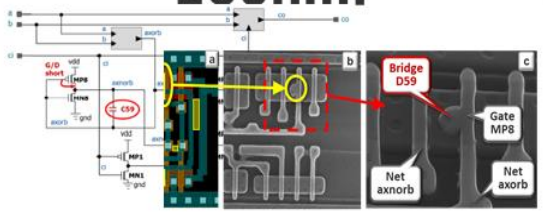
TEM 1-shot PFA

↓

Requires diagnosis resolution of one transistor

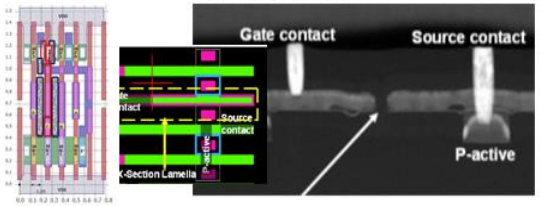
Tessent Cell-Aware Diagnosis
transistor level accuracy and resolution

160nm:

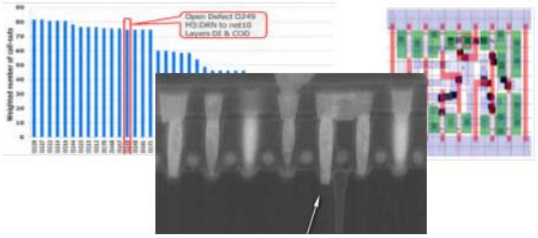


P. Maxwell, et. al., (**ON Semi**, MGC) "Cell-Aware Diagnosis: Defective Inmates Exposed in their Cells", ETS 2016

32nm:



F. Hapke, et.al, (MGC, **AMD**) "Cell-aware Production Test Results from a 32nm Notebook Processor", ITC 2012

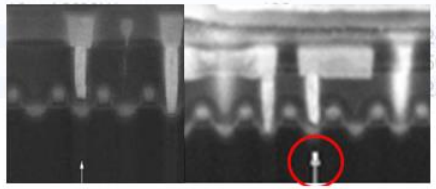


F. Hapke, et.al., (MGC, **AMD**, **GF**) "Improving FA for Cell-internal Defects through Cell-aware Tech.", ISTFA 2013

28nm:

Case	Cell	# Total cell-internal faults	# Suspects
1	FAX1	277	4
2	SFF1	350	13
3	INVX1	154	12
4	SFF2	323	48
5	NAND2X1	57	35
6	OAI22X1	123	13
7	OAI2[illegible]	[illegible]	9
8	SFF3	277	15
9	NAND2X1	57	9

11X resolution improvement



H. Tang, et.al., (MGC, **AMD, GF**) "Diagnosing Cell Internal Defects Using Analog Simulation-based Fault Models", ATS 2014

14/16nm FinFET:

Case	Cell	#Faults	#Suspects
1	CLKBUF	12	8
2	[illegible]	[illegible]	[illegible]
3	NAND3	81	6

12X resolution improvement

H. Tang, et.al., "Diagnosing Timing Related Cell Internal Defects for FinFET Technology", VLSI-DAT 2014

10 nm FinFET:

ITC 2016 PO 8:

Diagnosing Cell Internal Defects for FinFET Technology

Huaxing Tang[1], Dong Kwan Han[2], Wu Yang[1], Mohammed Abdelwahid[1], Stephen Park[1]

Mentor Graphics SAMSUNG

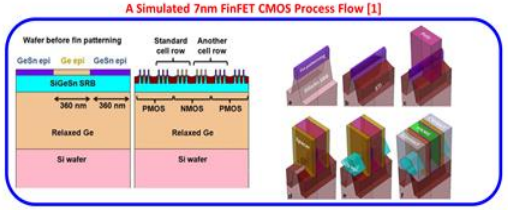
Challenges for FinFET Technology

- FinFET process is very sophisticated
- New process steps and materials are used for FinFET cells
- New cell internal defects are observed
- Yield ramp up is very challenging

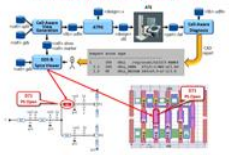
Proposed Solution

- Generate enhanced UDFM models for FinFET defects, e.g. intra-layer bridges, inter-layer bridges and exhaustive opens
- Run cell-aware diagnosis to accurately diagnose such defects
- Perform yield analysis based on volume CAD results

A Simulated 7nm FinFET CMOS Process Flow [1]

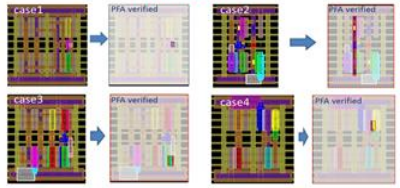


Cell-Aware Diagnosis Flow [2]



Diagnosis-Driven Yield Analysis

Experimental Results



[1] S. Gupta et al, "7-nm FinFET CMOS Design Enabled by Stress Engineering Using Si, Ge, and Sn", IEEE Tran. on Electron Devices, pp 1222-1230, 2014
[2] H. Tang, et al, "Diagnosing Cell Internal Defects Using Analog Simulation-based Fault Models", Proc. ATS, pp.318-323, 2014

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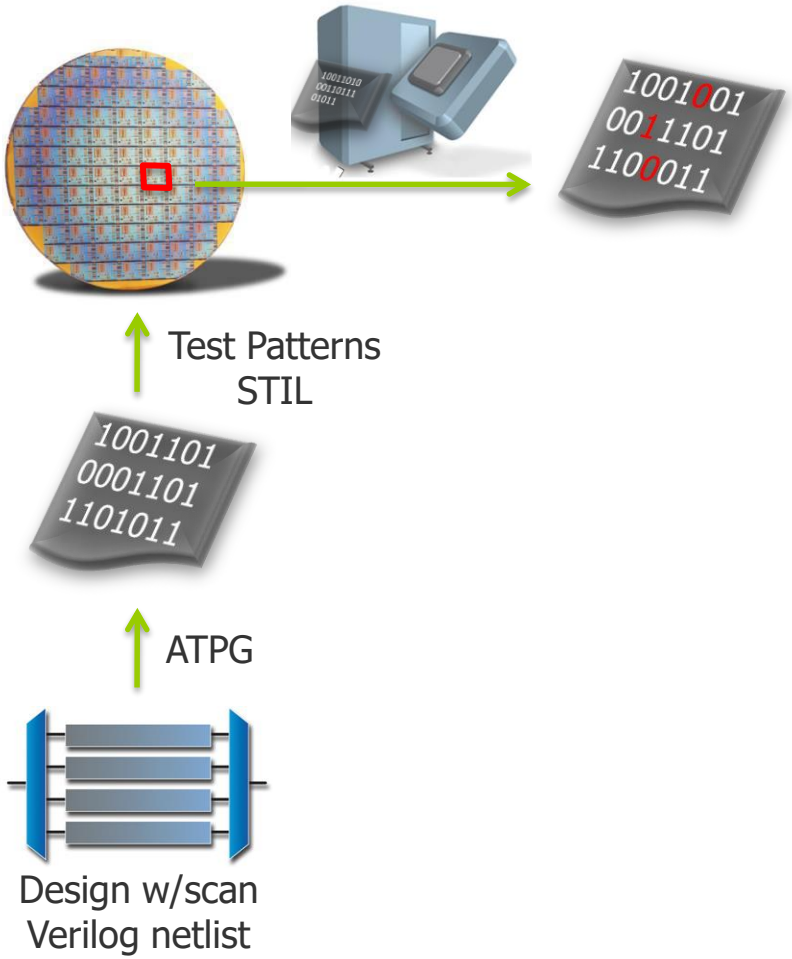
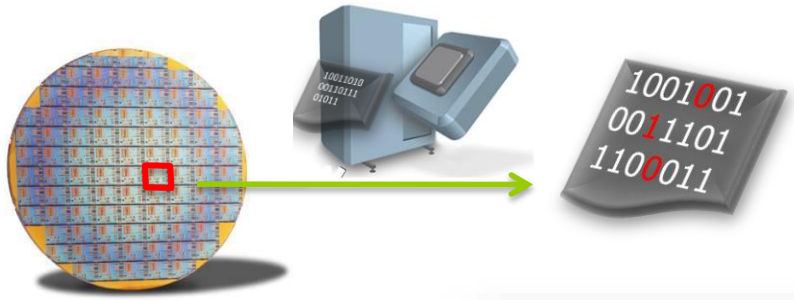
SCAN DIAGNOSIS BASICS

Scan Test

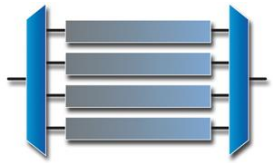


Scan test: How most digital ICs are tested

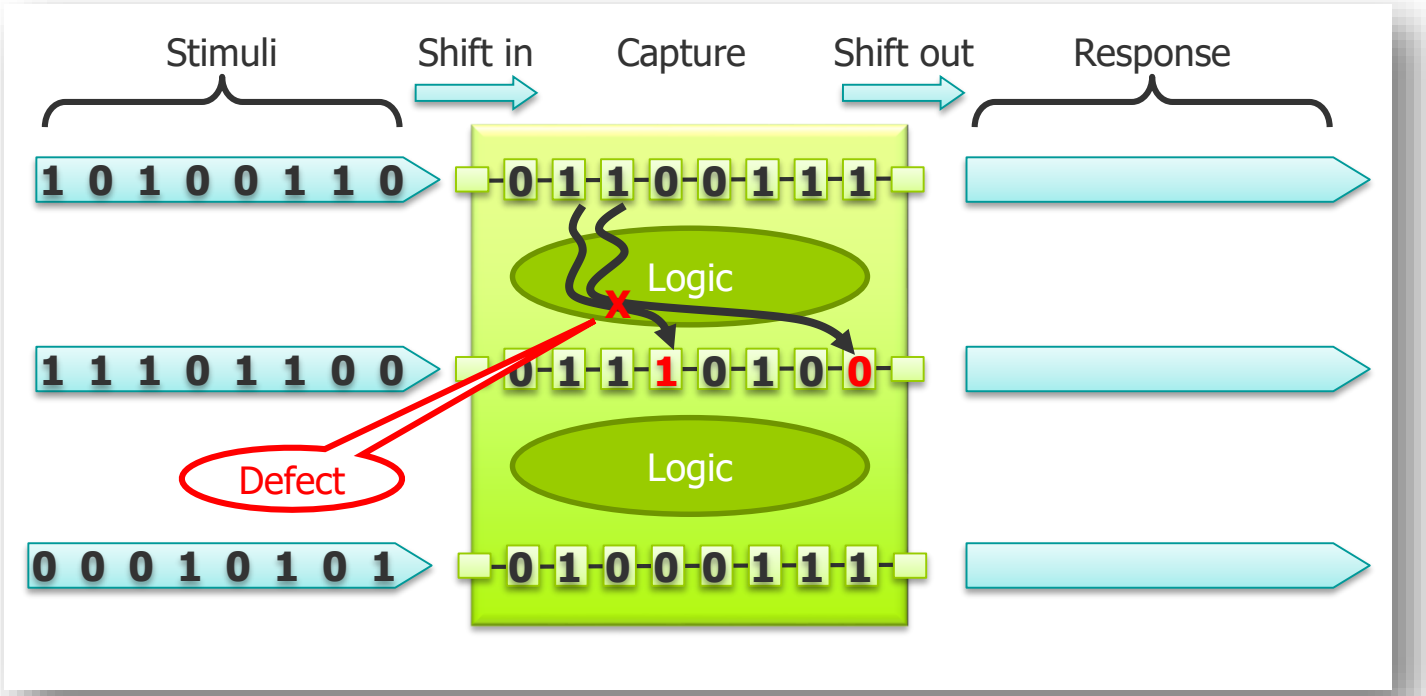


Test Patterns
STIL

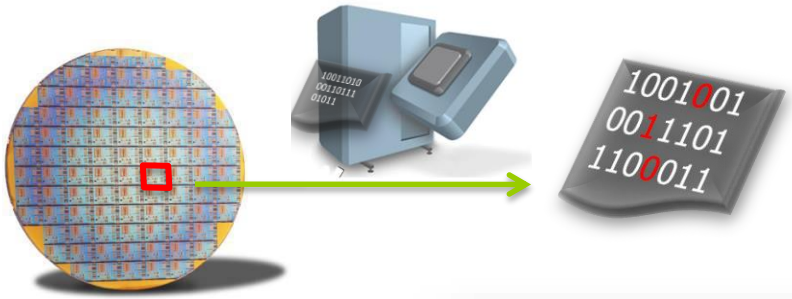
ATPG



Design w/scan
Verilog netlist

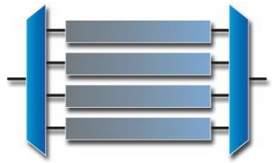


Scan test diagnosis: Software-based defect localization

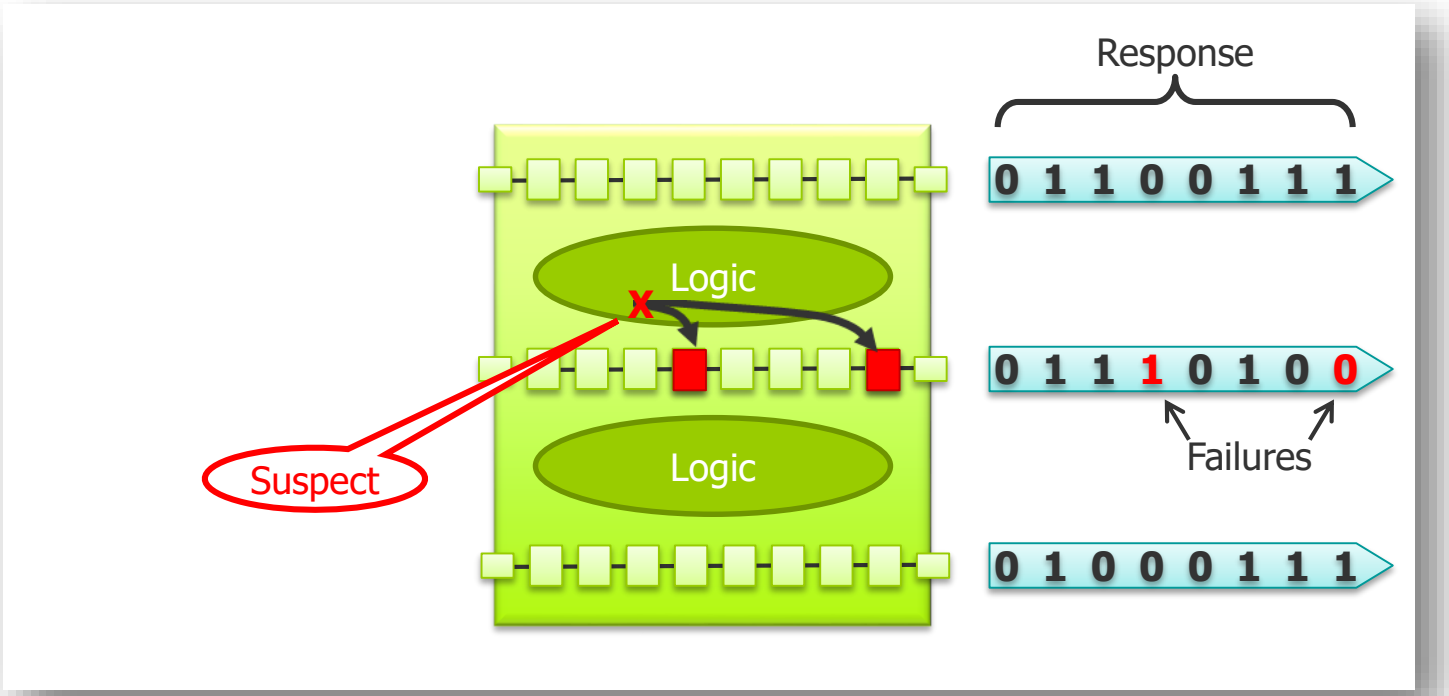


Test Patterns
STIL

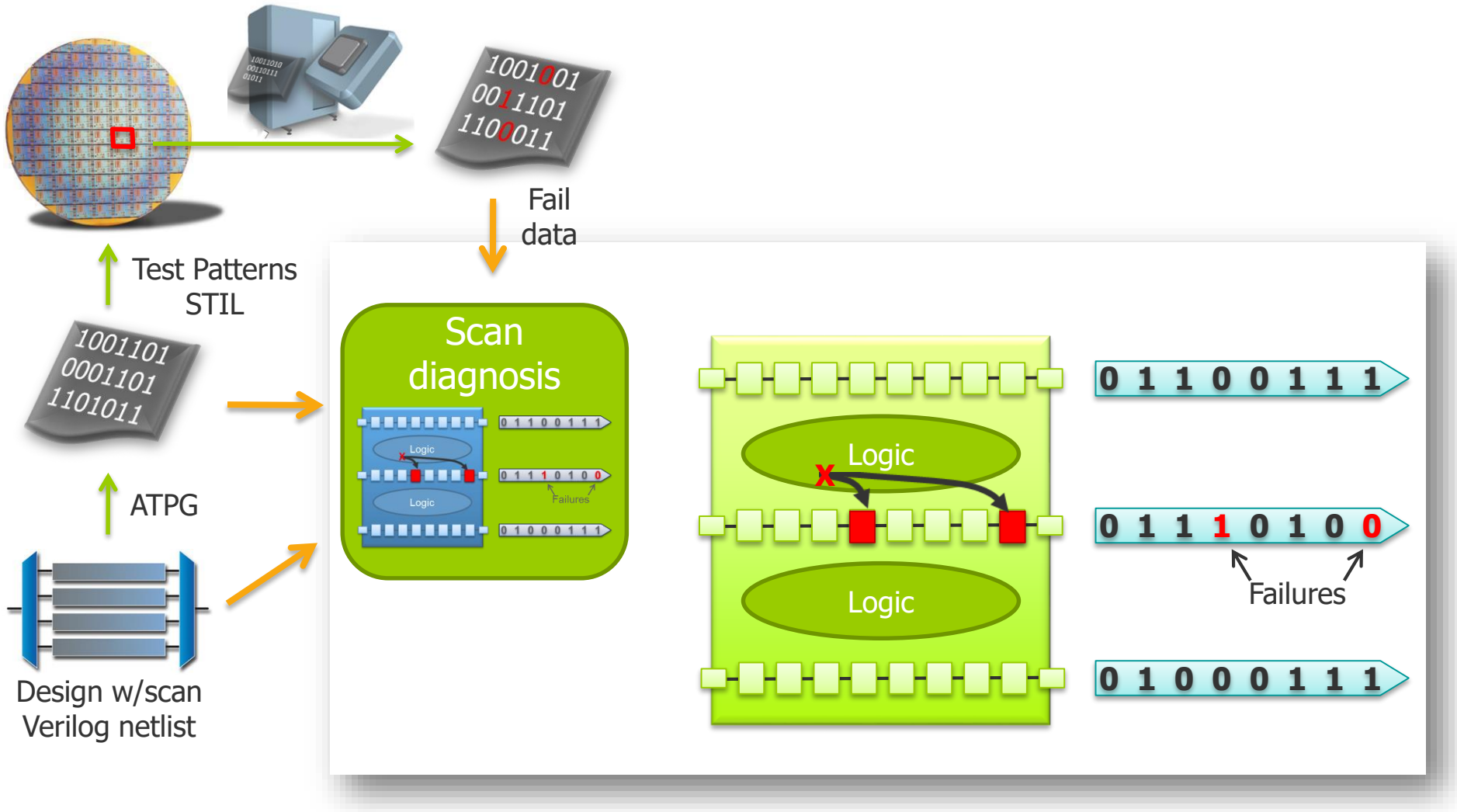
ATPG



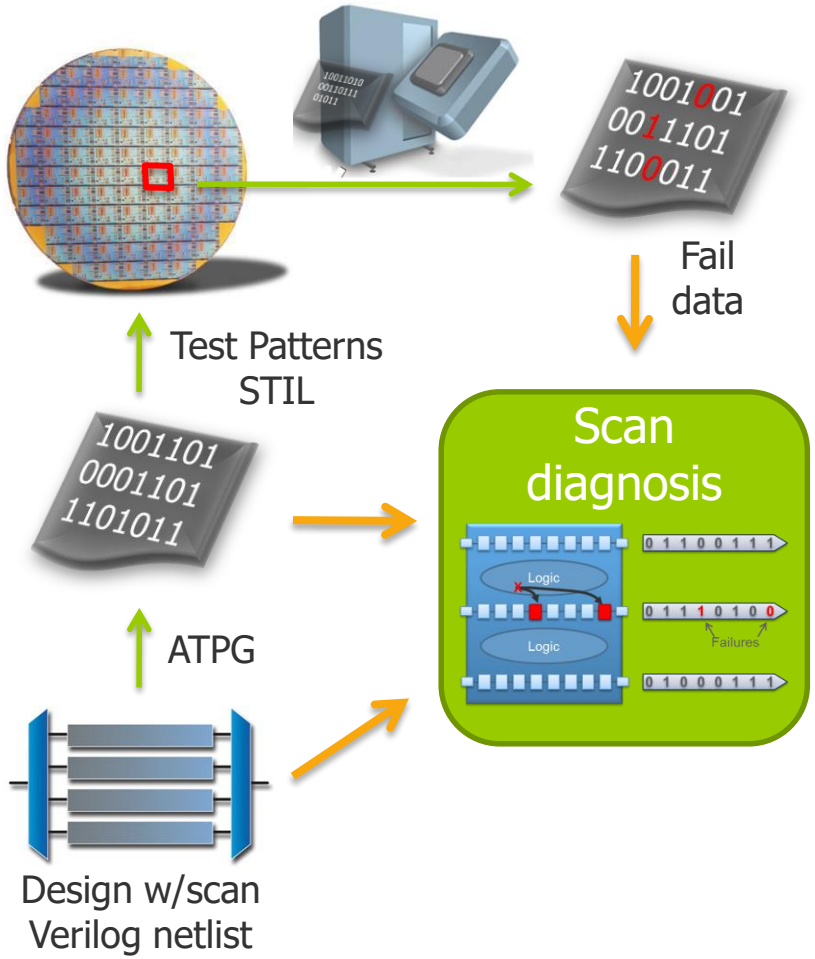
Design w/scan
Verilog netlist



Scan test diagnosis: Software-based defect localization

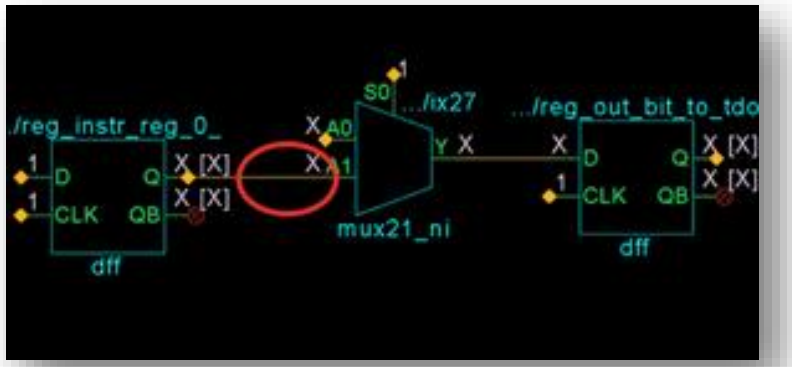


Traditional Scan Diagnosis



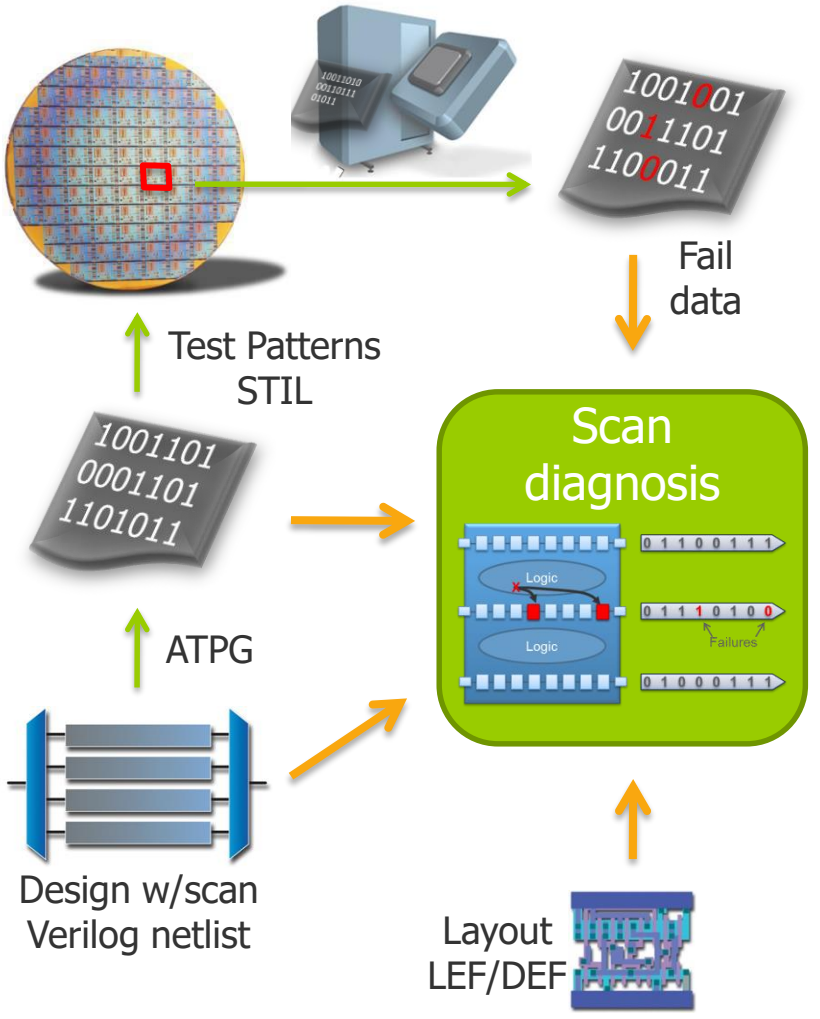

```
#symptoms=1 #suspects=4 CPU_time=21.39sec fail_log=fail1
#failing_patterns=164, #passing_patterns=99
symptom=1 #suspects=1 #explained_patterns=164
suspect score  fail_match pass_mismatch type    value  pin_pathname cell_name …
-------------------------------------------------------------------------------
1       100    164        0            OPEN/DOM both   /a0/m_1/m_55/B  NR2M2D
-------------------------------------------------------------------------------
```

Logic location (net and cell name)

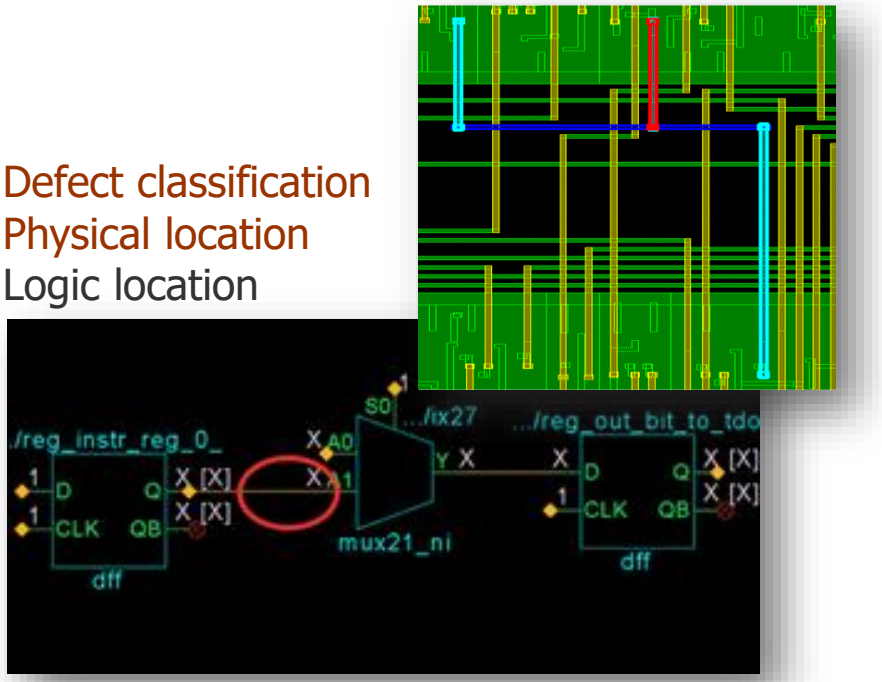


- Identifies logical failure and type
  - Nets – can be long
  - Bridges – might be unlikely due to physical proximity
- Poor classifications for yield analysis

Layout-Aware Scan Diagnosis



Defect classification
Physical location
Logic location



- Improves resolution
- Physical call-outs provide valuable classifications for yield analysis
- Reduced suspect area accelerates failure analysis (FA)

Diagnosis-Driven Yield Analysis

WHAT IS NEEDED?

Tessent Diagnosis Collateral

Tessent FastScan
Tessent TestKompress

Flat Model

Cell-Aware UDFM

Test Pattern Files

ATE

Failure Files

Tessent Diagnosis

Consistency Checks

Chain Diagnosis

Logic Diagnosis

Physical Data LEF/DEF

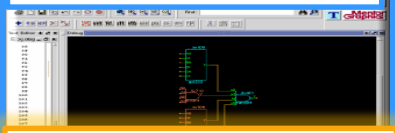
Diagnosis Report

Marker File (optional)

Views

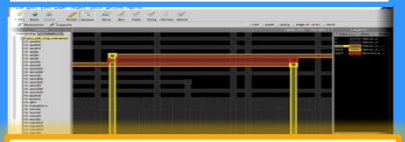
Defect Classification

Logical View



DFTVisualizer

Physical View

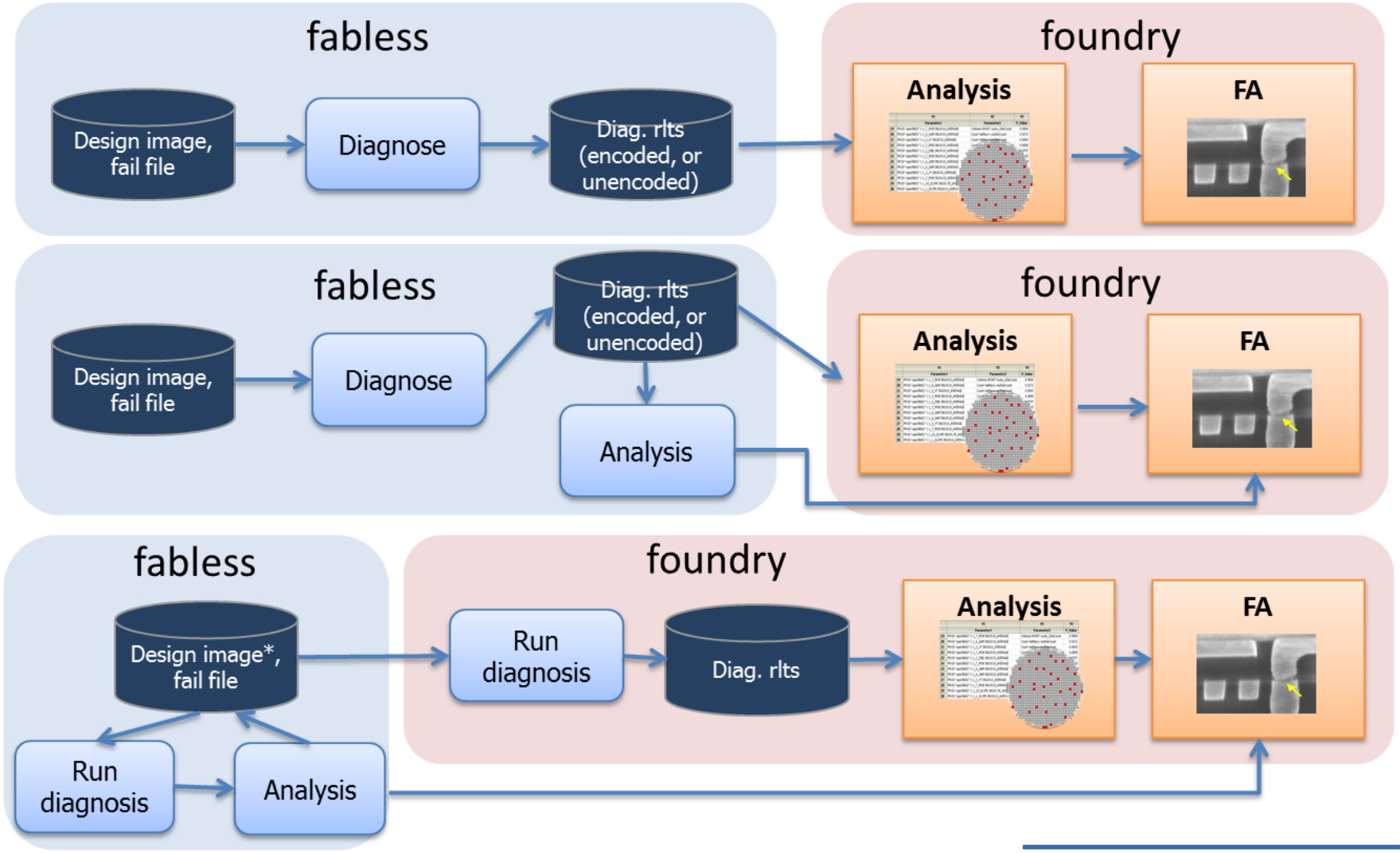


YieldInsight ®
Calibre ®

Scan Diagnosis Input Requirements

- Logical design data
  - Design netlist/data
  - ATPG settings and constraints used to generate the test patterns
- Scan Patterns
  - Cycle-based scan pattern formats – WGL or STIL
  - Pattern-based scan format – ASCII
- Failure file (log) formats
  - Cycle based failure log for cycle-based patterns
  - Pattern based failure log for pattern-based format
  - STDF (v4-2007) supported via DlogUtil converter tool
- Physical design netlist
  - LEF and DEF for design

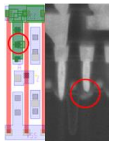
Proven Data Flows…one size does NOT fit all



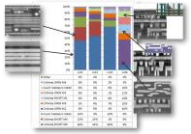
Foundry Successes

"Diagnosis-driven yield analysis is an **established yield-learning methodology** at GLOBALFOUNDRIES for **test chips** as well as for yield ramp of **customer products**" TDF 2011

"The diagnosis resolution for cell internal defects is improved by **11.3X** on average" ATS 2014

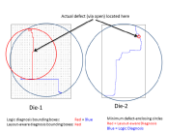


"RCD determine **the underlying root causes** represented in a population of failing devices from **test data alone**" IEEE D&ToC, 01/12

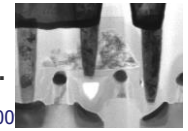


"Mentor and Samsung are also leveraging production test diagnosis by exchanging information between the Tessent tools and the Calibre Pattern Matching facility to **quickly identify and eliminate design-specific yield limiting features** during design ramp up." Press release 2012

"The use of design layout information during diagnosis … **directly results in more die becoming suitable for PFA**" ISTFA 2011

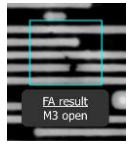


"Our experience shows that using scan **chain diagnosis** … PFA hit rate is over **80%**." ATS 200



"Fixing this problem **improved baseline yield about 8%**. It is impossible … with the traditional method." ElectroIQ, Nov 2011

"Layout-aware diagnosis … directly translates into **improved FA success rates** and turnaround time." EDFA, 5/2010



Recognition

"The addition of DFM-aware yield analysis helps us and our customers to separate design-and process-related yield limiters, and reduces the time to find the root causes of yield loss. We can also use the technology to optimize DFM rules to address specific customer needs."

- Thomas Herrmann, MTS product engineer, ***GLOBALFOUNDRIES***

"Using the statistical analysis features of Tessent YieldInsight we are able to identify yield issues in days as well as determining the impact of process modifications."

- Davide Appello, Design-to-Test Engr. Manager, ***STMicroelectronics***

"We have found that Mentor's unique chain and at-speed diagnosis capabilities accurately diagnose failing die and can effectively pin-point problem areas within the die, even when the problem is internal to a cell, which is very important for physical failure analysis."

- Shauh-Teh Juang, Sr. Director of Design Infrastructure Marketing, ***TSMC***

"By incorporating critical area analysis (CAA) and volume scan test diagnosis in our yield analysis process, the physical failure analysis cycle time is significantly reduced and the impact of each PFA is significantly higher, allowing us to take faster corrective action."

- Kyu-Myung Choi, VP Infrastr. Design Center, System LSI Division, ***Samsung Electronics***

EDN Hot 100 2009

EDN Innovation Honoring Excellence in Electronics WINNER 2009

DesignNews Golden Mousetrap Best New Products Awards 2011 FINALIST

BEST IN TEST

Best in Test finalists

http://www.mentor.com/company/news/

Conclusions

- Leading edge process nodes challenged by new levels of in-cell complexity.
- Scan diagnosis provides unique, actionable information on systematic yield limiters, reducing PFA cycle time.
- Volume diagnosis can help avoid PFA and reduce costs.

- Where there's a will (value) there's a way.
- **Data sharing among fabless/foundry/tester is always a challenge and worth it to both fabless and foundry.**

THANK YOU!