Efficient HW/SW Co-Design & Validation of Complex Emerging Systems

Pre-silicon Prototyping Tools, Flows and Methodologies (TFM) for a first-pass silicon success!

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Presentation Outline

- System Design & Validation Challenges
- Pre-Silicon Prototyping TFMs
- Explore, Optimize and Validate
- Co-Optimization for First-Silicon Success

“Linksters” Driving Complex Emerging Systems!

Have you heard of the Linksters?

AUTONOMOUS VEHICLES | AR/VR | 5G NETWORKS | ARTIFICIAL INTELLIGENCE

Who are the Linksters?

- Everyone born post 2002 (iPad Era) ➔ fully digital life ➔low tolerance to technology problems of any magnitude!

Emerging System Characteristics

- Smart (AI, Deep Learning)
- Connected (AON, AOC, 5G)
- Safe (security; ~750M hacks/day)
- Blazing user response (Perf/Watts)
- Yearly Refresh (2X Perf @ same cost)

Systemic complexity growth explosion!

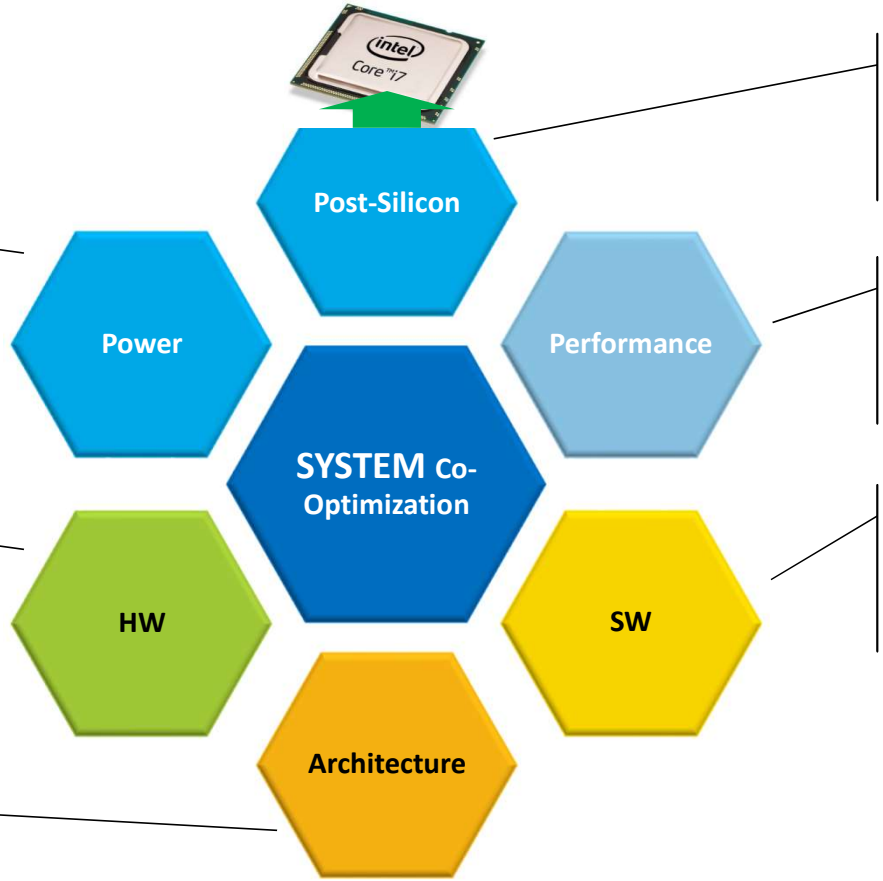
Innovation is moving at a *scarily fast* pace!

Emerging System Design Challenges – simplified

Avg/Peak Power Estimation and Analysis

High-levels of Integration (sensors, IO, SS)

Architectural Exploration with HW/SW tradeoffs



First silicon success! Silicon re-spins ➔ TTM

Performance Analysis with real/representative work-loads

SW Readiness (FW/BIOS/OS/Drivers/Apps)

Structured Design Methodology with cross-domain optimization is critical to design efficiency

HW/SW Co-Optimization Pre-Silicon Shift-Left

EXPLORE → OPTIMIZE → VALIDATE

Pre-Si TFM Suite:

HW Design & Validation:

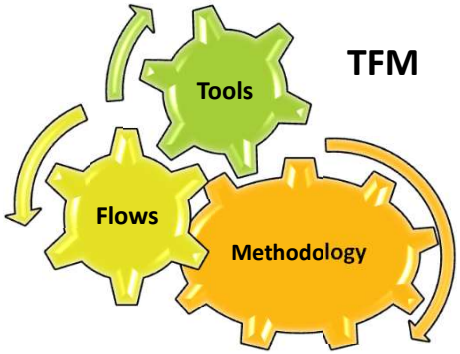
- Simulation, Emulation

SW Design & Validation:

- Virtual Platform

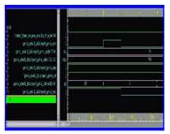
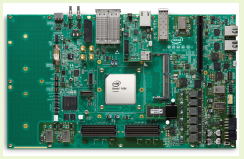
Co-Optimization:

- Emulation
- FPGA
- Hybrids



Pre-Silicon Co-Optimization Shift Left is foundational to Product Development Efficiency

Pre-Silicon Prototyping Tool Portfolio

	Simulation	Emulation	FPGA	Virtual Platform
				 
Application	find logic bugs	Find complex system-level bugs; Si bug reproduction, PnP, FUSA	IP-level FW development, real-world devices	HW/FW/SW co-dev and integration
~~Accuracy~~	RTL	RTL	RTL	registers/ behavioral
~~Speed~~	~10-100 Hz	~500hz - 2 kHz	10-100 Mhz	50-500+ Mhz
Cost	$	$$$$	$$	$
Scale	IP, SS, SOC	Mega IP, SS, SOC	IP, SS, SOC subset	IP, Platform

Effective Pre-Silicon TFMs are critical to managing emerging design complexity

Pre-Silicon Prototyping Typical Applications

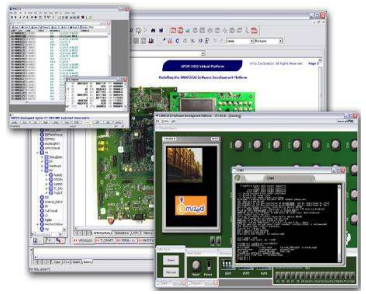
Platform	What it is:	Objectives
Virtual Platform	VP for FW/SW Development	Boot Android, Windows, IP level FW Development and Validation & System SW/driver development.
FPGA Platform	FPGA HW platforms	Real-world devices/sensors with FW, BIOS, OS and Driver development with real use-cases.
N-1 FPGA Hybrid	Silicon tightly coupled with new logic in FPGA	Architectural exploration with real application-level workloads in a real world env (full FW+BIOS+OS+Driver+SW applications).
Emulation Platform	Emulation Platforms	Validate all IPs, Sub-systems and SoC HW – focused on HW Validation, Power Estimation and Performance Analysis.
Hybrids	VP tightly coupled with Emulation/FPGA	Provides full system context to HW under test

Prototyping ➔ Virtual Silicon➔ Early Customer Enabling/Engagement

Virtual Platform: Quick Intro

Basics:

- Fast, System-level models, “real world IO”
- Short development time, full visibility, runs prodn sw



Typical Industry uses:

- FW, SW Development primary vehicle, Boot OS, run real SW workloads
- Early collaboration with customers/partners
- Hybrids to provide system-level context for Emu/FPGA

Challenges:

- Very high abstract models – more details slow down

Emulation: Quick Intro

Basics:

- RTL, UPF, TB and collaterals transformed to a “virtual silicon”
- 3 types – FPGA, Custom FPGA, Custom processor type emulators from 3 big EDA Vendors .

Typical Industry uses:

- SoC, SS, IP Functional validation where simulator runs-out-of gas
- Directed and synthetic validation content; mfg test-scan, reset flows
- HW/Software Co-Validation, Global System Flows (Boot, Reset, Scan)
- Power and Performance Estimation & Analysis

Challenges:

- Cost, Long Model TAT

FPGA Prototyping: Quick Intro

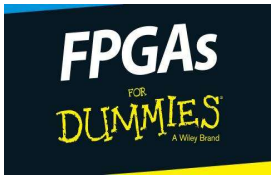
Basics

- Vendor Tools transform RTL to FPGA Bit-stream ➔ Downloaded to FPGA HW
- Many HW Board Vendors; Fewer SW FE Tools; BE provided by FPGA Provider
- New tools: emulation like ease-of-use to enable “prototyping for validation”

Intel Stratix FPGA Family

Typical Industry uses:

- Traditional FPGA Prototyping: FPGA vs. ASIC trade-offs (Industrial, embedded)
- Emerging Uses: AI, ADAS, New/Dynamic algorithm implementations; CPU Co-Die
- SW Stack Validation, Real World Device, OS-Based Validation ➔ Focus Areas



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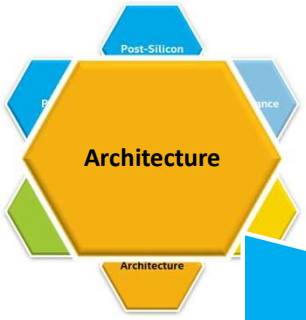
Challenges:

- Time-to-First Prototype (TTFP), Model TAT, Debug, effort intensive
- Limited to 8-12 FPGA Capacity, Expanding to FC, HSIO Enabling (e.g. PCIE)



Architecture Exploration for Emerging Ideas

Virtual Platform

System-Level Simulation

- Models Platform-level HW (CPU, Storage, etc.)
- Runs Real SW Workloads
- Fast iterative idea exploration – dream it, simulate it

HLS

Unit-Level Implementation

- System-C/C++ Model for unit under exploration
- Fast Simulation
- HLS Tool handles uArch details
- High Productivity
- Targets RTL for Emu & FPGA directly

Emulation/FPGA

HW-SW Co-optimization

- HW/SW Co-Validation
- Interface to real-world devices
- Run system-level flows
- Performance & Power Analysis

VP + HLS + FPGA Prototyping ➔ perfect for creating new smart products with disruptive architectures like AI

FPGA Prototyping: Concept to Product Fast Path

FPGA SoC

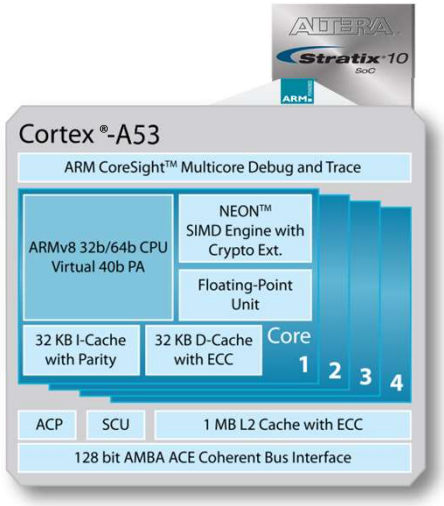
64-bit CPU+User logic➔ Dynamic HW+SW Algorithms

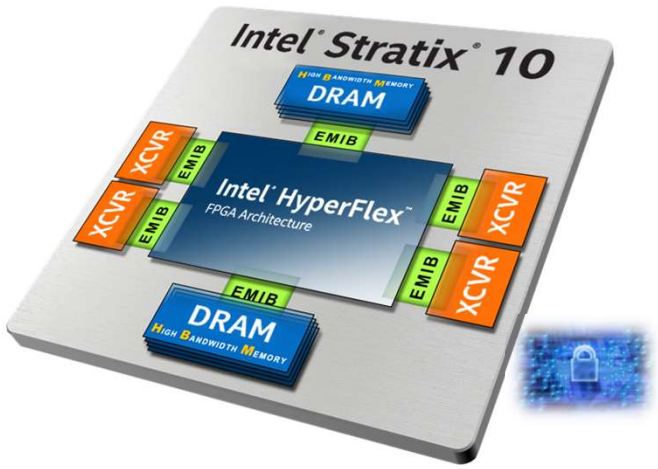
FPGA HBM DRAM

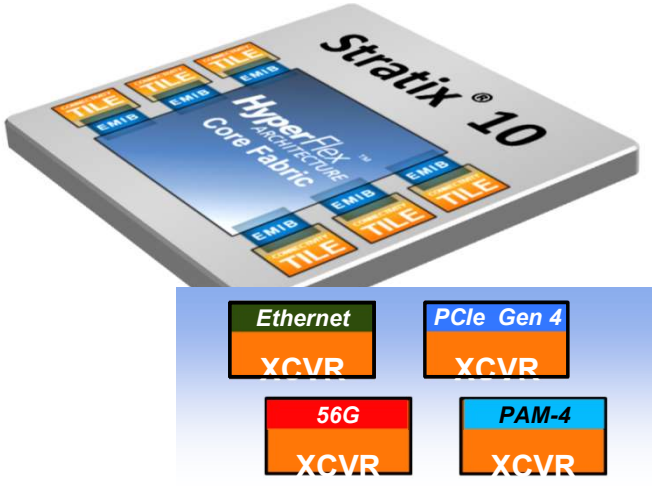
Security, Memory bandwidth, for data-intensive ideas

FPGA High-Speed IO

Full systems (with IOs) for evolving protocols/standards

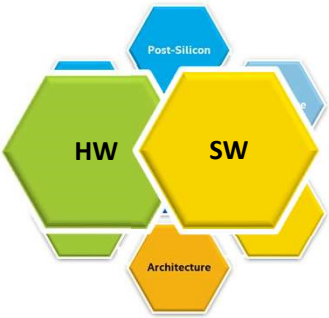


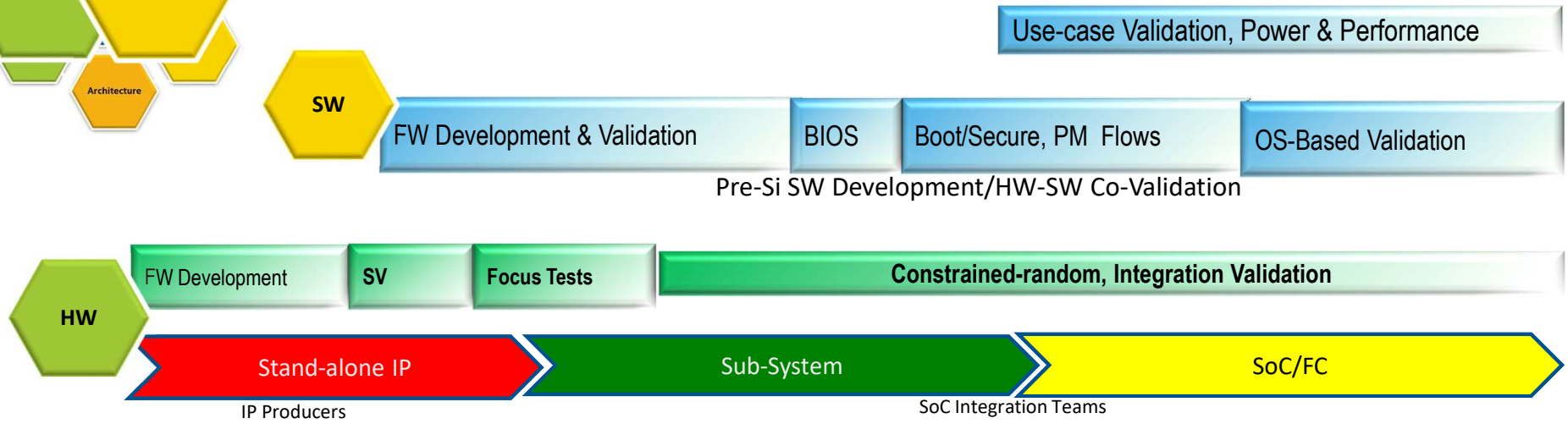


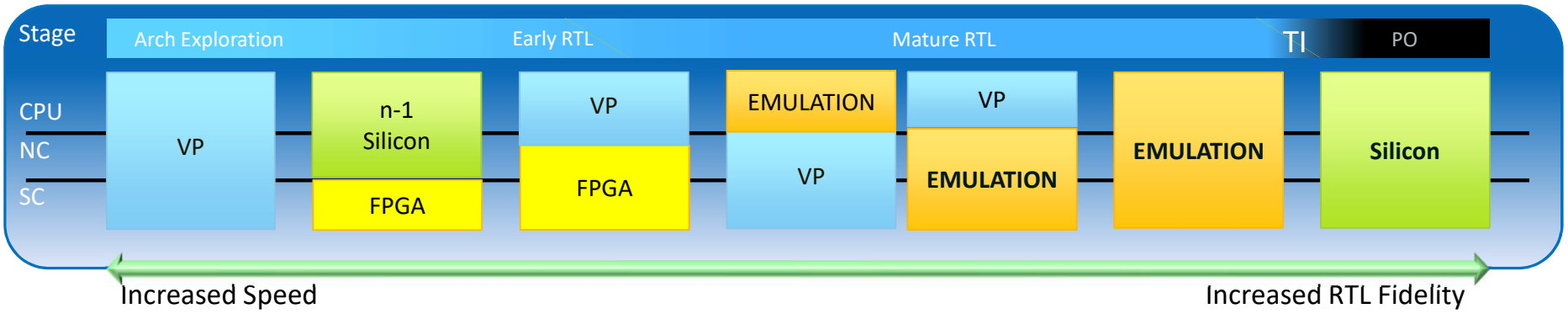


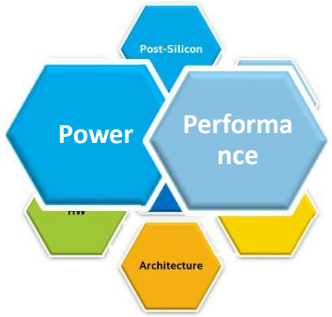
Security, Performance and Flexibility to replace low-volume ASICs for dynamic new market segments

HW/FW/SW Co-Optimization



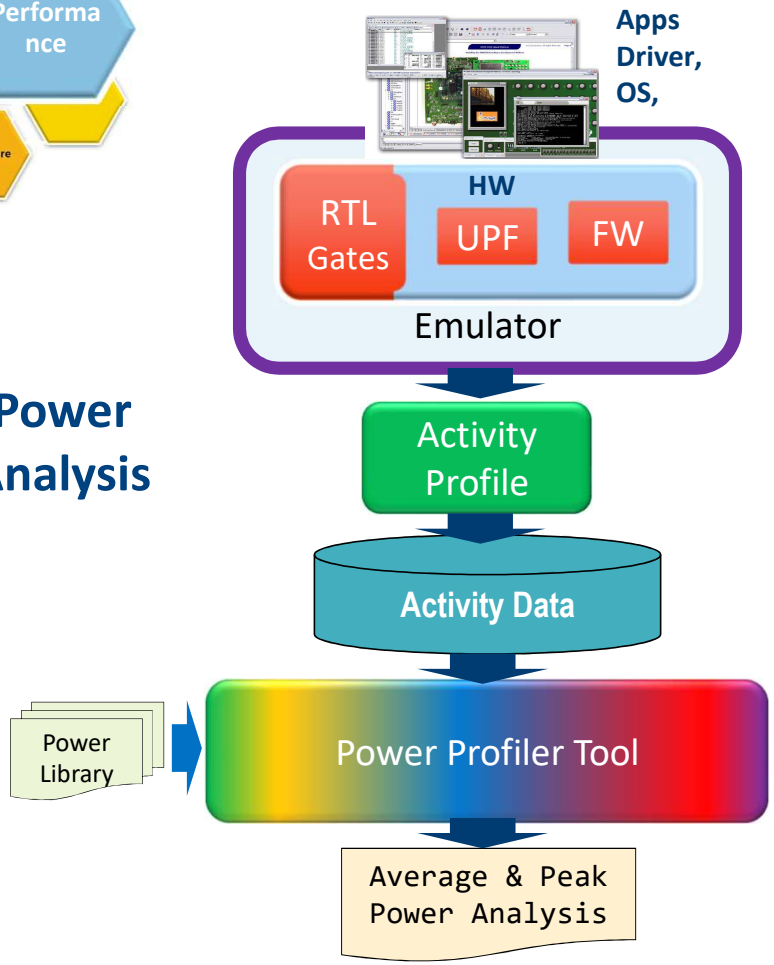






Power & Performance Analysis

Power Analysis

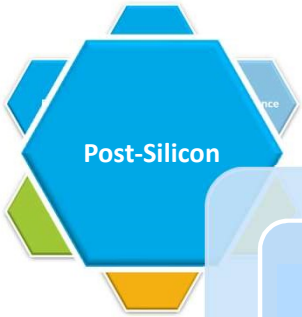


Performance Analysis:

- Similar approach/setup to Power Analysis
- Instrument models with perf counters in design
- Run real workloads
- Capture Data for entire workload

Smart Query and GUI help visualize and flag performance issues:

- Latency, Backpressure, Bandwidth issues



Optimizing Post-Silicon for Faster Product Launch

Power-On Readiness

- HW/FW/SW Readiness for PO
- Silicon Validation Content Readiness
- SV Debug Tool Readiness
- No blocking bugs

Manufacturing Readiness

- DFX Validation
- Scan Validation
- Gate-Level Emulation
- Reset/Boot Flows

Debug & Fix Validation

- Reproducing Si Bugs
- Use full-visibility on emulation to root-cause Silicon Debug
- Bug-fix validation

Primary vehicle: Emulation

Reducing Post-Silicon phase for a faster TTM

Summary

- Linksters driving vicious cycle of systemic complexity growth
- Cross-domain optimization is crucial to product development!
- Suitable application of Prototyping TFMs is key to high RoI
- Effective Pre-Silicon HW/SW co-optimization is key to First Silicon Success and TTM!
- FPGA Prototypes can help you fast track concept to products

Inventing the Future

Others predict the future. At Intel, we're building it.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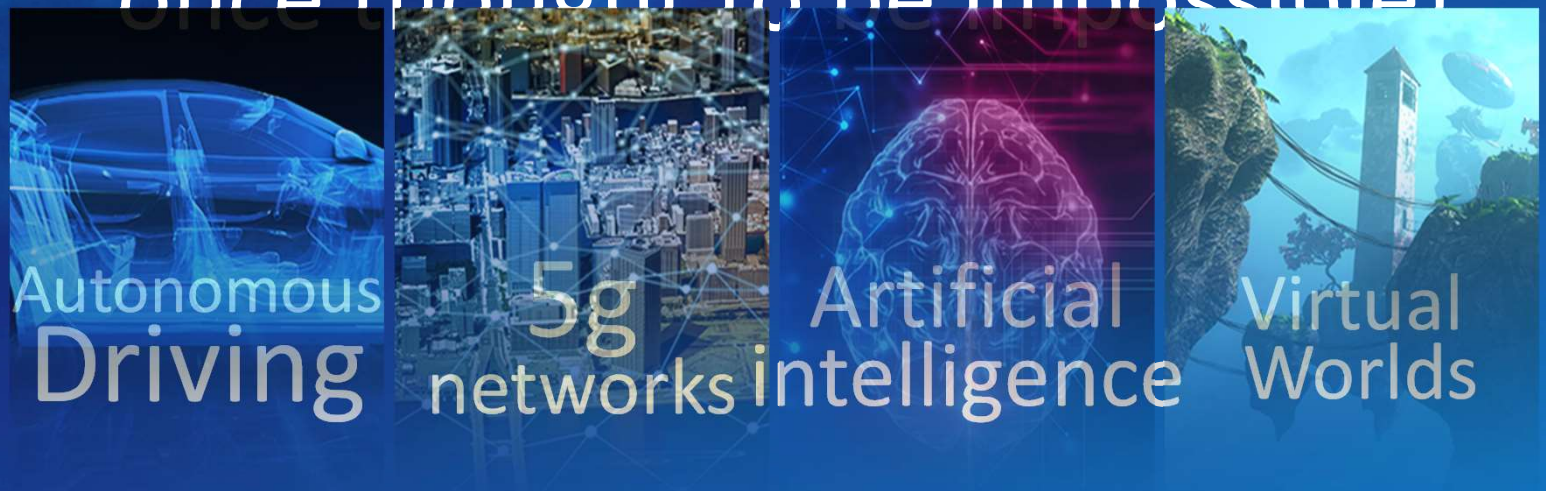
BACKUP

At Intel

We’re EMpowring the LINKSTERS BY DELIVERING experiences once thought to be impossible!



Products that awe tough-to-please Linksters!

Wind River® Simics®

Maximize software development velocity by using virtual hardware in a virtual Lab

With Intel Wind River® Simics® you can simulate anything, chip to system, and get the access, automation, and collaboration tools required for Agile development practices.

Simulate anything, Chip to system

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What CAN you Do with Simics

Experiment
DREAM IT. SIMULATE IT. VALIDATE IT.

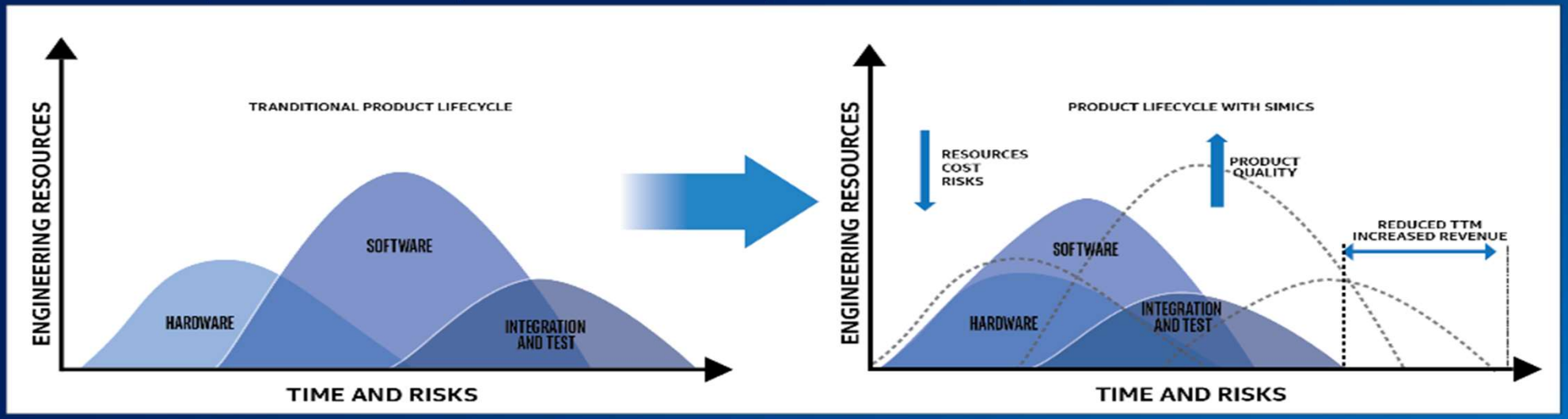
DEBUG
HUNT FOR BUGS AT ANY TIME

SHARE
EMPOWER ALL COLLABORATORS

TEST & RUN
NO NEED TO STAND IN LINE

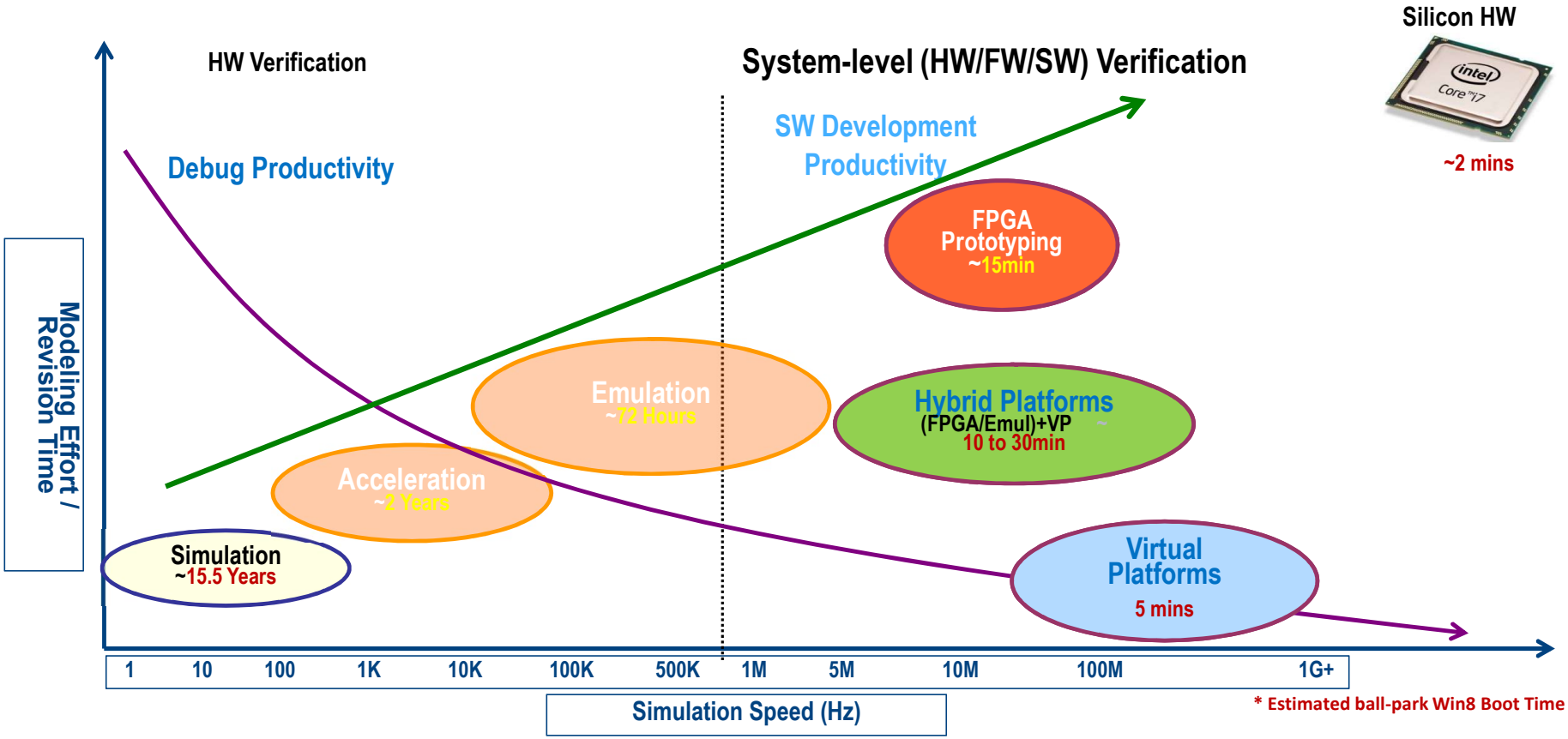
Configure
ENDLESS CONFIGURATIONS WITH EASE

DEVELOP
DEVELOP ON THE ACTUAL SYSTEM FROM THE START



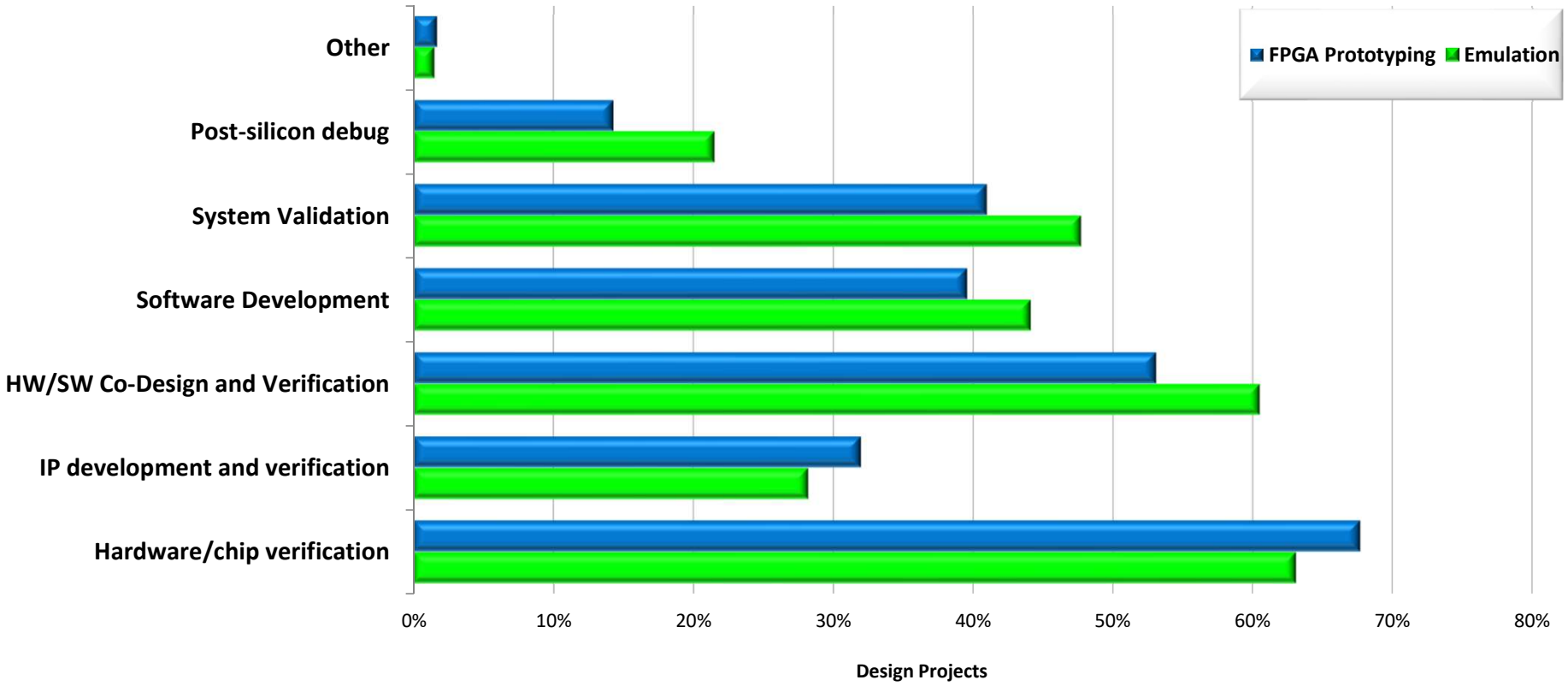
on-demand access to any target system, so that you can create and deliver better software faster

Pre-Silicon Prototyping Tool Profile



Understanding Capabilities and Limitations of each Tool is key to Prototyping success!

Industry Usage of Emulation & FPGA Prototyping

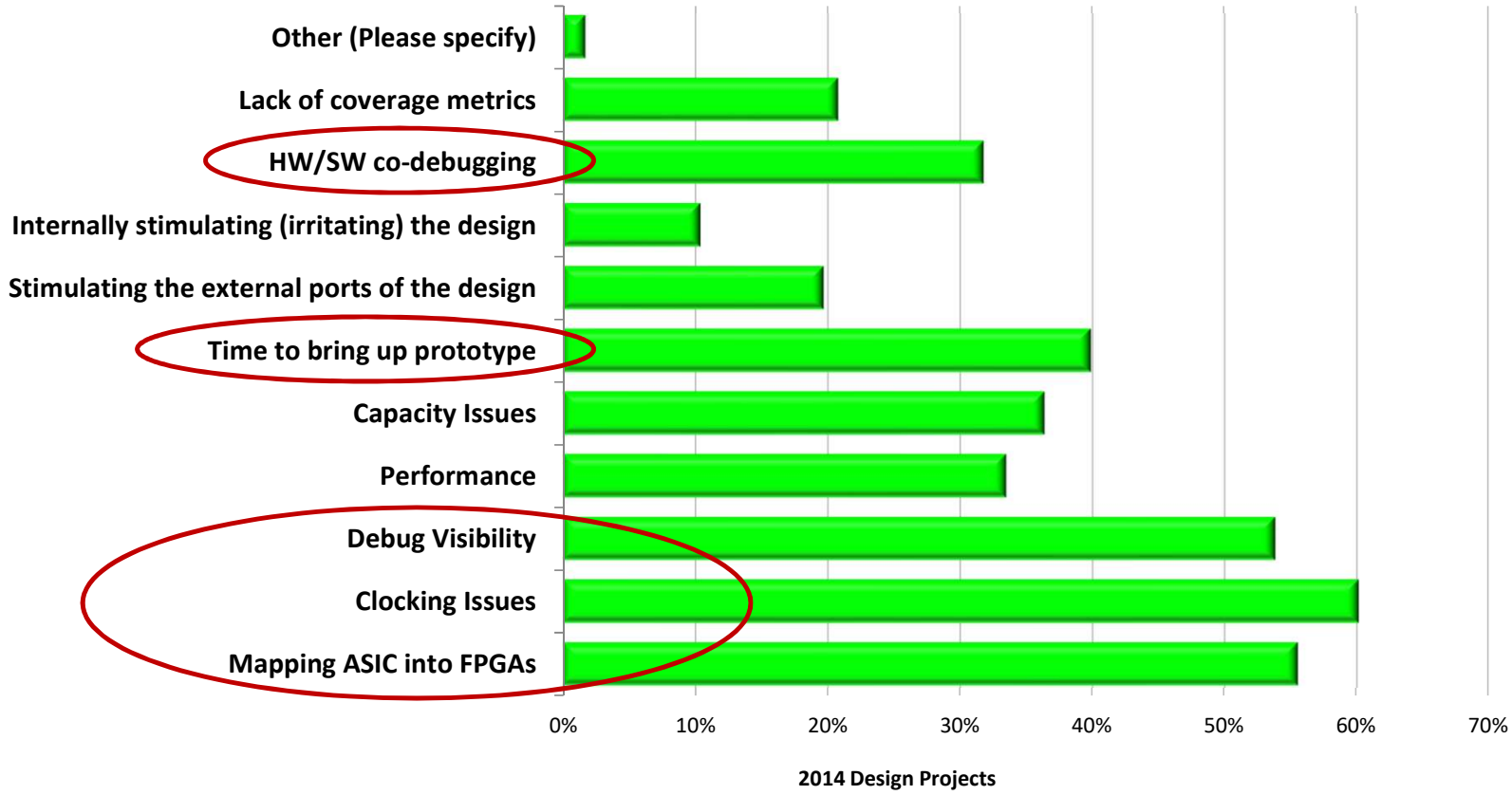


Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

FPGA Prototyping Vs. Emulation

Features	FPGA Prototype	Emulation
General:		
Capacity Expandability	Good	Very Good
Memory Capacity	Very Good	Good
Ease of use	Low	Very Good
Cost	Low	High
Model Build Efficiency:		
Compile Time	OK	Very Good
Model Size	Smaller	Bigger
RTL Flexibility	OK	Good
Test bench support	OK	Very Good
Simulation Efficiency:		
Simulation Speed	Very Good	Good
Save/Restore	No	Very Good
IO Expandability (PCIE,Ethernet etc)	Very Good	Good
Debug Efficiency:		
Signal Visibility	Limited	Very Good
Waveforms w/o re-run	No	Very Good

Industry FPGA Prototyping Challenges



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

Abstract

Advancements in silicon and software technologies have paved the way for highly complex, interconnected systems targeted at emerging applications in Mobile, AI, ADAS, VR, and IoT. The design and development of these complex systems calls for a tightly coupled HW/SW co-design shift-left to eliminate costly silicon re-spins and reduce TTM. This presentation will share deployment and successful leverage of pre-silicon Emulation and FPGA Prototyping technologies that accelerates the much needed paradigm shift for an efficient and effective validation of system HW and SW Stack(FW, BIOS, OS & Apps). I will share suite of pre-silicon prototyping TFM solutions and their relative strengths with guidance on their applications throughout the system development cycle while maximizing RoI. I will also share game-changing applications of prototyping technologies that drives architectural, software, security, and power management explorations that are at heart of new products in the fast evolving market segments like AI.

FPGA Platform Basics