# Welcome to EDPS 2018 Electronic Design Process Symposium www.ieee-edps.org

Shishpal Rawat, IEEE





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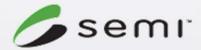




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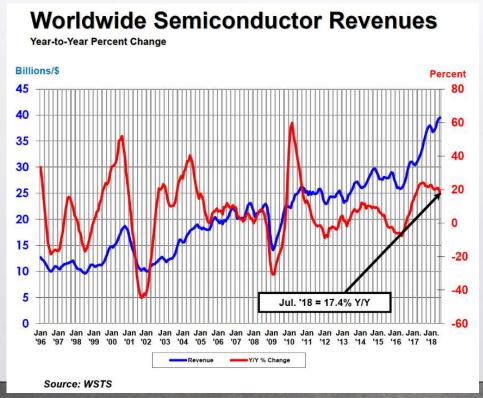


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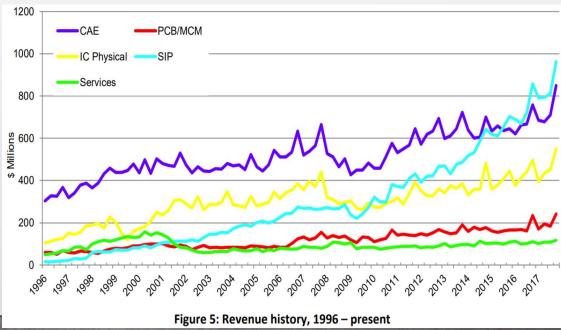
And special thanks to Jim Hogan and Bob Smith

# Future of our Industry – Bright



### World Wide EDA/SIP Revenues

**Source ESDA** 



# EDPS – In its 25<sup>th</sup> edition

2<sup>nd</sup> year in the valley (after 23 years in Monterey)

Continues to address the current challenges of our industry

- Establish closer ties between Design, Test & Manufacturing
- New technologies to enhance performance even with slow down in "transistor scaling"

Working closely with professionals & academia in the field to modernize tools and methodologies

## Your EDPS Committee

2017 2018

Aparna Dey

Claria Reila v

Camille Kokozaki Devangkumar Jariwala

Darshan Patra Don Draper

Dwight Hill

Herb Reiter Huafeng Yu

John Swan John Swan

Naresh Sehgal Naresh Sehgal

Shishpal Rawat

Norman Chang

Rawat Rawat

Ramond Rodriguez

Steve Grout Shishpal Rawat

Vivek Joshi Steve Grout

Vivek Joshi

Chris Bailey

# EDPS 2018 Agenda

EDPS 2018		Presenter / Session Chair	Company	Talk Title		
Thu Sep 13						
8:00 AM	M Breakfast, Registration and Networking					
8:45 AM	Opening	Shishpal Rawat	IEEE CEDA	Welcome & Introduction		
9:00 AM	Keynote	Chris Rowen	BabbleLabs	The Deep Learning Revolution: From Theory to Impact		
9:50 AM		Break				
10:00 AM	Session 1		In	novative Design Techniques		
		Ramond Rodriguez, Devang Jariwala	Intel Corp.	Session Chairs		
10:00 AM		Patrick Groeneveld	Cadence/Stanford	EDA in the Age of Machine Learning		
10:25 AM		Balachandran Rajendran	Dell EMC	Machine Learning in System Design and EDA		
10:50 AM		Rohit Sharma	Paripath	Exploring Machine Learning for EDA		
11:15 AM		Joonyoung Kim	NVXL Tech	Design Flow for Machine Learning FPGA		
11:40 AM		Jai Kumar	Intel Corp.	Efficient HW/SW Co-Design of Complex Emerging Systems		
12:05 PM				Lunch		
1:00 PM	Keynote	Andrew Kahng	UCSD	Evolutions of EDA, Manufacturing and Design		
1:35 PM				Break		
1:50 PM	Session 2	Smart Manufacturing				
		Herb Reiter, Don Draper, Chris Bailey	eda2asic, Consultant, Univ of Greenwich	Session Chairs		
1:50 PM		Tom Salmon	SEMI	Smart Manuf:Convergence,CoDesign,CoOptimization,Supply Chain		
2:20 PM		Wilfried Bair	NextFlex	Flexible Hybrids Design, New Challenges, New Opportunities		
2:50 PM		Matt Knowles	Mentor	Connecting Advanced Manufacturing Test to Design, Fab and Final Product Yield for Complex FinFET Defect Challenges		
3:20 PM		Dave Armstrong	Advantest	Device Manufacturing in the Era of Neural Networks		
3:50 PM				Break		
4:15 PM	Session 3		System Reli	ability for ADAS, AI, 5G and Photonics		
		Norman Chang & John Swan	Ansys, Intel Corp.	Session Chairs		
4:15 PM		Di Liang	HP Labs	Integrated Photonic Interconnect Reliability for Datacom Applications		
4:45 PM		Amisha Sheth	Intel	5G Validation Process & Challenges		
5:15 PM		Ritesh Tyagi	Infineon	Functional Safety Architecture Challenges to Achieve Failsafe Operation in ADAS/AD Applications		
5:45 PM		Norman Chang	Ansys	Achieving 5G/ADAS/AI Reliability for Advanced FinFET Designs		
6:15 PM				Break		
6:30 PM	Dinner & Panel	Bob Smith	ESDA	Jim Hogan interviews Amit Gupta (Mentor Graphics): Crossing the Chasm: Building a Startup to a Successful Exit		

Fri Sep 14						
8:00 AM		Breakfast & Networking				
8:45 AM	Keynote	Simon Johnson	Intel	Confidential Cloud - HW based Security		
9:30 AM		Break				
9:45 AM	Session 4 CyberSecurity					
		Naresh Sehgal & Huafeng Yu	Intel Corp., Boeing	Session Chairs		
9:45 AM		Gang Qu	Univ of Maryland	Polymorphic Gates and Their Applications in Hardware Security		
10:15 AM		Alessandra Nardi	Cadence	Functional Safely for Semiconductor Designs		
10:45 AM		Ujjwal Guin	Auburn Univ	Cybersecurity solutions in HW		
11:15 AM		Naresh Sehgal	Intel	Intro to Block Chain and its potential applications to EDA.		
11:45 AM	Lunch					
1:00 PM	Session 5	PANEL:	Block Chain - Will i	t work for Security? Specialized verification? Manufacturing?		
		Shishpal Rawat		Session Chair		
		James Hogan	Vista Ventures LLC			
		James Gambale	LomasoftCorp			
		Naresh Sehgal	Intel Corp.			
2:15 PM	Wrap-up	Shishpal Rawat	IEEE CEDA	Closing comments & Feedback		

EDPS 2018
3 keynotes, 17 talks, 1 panel
Networking & Dinner with ESDA

Thank you speakers, committee members and the attendees
Have a great 2018

# It's a Symposium – Participate & Network ....

- Please silence your alerts Our speakers will appreciate that
- Please (as much as practically possible) occupy the back seats if you are taking notes on the laptop.
- Let a committee member know if we can help you with something.
- And most of all Ask Questions, Provide Feedback to organizers and Network with colleagues
- And if you must -- WiFi network is SEMI-Guest; password SEMIguest