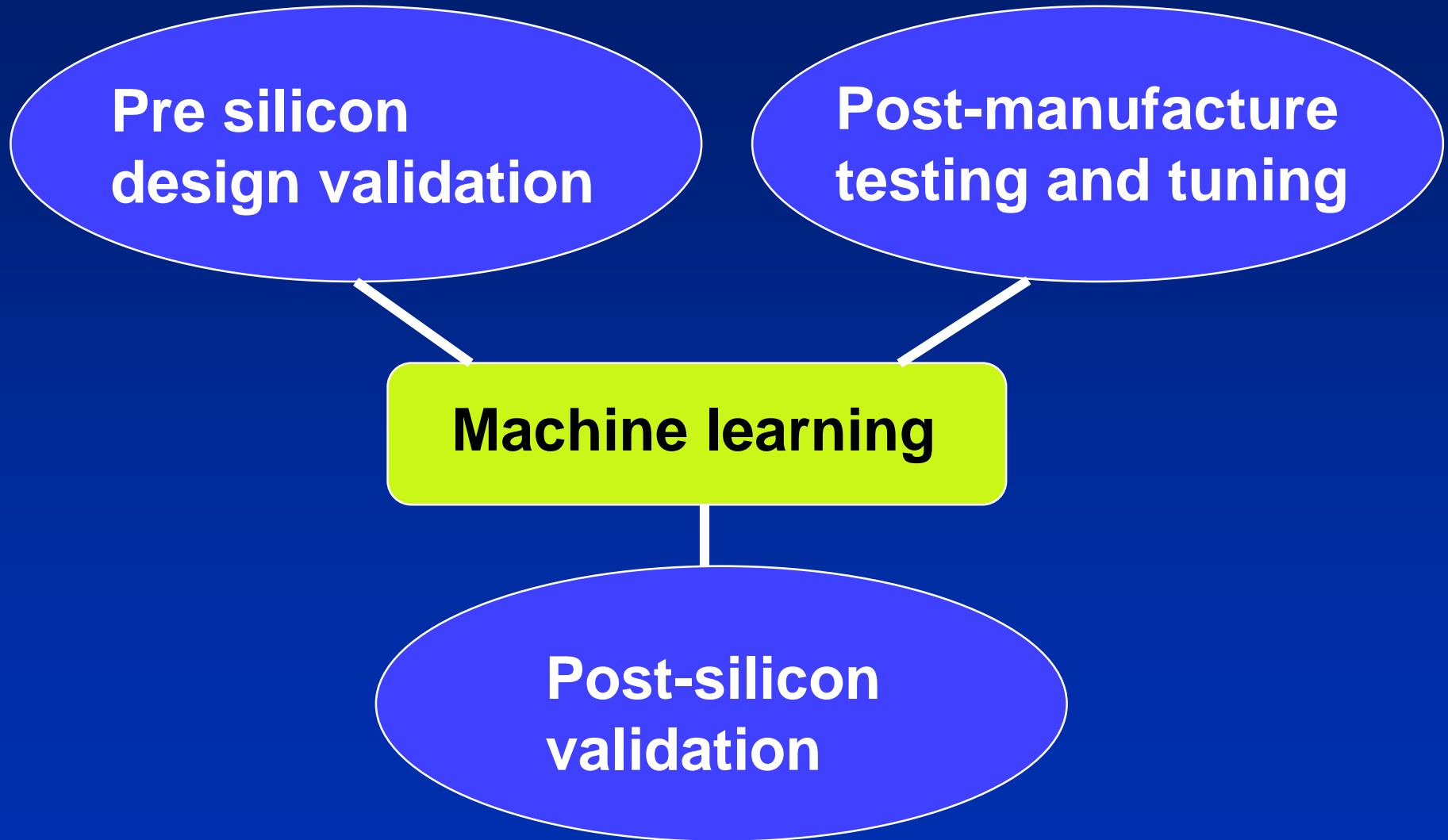# VALIDATION, TESTING AND TUNING OF MIXED-SIGNAL/RF CIRCUITS AND SYSTEMS:

A MACHINE LEARNING ASSISTED APPROACH

A. Chatterjee,

Georgia Tech

GRAs: S. Deyati, B. Muldrey, S.Akbay, V. Natarajan, R. Senguttuvan, S. Sen, R. Voorakaranam, S. Cherubal, P. Variyam, S. Chakrabarti, D. Han and X. Wang
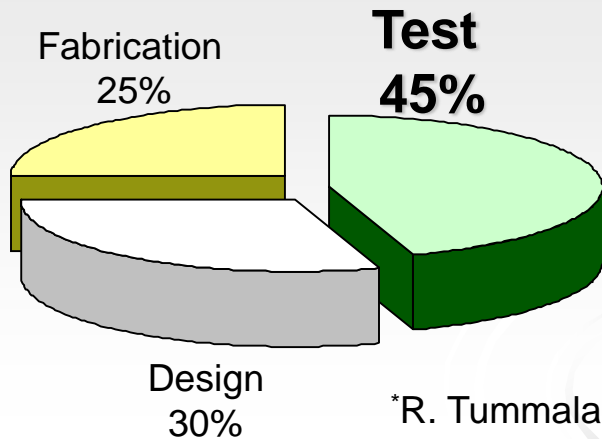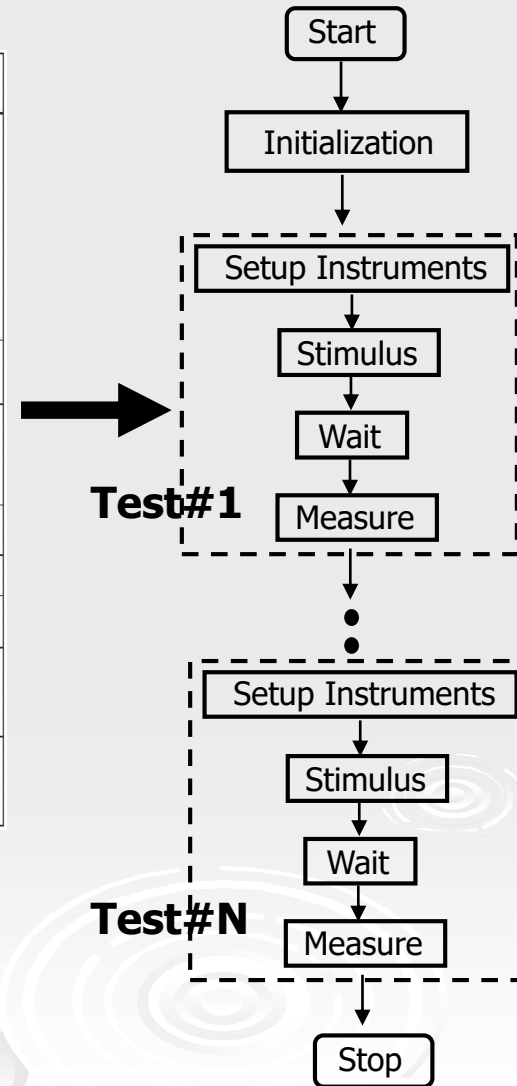
State of the Art in Test: Mixed-Signal SoCs

- Specification Tests
- Each test requires a different setup
  - Total testing time
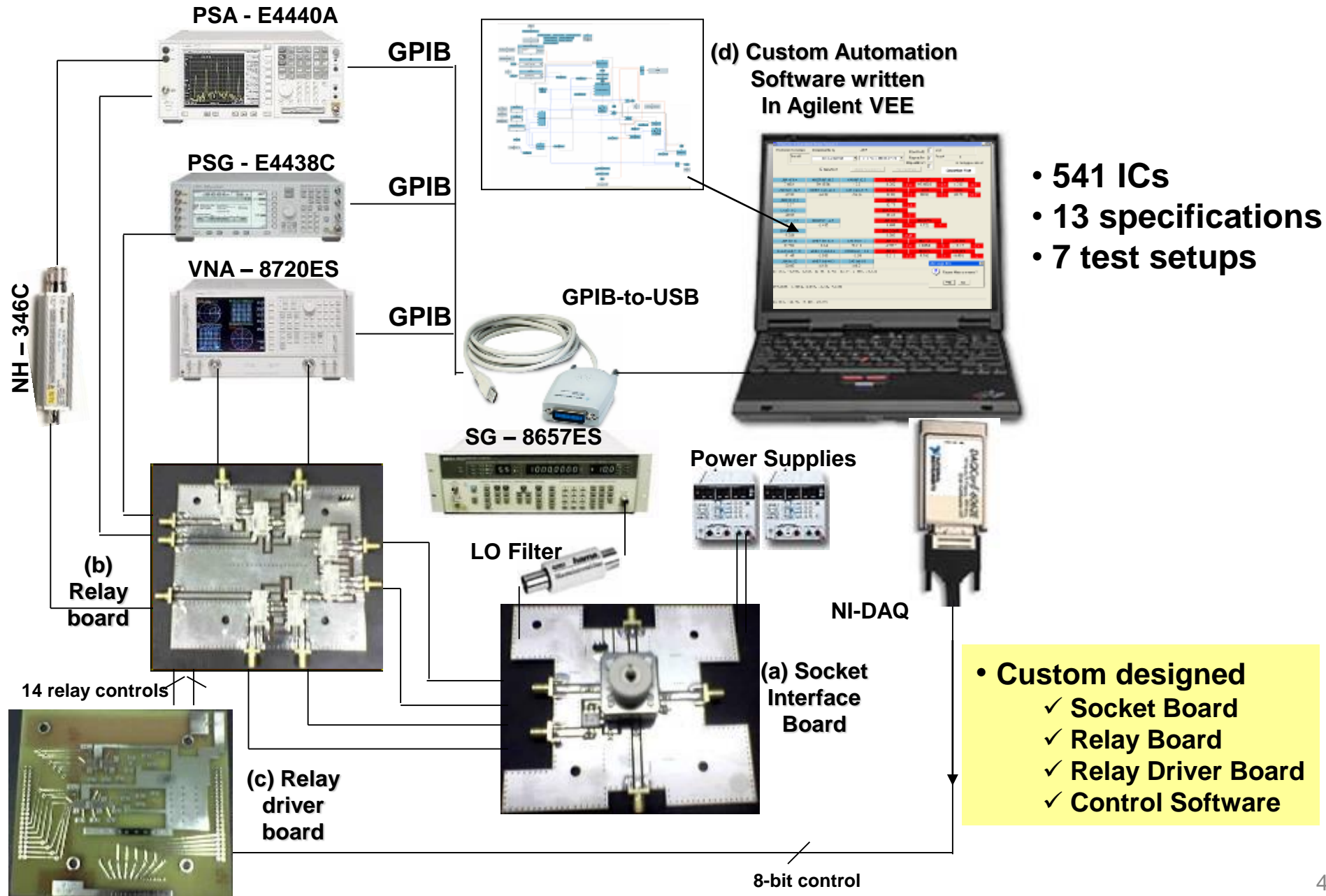 - ATE complexity
  - Load board complexity
- Test cost up 30%- 45%[*]

Datasheet

Fabrication 25%

Design 30%

Test 45%

Start

Initialization

Setup Instruments
Stimulus
Wait
Test#1 Measure

Setup Instruments
Stimulus
Wait
Test#N Measure

Stop

[*]R. Tummala, Fundamentals of Microsystems Packaging, 2001.

Standard Specification Tests

PSA - E4440A

GPIB

PSG - E4438C

GPIB

VNA – 8720ES

GPIB

NH – 346C

(b) Relay board

14 relay controls

(c) Relay driver board

GPIB-to-USB

SG – 8657ES

LO Filter

Power Supplies

(a) Socket Interface Board

NI-DAQ

8-bit control

(d) Custom Automation Software written In Agilent VEE

- **541 ICs**
- **13 specifications**
- **7 test setups**

- **Custom designed**
  - ✓ **Socket Board**
  - ✓ **Relay Board**
  - ✓ **Relay Driver Board**
 - ✓ **Control Software**

Key Issues:

Manufacturing test time: Relay settling time (ms) >> actual test time (usec) ! Test multiple specs.

Built-in test of complex specifications: Difficult to place test instruments and circuitry on-chip for multiple specifications !

Post-manufacture and field performance tuning: Tune *multiple* specs while minimizing power ? Need to tune devices *without extended test costs*.
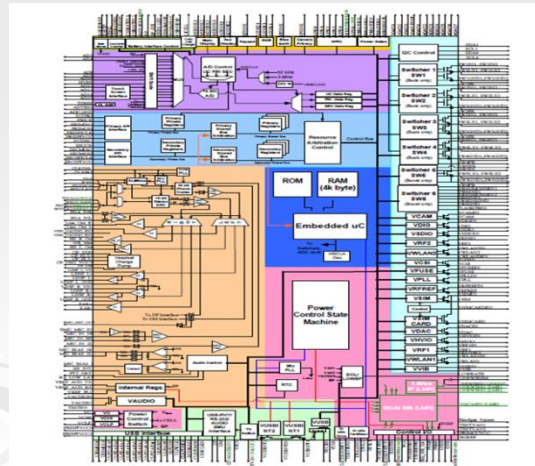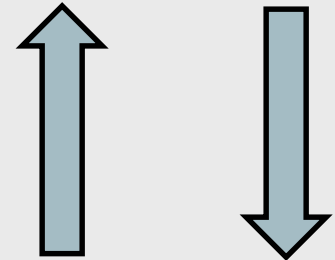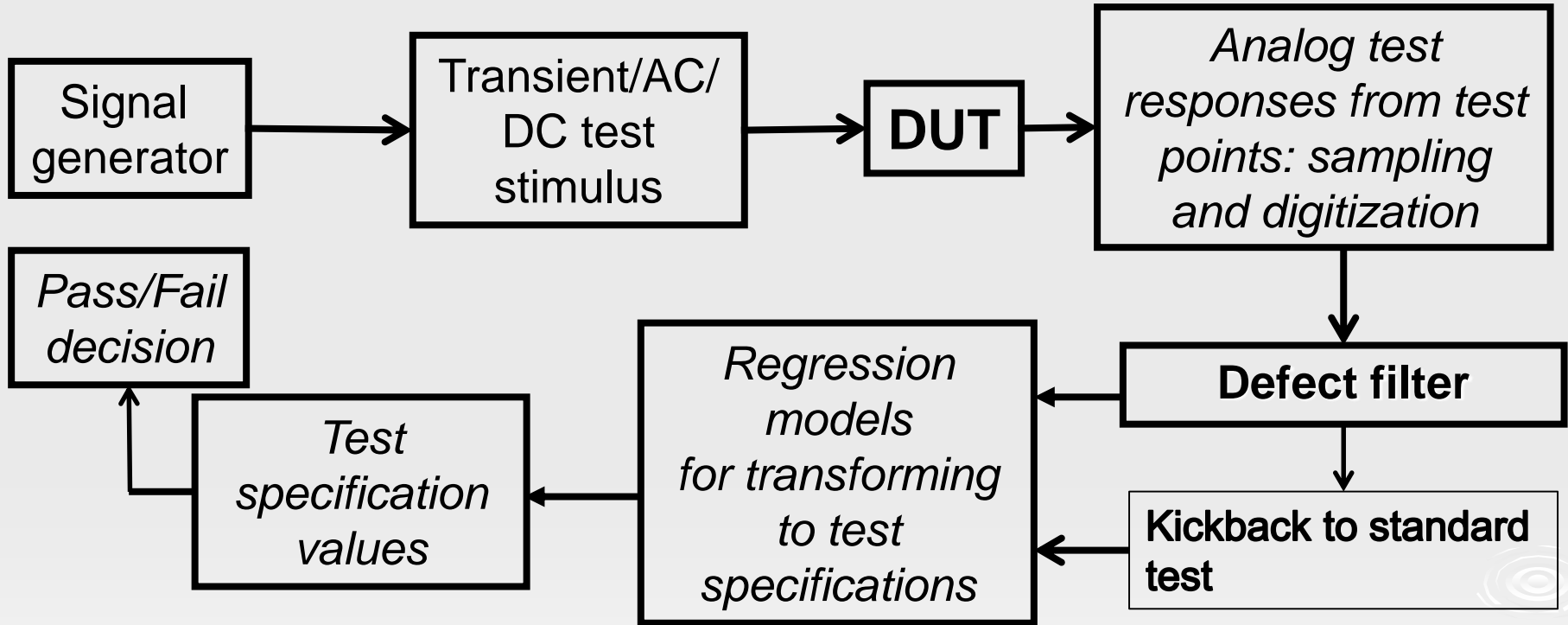
Alternate Tests: Key Principles
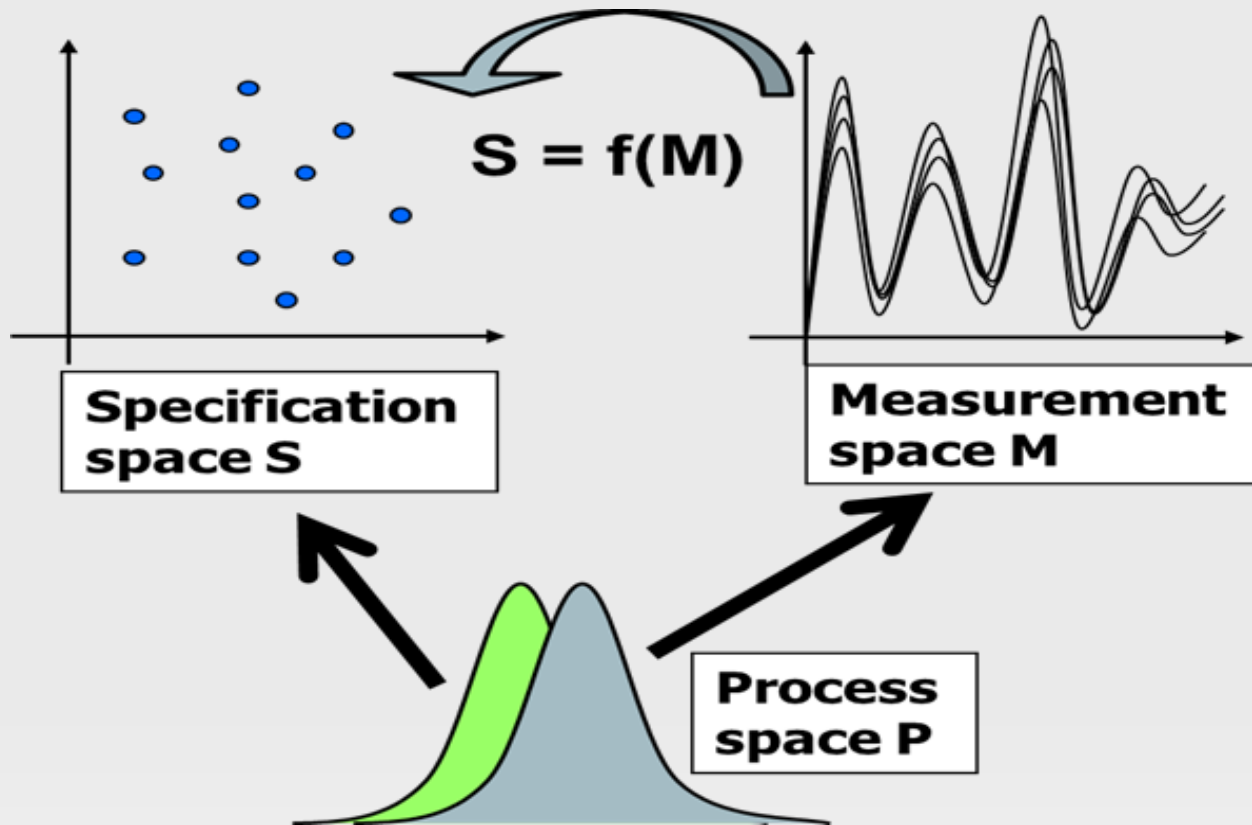
➢ **The mapping *S=f(M)* is derived using nonlinear regression (multiple adaptive regression splines: MARS)**
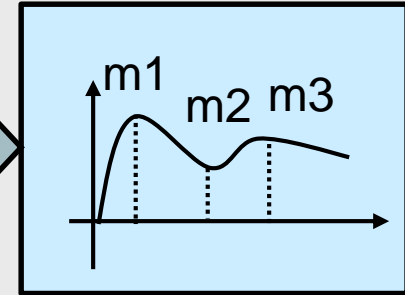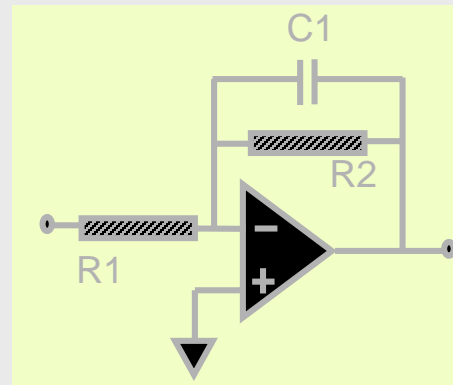
Signature Test Methodology
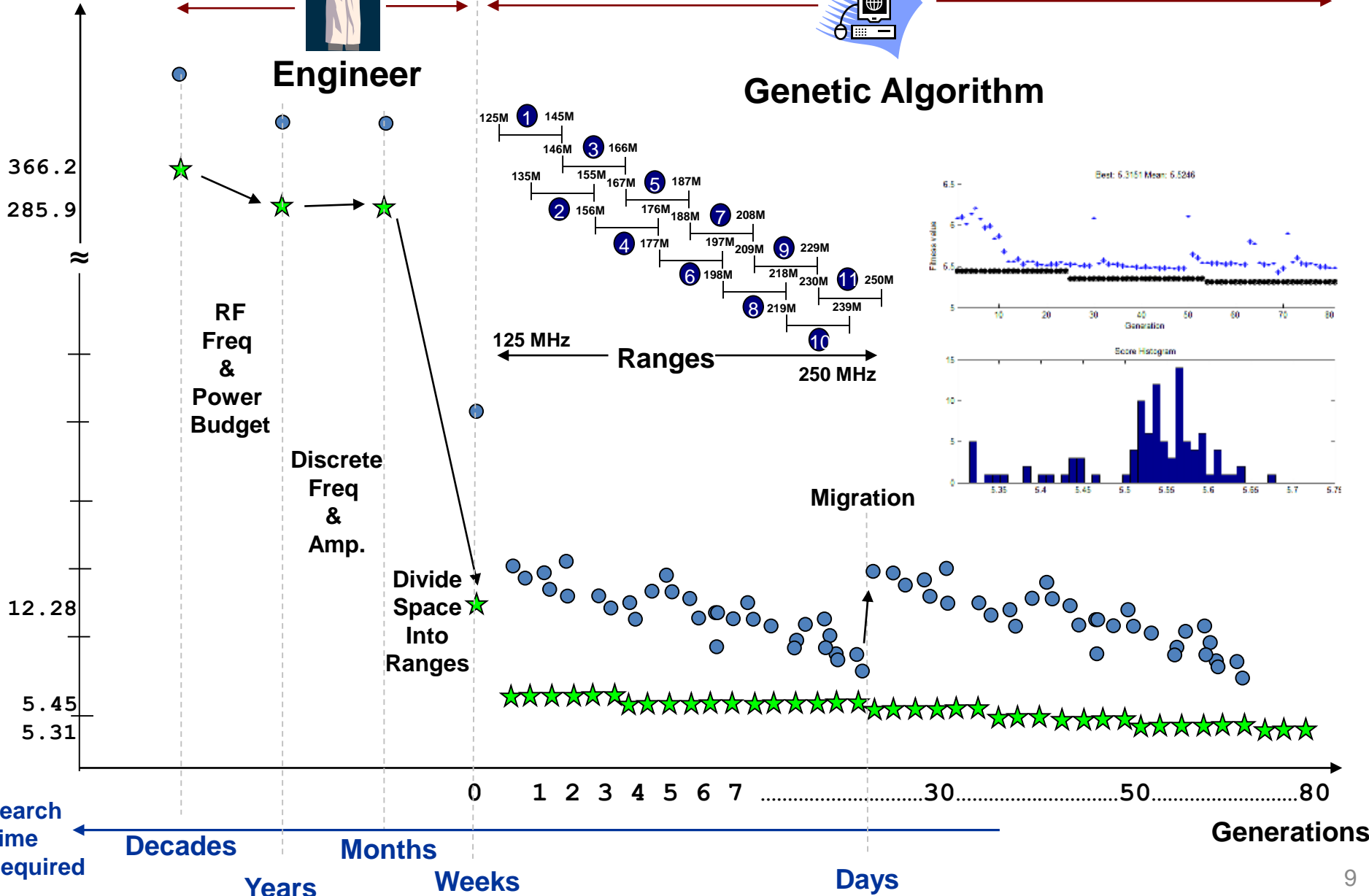
Stimulus Search

★ **Best fitness value in a generation**
● **Mean fitness value in a generation**

Engineer

Genetic Algorithm

366.2

285.9

**RF
Freq
&
Power
Budget**

**Discrete
Freq
&
Amp.**

**Divide
Space
Into
Ranges**

125 MHz ─── **Ranges** ─── 250 MHz

125M ① 145M	
146M ③ 166M	
135M ⑤ 187M	
155M 167M	
② 156M 176M ⑦ 208M	
④ 177M 188M	
197M 209M ⑨ 229M	
⑥ 198M 218M	
230M ⑪ 250M	
⑧ 219M 239M	
⑩	

Best: 6.3151 Mean: 6.5246

Score Histogram

Migration

12.28

5.45

5.31

0   1 2 3 4 5 6 7 ....30................50................80

**Search
Time
Required**

Decades   **Months**

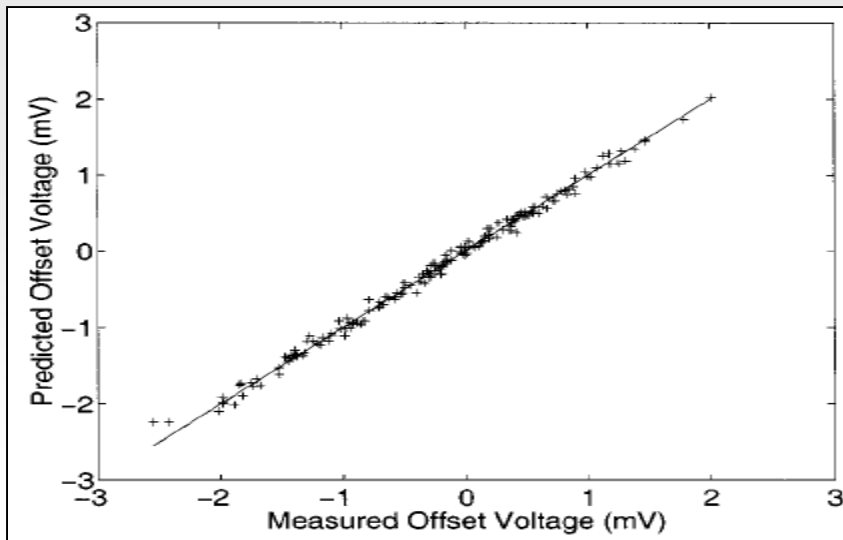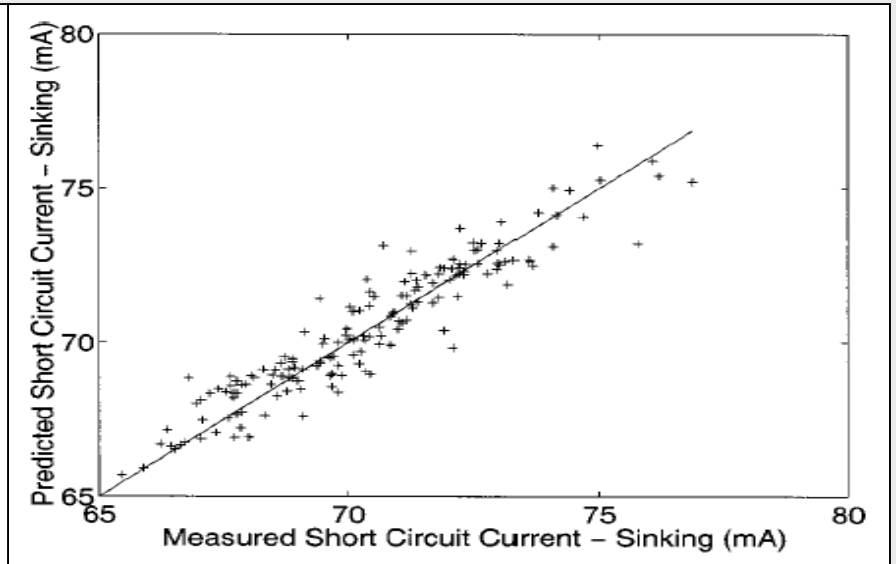**Years**   **Weeks**   **Days**
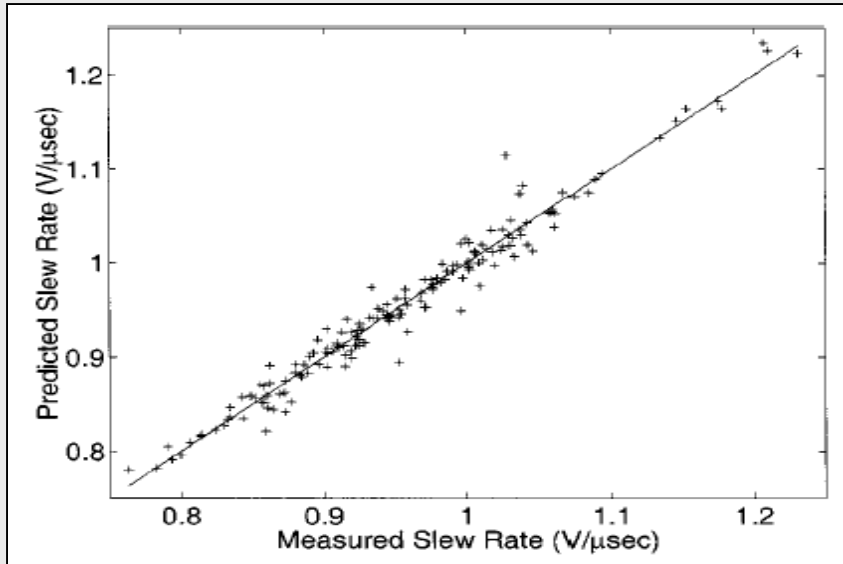
Generations

9
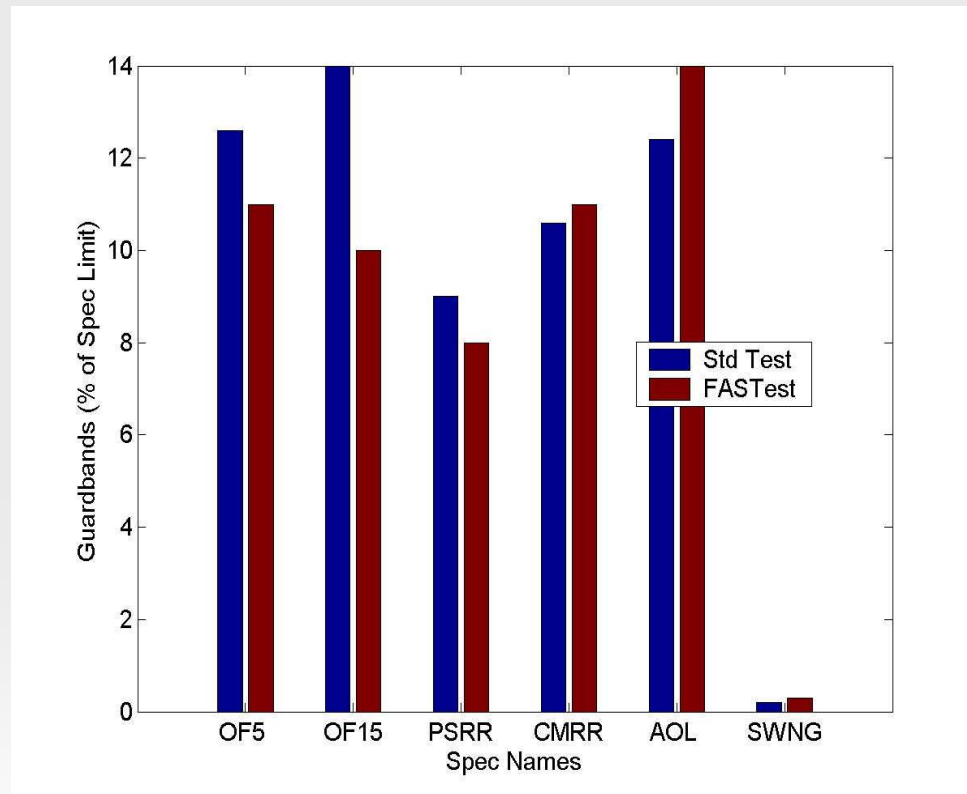
TI Precision Opamp
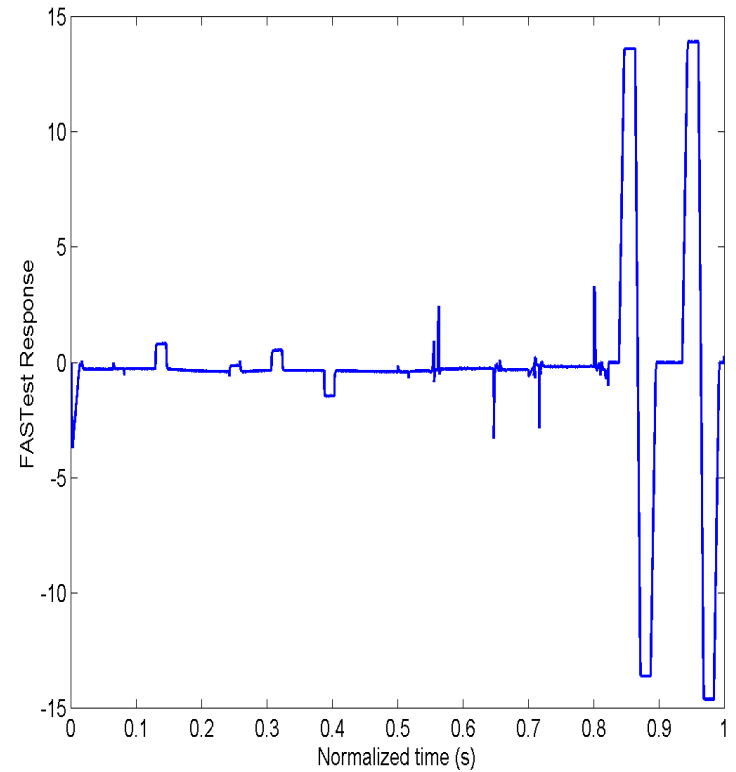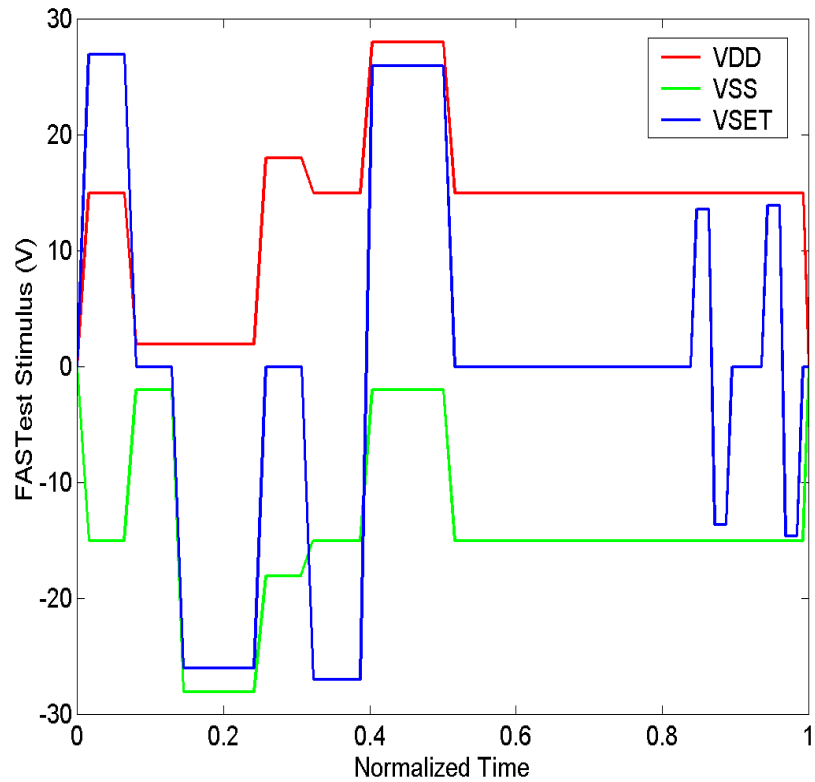
>3X test time reduction
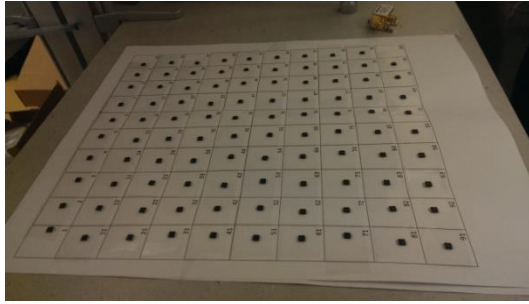
Alternate Test: Performance
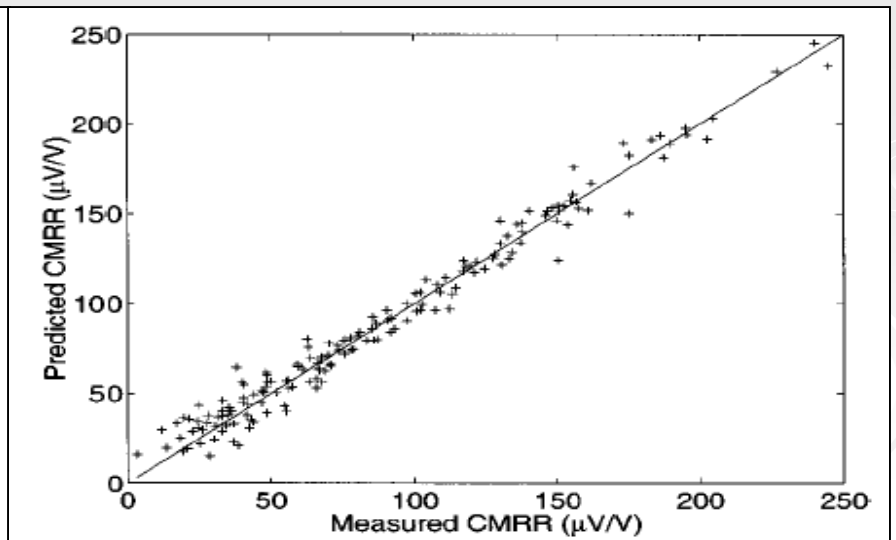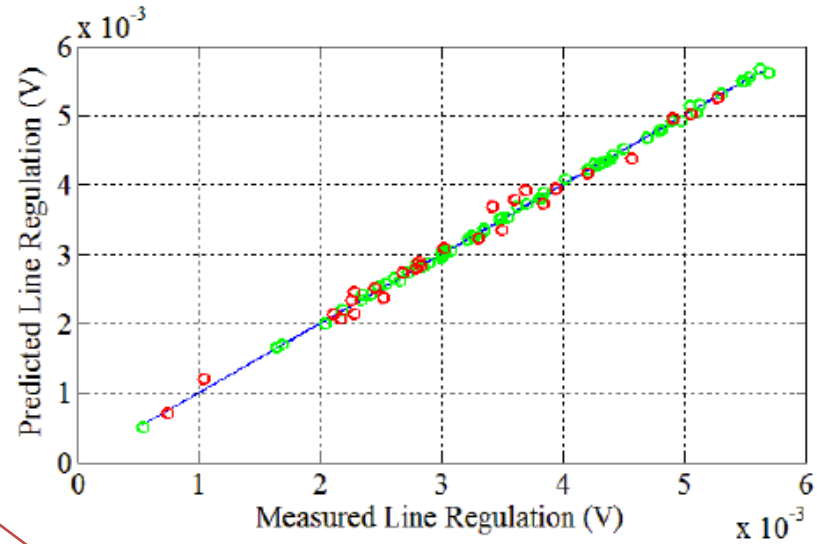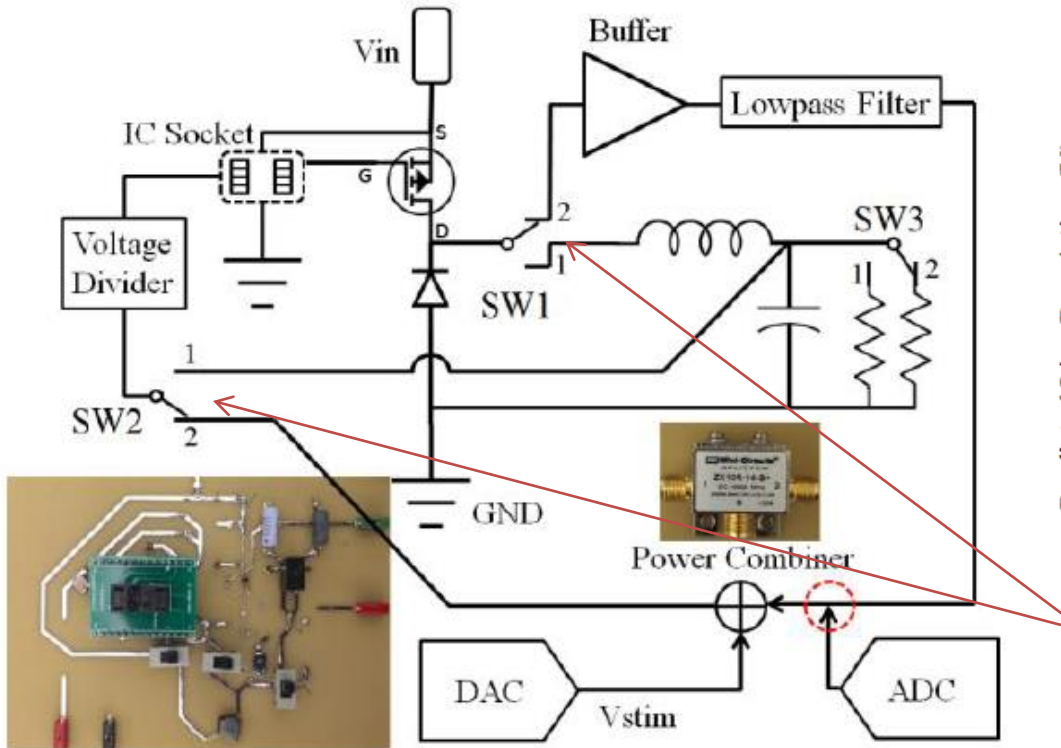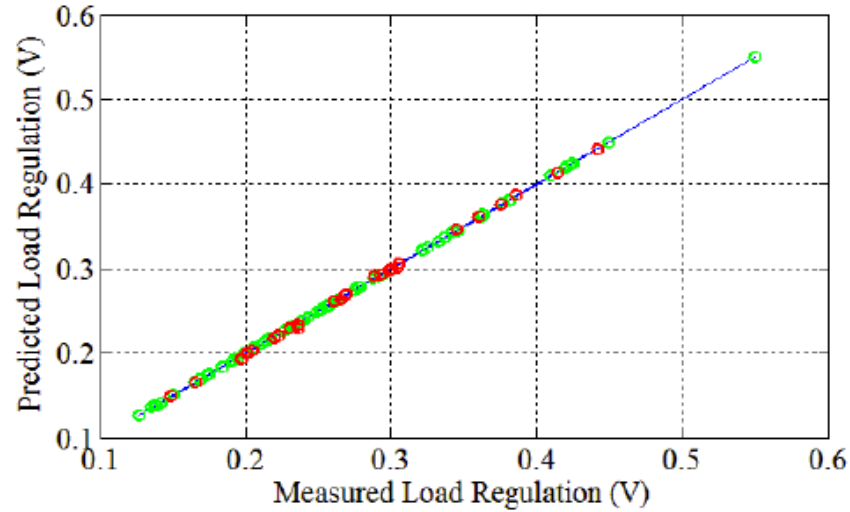
Capability Study (Guardbands)

● For most specs, identical or better guardbands resulted

Hysteretic Buck Converter

100 chips (LM3485)

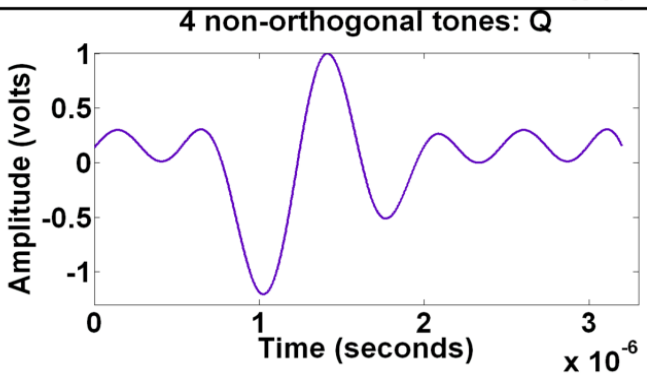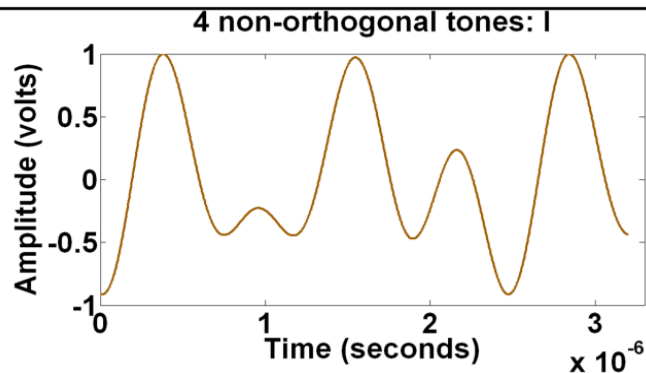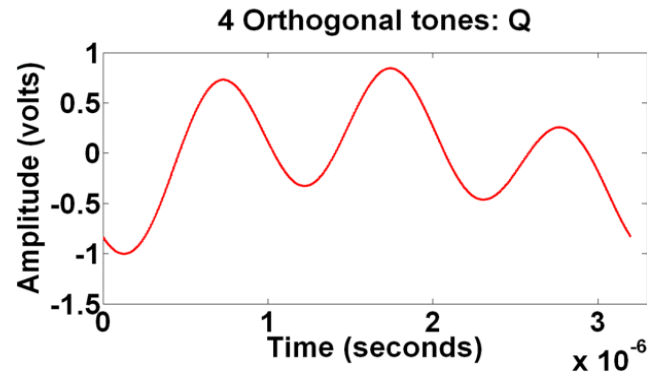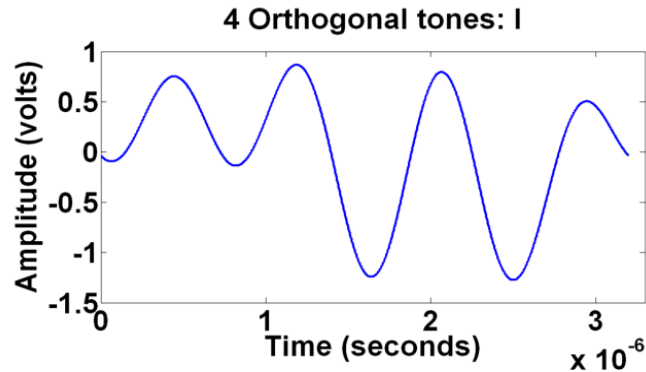SW1 and SW2 in positions 2 for proposed test and position 1 for conventional test

Signature-BIST: Overview
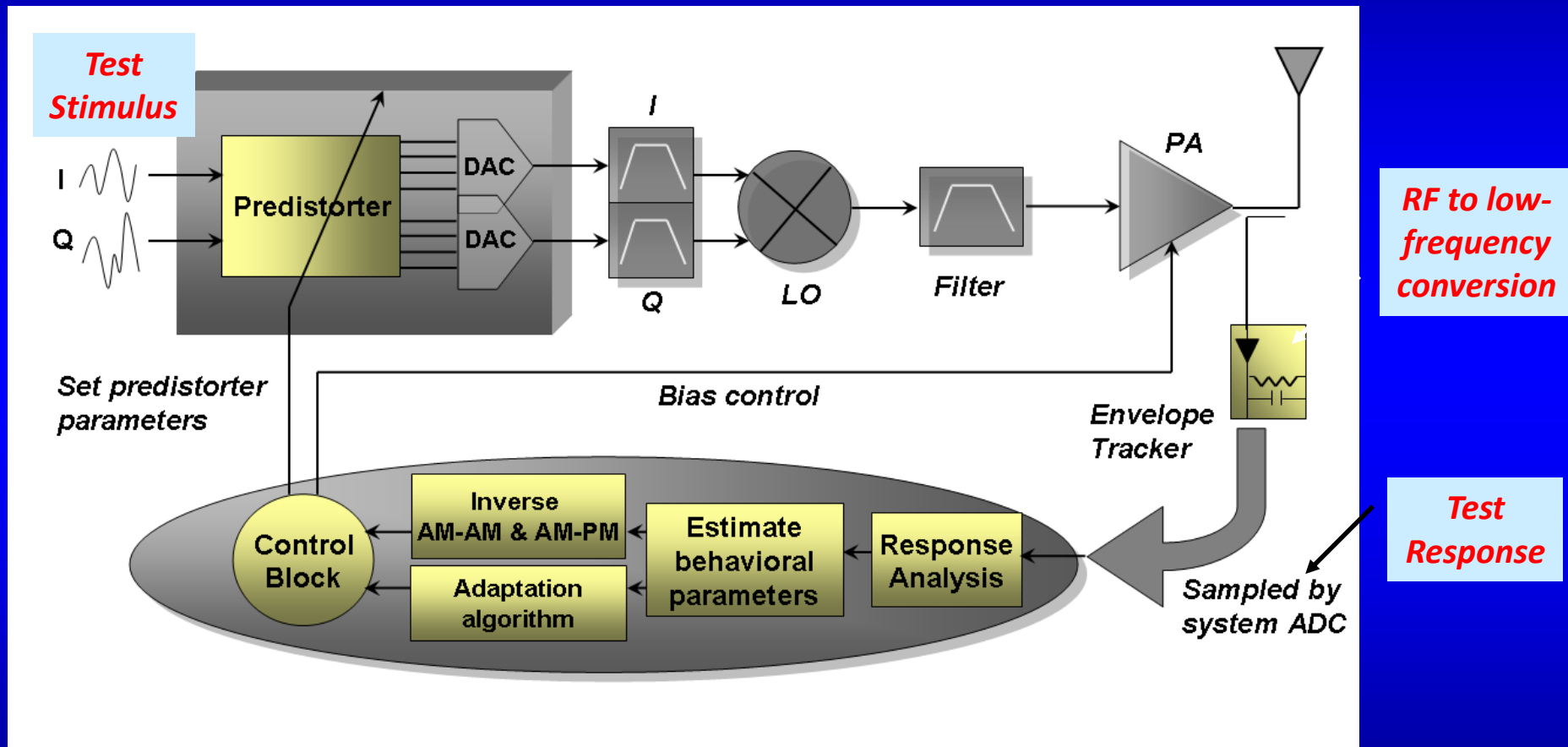
Ref: Variyam, Chatterjee, TCAD 2000

Optimized Diagnostic Tests
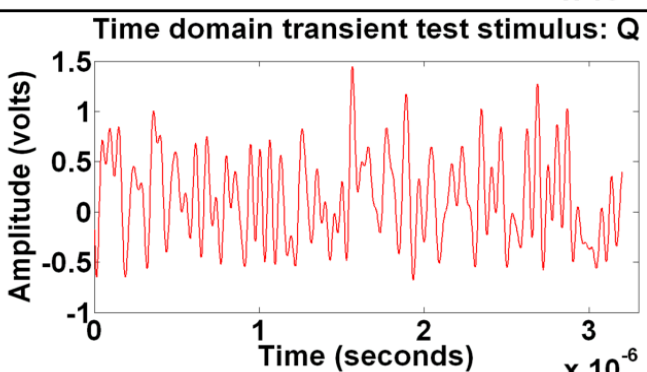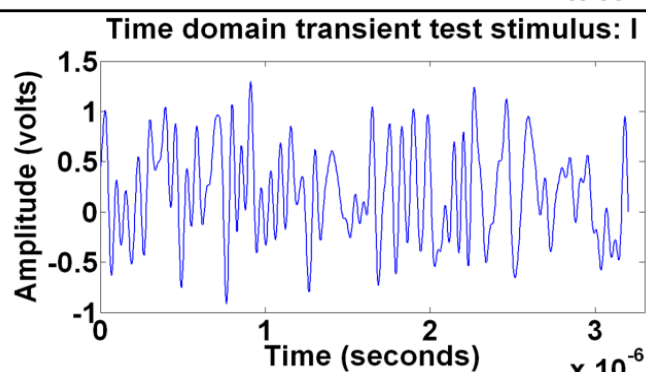
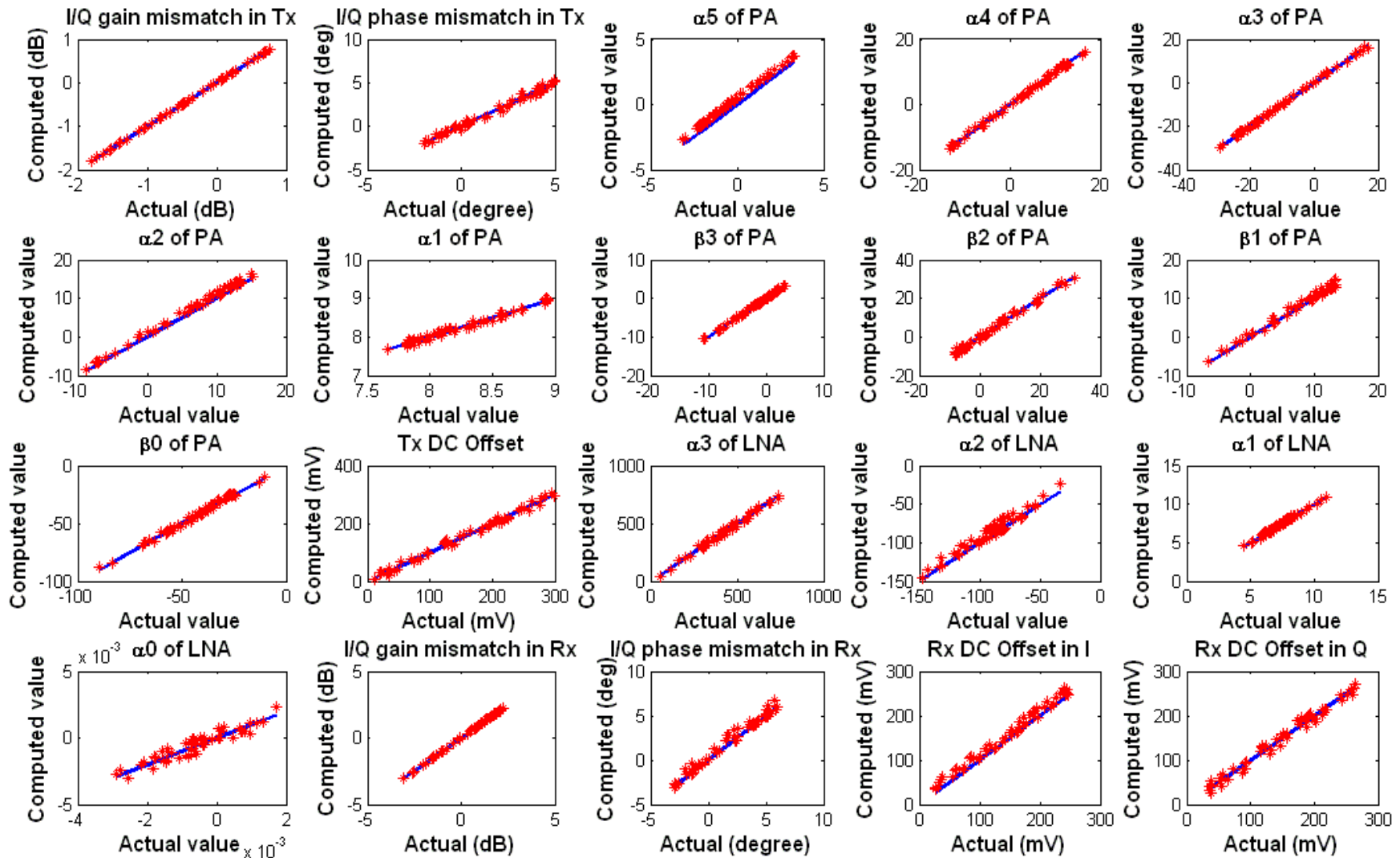Orthogonal tones

Non-orthogonal tones

Time domain test stimulus

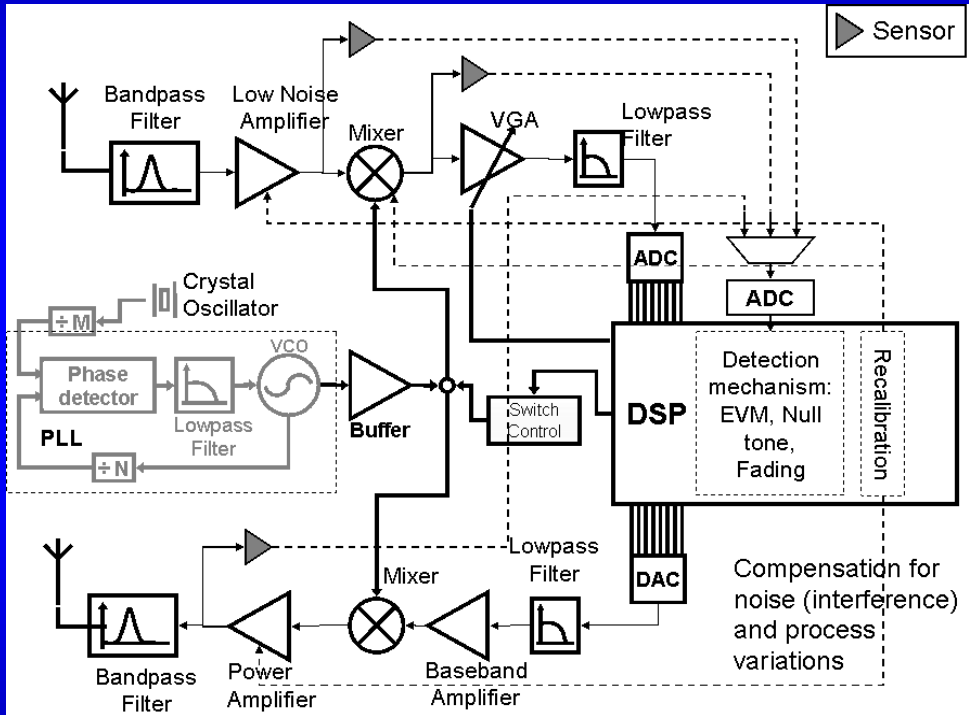# Signature Based Model Parameter Estimation
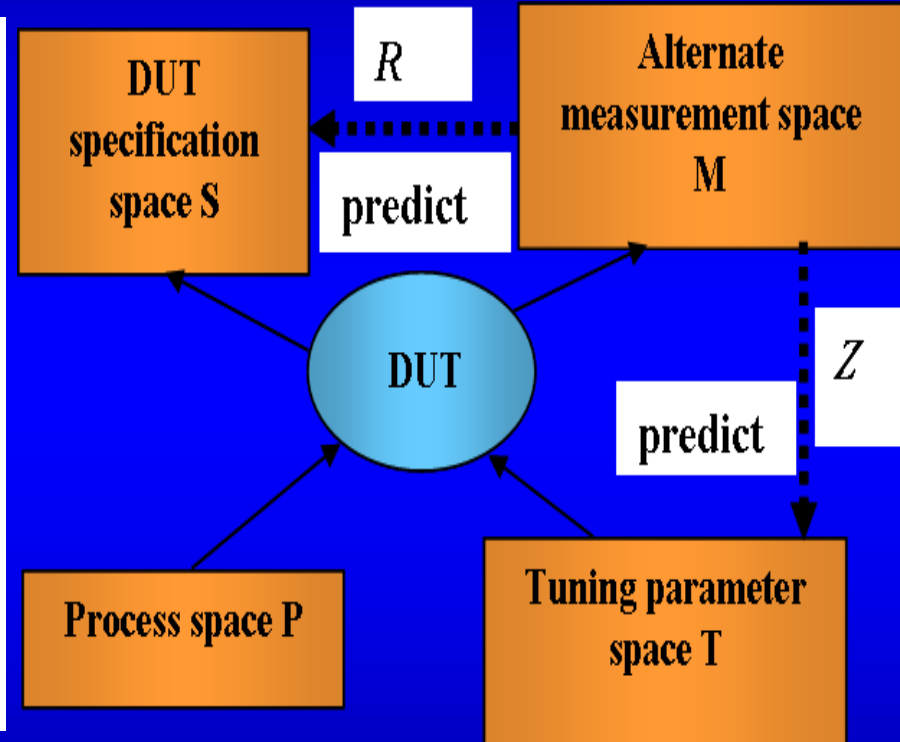
Ability to diagnose parameters of embedded modules !

Tuning: Learning Driven

Tuning Architecture

Supervised Learning

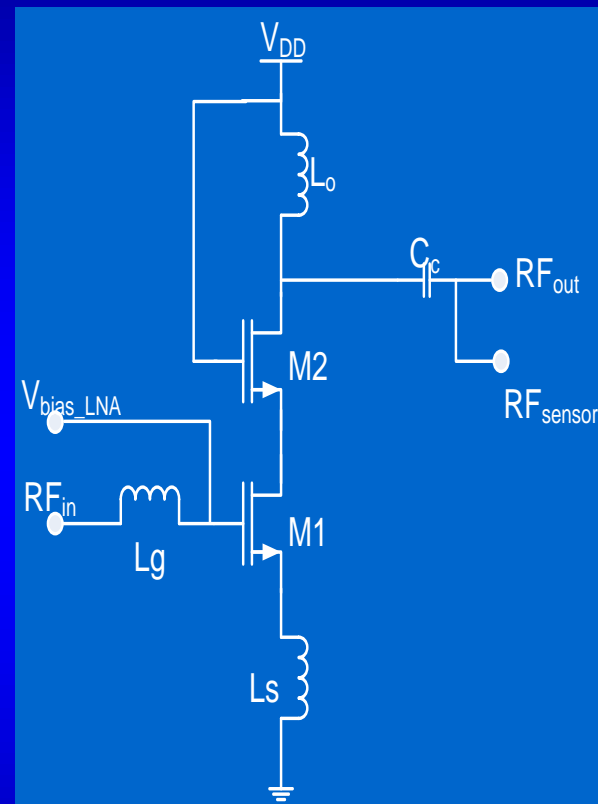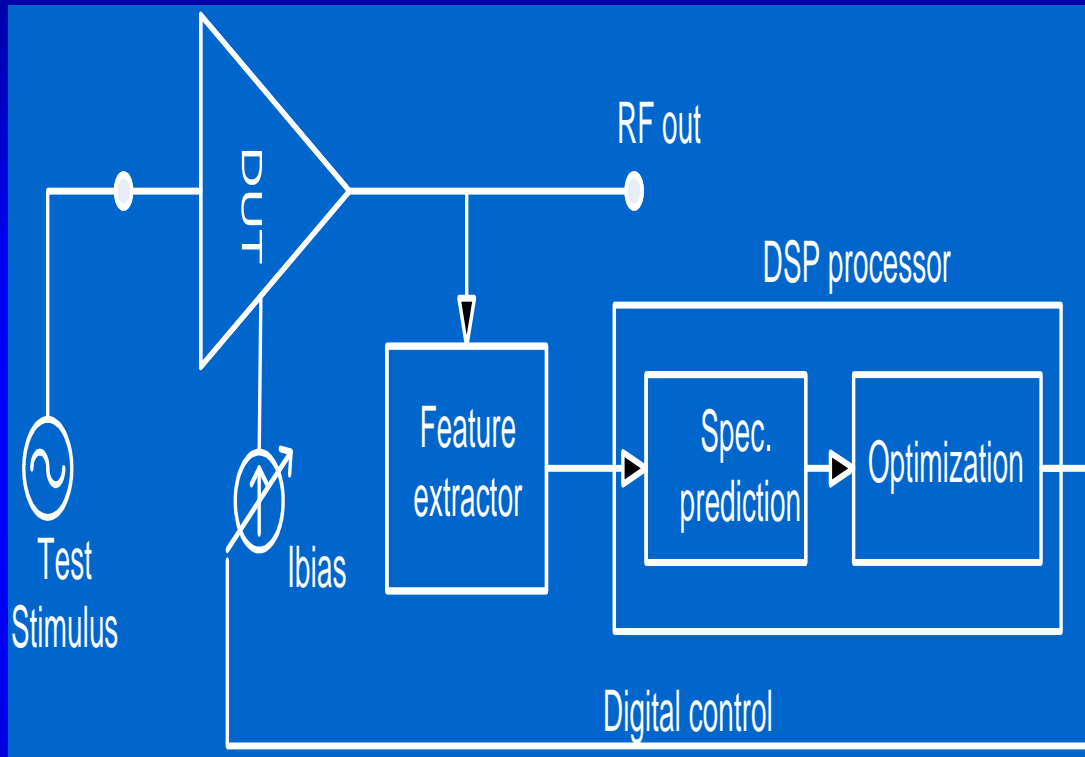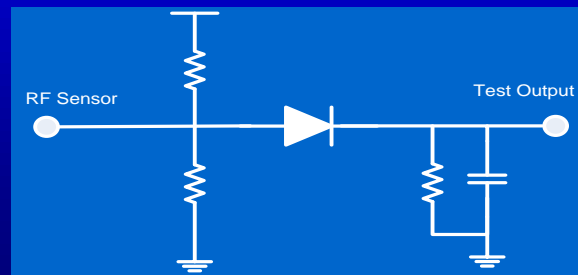- Ability to tune for multiple specs using *single data acquisition*
- Ability to perform *near optimal tuning*
- *Minimal on-chip hardware* overhead
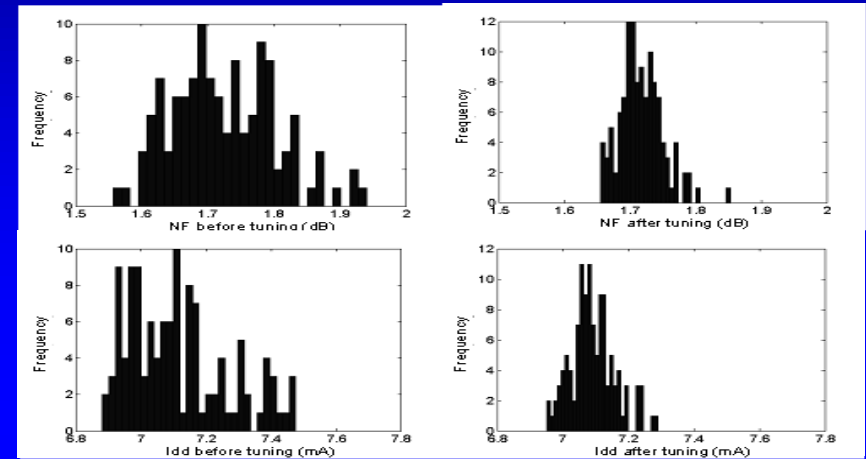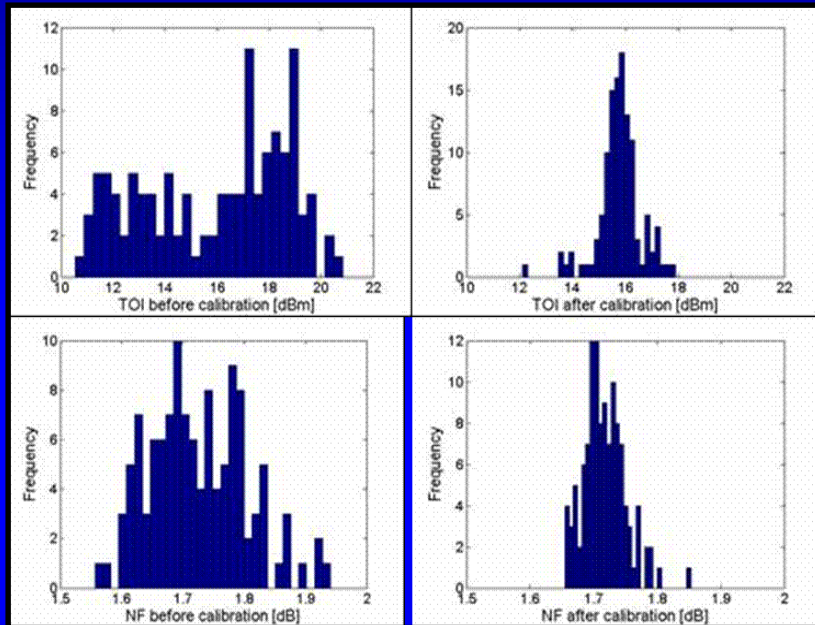
Learning driven tuning algorithms

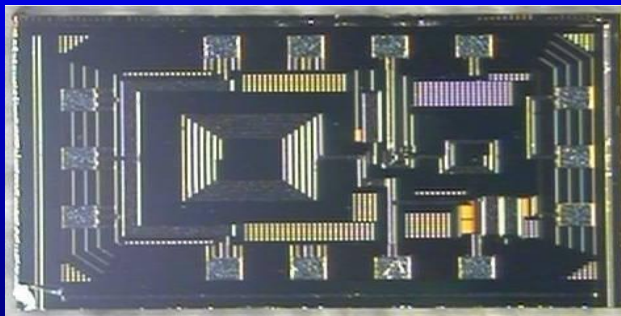*Need accurate learning algorithms!*

Learning driven tuning algorithms

NF (top) and Idd (bottom) before tuning.

NF (top) and Idd (bottom) after tuning

Self-healing LNA !

70% to 99% yield improvement

Experimental Results: Full Receiver

Nominal Specs

	Gain	IIP2	IIP3
Nominal	42.5 dB	-11.5 dBm	-7dBm
Lower bound	41.5 dB	-12.5 dBm	-8dBm
Upper bound	43.5 dB	-10.5 dBm	-6 dBm

One-Instance (P1)

	Gain	IIP2	IIP3
Before	40.1	-10	-5.3
After	41.5726	-11	-7.2569
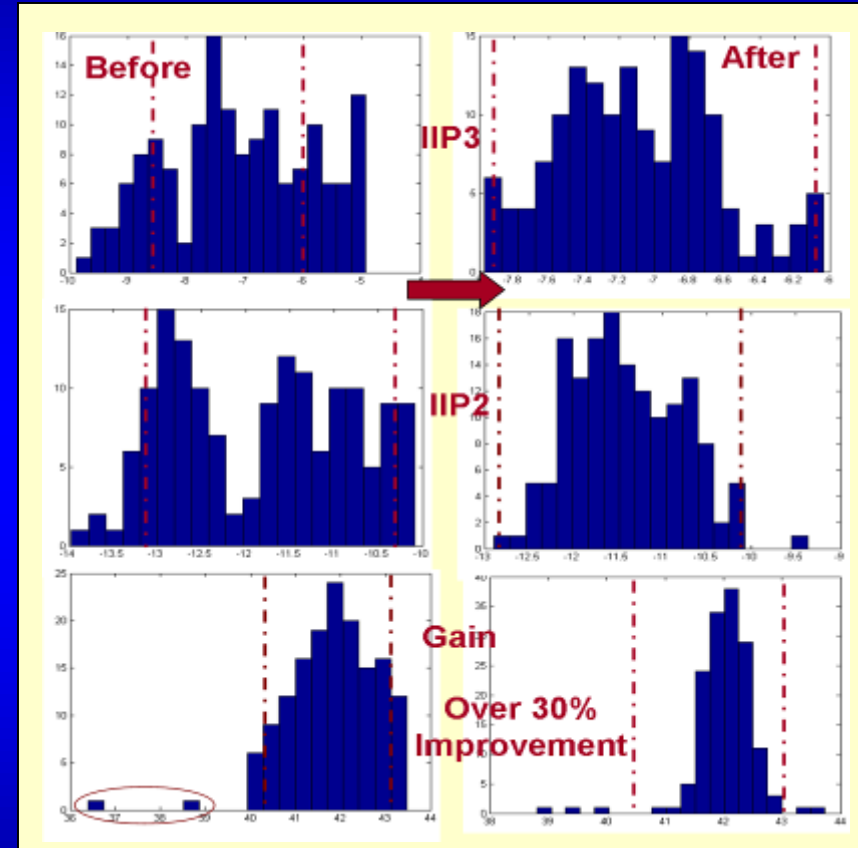
- 207 possible knob combinations (P1) for yield recovery
- Power conscious knob combination (P1) : 0.5724W
- Converged Knob combination (P1) : 0.5724W

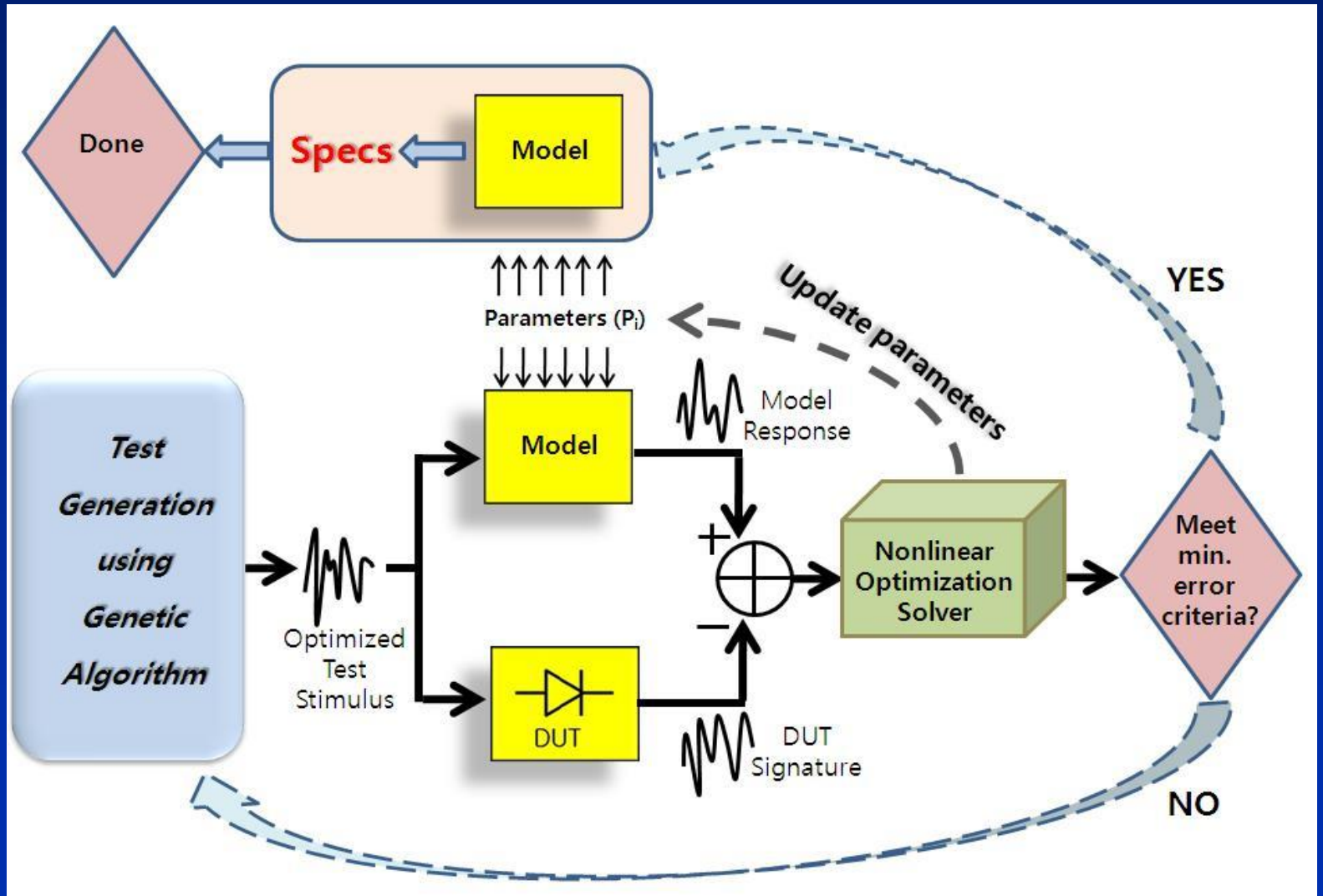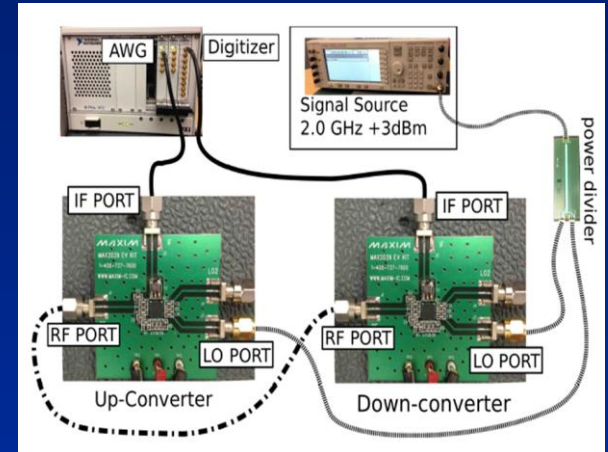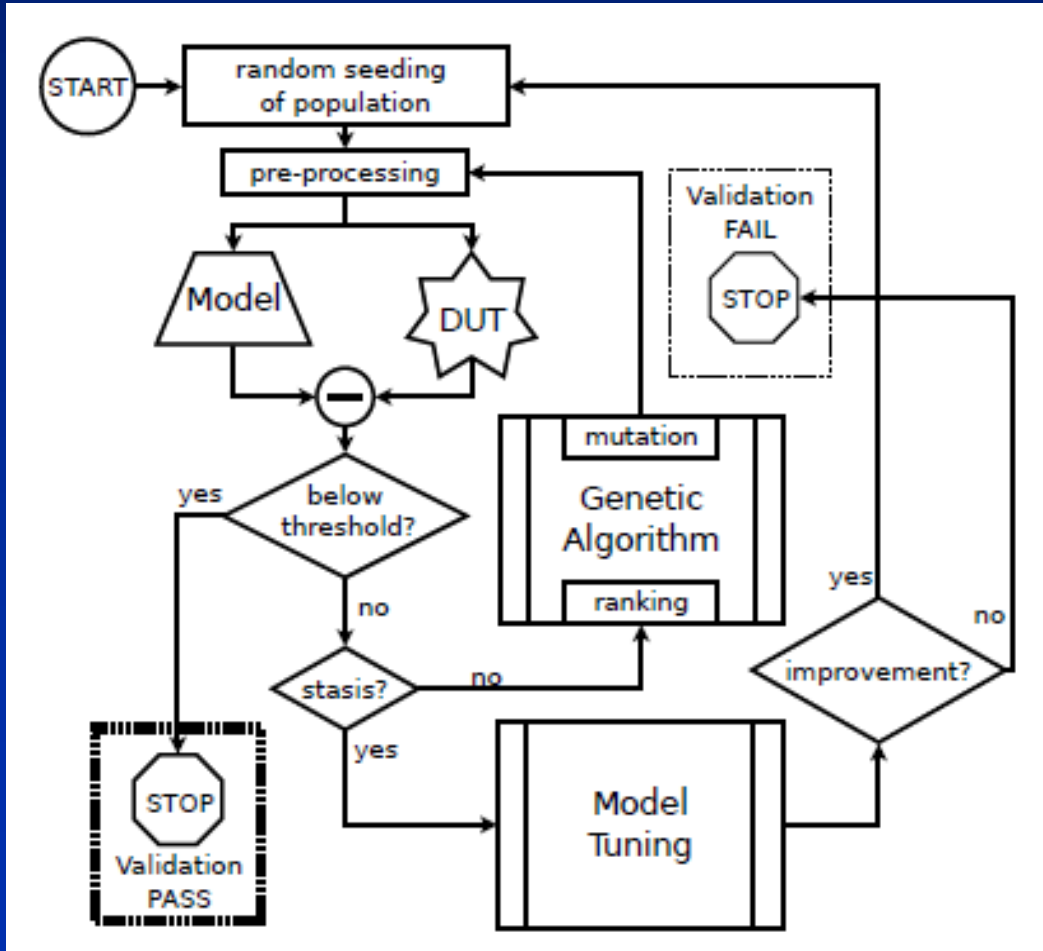# Post-Silicon Challenges

- Models for design bugs are not known a-priori and must be detected, learned and diagnosis

- Need to automate generation of bug models using learning algorithms

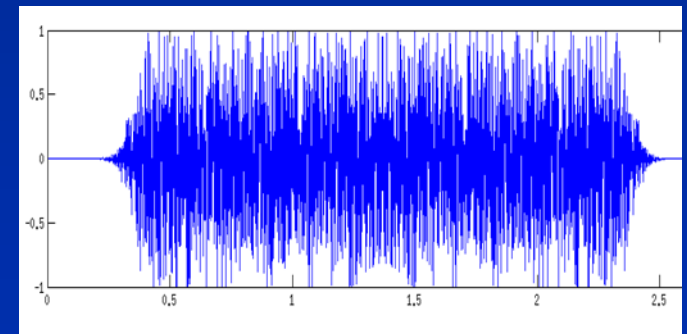- Diagnosed bugs must eventually be mapped to physical design parameters

Model Tuning

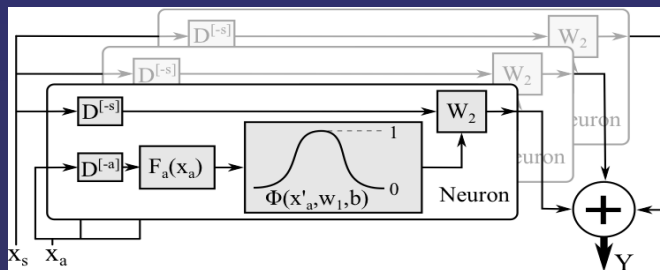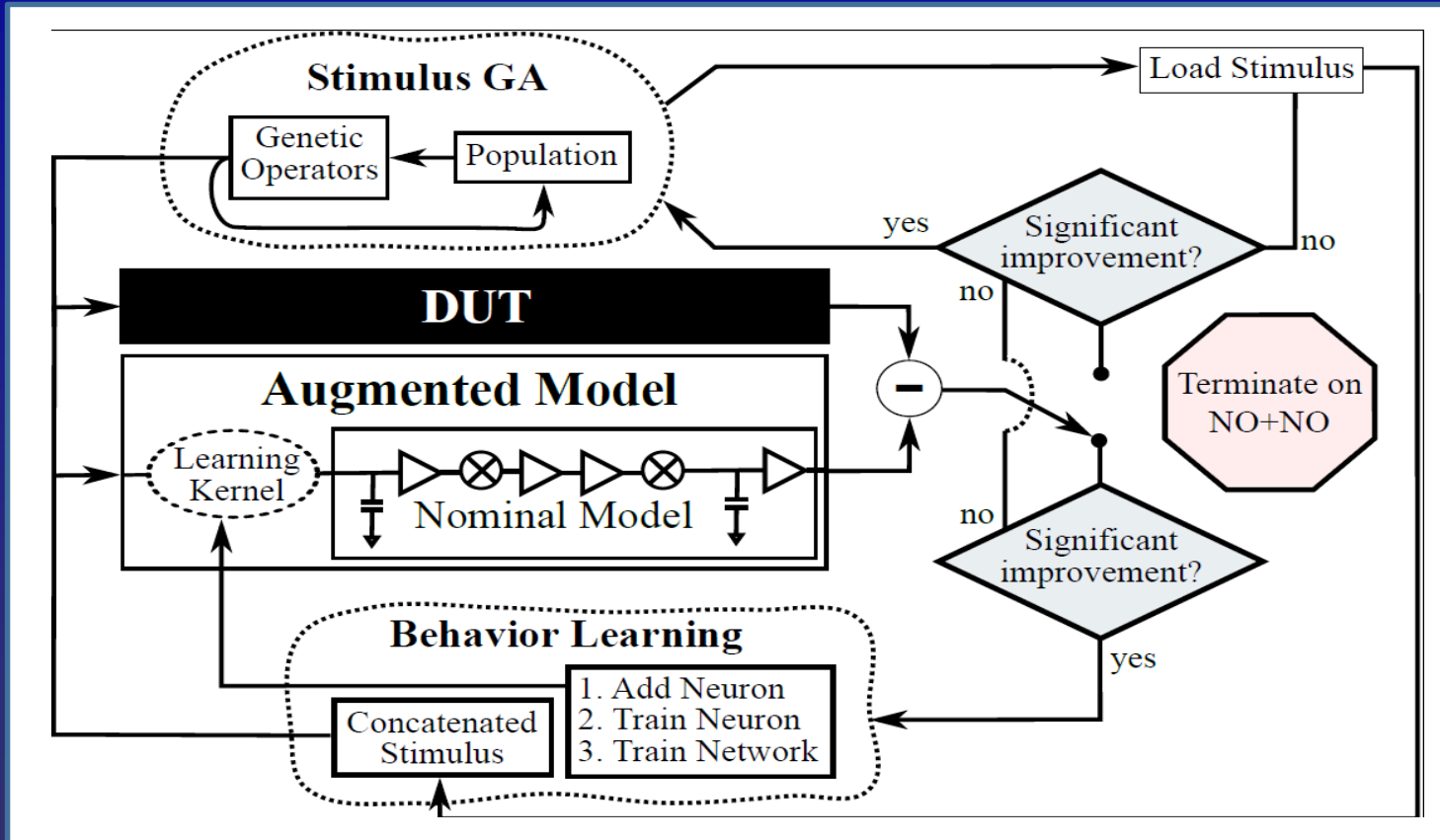# Test Stimulus Generation for Exposing Design Bugs
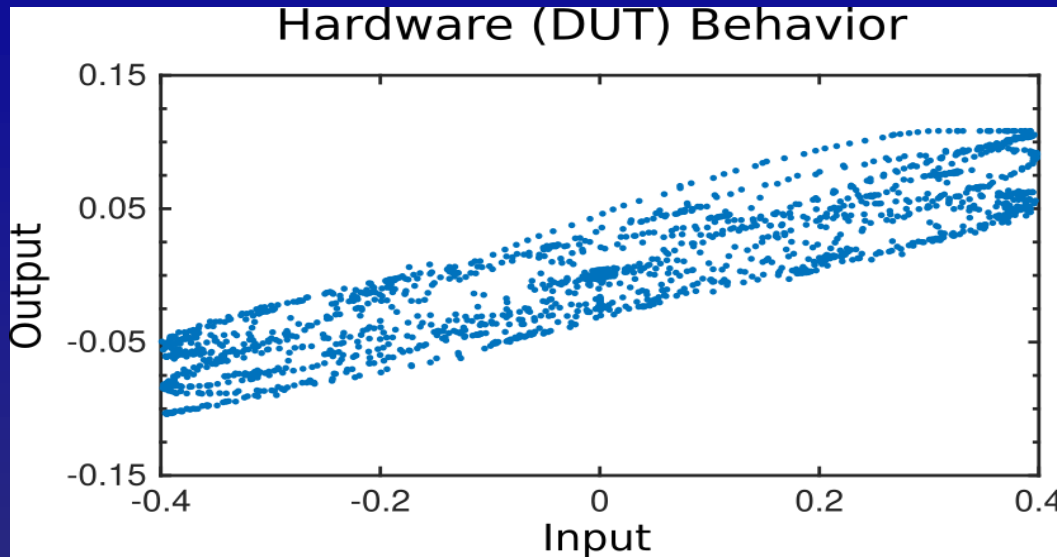

Test setup

Best stimulus

System Level Bug Learning

Sparse Weiner learning kernel

Experimental Results: Maxim MAX2242 RF PA
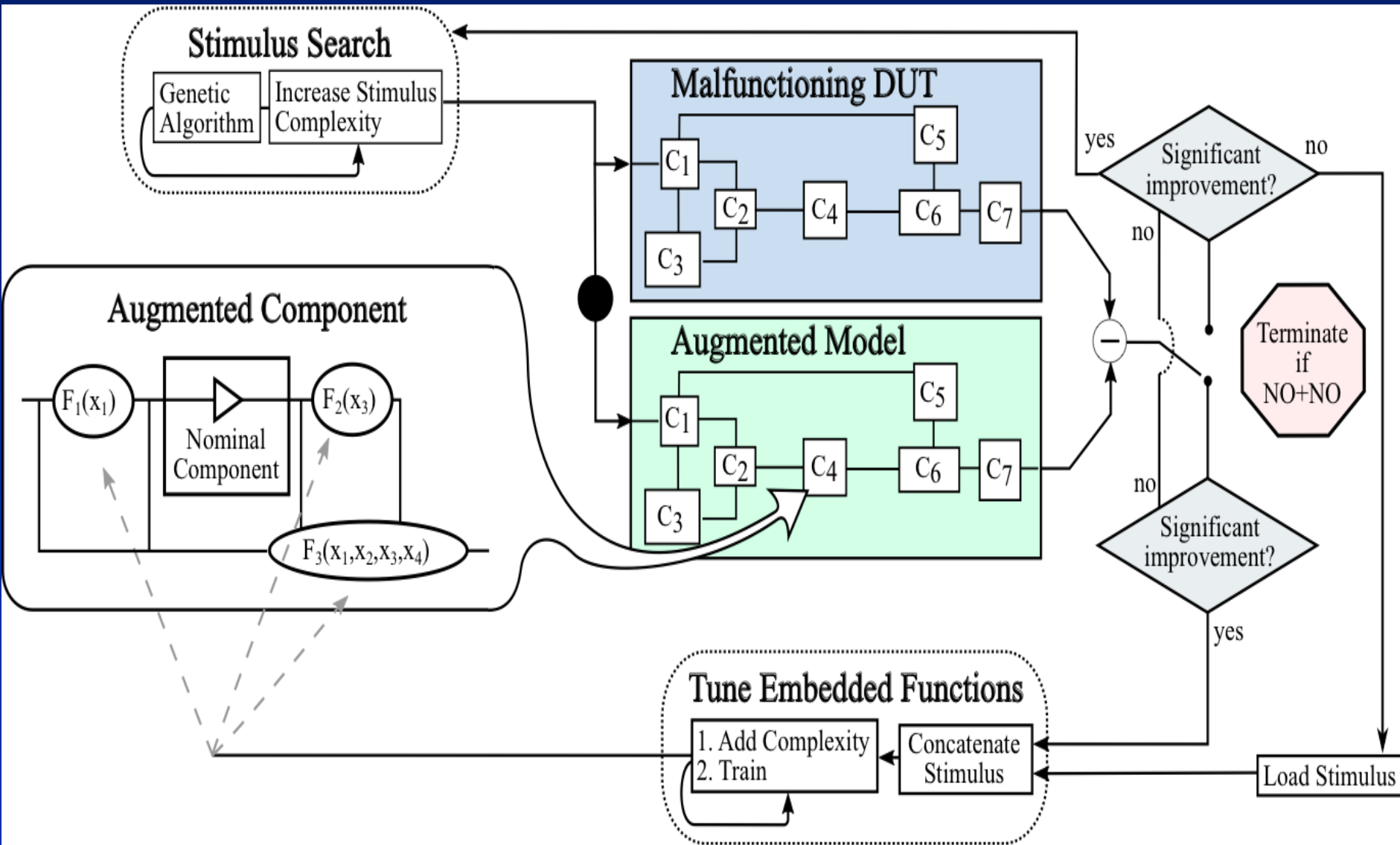

Hardware (DUT) Behavior
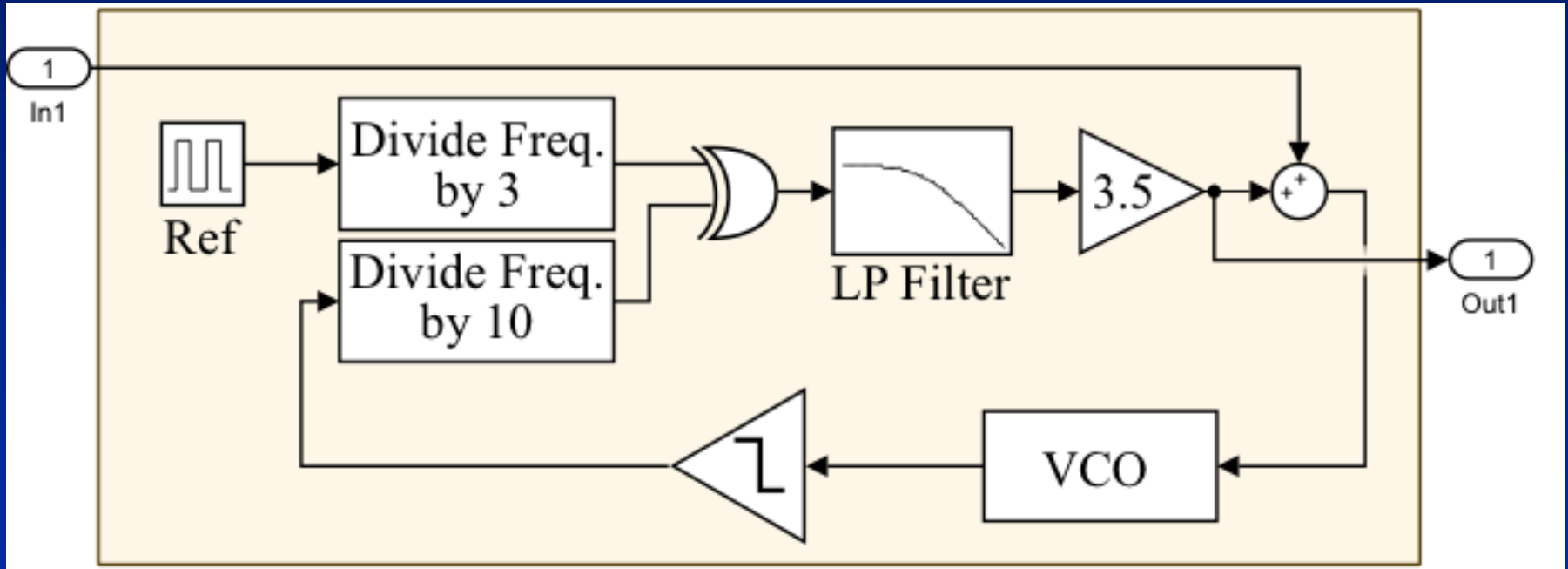

Model Behavior After Augmentation and Training
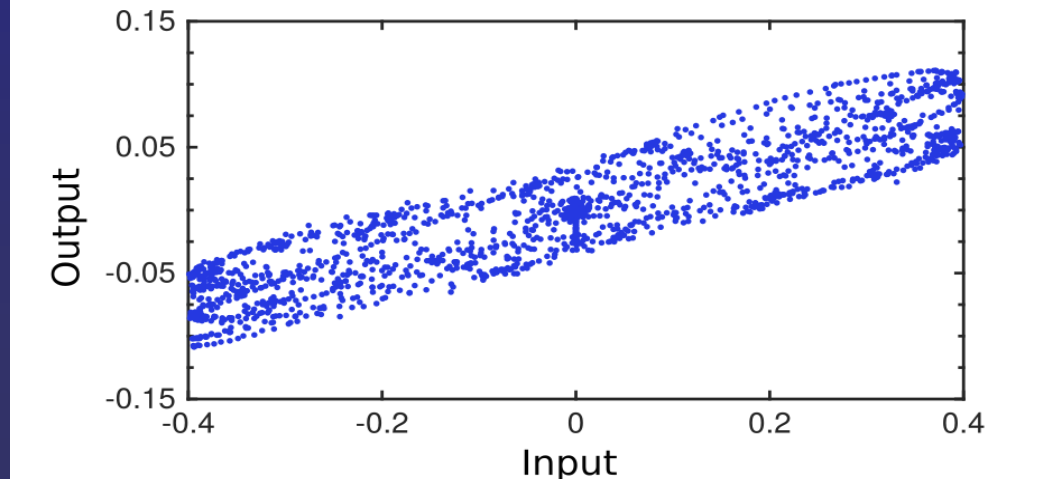
Captures hysteresis and memory effects automatically
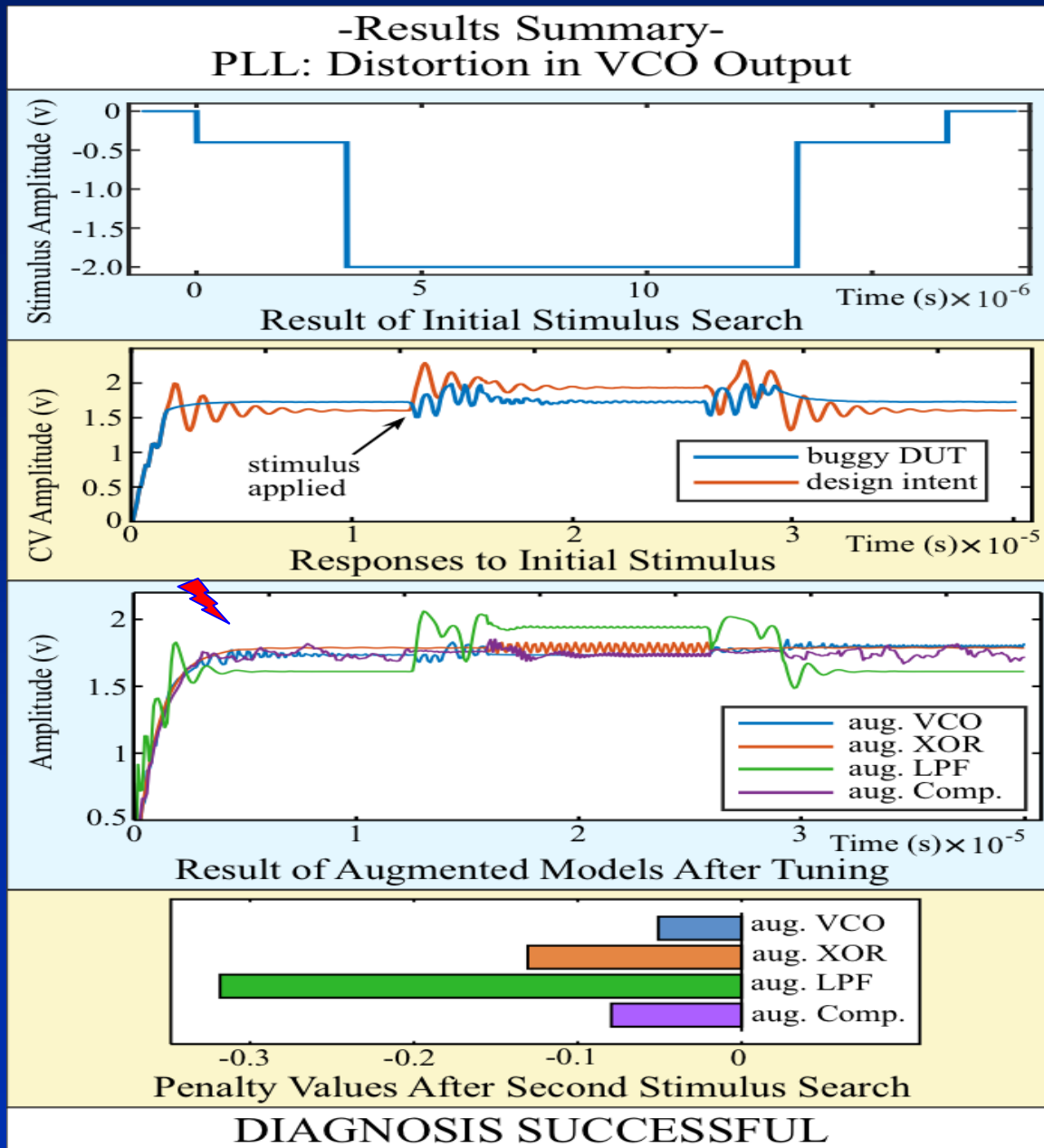
Diagnosis of Static Design Bugs

PLL Experiments

- **System stimulated by summing LP signal at VCO input**

- **System observed immediately prior to summing**

PLL Experiment: Buggy VCO Output

-Results Summary-
PLL: Distortion in VCO Output

Result of Initial Stimulus Search

Responses to Initial Stimulus

Result of Augmented Models After Tuning

Penalty Values After Second Stimulus Search

DIAGNOSIS SUCCESSFUL

Questions ?

"I'd do better if she'd ask questions more closely matching my answers."