EDPS 2017
IEEE CEDA System Validation & Debug Technology Committee

Validation Coverage Working Group Update

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Agenda

- **IEEE CEDA System Validation & Debug Technology Committee**
  - Formed mid-2016
- **Validation Coverage WG**
  - Our Focus
  - Latest activities
  - SW Drivers
  - Emulation to Post Silicon
  - Test Instruments

Scope of Activities

- **Extending functional coverage to post-silicon**
  - Power, performance, or other system-level use cases
  - Pre- and post-silicon teams come together early on to figure out how to attain required coverage
- **HW/SW/OS together as a system should be treated as a unit**
  - It's the product, stupid!
  - Or, it's the stupid product!
- **Electrical design defects (based on design) and subjective functional coverage**
- **Need a systematic way of defining and measuring coverage**
  - Automation-ready and automated ultimately
- **Extracting functional coverage**
  - Need automation of extracting functional coverage from specifications linking to platform
  - How do we extract functional coverage from post silicon validation that were NOT part of the initial requirements
    - There are always escaped coverage points that occur in silicon

Coverage Working Group Focus

- **Validation extends from pre-silicon to post-silicon, so need a unified view**
  - Extending pre-silicon tools and methodology to post-silicon, including random testing
    - For example UCDB and verification planning tools
    - Acclera Portable Stimulus Working Group … except post-silicon is not a priority!
  - Extend to use of validation analytics / big data

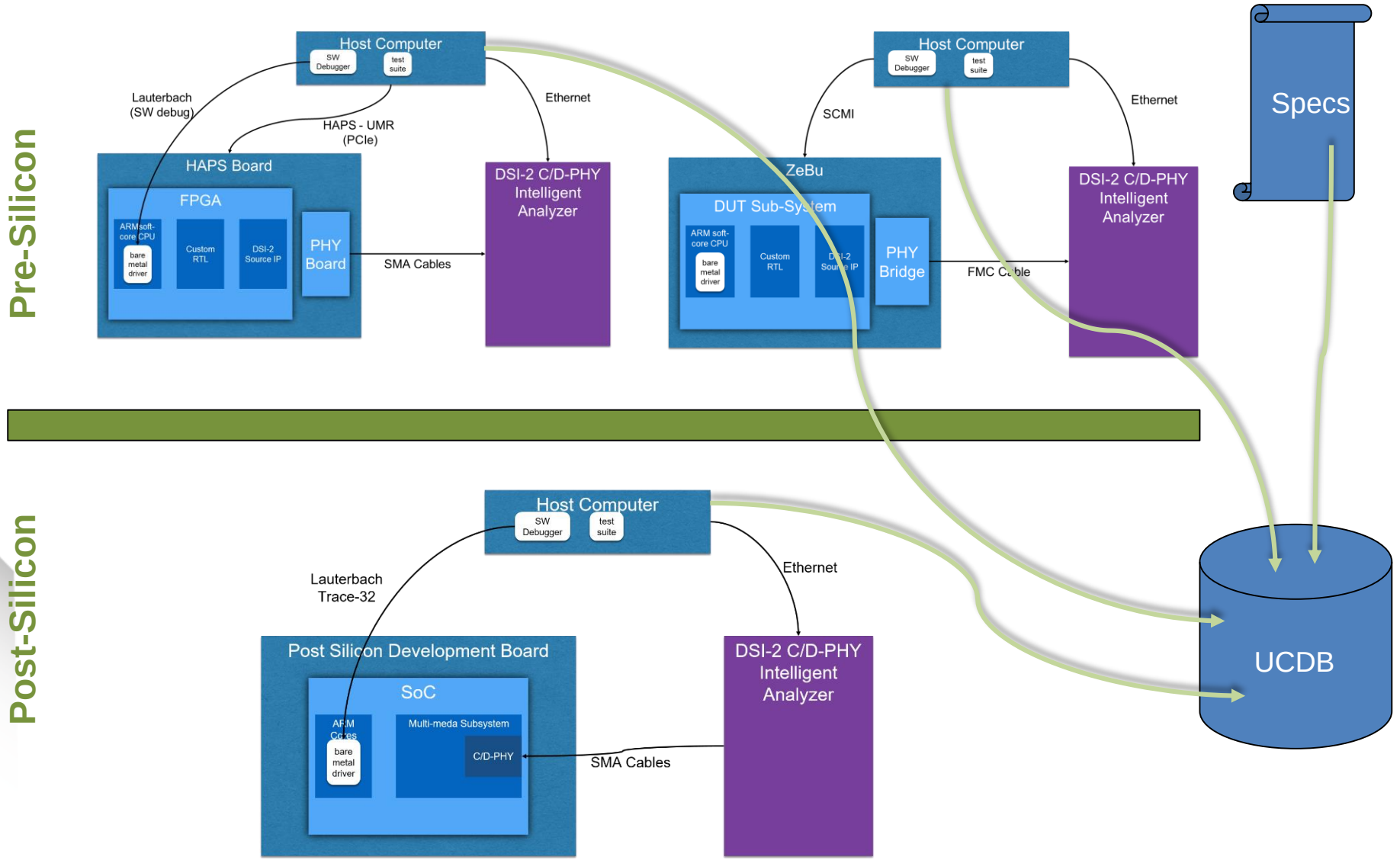
BUT

- **No clear idea what to measure**
  - Even in pre-silicon let alone post-silicon.
  - Different people have different ideas.
- **Need coverage to know when you're done.**
  - Most of the time we struggle with the definition.
  - Very subjective.
- **Very difficult to directly view the nature of electrical problems.**
  - Two classes of bugs caught in PSV
    - Functional
    - Electrical (not necessarily manufacturing defects, but rather design defects).

Latest Activities

- **Finished the first cut at the industry survey**
  - Organized the data points and prioritized
  - Started assigning owners to tasks based on interest
- **Identified primary focus areas …**
  - Power - functional measurements vs spec.
    - Automated way to match spec to characterization activities
  - Have test equipment / protocol analyzers capture state that can roll up to an overall coverage DB
  - SW driver coverage of HW features
  - How do you automate functional coverage points from specs
    - Pre-silicon to post-silicon
- **… and secondary focus areas**
  - Portable stimulus for full-chip, emulation, PSV covering the same thing
    - Useful for low-power measurements and additional coverage
- **Started working**
  - Recommendations now, looking at standards longer-term
  - Use case descriptions and implementation details

Pre- to Post Silicon Validation Coverage



Software Driver Coverage Initiative

- **Starting point**
  - Hardware features list (Master Coverage Plan)
    - Simple IP coverage, mixed cross IP coverage, or stress related definitions
  - Knowledge Base with set of rules based on architecture
    - Also can be generic in nature
  - Register database for IPs
  - Two types of stimulus, where
    - Code instrumentation is allowed
      - **Randomized test code written in PSV environment and controllable**
    - Standard software drivers which may be read-only code
- **Run and post-process**
  - Generate runtime logs based on code instrumentation to post process
    - Define a standard format
  - Leverage Debug Logic present in modern SoC's
    - Trace and event capability
    - Used where code instrumentation is not possible
  - Post process instrumented logs/traces/events
    - Compare with knowledge base to extract coverage information & register in UCDB

Emulation to Post Silicon Initiative

- **Coverage Methodology which Spans Emulation and Silicon**
  - Starts with the spec!
  - Flow defined from Coverage Event Definition to Register Data Collection
  - Post-silicon event baseline and readiness
    - Register Coverage, Cross functional Event definition
  - Automated pre-silicon coverage collection on emulation
  - Automated post silicon coverage collection on post silicon platform

- **Run and post-process**
  - Event Validation on emulation and mapping to Test Content
    - Add to UCDB
  - Post Silicon coverage collection of events and register UCDB

Test Instruments Initiative

- **Addresses the following areas**
  - Test abstraction levels
    - IP, subsystem, system
  - Various configurations
    - Bare metal, diagnostic, HW/SW, product
  - Types of test
    - Low-level, performance, power, use-cases
- **Test equipment / protocol analyzers capture state**
  - That can roll up to an overall coverage DB
  - That aligns with the overall validation plan of the SoC
    - Pre-silicon to post-silicon
    - Across verification/validation platforms
- **Run and post-process**
  - Run with one or more coverage enabled test instruments
    - Download event state and test/DUT configuration
  - Post-process across interfaces, configuration, events, and time
    - Register with UCDB that encompasses pre-silicon and post-silicon

Interested in Contributing?

- **SVDTC currently has these key working groups**
  - Validation Analytics
  - Array & Scan dumps
  - Validation Standards
  - Post-silicon/FW debug

- **Validation Coverage WG can use help too**
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- **Test Instruments that allow pre- to post-silicon leverage NOW for**
  - Test content
  - Coverage
  - Debug

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