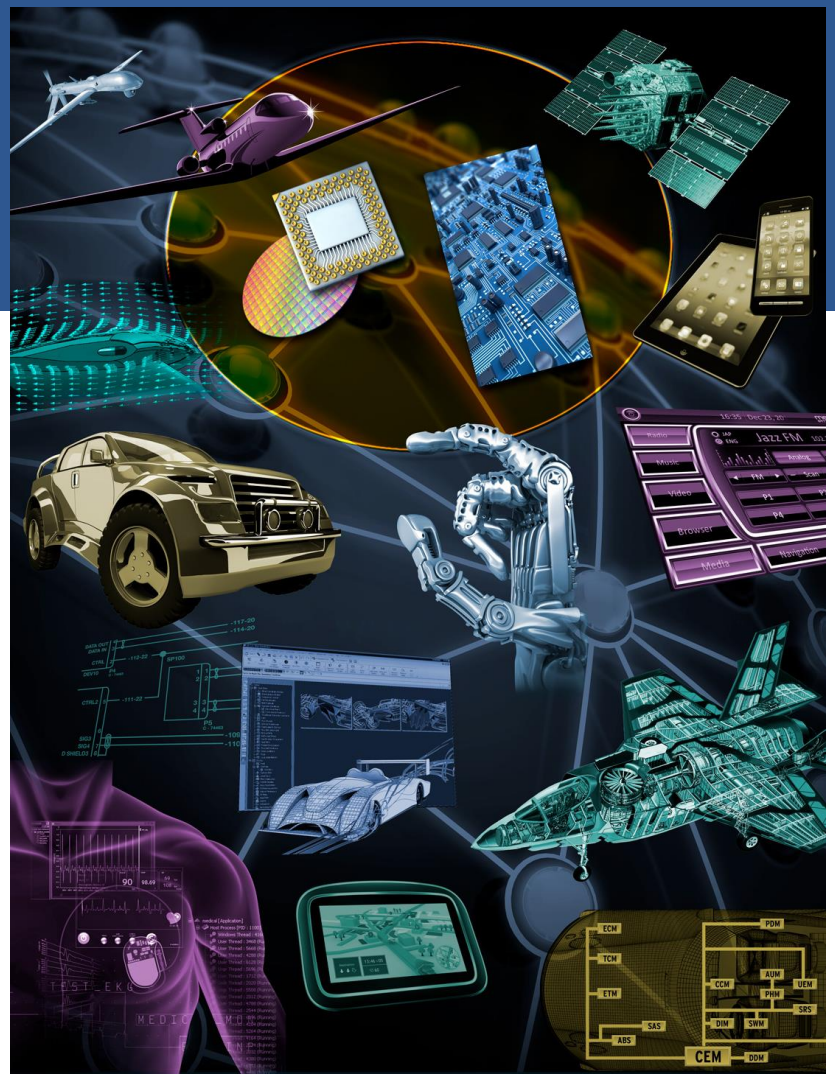

Design to Manufacturing Considerations in 3D IC Design

Juan C. Rey

Vice President of Engineering

Calibre – Design to Silicon Division

Mentor, A Siemens Business

September, 2017

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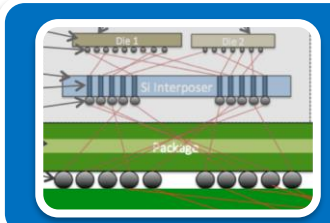
Overview

- Extensions to established physical verification flows:
  - Chip-Package Co-design
  - Expanding from IC to Assembly-Level PDKs
- Design for Test and 3D
- The Known-Unknowns (aka "I know I can calculate this – but, do I really need to do it?")
  - Parasitic Extraction
  - Sahara: Thermal Analysis
  - Glacier: Stress Effects
  - Electromigration
- Summary

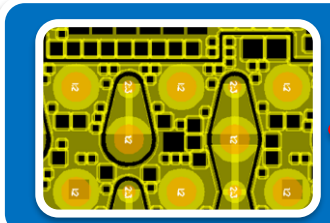
EXTENSIONS TO ESTABLISHED PHYSICAL VERIFICATION FLOWS

Design and Verification Challenges for High-density Advanced Packaging (HDAP)



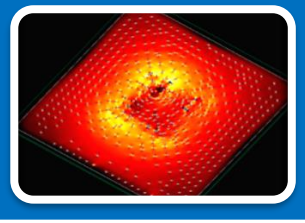
2.5D/3D multi-substrate/device architectures

- Connectivity & interface planning across substrate boundaries
- Assembly level verification, and electrical extraction/analysis



Physical implementation of new technologies

- Shrinking feature sizes and new geometries
- Increasing pin counts on devices and overall design



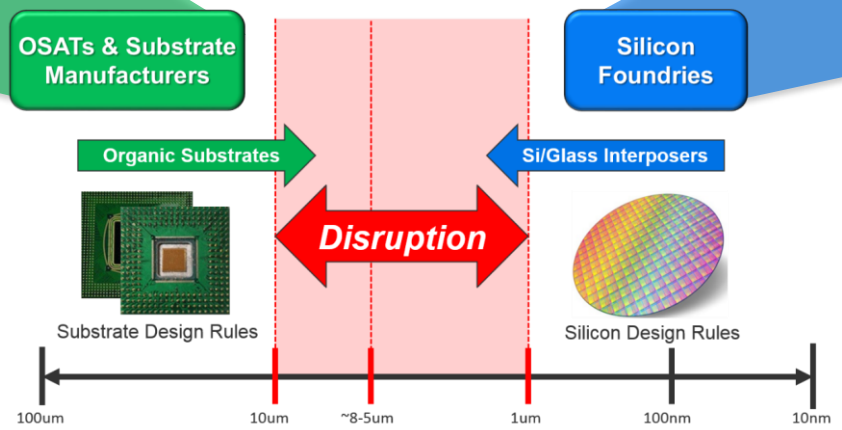
Final sign-off and verification

- LVS/LVL on both final assembly and individual substrates
- Assembly level electrical and thermal performance

2.5D/3D Technologies are Part Silicon Part Package with Different Design Methodologies and Characteristics

- Gerber output
- Windows based tools
- Design drives manufacturing
- Non-Manhattan shapes
- Organic RDL layers
- Built-in DRC checks performed within design database

- GDSII output
- Linux based tools
- Manufacturing drives design (PDKs)
- Manhattan based shapes
- Silicon RDL layers
- Separate verification (DRC) performed on mfg. output



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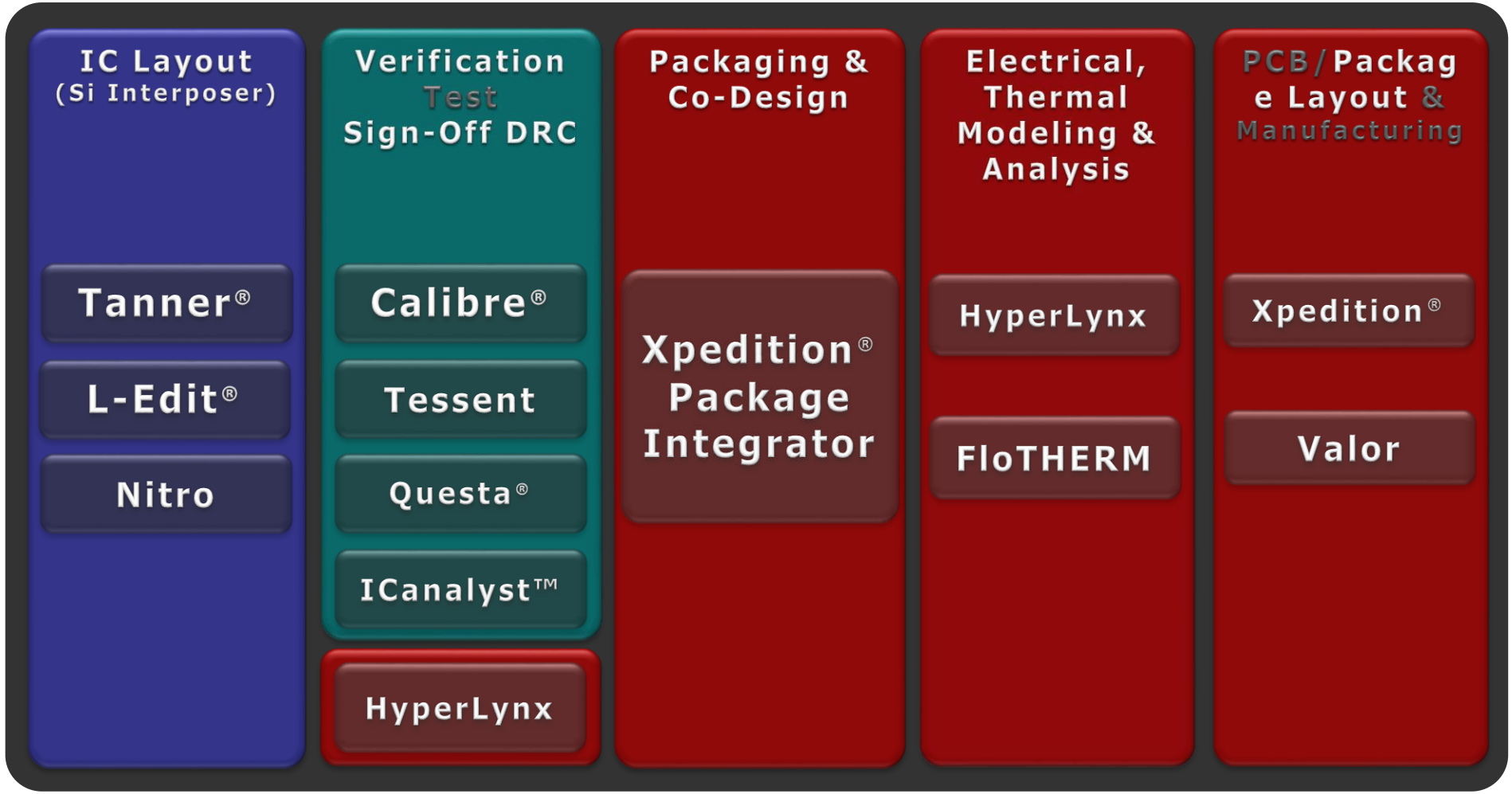
Mentor Solutions for Advanced Packaging and Co-Design



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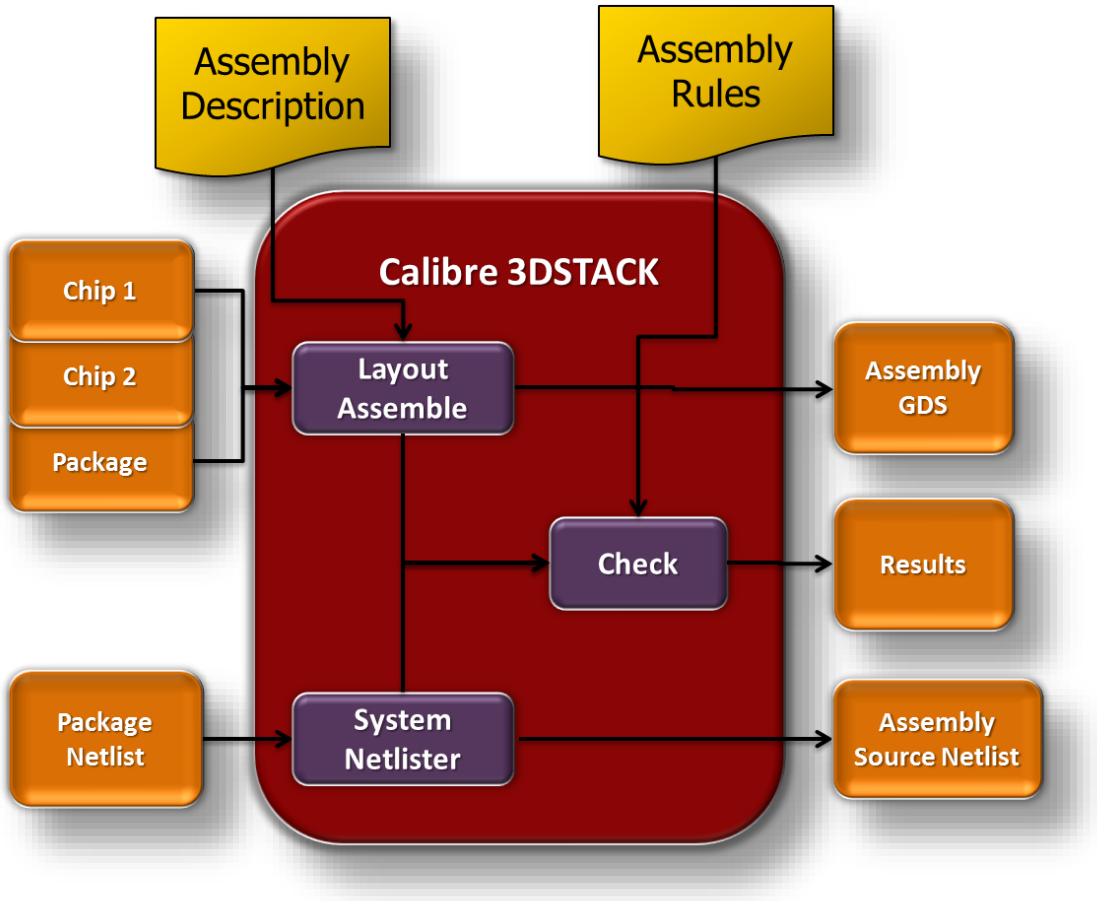
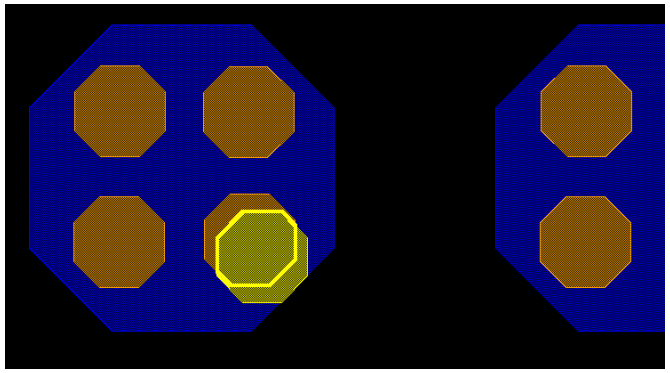
Package Sign-Off: Calibre 3DSTACK



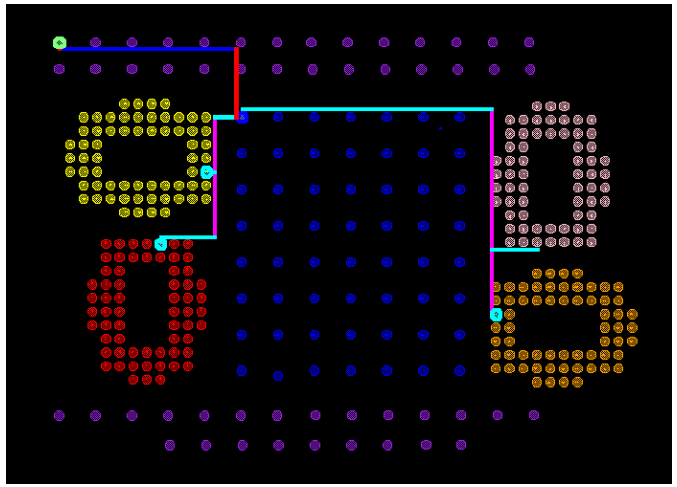
- Manufacturing DRC
  - Package checks
  - Die-Package checks
  - Process independent
  - Curve sensitive
- Signal Integrity
  - CSV, AIF, Spice, Verilog
  - LVS through package
  - Package level PEX

Physical Verification Checks

- Physical Checks (DRC)
  - Geometric overlap constraints
  - Center to center alignment
  - Grid and spacing constraints
  - User defined checks from SVRF/TVF



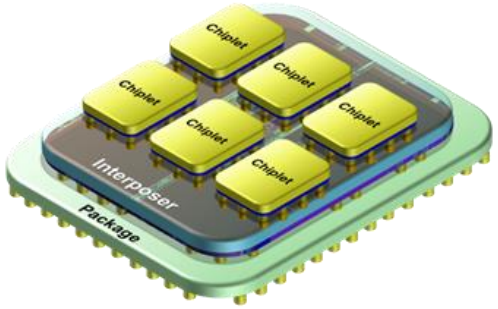
- Logic Checks (LVS)
  - Identify mismatch connections
  - Pad label checks
  - Layout ports not in the source

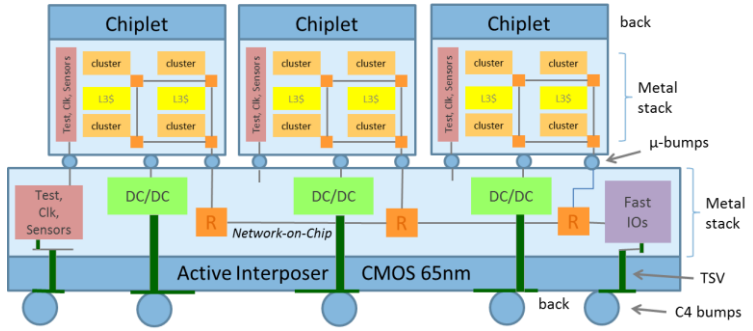


- Location Checks
  - Verify every location for each electrical pin
  - Associated with package netlists (aif, spreadsheet)

3DSTACK Success Story

- Leti proceeded to final 3D verifications before sending INTACT.gds to the ST fab
  - 65nm Interposer
  - Black box: chiplet to interposer connections successfully validated
  - White box: chiplet to chiplet connections found isolated and shorted bumps
- Customer experience
  - Avoided the tape out of a bad design
  - Would have lost ¼ of the functionality
  - Would have lost months of schedule and $$$
- Now a mandatory step!





NANOELEC.

IRT Nanoelec open 3D Program

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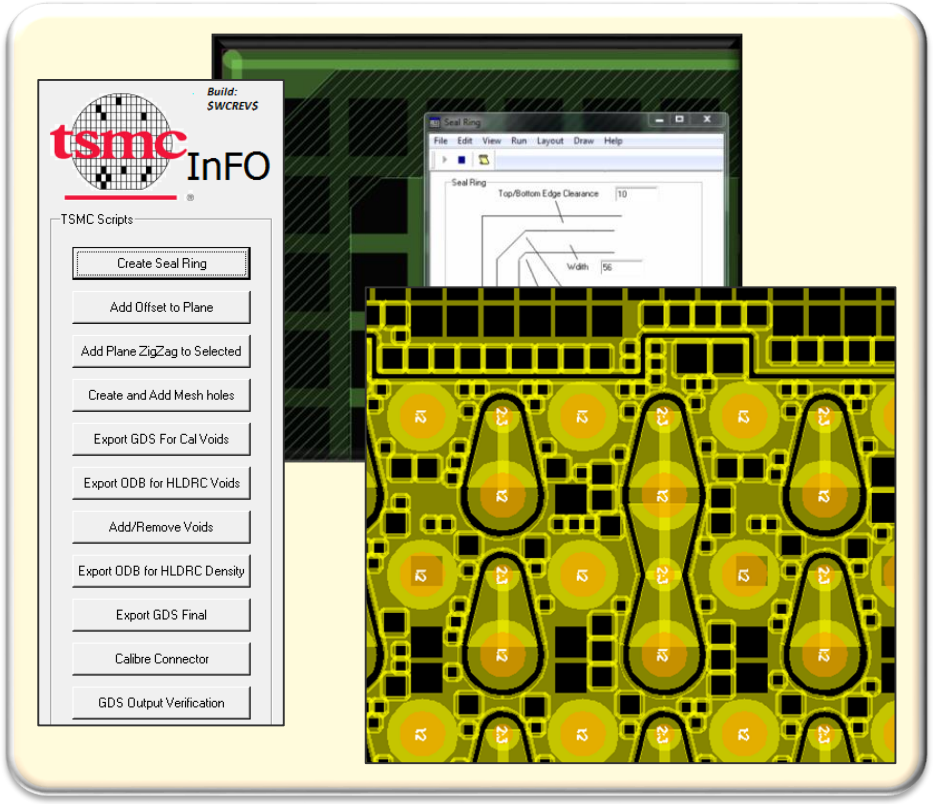
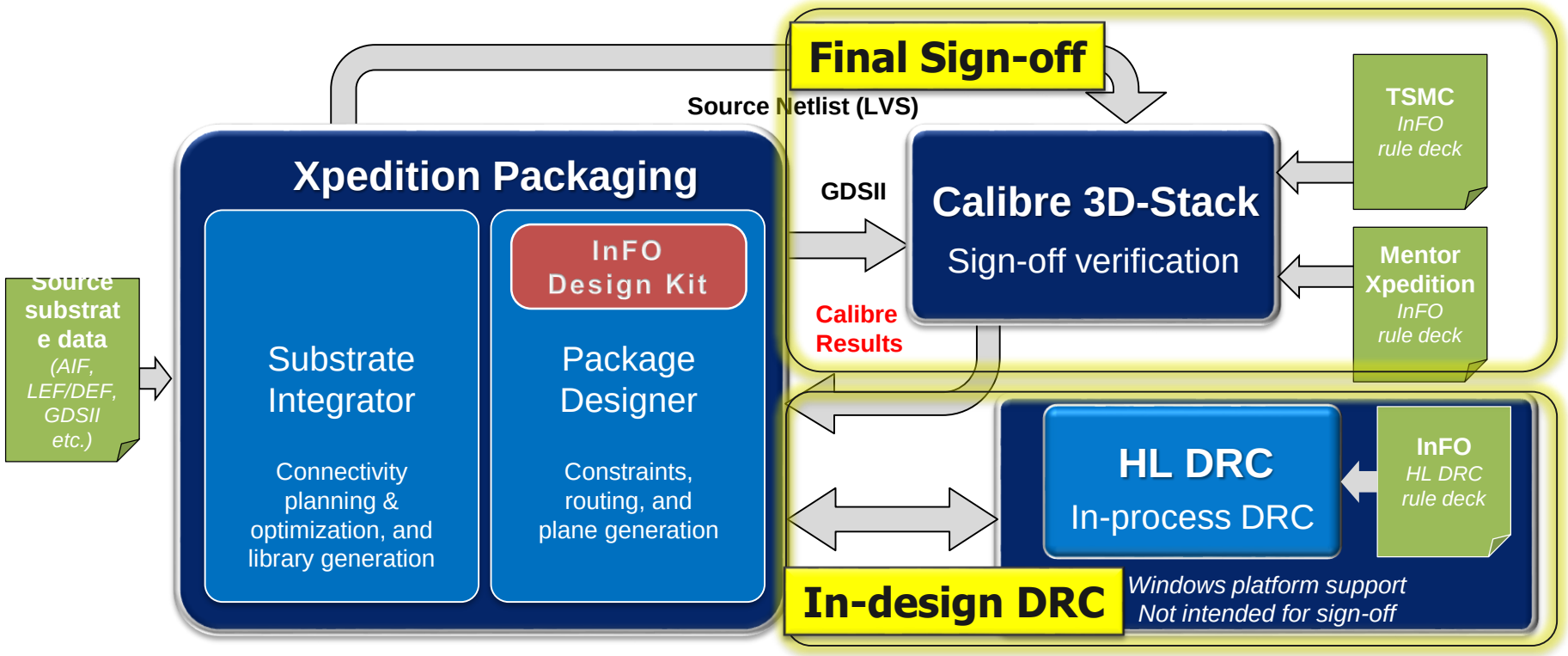
TSMC/Mentor InFO Design Kit
Specialized functionality in a comprehensive flow



- InFO specific PDK and templates
- Produces the unique geometries necessary for InFO manufacturing
- Automated stress relief features – mesh pads, zig-zag, and graduated degassing
- Fast optimized GDS output with accurate representation of non-Manhattan geometries
- Comprehensive LVS/LVL assembly level verification using Calibre 3DSTACK with real-time Xpedition integration

TSMC Certified InFO Design and Verification Flow
InFO_S & InFO_POP Certified



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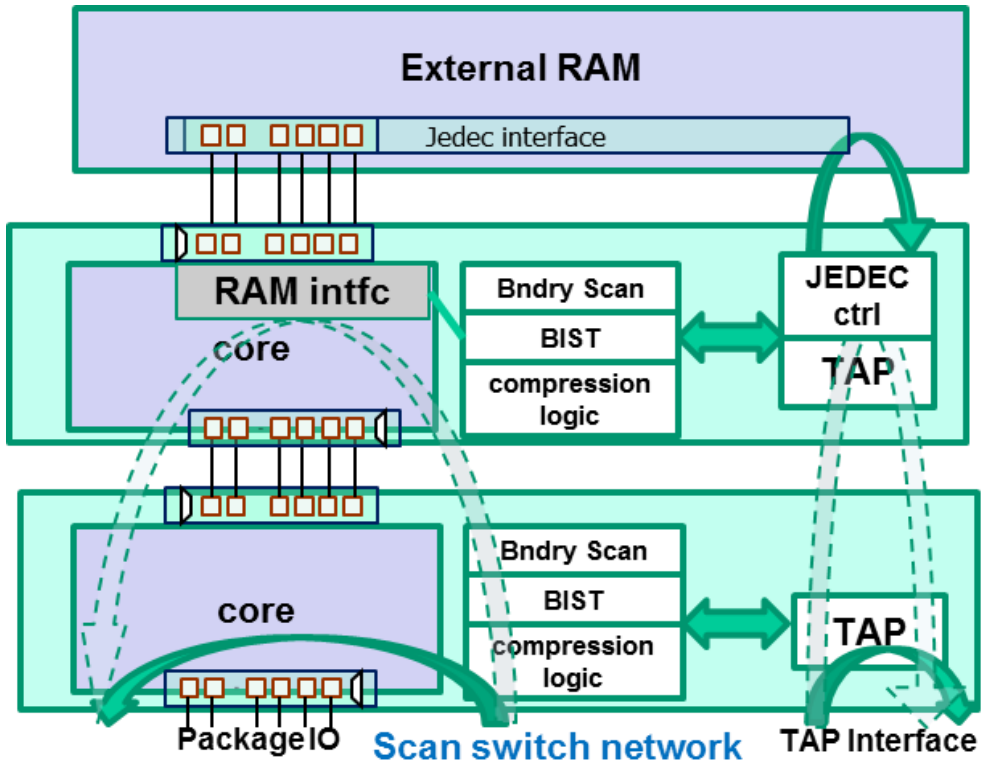
DESIGN FOR TEST AND 3D

Overview

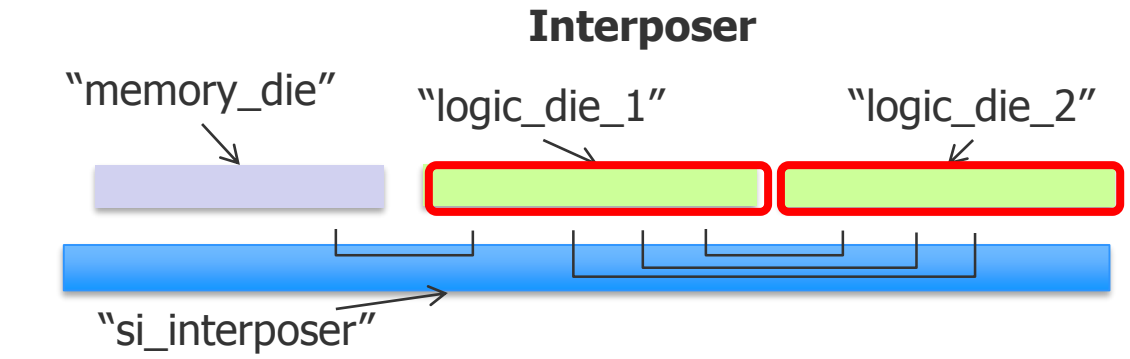
- Extensions to established physical verification flows:
  - Chip-Package Co-design
  - Expanding from IC to Assembly-Level PDKs
- Design for Test and 3D
- The Known-Unknowns (aka "I know I can calculate this – but, do I really need to do it?")
  - Parasitic Extraction
  - Sahara: Thermal Analysis
  - Glacier: Stress Effects
  - Electromigration
- Summary

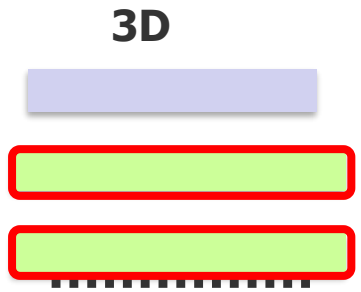
Test Solutions for 2.5/3D

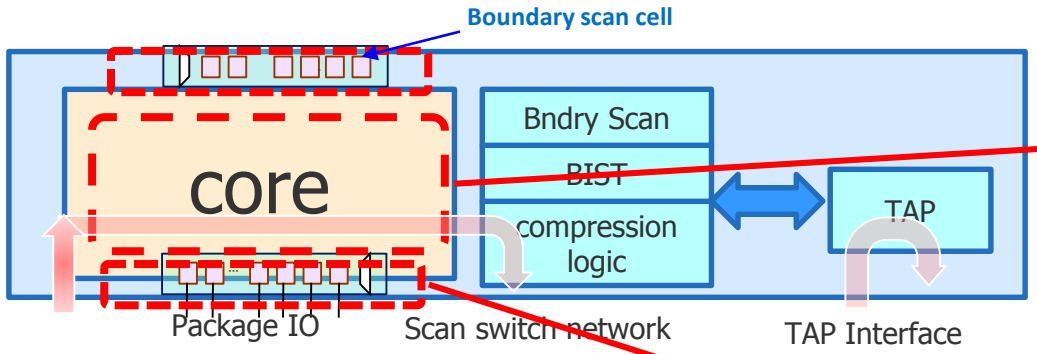


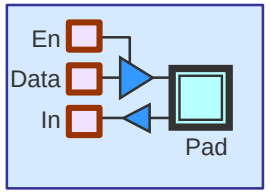
- Key requirements for 3D testing
  - High quality test for known good die
  - Test access to die in package
- Plug-and-play Hierarchical DFT is critical for efficient implementation
  - Allows complete DFT signoff at core level
  - Seamless DFT integration at Chip and Chip-stack level
  - Eliminates redundant test generation
  - Enabled by widely used IJTAG and Pattern Retargeting solutions for SoC
- Solutions and TSMC CoWoS reference flow available

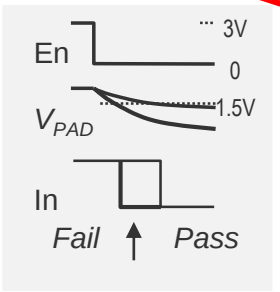
Pre-bonding Test











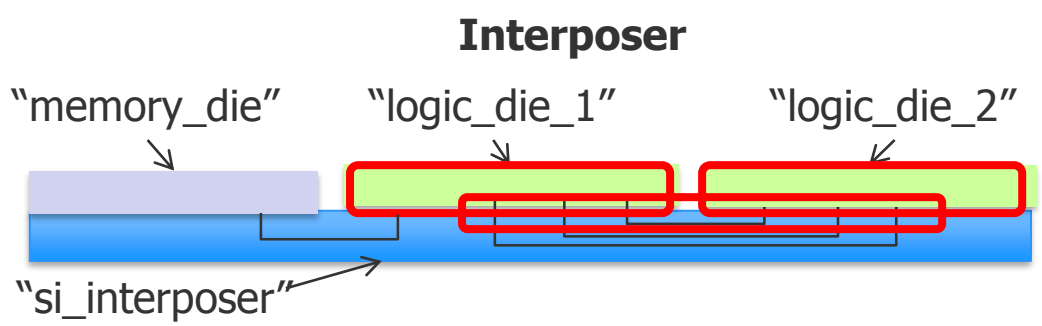
Die Level Test

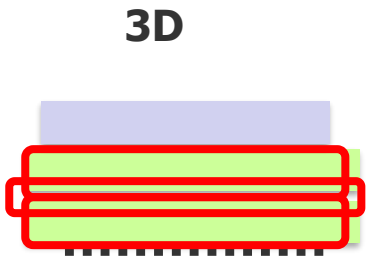
- Compression ATPG
- BIST (memory, logic)

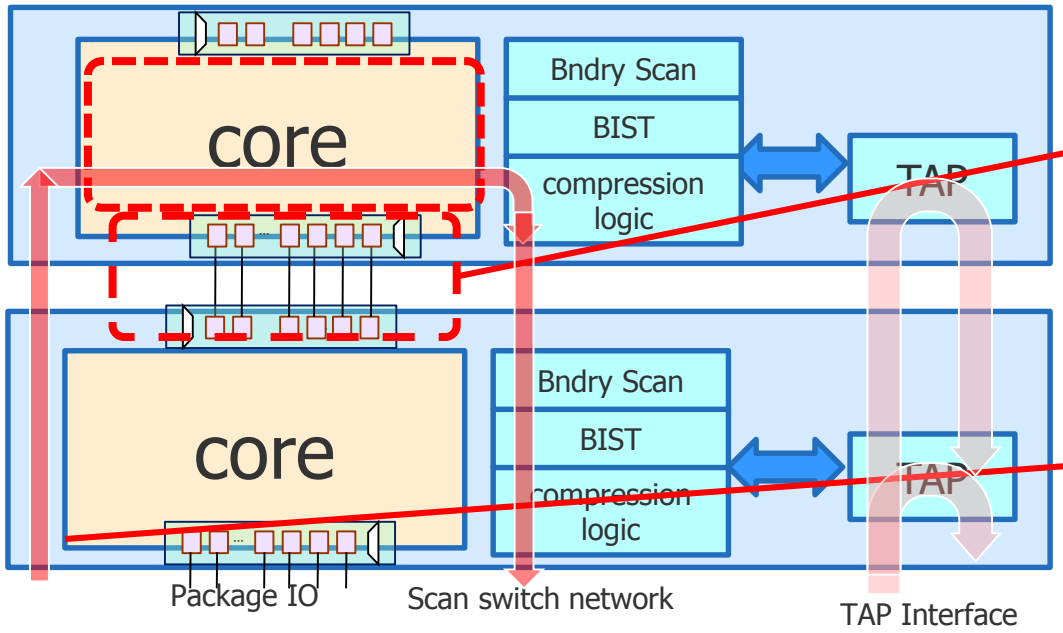
IO Wrap & Contactless IO Test

- Bidi JTAG for each die IO
- Leakage check and verify bidi operation

Post-bonding Test: Logic-to-Logic







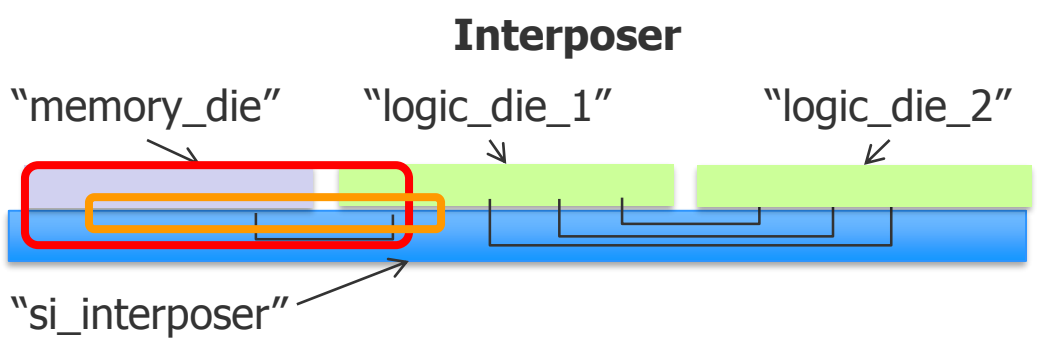
Interconnect Test

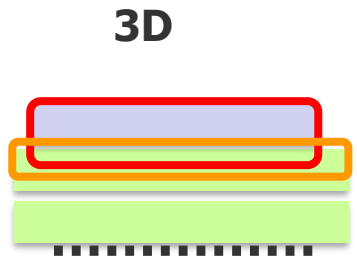
- IEEE 1149.1 approach
- Test TSVs/interposer – open & short

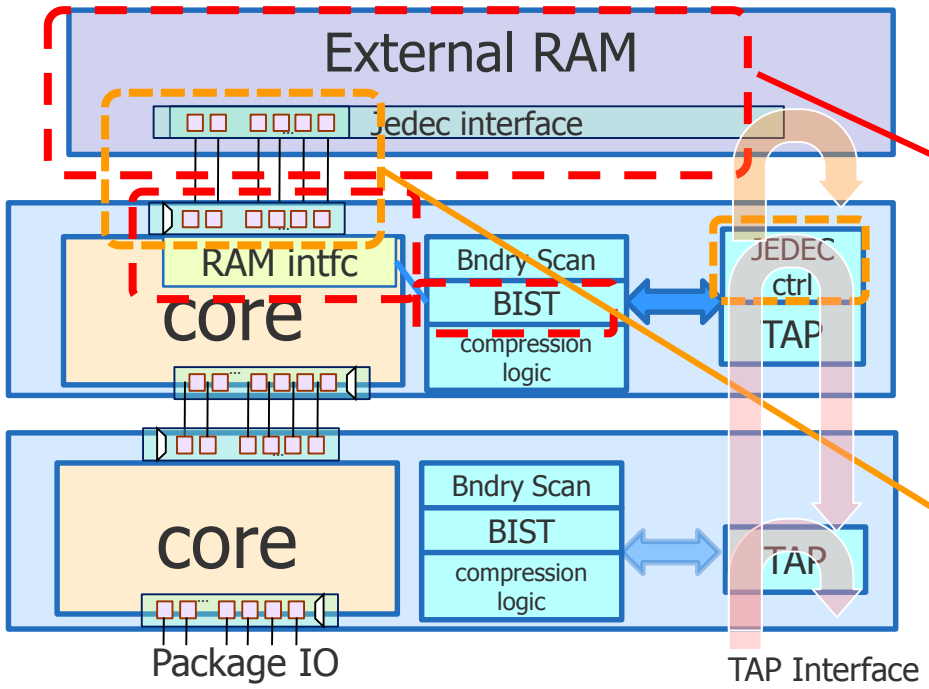
Pattern Retargeting

- Die level patterns retargeted to package

Post-bonding Test: Logic-to-RAM







External RAM Test

- Based on Tessent MemoryBIST
- Random data memory BIST

Logic to RAM Interconnect

- Control JEDEC cells in RAM die
- Control logic for JEDEC on top logic die

THE KNOWN-UNKNOWNS

Overview

- Extensions to established physical verification flows:
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  - Glacier: Stress Effects
  - Electromigration
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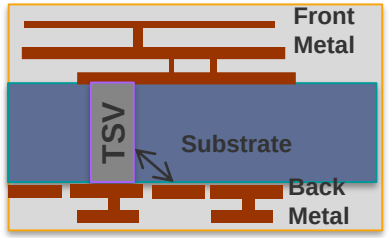
Extraction of TSVs and TSV to RDL couplings Mentor – Georgia Tech joint Project

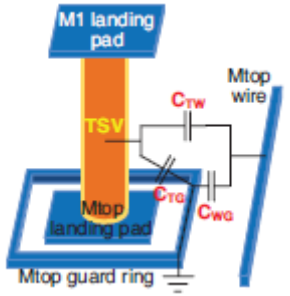
- Analyze, Model and Extract TSV to interconnect extraction
- Significant impact of TSV to RDL coupling on the design parameters

TABLE I
TSV-TO-WIRE COUPLING FULL-CHIP IMPACT.

Is TSV-to-wire included?	no	yes
Longest path delay (ns)	4.48	5.08 (+13.4%)
Total power on TSV net (mW)	0.303	0.356 (+17.6%)
Total net switching power (mW)	2.42	2.50 (+3.3%)
Total noise on TSV net (V)	32.5	78.2 (+104%)



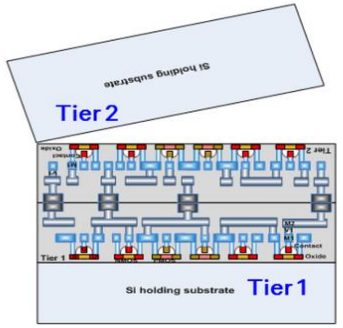
- Proposed methodology to reduce the impact of TSV to RDL coupling
  - Keep out zone
  - Guard ring



- Yarui Peng, Taigon Song, Dusan Petranovic and Sung Kyu Lim, "On Accurate Full-Chip Extraction and Optimization of TSV-to-TSV Coupling Elements in 3D ICs," IEEE International Conference on Computer-Aided Design, 2013.
- Yarui Peng, Taigon Song, Dusan Petranovic, and Sung Kyu Lim, "Silicon Effect-aware Full-chip Extraction and Mitigation of TSV-to-TSV Coupling," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 33, No. 12, pp. 1900-1913, 2014.
- Yarui Peng, Dusan Petranovic, and Sung Kyu Lim, "Fast and Accurate Full-chip Extraction and Optimization of TSV-to-Wire Coupling," ACM Design Automation Conference, 2014.
- Yarui Peng, Dusan Petranovic, and Sung Kyu Lim, "Multi-TSV and E-Field Sharing Aware Full-chip Extraction and Mitigation of TSV-to-wire Coupling," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 34, No. 12, pp. 1964-1976, 2015

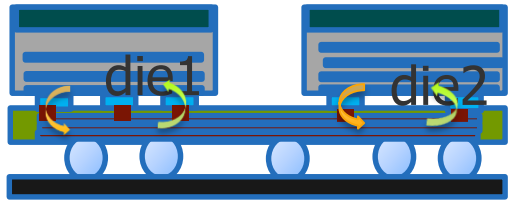
Wafer-on-Wafer (WoW) and Fan-Out Wafer-Level-Packaging Cooperation with Georgia Tech

- Parasitic extraction in Face-2-Face bonded dies
  - Mentor joint work with Georgia Tech and Qualcomm
  - Inter-die capacitance becomes important when die-to-die distance is small, in face-to-face (F2F) bonded structures with direct copper bonding
  - In-Context extraction methodology proposed



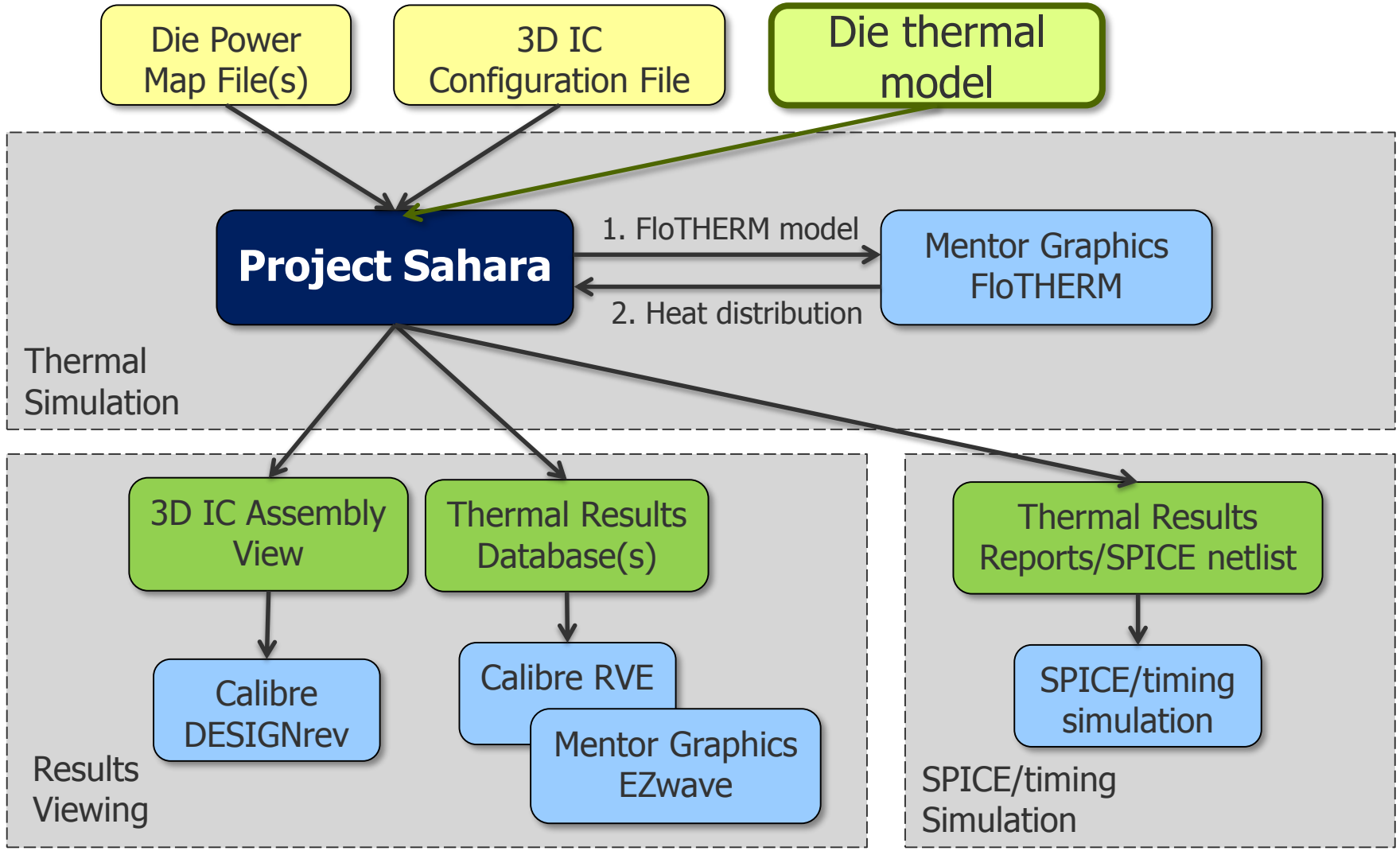
- Yarui Peng, Taigon Song, Dusan Petranovic, and Sung Kyu Lim, "Full-chip Inter-die Parasitic Extraction in Face-to-Face-Bonded 3D ICs," IEEE International Conference on Computer-Aided Design, 2015.

- FO WLP: Extraction of die-package interaction
  - Analyze impact of capacitive and inductive couplings between the dies and package on the system design parameters
  - Inductive couplings might be more significant
  - Methodology to extract the couplings proposed



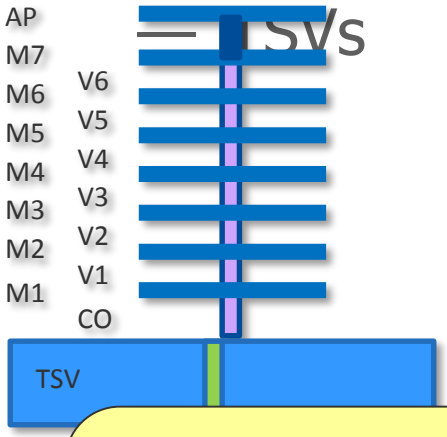
- Yarui Peng, Dusan Petranovic, and Sung Kyu Lim, "Die-to package RCLM Extraction and Signal Integrity Co-Analysis for Fan-out Wafer-Level-Packaging," submitted for Design Automation Conference, 2017.

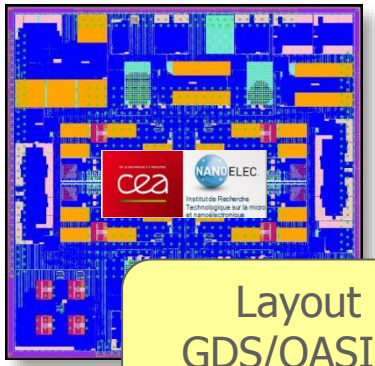
Thermal Simulation with Die Thermal Model



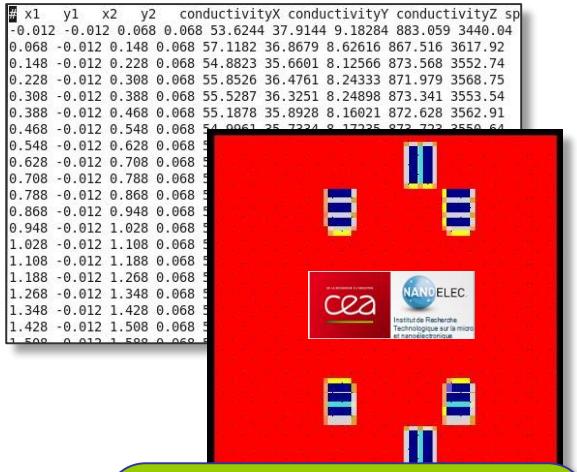
Effective Thermal Properties Extraction

- Accounts for non-uniform thermal properties in the die
  - Metallization
  - TSVs





Layout
GDS/OASIS/
LEF-DEF



Property Extraction Configuration file

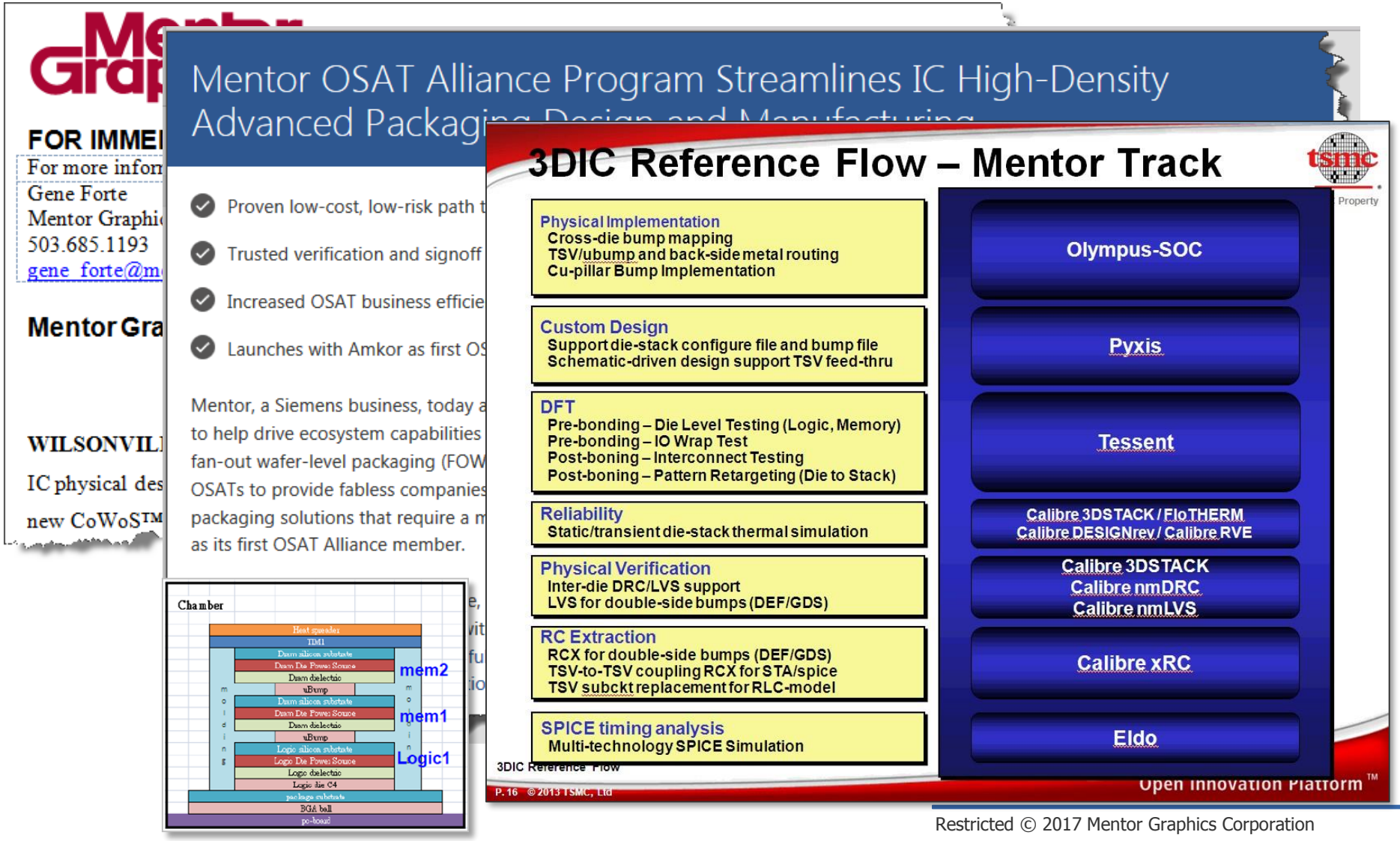
- Layer sequence, direction, thickness, thermal properties, binning size

Project Sahara

Thermal Properties File

- heat conductivity, heat capacity, density

Calibre in TSMC Reference Flow



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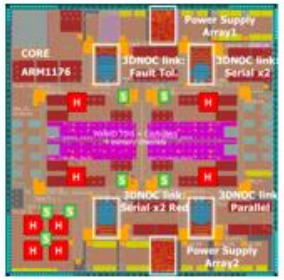
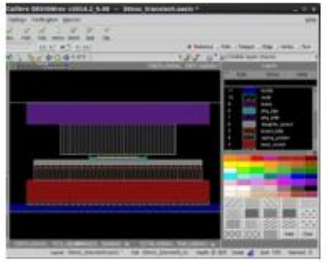
3DNOC: Thermal Analysis with Sahara & Correlation

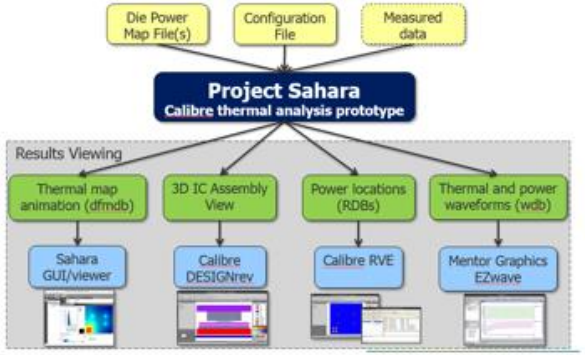
- 3D Thermal Simulation of the 3D Stack
  - Using Calibre® thermal analysis prototype
  - *New feature to visualize measurement data*



3DNOC Circuit , with 2 layers :
- *8 Heaters (up to 8 Watts)*
- *7 Thermal Sensors per die (1°C accuracy after calibration)*



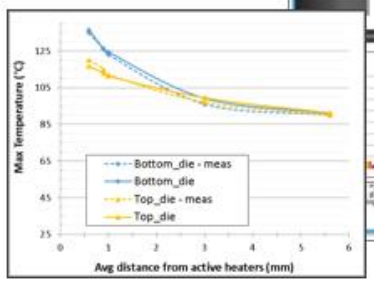
3DNOC Thermal Model



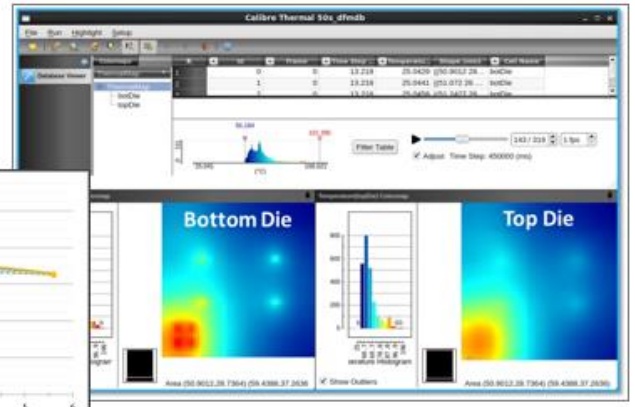
3D Thermal Analysis (Calibre® thermal analysis prototype)

Simulation ⇔ Measurement correlation:
- **2% error for steady state analysis**
- **Similar time constant for transient analysis**

[*P. Vivet et al.*, in ISSCC'16]



Thermal impact of a 370 Watt/cm² Hotspot
15°C difference between bottom & top dies



3DNOC Thermal Maps (bottom & top dies)

Project Glacier - Technology

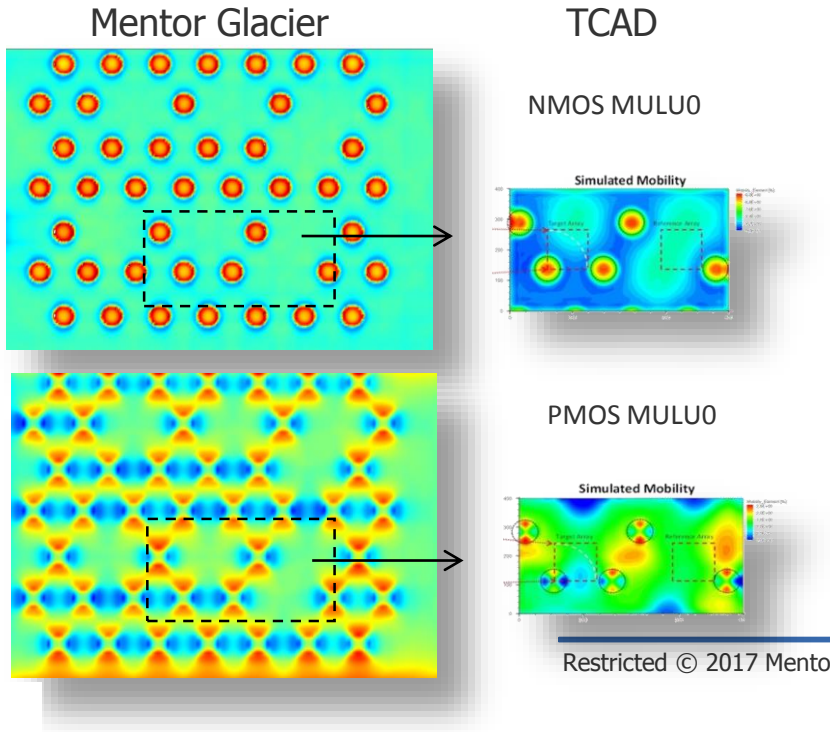
- Developed a prototype that will analyze layout for unexpected CPI stresses and impact on device performance
  - Floor Planning
  - Course and detailed drill down
- Rationale for development
  - CPI mechanical stress effect on MOSFET/FinFET characteristics
    - Stress generated by warpage of thin dies, TSV and solder bump-induced stresses
  - New CPI stresses have a global character and penetrate long distances
  - Traditional FEA-based tools cannot help due to the long range analysis needed
  - Empirical models cannot handle the wide range of variations
  - Large keep out regions are too expensive to die area
- Verified in multiple customer test cases

Project Glacier - Customer Results

- Customer benchmark: (Design - N28, 7.5mm x 5.7mm)

Flow	Tool Flow	Runtime (# CPUs)	Memory requirement (MB)
LEF/DEF Flow	Coarse Screening (averaged metal densities)	11 min. (4)	312
GDS/Oasis Flow	Coarse Screening	4 hrs (4)	8,722
	Detailed Analysis on (0.3 mm x 1 mm)	5 hrs (4)	2,006

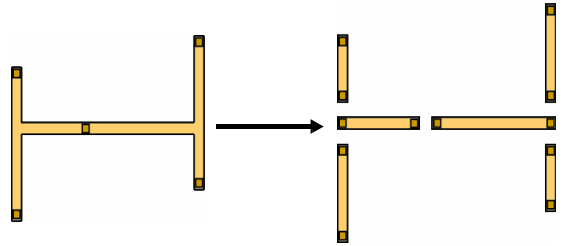
- Glacier:
  - TCAD accuracy
  - Full chip capacity



Electromigration Assessment

- Industry wide accepted electromigration (EM) assessment methodology is based on decomposition of interconnect metal grid on the individual segments and assessing them individually with the calibrated Black's equation.

$$MTF_{USE} = MTF_{TEST}\left(\frac{j_{USE}}{j_{TEST}}\right)^{-n}\exp\left\{-\frac{E_A}{k_B}\left(\frac{1}{T_{USE}}-\frac{1}{T_{TEST}}\right)\right\}$$

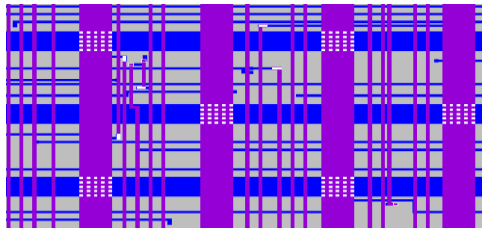


- It results a very little margin between the designed in current densities and that allowed by EM design rules, which makes a chip design sign off as very difficult task.

$$j_{USE} = j_{TEST}\left(\frac{MTF_{TEST}}{10\,years}\right)^{\frac{1}{n}}\exp\left\{-\frac{E_A}{nk_B}\left(\frac{1}{T_{USE}}-\frac{1}{T_{TEST}}\right)\right\}$$

- This problem is caused by the inaccurate and oversimplified nature of EM models used by existing tools, mainly due to ignoring the material flow between branches as well as the mesh structure of modern power grids characterized by an inherent redundancy.

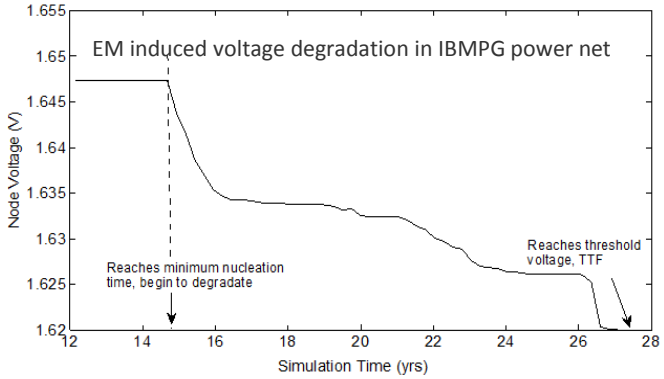
- This calls for significant over-design. We found that the pessimism is very high: grids that must survive 10 years, are being designed to survive ~ 40 years. It leads to overuse of metal area, leaving little room for signal routing, which makes EM signoff extremely difficult in modern designs, thus increasing design complexity and design time.

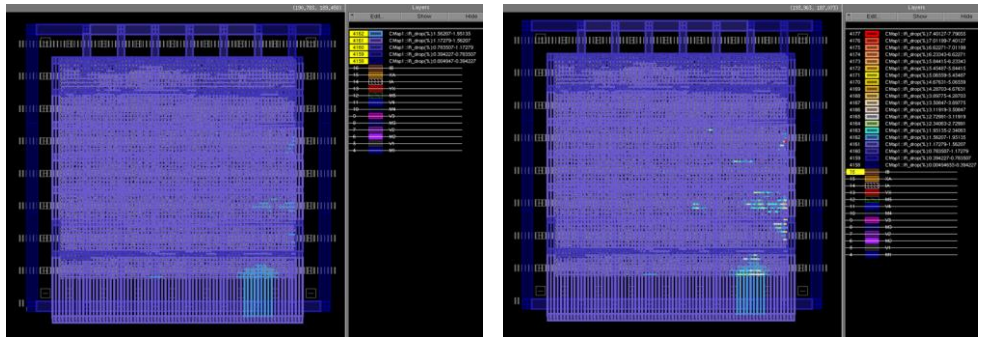


- Traditional empirical models are no longer sufficient and we need better physical models.

IR-Drop Degradation = EM Failure

- As an alternative to the current EM assessment methodology Mentor had developed the EM mesh model to account for the redundancy and material flow between mesh segments.
- Key feature: Grid is deemed to fail when the voltage drop at any grid node exceeds a user specification, not when the first line fails.
- Major function of the p/g grid is delivering voltage (V_{dd} and V_{ss}) to every gate. EM induced resistance degradation can affect this functionality.
- Voiding induced increase in the resistance of p/g segments is responsible for IR-drop increase, which can result a parametric failure.





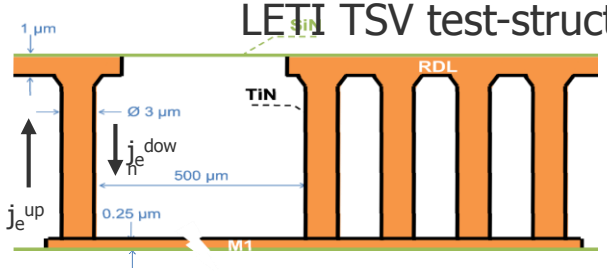
Initial (left) and final (right) IR drop distributions in 32 nm test-chip.

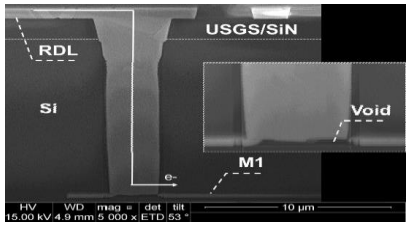
- **The EDA tool-prototype for fast and scalable EM checking in on-chip power grids including 3D IC is available: Project Denali.**

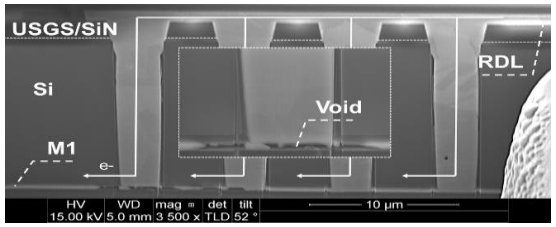
EM Assessment for 3d IC Test-Structure

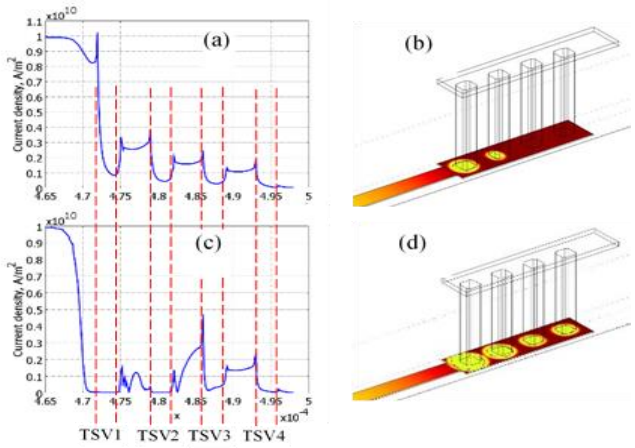
- **As an example we can consider the EM assessment performed on LETI 3D IC test-structure with the standard Black's model and Mentor's Denali approaches.**

LETI TSV test-structure for up- and down-stream currents

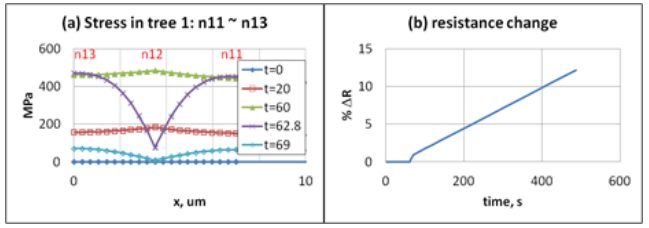








FEA results for up-stream configuration showing (a) initial current distribution, (b) first TSV failure, (c) current distribution after failure of two TSVs, and (d) the circuit failure. A color map in (b) and (d) corresponds to the value of hydrostatic stress: yellow is zero, the darker red means higher tensile.



Denali's (finite-difference) based simulation results for downstream case: (a) stress evolution in M1 tree, and (b) resistance vs. time.

Atomic flow	TTF summary			
	Black's Model	FEA ,a.u.	Finite-difference, a.u.	Experiment, a.u.
DOWN	204	204	**463**	204
UP	204	592	**1711**	749
UP / DOWN	1.0	2.9	**3.7**	3.7

Black's model determines TTF at weakest branch, which is identical for both current directions: it fails to account for parallel paths in upstream case.

SUMMARY

Summary

- The multiple 2.5D-3D flavors bring new challenges to package and IC designers
- Physical Verification activities such as Design Rule Checking and Layout Vs Schematics have been naturally extended and have been encapsulated in Assembly Development Kits
- Design for Test IC methodologies are well established for memory-on-logic. Ready for test for logic-on-logic
- Multiple physical effects that are been impacted by the smaller dimensions between multiple dice and interposers (such as variations on R/C/L, impact of stress on carrier mobility, thermal variations, electro-migration) can be accurately modeled and with the required performance –
  - if and how they will impact design flows and activities is still an open question

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