Multi-Die Production Test Challenges

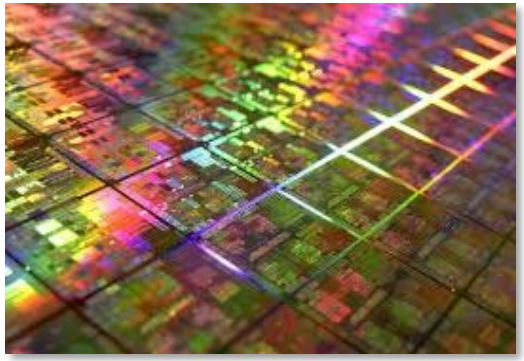
HC Peng l Director, Test Business Development

Gerard John l Sr. Director, Advanced Test

Agenda

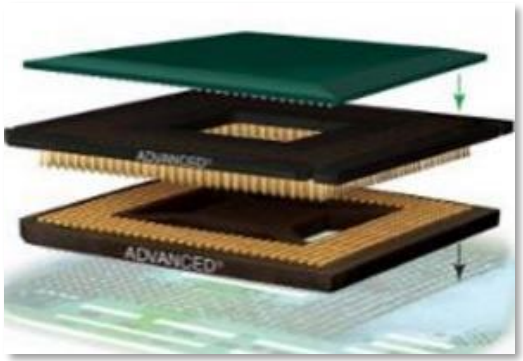
- Reason for Test
- Advanced Packaging = Advanced Test
- Factory Mindset
- WS/FT/SLT Capabilities
- Summary

Why Test? – Process Imperfections



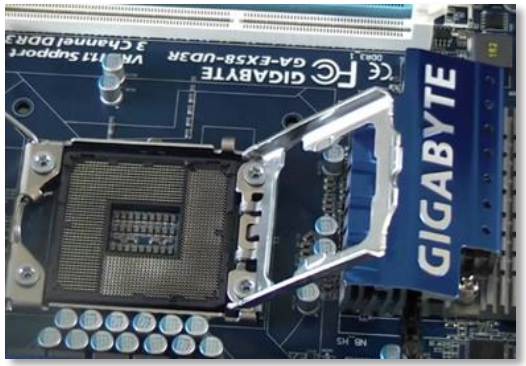
Wafer Sort

- Verify the fab'd die functions as per design



Final Test

- Verify package assembly
- Validate device functionality & performance

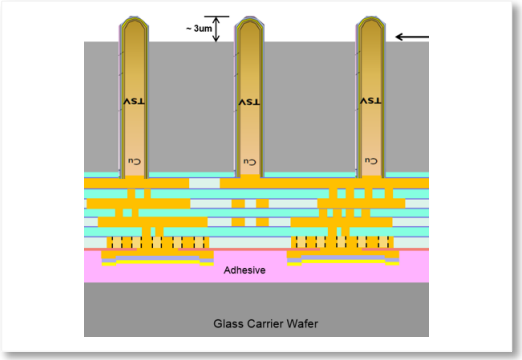


System-Level Test

- Validate device functionality in final application board

How much to test? **Just enough to know with confidence the device under test is good!**

New Assembly Techniques = New Test Challenges

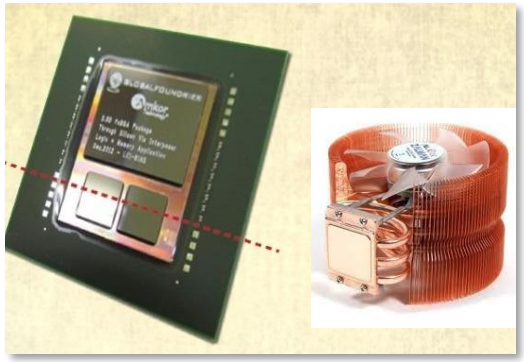


Interposer Test

- Known good interposer
- Test techniques

Small Pad Size & Pitch

- Active die attach to micro bump (~20 µm)
- Current capability 30/50 µm



Lower Scrap Cost

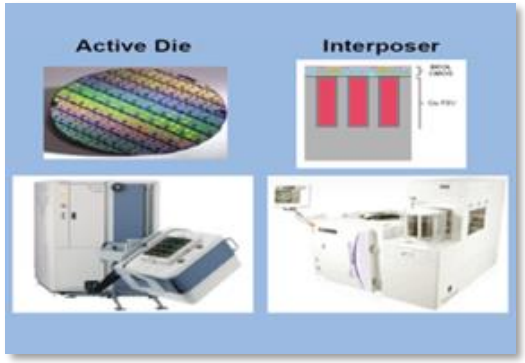
(find assembly defects early)

- Partially assembled test
- Heat dissipation

Factory Mindset

- Buy more of the same (equipment)
- Look for multiple uses for each buy
- Shun “One-Trick Ponies” such as double sided probers
- Reuse existing equipment with minor modifications or minimal upgrades

Adapting Existing Test Equipment



Wafer Sort & Interposer Test

Upgraded tester to support higher speed & increase prober accuracy

Partially Assembled & Final Test

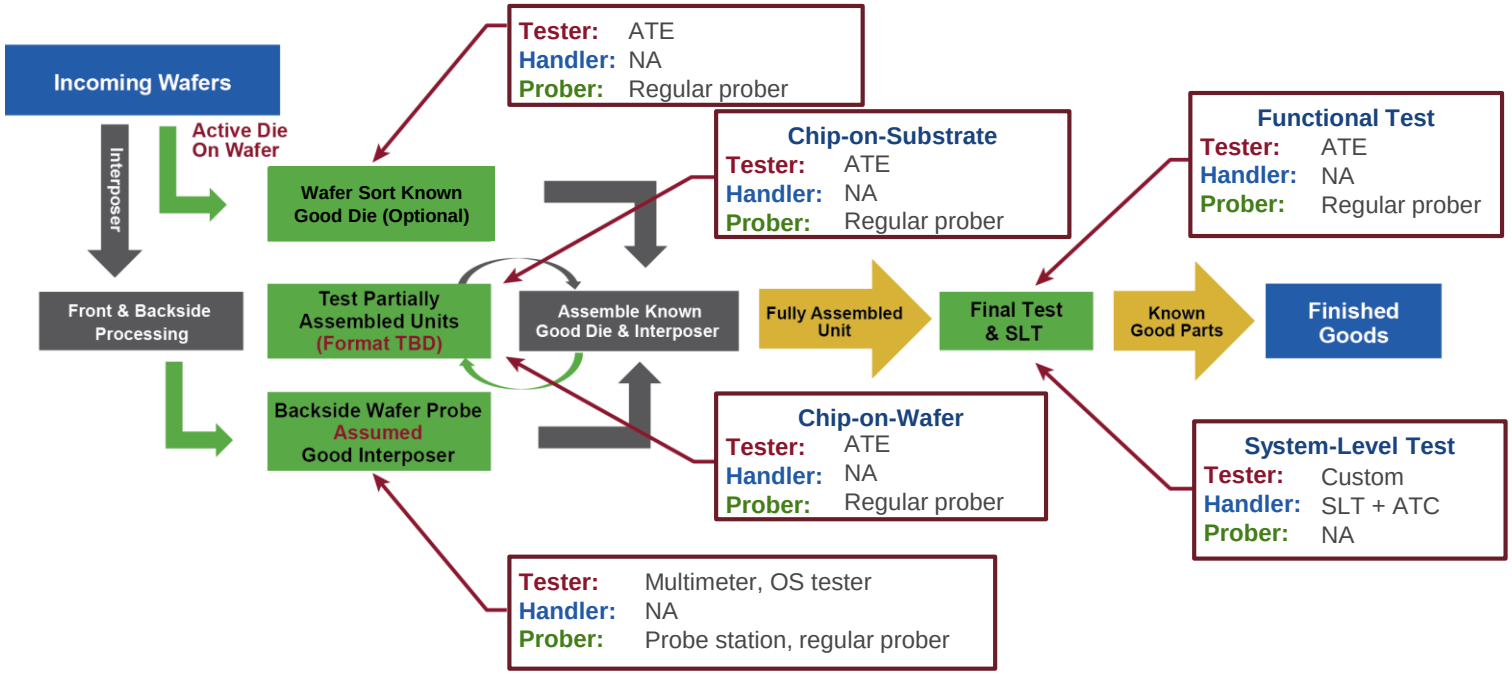
Same tester, added active thermal control to handler

Partially Assembled & Final System-Level Test

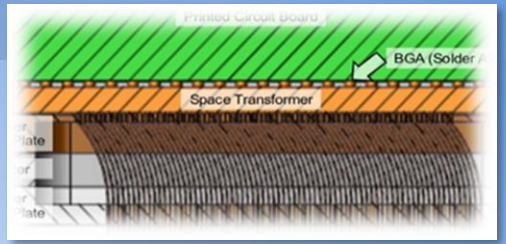
Increase parallelism and added active thermal control

Amkor’s Proposal for Multi-Die Package Test

Test Coverage Through the Assembly Flow



Wafer Sort



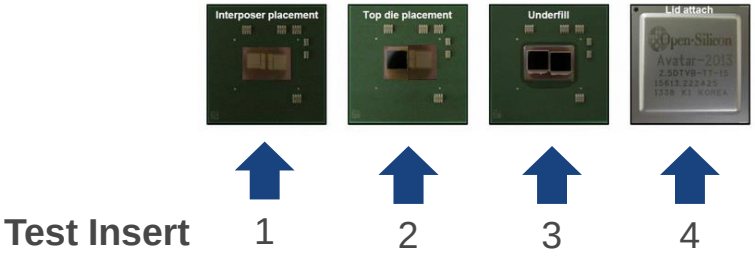
Current WS Capability for Advanced Packages

- Probing at speed with high probe count
  - Direct docking
  - 22K needles touching down
  - Total contact force ~100 Kg
- High-speed testing (4 Gbps – 9 Gbps bus speed)
  - Large amount of heat generated by DUT
  - Test temperature set at cold to prevent die from over heating during test
  - Special gasket to prevent condensation on chuck/wafer
- Pad size and pitch
  - 30 µm pad size with 50 µm pitch

Final Test

Current FT Capability for Advanced Packages

- Partially assembled functional test
  - Testing bare die that is assembled on substrate or interposer (LGA)
- Automatic thermal control for 300W die
- Subsequent testing at BGA after memory and ball attach
- Support product harvesting/down binning/new product codes



System-Level Test

Current SLT Capability for Advanced Packages

- Die are tested in the final application – motherboard or video card
- Automatic thermal control for 300W die
- Testing performed before memory attach (LGA)
- Testing performed after memory and ball attach (BGA)
- Support down binning of parts

Summary

- Multi-die, advanced packages – need to think test differently
- Be ready to manage interim steps of test, learning curve
- Interposer – design, from O/S to impedance test
- C/P – at speed and stringent probe card requirements
- F/T, SLT – ATC to be in the game

Thank You