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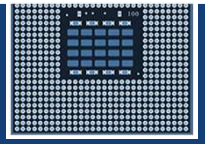

High Volume Manufacturing Supply Chain Ecosystem for 2.5D HBM2 ASIC SiPs

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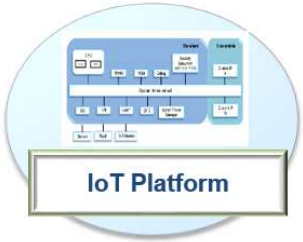
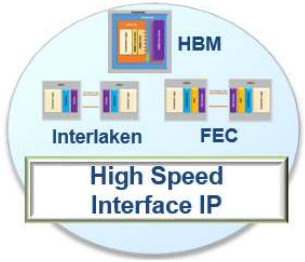
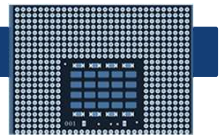




Asim Salim

VP Mfg. Operations

- 20+ experience in semiconductor operations engineering (product engineering, device physics, reliability, supply chain)
- Early adopter of SiPs – shipped >5M mobile graphics processors with DDR KGD memories in 1999



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The Need for 2.5D Integration with HBM (High Bandwidth Memories)

Why 2.5D Has a Future → Memory Wall

- CPU performance is increasing 4x-8x compared to memory performance (processor can be idle for 50-75% idle times)
- Power is a big issue
  - *wide-IO to reduce frequency → lower power*
- IO space is limited → Integrate to reduce size
  - *Memory cannot become wider*
- Faster data
  - *USB, PCIe, SATA, all are faster now*
  - *Multiple interfaces vie for same DRAM*
  - *Larger on-chip storage is needed (video/graphics is the biggest contributor)*

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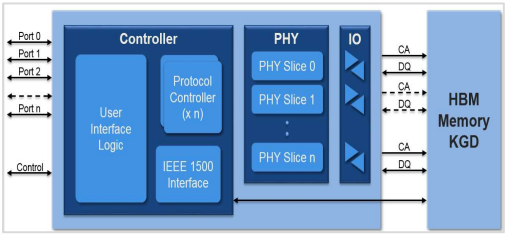
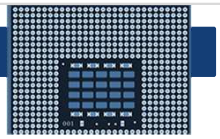
High Bandwidth Memory IP

- *In-house design (Controller/PHY/IO)*
- *Leveraging 2.5D die2die "channel" experience from Avatar*
- *e.g. on Interposer interconnect electricals, ESD, DfT, etc.*
- *CMOS IO driver, 1GHz/2Gbps DDR with light output loading*
- *Electrically compatible with JEDEC HBM2 DRAM spec*
- *TSMC 16nm implementation*





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HBM Applications & Comparison

Data Centers

Networking

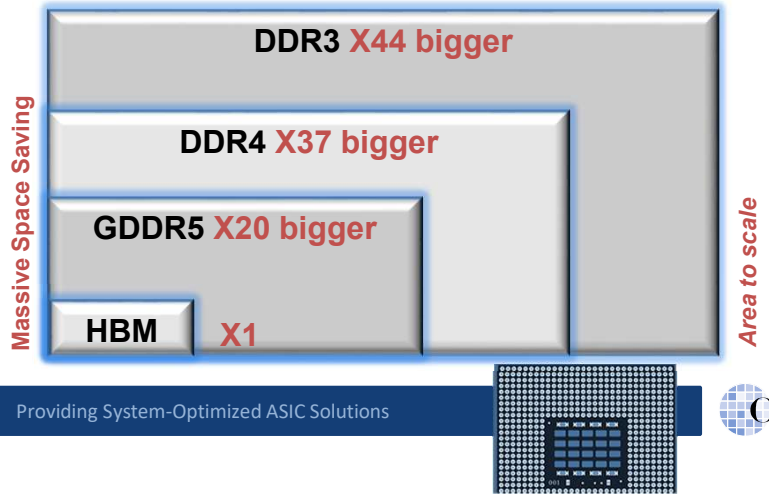
Artificial Intelligence

AR and VR

Cloud Computing

Neural Networks

	DDR4	GDDR5	HBM2
Bus Width (per chip)	16-bit	32-bit	1024-bit
Clock Speed	3.2Gbps	7Gbps	2.0Gbps
Bandwidth (per chip)	6.4Gbytes	28Gbytes	256Gbytes
Power Efficiency (Gbits per sec/pin)	1mW	-	0.33mW
Voltage	1.2V	1.35V, 1.5V	1.2V
Package Type	Discrete	Discrete	Si-Interposer



Major Advantages of 2.5D + HBM

High Performance/Bandwidth

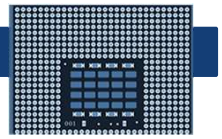
- Accelerate memory access, reduce processor idle times

Lower Power

- HBM uses wide IO's that clock at lower frequencies and result in lower power consumption (~40% reduction)
- 2.5D memory placement is very close the core die (~70um vs. 2 cm. on a PCB)
  - → Smaller IO drivers are needed which reduce IO power

Smaller Footprint due to integration / high packing density

- <50um micro-bump pitch for HBM memories can be accommodated on the silicon interposer providing high routing density (>5000 ubumps)
- Substantially smaller than DDR4/GDDR5
- Capable of signaling up to 2Gbps DDR between 4-5mm trace lengths



2.5D System

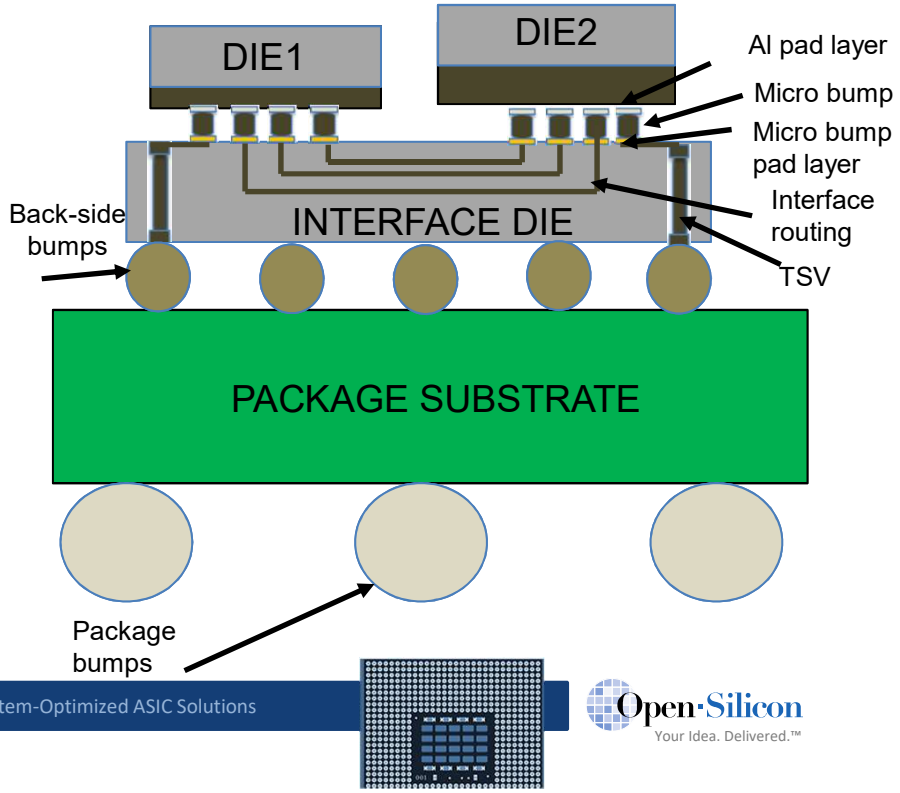
2.5D System Involves

- Mounting 2 or more Silicon DIEs onto an Interface DIE.
- Assembling the whole system into a single package.

2.5D System for High Performance Computing, Graphics, Network Applications

2.5D Systems Enable

- Cost Reduction
- Lower Area
- Higher Bandwidth
- Lower Power
- Improved Yield due to Lower Area
- Heterogenous Integration etc



Avatar 2.5D Solution Demonstration

First ASIC vendor to bring 2.5D to prototype silicon (Avatar). Awarded best chip design at ARM TechCon 2013, Santa Clara

Avatar logic die	• 2 dies of an ARM dual-core A9 SoC on 28nm process
TSV Si Interposer	• "65-nm" 4 front-side, 1 back-side metal interposer
Package Assembly	• Assemble 2 die on interposer, and placement on FlipChip package substrate
High Level Goals	• Develop a complete 2.5D KGD solution • Demonstrate reusable portfolio of verified silicon dies with a higher level of chip abstraction

SysC Modeling

Demo Board Hardware and software development

P & R,GDSII

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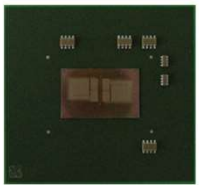
RTL design, Verification

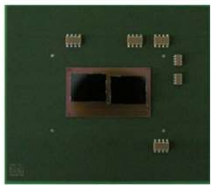
Custom die-to-die IO
Compact, 2Gbps signalling, fit under ubump,

Reliability testing
Thermal, Mechanical

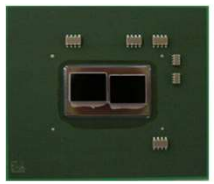
Interposer + Cap



w/AVATAR



w/Underfill



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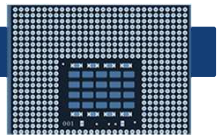

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Components & Stakeholders Involved

ASIC DIE

- HBM2 PHY & I/O
- HBM2 Controller
- Manufacturing at a Foundry
- Micro-Bumping

(*Foundaries like TSMC, GF etc or OSATs like ASE, Amkor etc*)

HBM2 MEMORY DIE

- SK Hynix, Samsung etc

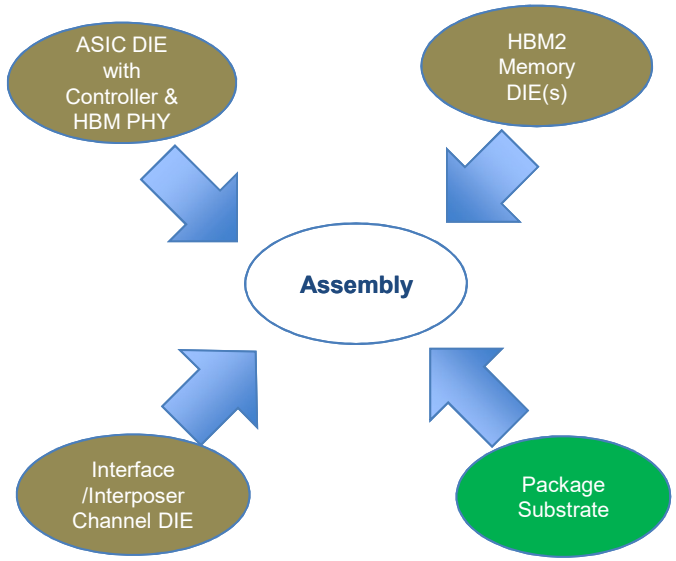
Interposer DIE

- Foundries like TSMC, GF, UMC etc
- Back-grinding and exposing TSVs, solder bumping (OSATs)

Package Substrate

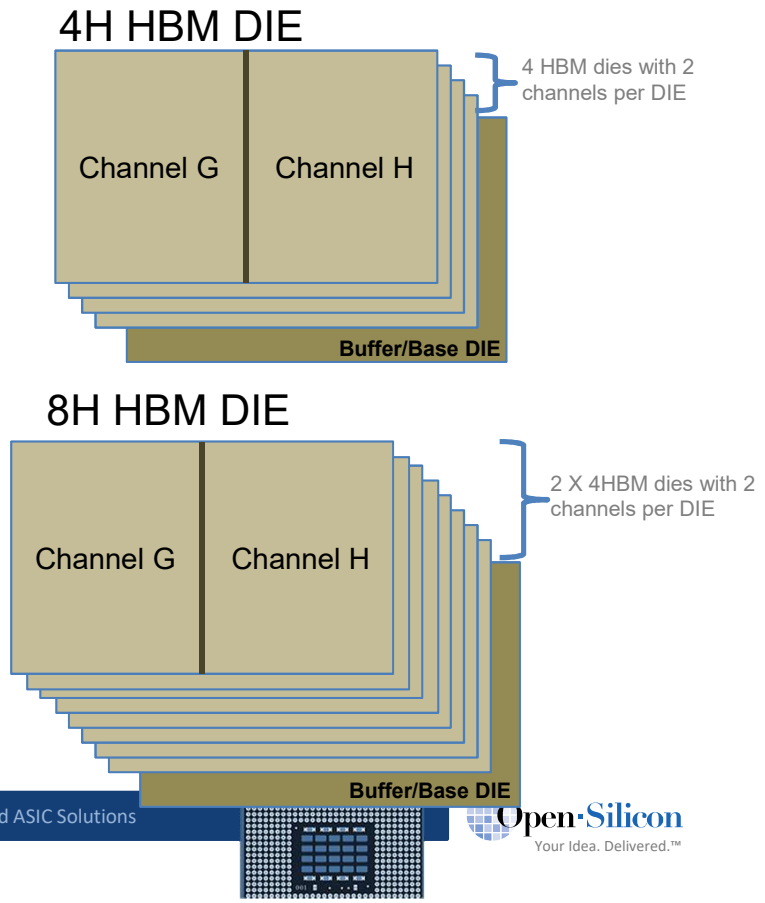
Assembly

- OSATs (e.g. ASE)
- COWOS (TSMC)



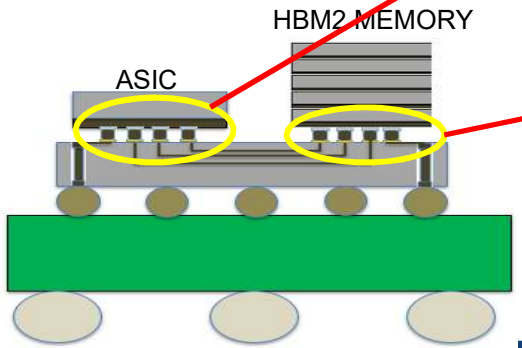
HBM2 Memory

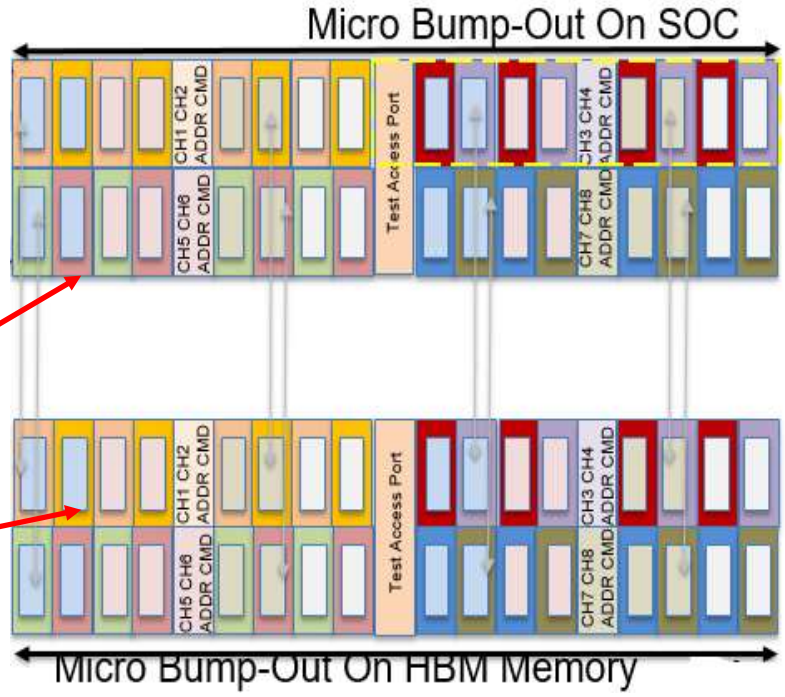
- Stacked DRAM with a base die
- 4H, 8H stack options
- Up to 8GB memory density
- 8 independent channels to interface
- Wide interface architecture for low power and high speed operation
- Each channel has 128b data bus
- IO voltage is 1.2V
- Unterminated data/address/cmd/clk interfaces
- DRAM core voltage is 1.2V independent of IO voltage
- Base die has micro-bumps to connect to interface
- ~ 700 um high
- HBM2 targets 2Gbps data rates and higher
- 256 GBps bandwidth possible with 8H HBM2

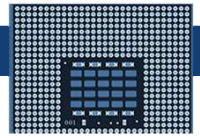


ASIC Die: HBM2 Specific 2.5D System Connections

- 8 channels to interface through micro-bumps
- Micro-bumps at 55 um X 48 um pitch
- Interleaved channels
- Each channel has 212 signals
- Test access signals common to 8 channels
- Reset, temp, cattrip signals common
- All signals and power/gnd connections made using routing layers on interface DIE (interposer)







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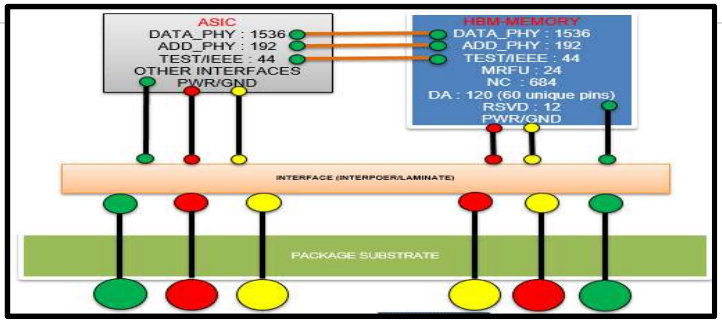
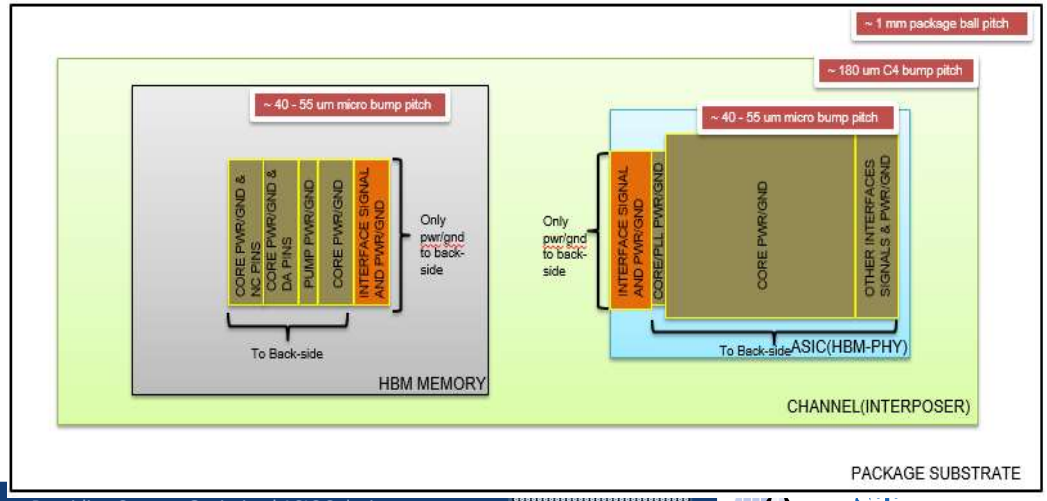
ASIC Die and Interposer: 2.5D Requirements: Bump Design

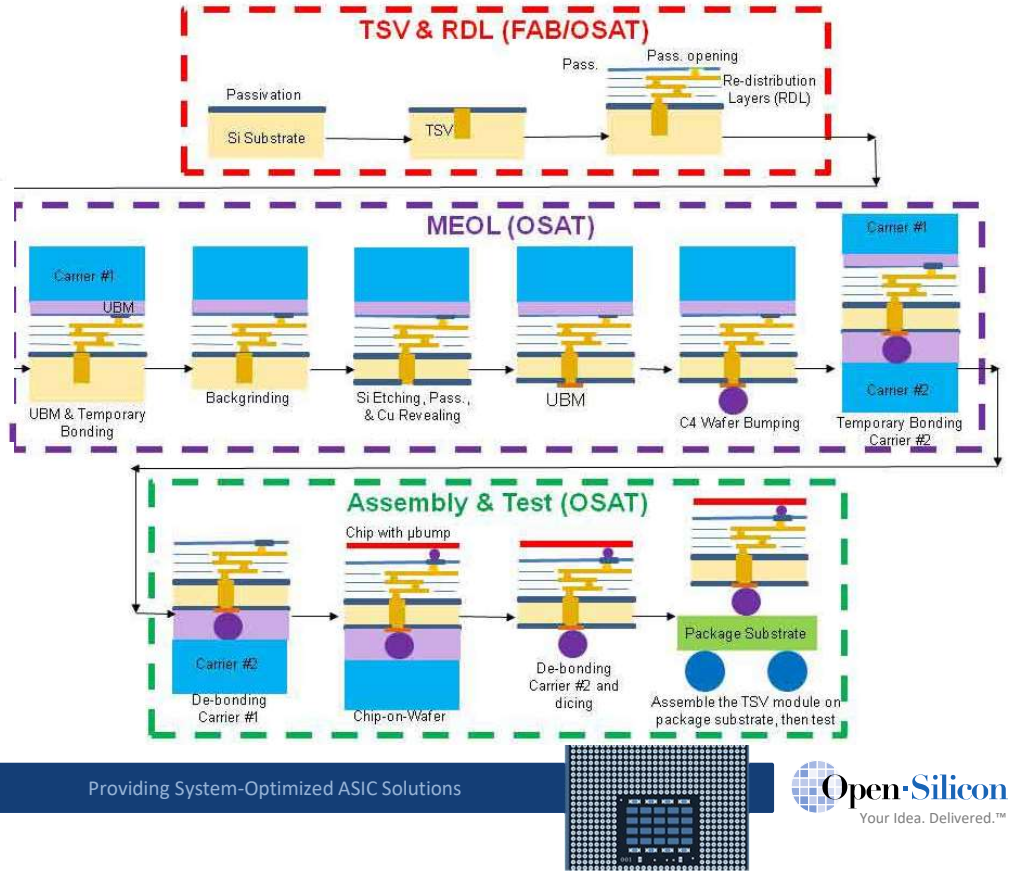
- Micro-bump rules guided by bumping scheme
  - OSAT or Foundry
- Memory bumping scheme set by JEDEC
- PHY bump scheme guided by memory bumps
- Bump scheme to consider probe placement
- Back-side bumping on interposer for
  - ASIC pwr/gnd
  - Other ASIC interfaces
  - Memory pwr/gnd
  - Memory direct access
- Back-side bumping rules by assembly house
- Assignment to consider
  - Power delivery efficiency
  - Signal integrity
- TSV pitch guided by foundry





2.5D Package Assembly Flow (Typical)

- Interposer Manufacture
  - Fab, 65nm process
  - Additional TSV processes
- Interposer Preparation
  - Backgrind to 75-100um
  - Additional temporary bonding/de-bonding processes for carrier
- Package Assembly
  - Interposer attach to substrate
  - Die(s) attach to interposer
    - ✓ 40-60um pitch



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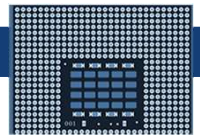
2.5D System: Test / Fault Coverage Challenges

Low DPPM - >> Low System Level Fallout is Essential for Expensive Systems

Low DPPM/High System Test Yields Drives

High Test Coverage /Quality (KGD) of all Components of the 2.5D System

DFT / Plan for 2.5D Manufacturing

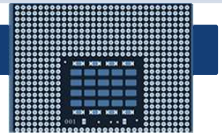


Test Coverage / KGD Plan for High System Yield/Low DPPM

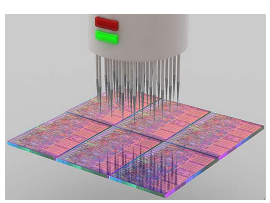
ASIC Die	• High speed probe testing (sacrificial probe test pads) • Direct dock testing (at-speed) • DFT with 98%+ fault coverage

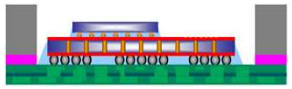
Interposer	• Test structures
	  • Physical – Wafer coplanarity, optical surface inspections, TSV depth
	  • Electrical – TSV leakage, metal pattern, via chain tests

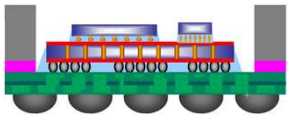
HBM Memory	• KGD + wafer level burn-in (supplier proprietary) • IEEE debug bus access
Substrate	• Electrical tests • Optical inspections



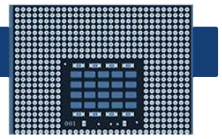
2.5D Test Flow



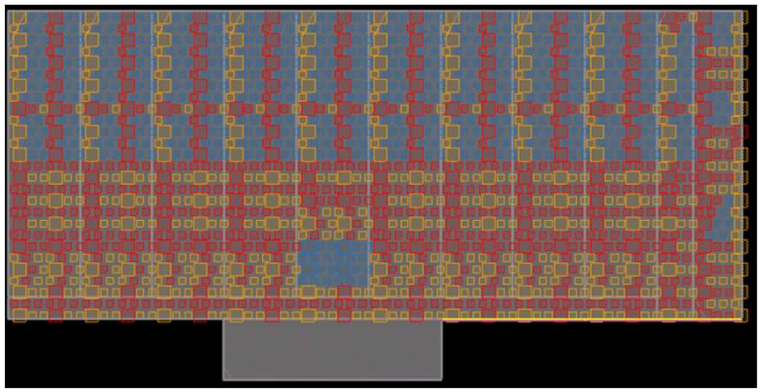




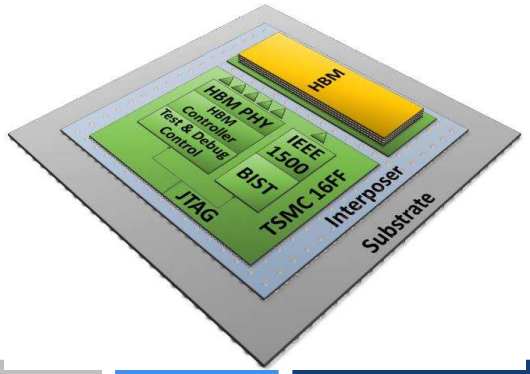
Wafer Sort → Assembly (CoW) → Partial Assy Final Test → Assembly (HBM) → Final Test



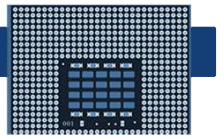
Open-Silicon's Probing Scheme for 2.5D HBM2 ASIC SiP



- Signal uBump
- Gnd uBump
- Power uBump
- Gnd Probe-Pad
- Power Probe-Pad

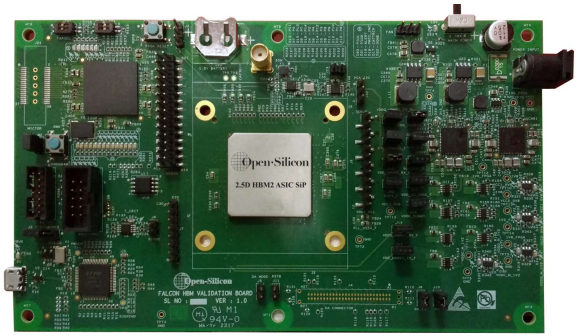


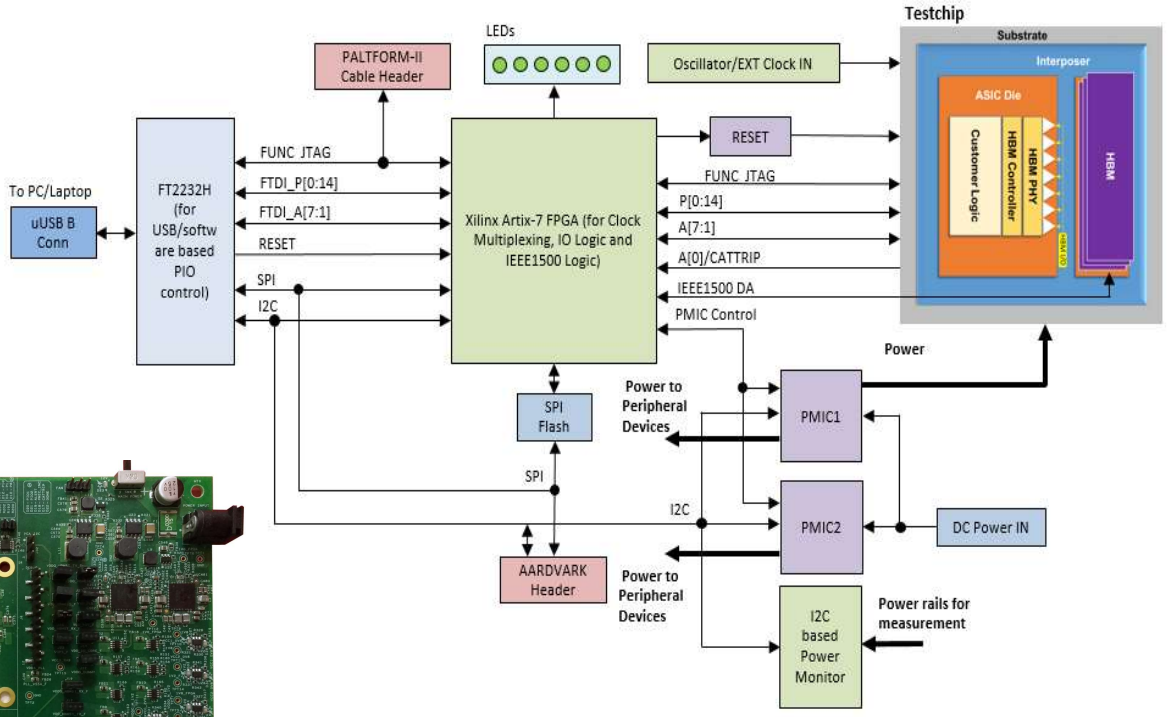
Testability feature deployed through probing mechanism for debug of ASIC SiPs with HBM memory embedded on a 2.5D interposer die

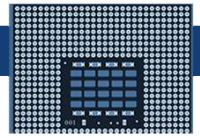


2.5D HBM2 ASIC SiP Validation/Evaluation Platform

Reference Board Design







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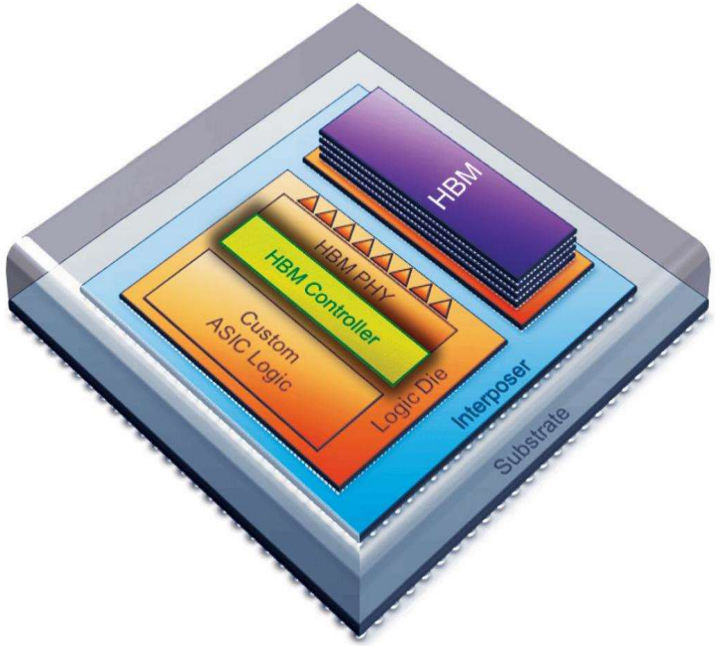
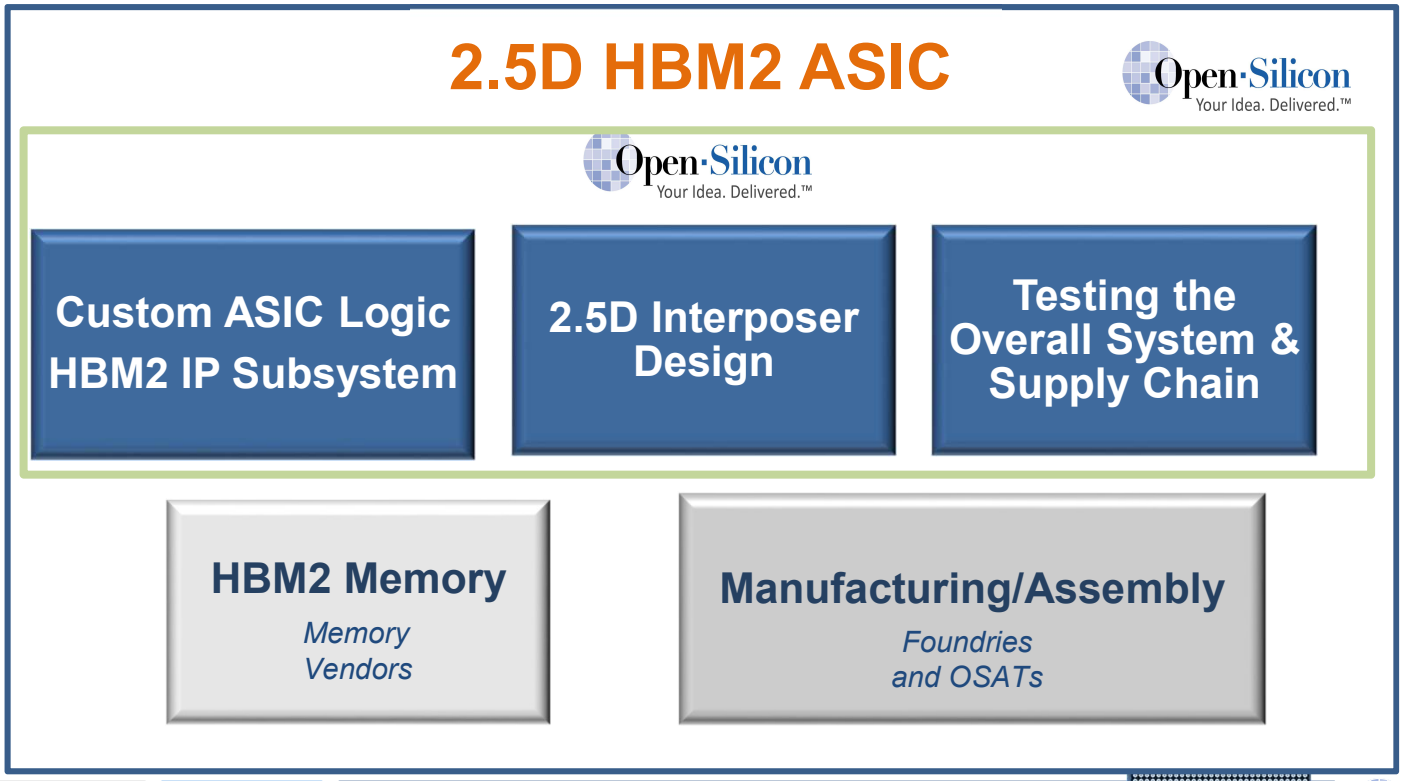
Open-Silicon's 2.5D HBM2 ASIC SiP for Silicon Validation Parameters

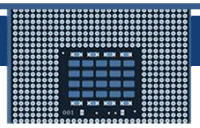
- ASIC Technology **16nm**
- Interposer Technology :**65nm**
- SiP Process :**CoWoS (2.5D)**
- **HBM2 Memory**
- **Open-Silicon HBM2 IP Subsystem**
- Core Voltage: **0.8V**
- I/O Voltage : **1.2V**



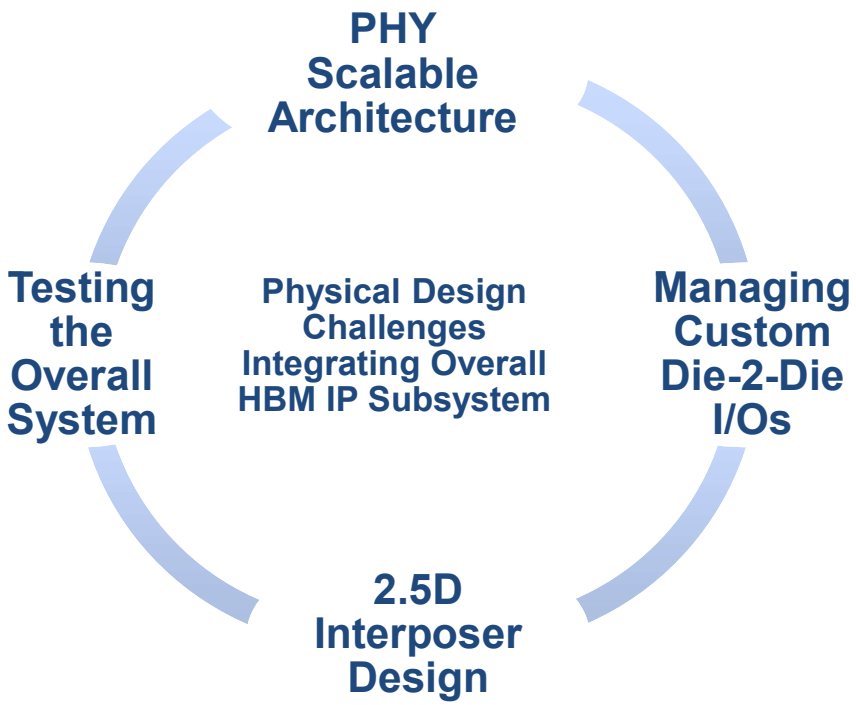
This Platform Demonstrates
Open-Silicon HBM2 IP Subsystem ⇔ HBM2 Die-Stack Interoperability

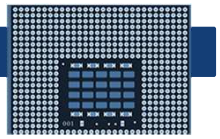
Full Turnkey HBM2-Based 2.5D System Solution





2.5D HBM2 SiP Implementation Challenges





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2.5D HBM2 SiP Manufacturing Challenges

Foundries
- Microbumping,
- > Interposers exceeding reticle size (XL)
- Reliability
- Cost

Interposer Foundries
- Keep costs low
- Optimize number of metal layers
- Integrate passives
- Test structures/DFT

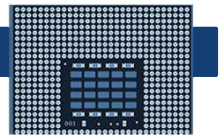
OSATs
- Low ESD environment
- Wafer level processing techniques
- Large stacked package reliability
- Costs

Semi's IP Houses Standard. Committees
- New additions and requirements (D2D IOs, ESD)
- new players

KGD Vendors
- Standards across suppliers on test/DFT, delivery metrics
- Heterogeneous integration

DFT/Test
- Probing microbumps
- Testing out at many different levels
- High-speed testing at probe (direct dock)

EDA
- Integrated tools connecting core die to interposer, package substrates



Building the Ecosystem

Foundries | Interposer | OSAT | Semi's Stds | KGD | DFT/Test | EDA

All-in-One Vendor

OR

Top Die Vendor | Interposer Vendor | 2.5D Assembly Vendor

uBump Collaboration w/ OSAT

Interposer Post-processing Collaboration w/ OSAT

Design rules for 2.5D Manufacturing

Bill of Materials Selection/Compatibility

Models & PDK for Interposer design

2.5D Package Reliability

Interposer material (silicon, organic, glass)

Thin wafer handling

Interposer optimized D2D interfaces

Wide IO & HBM memory controllers, etc.

HBM memory 3D stacks

Special IP (Serdes)

Fine-pitch probe technology

Probe pad design & test implementation

IEEE P1838 Working Group

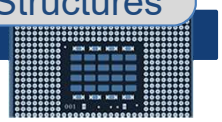
Interposer Test Structures

Area IO floor planning, die P&R, integration & verification

Signal & Power integrity, EM and ESD modeling & analysis

Thermal analysis (different Tj max)

2.5D ATPG



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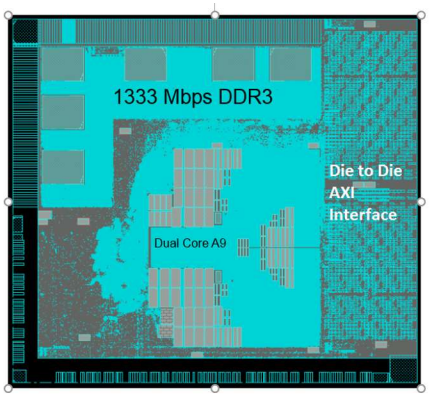
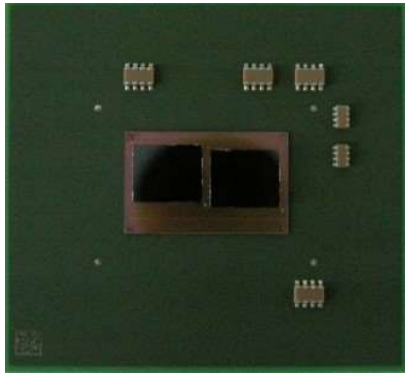
Open-Silicon 2.5D and HBM2 Programs

Proven Capability Across Foundries and OSATs

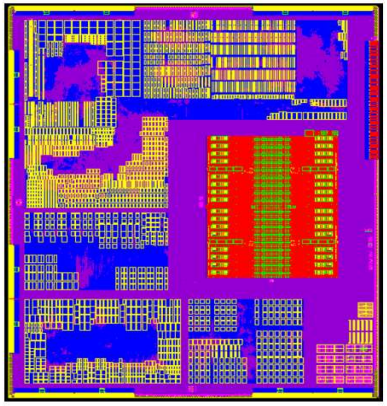
ASIC Die (GF 28nm)



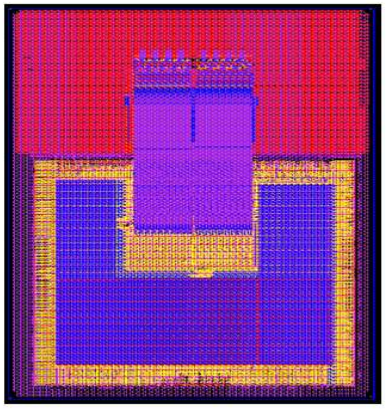
2.5D SiP



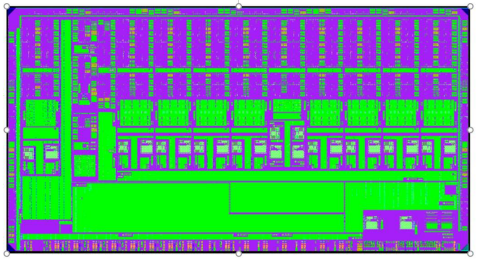
HBM2 ASIC Die (GF 55nm)



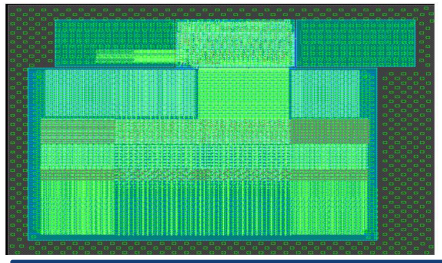
2.5D Interposer (GF 65nm)



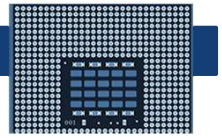
HBM2 ASIC Die (TSMC 16nm)



2.5D Interposer (TSMC 65nm)



HBM2 ASIC SiP (TSMC CoWoS)



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Summary

Multi die Integration for high performance ASICs is necessary

We have hit the memory wall

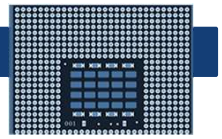
2.5D Integration of SoC with HBM memory is silicon proven

Result is major improvement in performance, lowering of power and reduced footprint

Silicon-proven HBM2 IP subsystem, design/manufacturing of HBM2 ASIC SiPs from a single vendor

Lowers risk and time-to-market

HBM ecosystem is ready for high volume manufacturing of HBM2 ASIC SiPs



THANK YOU