The Continuing Growth of Silicon Integration Technologies and Application / System Level Testing Prompts a Reflection on the EDA to HVM Highway

Zoë Conroy
Senior Manager – DFT, Test & PE
Component Quality & Technology

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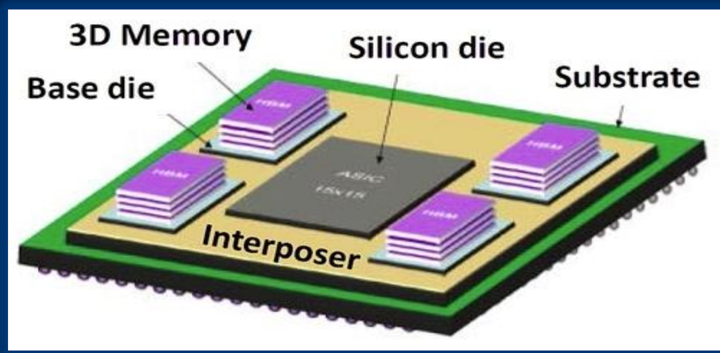
Today's Reflection

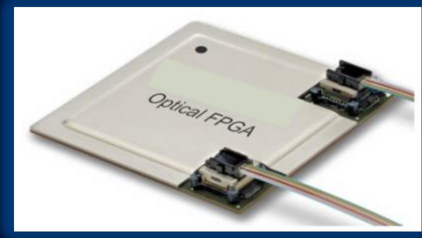
- Electronics market is demanding high growth, high function, yet cost-effective solutions
- Multi die heterogeneous integrations offer More than Moore
- Applications are requiring minimal defect rates
- Are today's development tools enough to sustain and improve required quality and reliability?
- How will EDA and manufacturing test reshape themselves to meet these needs?

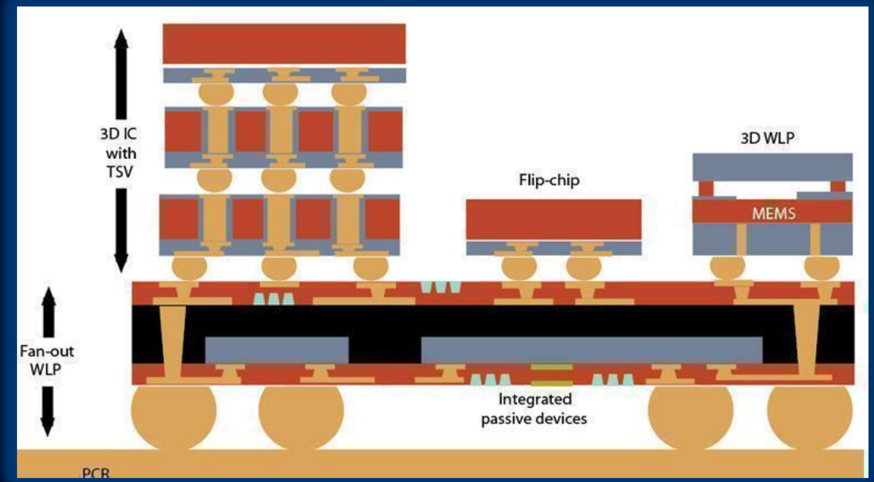
Continuous Innovation: More than Moore

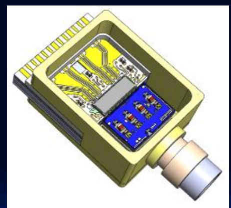
Networking - Graphics - Computing

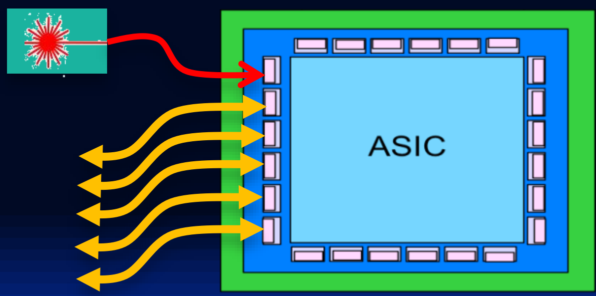
- 2.5/3D/SiP/WLP
- Optics, photonics
- MEMs, Sensors
- RF, analog
- Power











Where is the Industry at Today?

- Applications demand continuous uptime, with cloud/data-centers allowing more applications worldwide
- Automotive arena - <<100 DPPM
- More companies adding system level test to get highest level of test coverage and quality
- Gate counts/ heterogeneous integration and advanced packaging continue to push boundary on technologies requiring ‘perfect’, yet cost effective silicon

The Impact of Bad Quality

Home > Networking

Millions disconnected by NTT broadband outage

Massive British Airways IT outage

University Hospitals struck by computer outage

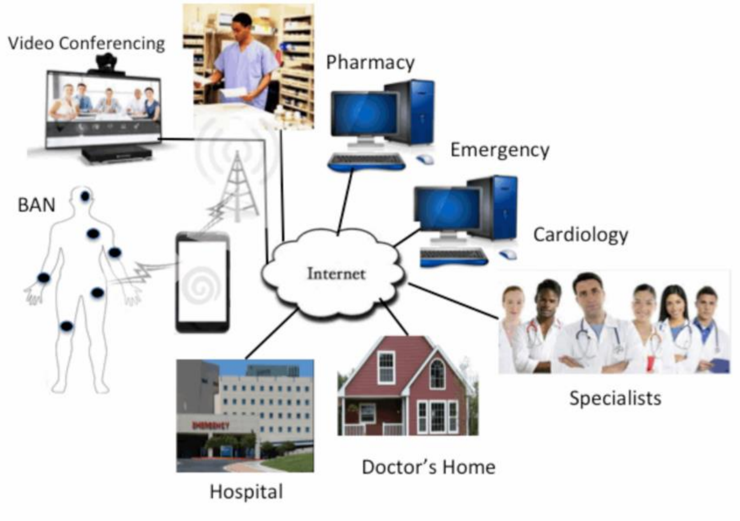
Verizon restores LTE data network after outage

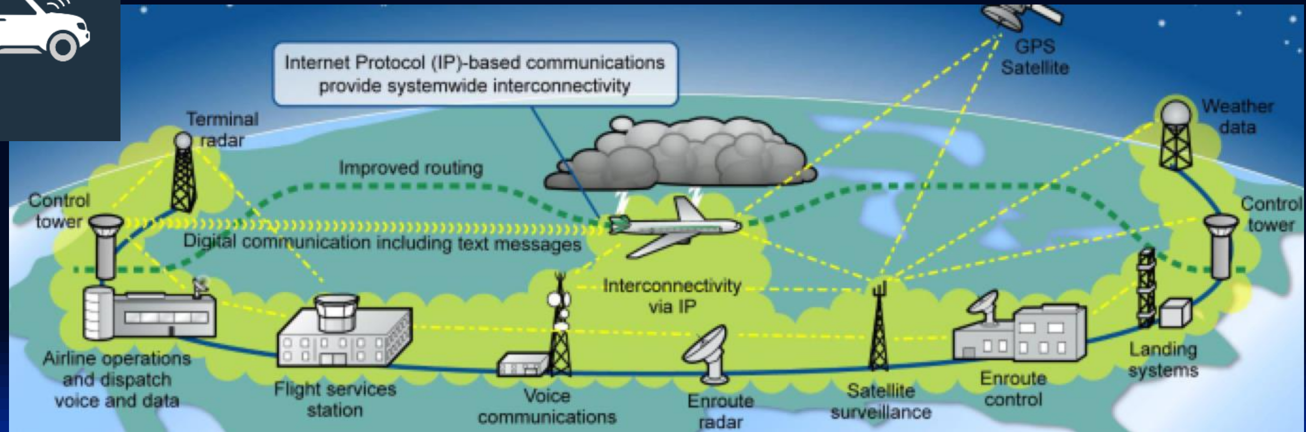
Hundreds of Southwest flights delayed after 'system outage' forces ground stop

The Impact of the Network

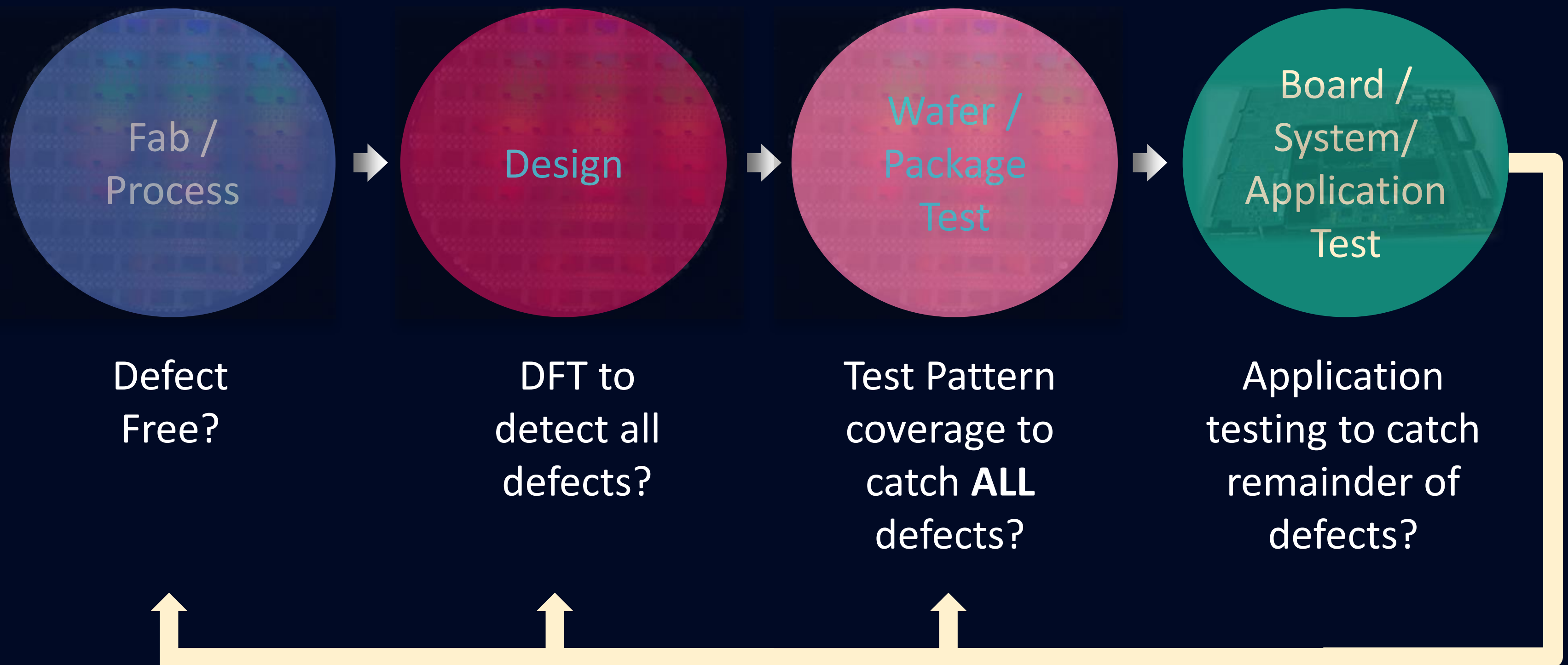
- Our lives NOW DEPEND on the network
- Highest Quality is a MUST, not a nice to have!

Hardware is Here to Stay!

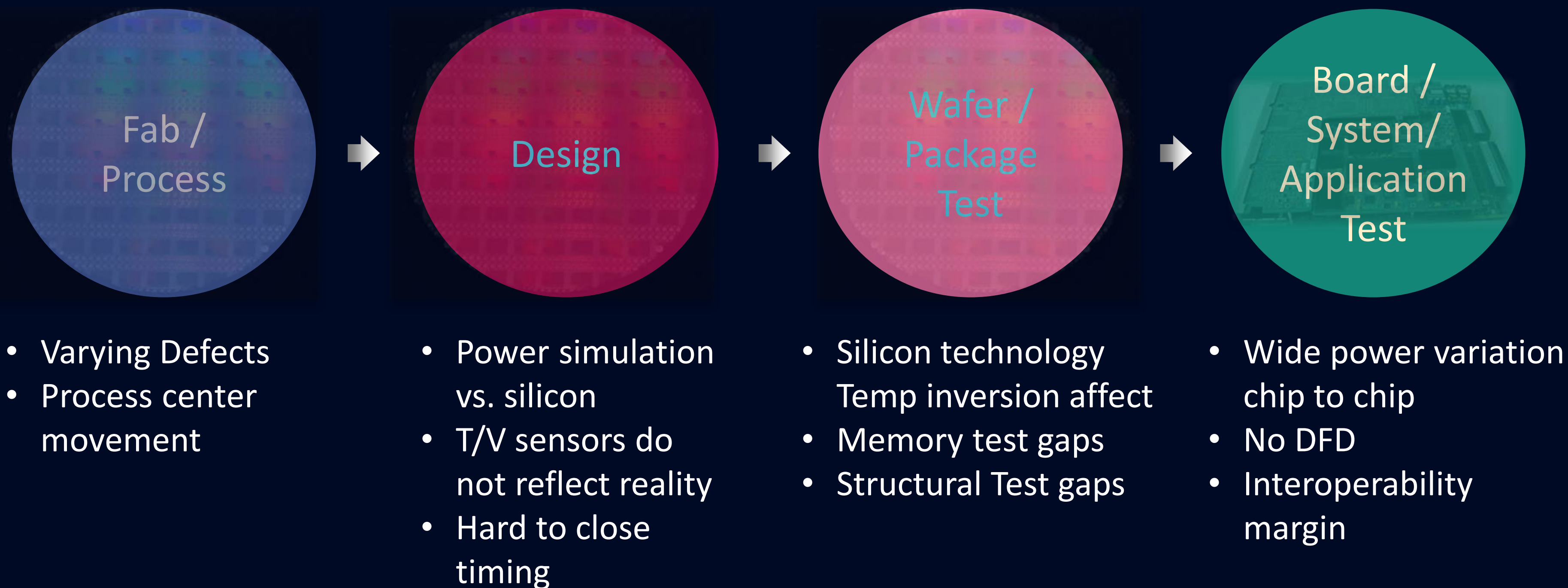




Catching Defects - What Comes First?



Where do Problems Occur?



- Varying Defects
- Process center movement

- Power simulation vs. silicon
- T/V sensors do not reflect reality
- Hard to close timing

- Silicon technology Temp inversion affect
- Memory test gaps
- Structural Test gaps

- Wide power variation chip to chip
- No DFD
- Interoperability margin

EDA to HVM Highway

End To End Manufacturing Flow

ATE to System Differences

Different types of coverage tests, environments,

- High coverage structural test program
- Low noise DUT-board design
- Low noise floor
- Very accurate power supplies
- Stable temperature

Typical networking board: ASICs, uP, FPGA, PHYs, CDRs, memories (DRAM, SRAM, TCAM, HDD, etc)

- Functional application test
- Complex board / system design
- Multiple components interfacing to each other
- Noisy environment
- Varying temperatures

ATE Structural Test

SerDes PRBS & 1149.6

SerDes PRBS & 1149.6

JTAG 1149.1

CPU 2JTAG

JTAG 2CPU

Scan: SAF, TF, PD, Ram Seq

Ring Osc

PLL check

Internal Memory BIST

Internal Memory BIST

TCAM BIST

Logic BIST

IOBIST

Embedded Instrument

Ext Mem BIST

System Traffic Test

Chico TX (CT)

Chico RX (CR)

Arbiter Exhange (AX)

Fabric Transmit (FT)

Fabric Receive (FR)

Reorder (RO)

Decision Engine Egress (DE)

Virtual Output Queues (VQ)

(AM)

Filter Block (FB)

Ingress Packet Buffer (IB)

Decision Engine Lookup (DL)

Egress Packet Buffer (EB)

Decision Engine Ingress (DI)

Port Logic (PL)

Port Logic Buffer

Port Logic (PL)

Security (SC)

Security (SC)

10GE Mac (XM)

IP

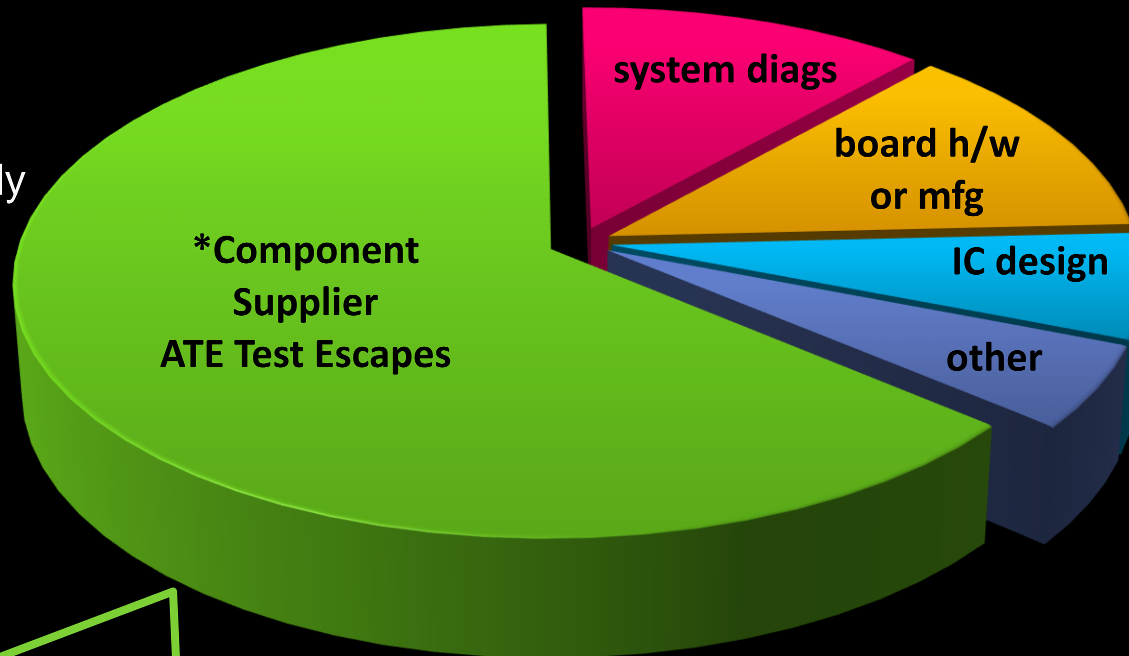
10GE Mac (XM)

Consequences of ATE and System Test Differences

- Board functional tests run different data from ATE BIST and structural testing
- Environmental conditions at system level can cause fails on marginal devices
- Components marginal for timing, voltage
- ATE test escapes
  - Hard to emulate functional environment with a standalone chip
  - Less than optimal structural/BIST coverage

Diagnosis of ASIC Fails at System Test

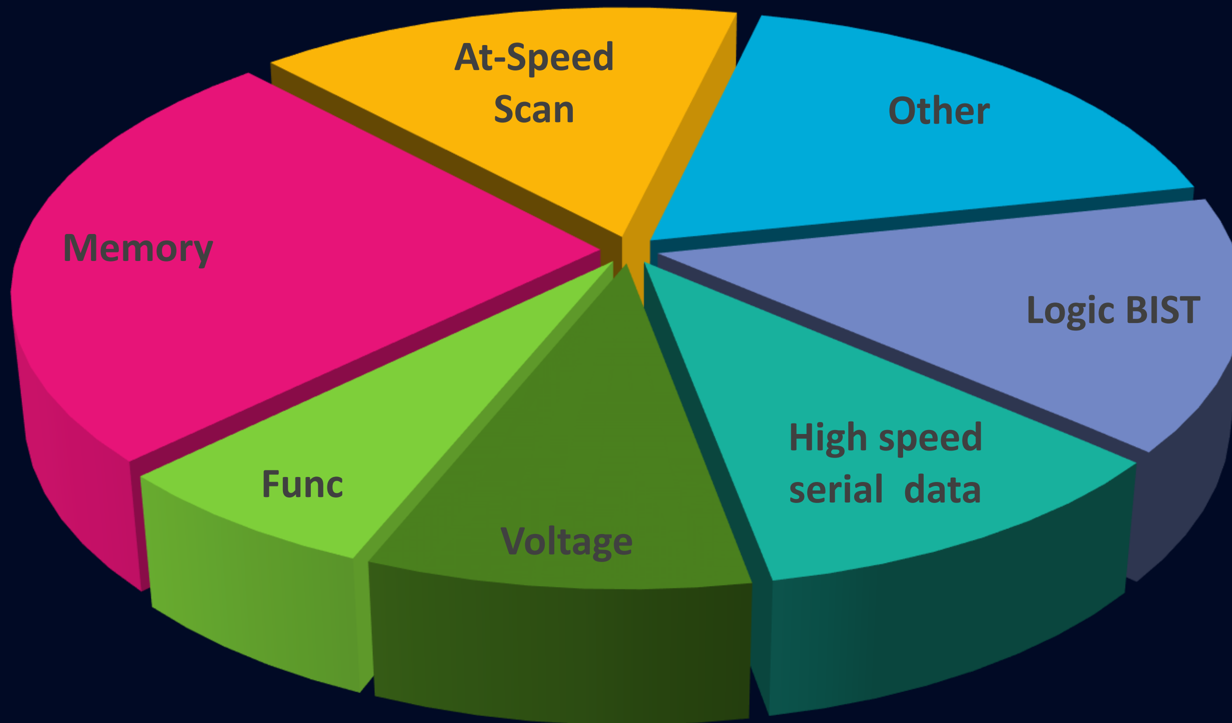
*ATE test escapes
Components that failed system test for functional or IC BIST test, and subsequently found to have a test gap at IC ATE test.



- Added coverage to existing test
- Added a new ATE test
- Ported a functional test from system to ATE
- Changed limits on existing Test

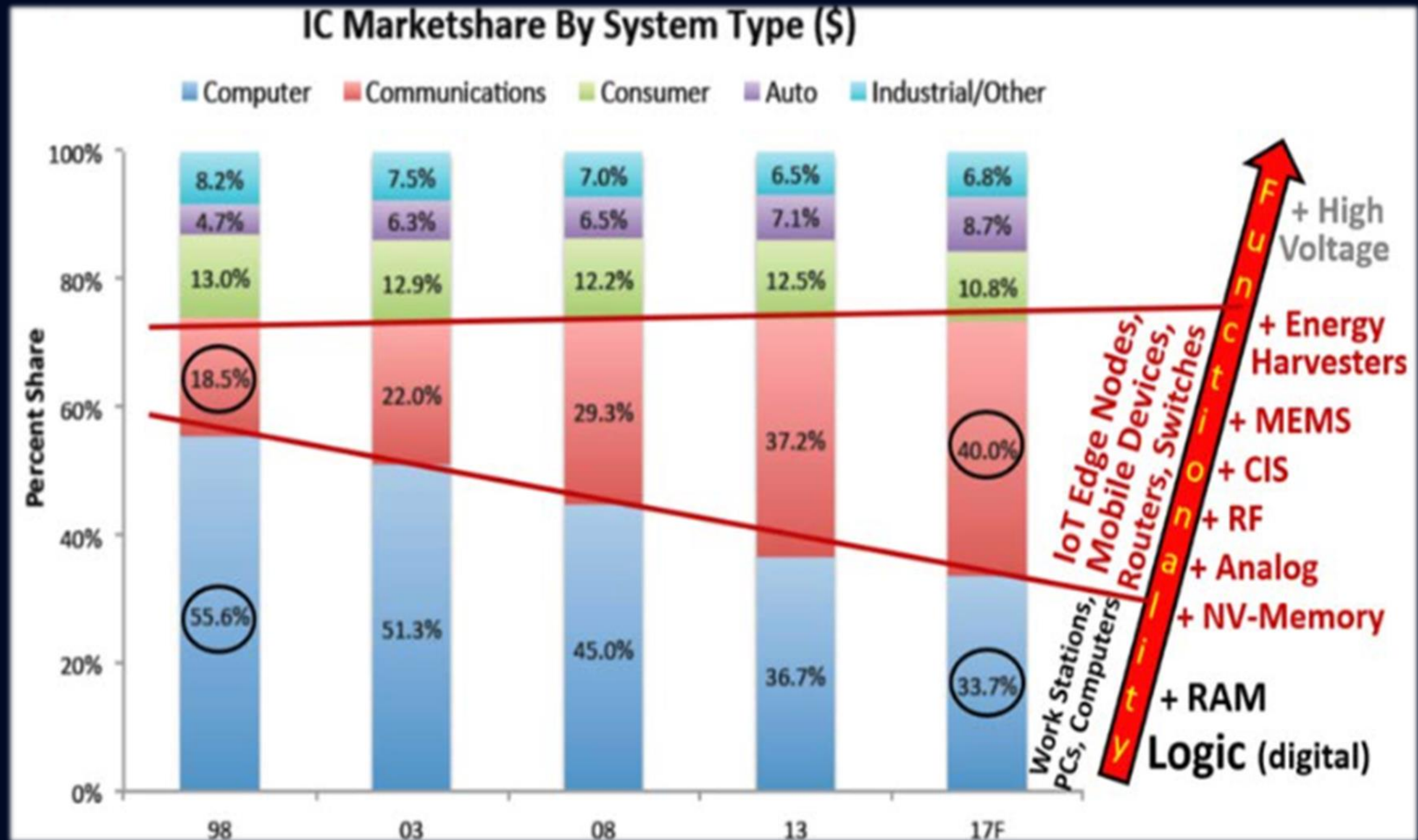
Data from various DPPM Reduction Initiatives 2005-2017

ATE Gaps - Breakdown by Test



- ATE tests added

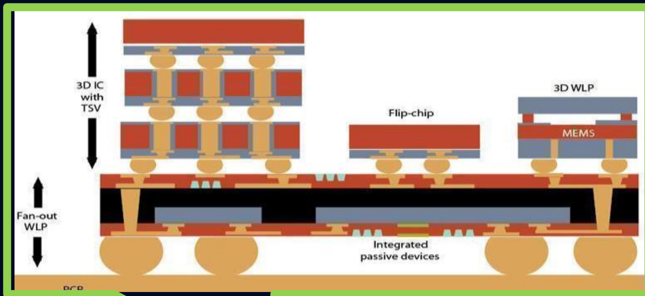
Heterogeneous Functions Drive Growth



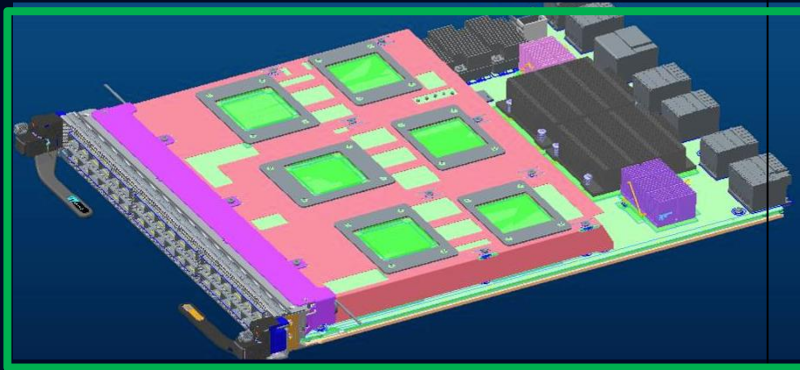
Based on "IC Insights Report", Sept 2014, 3DIn-cite.com

Increasing Levels of Integration

(sub-)component



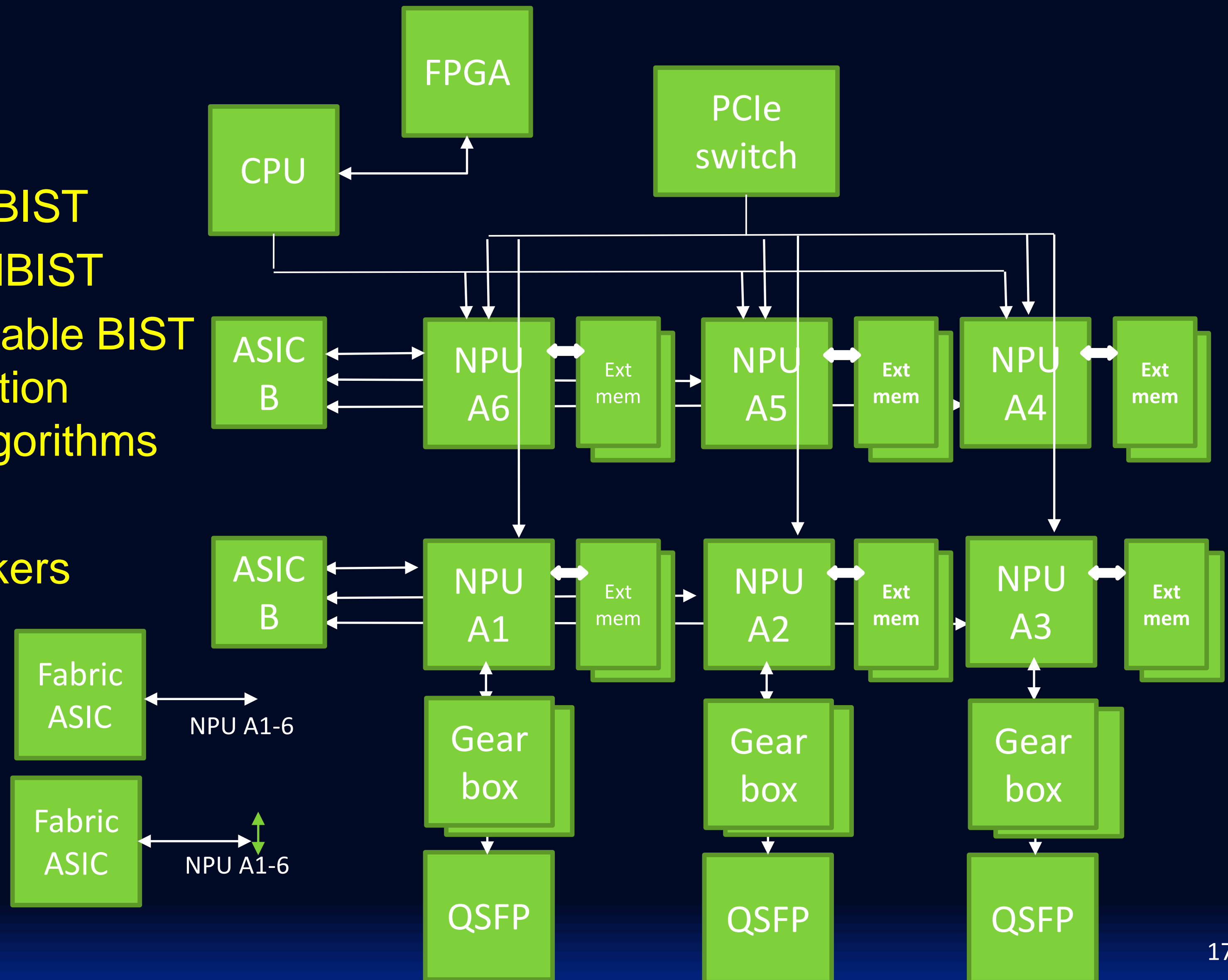
interoperability



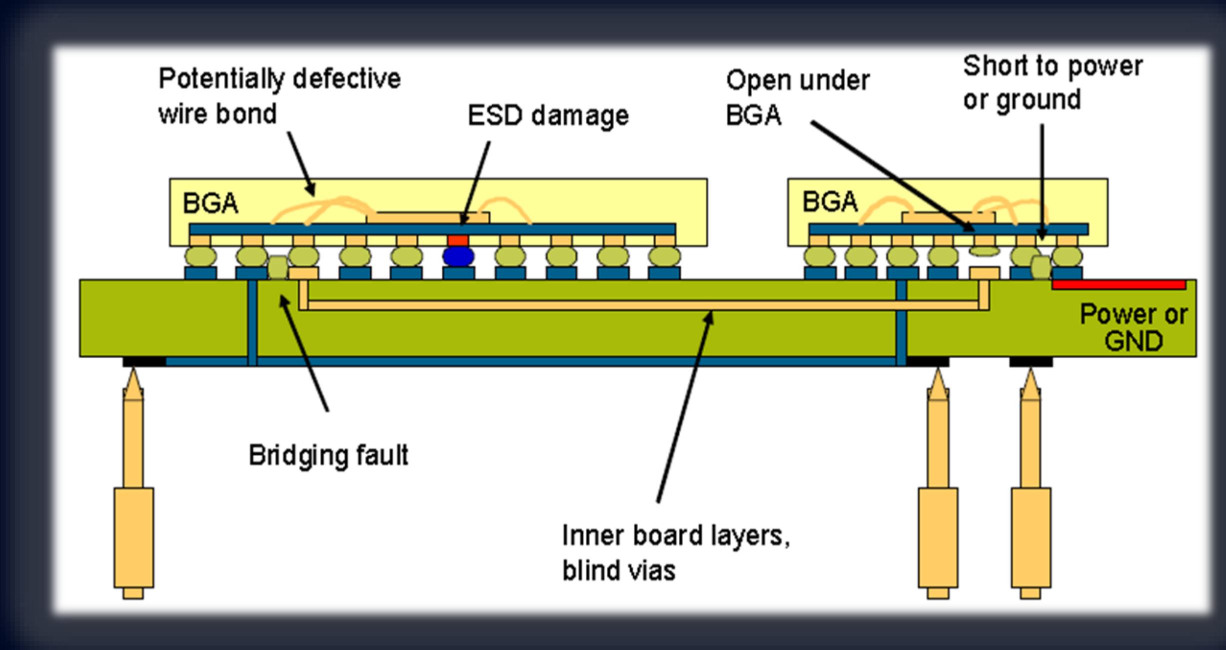
component to component

Using Components to Test the Board

- SerDes
- IOBIST
- Internal MBIST
- External MBIST
- Programmable BIST for application specific algorithms
- T/V Sense
- PLL Checkers
- Traffic



Reduced Structural Test Point Impact



- Test points reducing with denser routing
- Components BIST becomes critical for board testing*
- BIST can cover:
  - Board opens/shorts
  - Trace transitions,
  - High speed interconnect and SI

*iNEMI BIST Program http://community.inemi.org/bist

EDA Tool Portfolio Opportunities

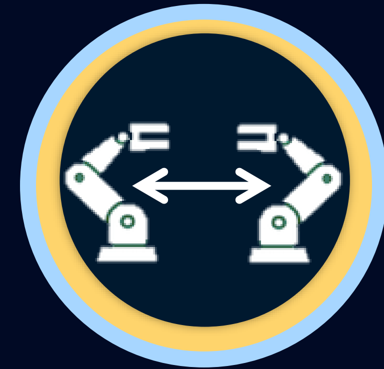
- SLT addition just keeps the status quo!
- Component applications' testing manifests unique coverage gaps in ATE tests
- Denser silicon and heterogeneous integration requires new types of defect modeling and ways to isolate defect locations in real time
- Embedded and external memories continue to be a challenge, with high application fall-out.

Connecting Suppliers & EMS Partners

Big Data Analytics

Cloud

Machine to Machine



Automation

End to End Collaboration

IoE and Adaptive Test to automate End to End Collaboration

Test Data Analytics and Adaptive Test

Improved Process/
Optimized Test

Data Templates

Faster Component FA

Component Test

Component Supplier

24/7
Data Loop

EMS Partner

System Test

Faster Time to Quality

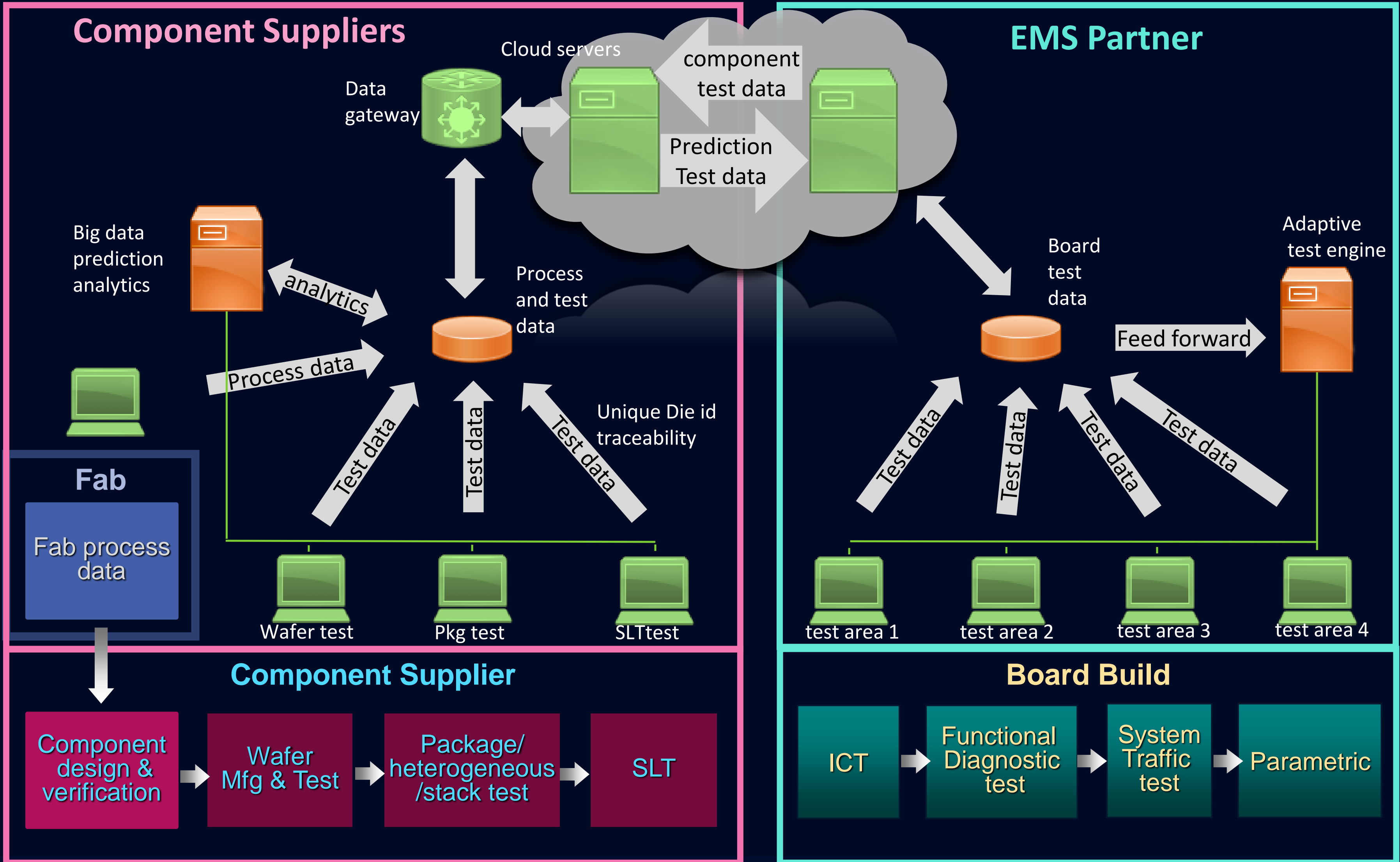
Sample

Population

Big Data Analytics/Machine Learning to predict probability of part failing in System Test.

Adaptive Testing:
Test only relevant portion of the population to catch 100% failures

Cloud Based Predictive Analytics



Closing Remarks

- There are gaps in ATE tests - structural tests do not exercise chips in the same way the application does.
- SLT provides an application test to weed out final defects.
- Actionable data at SLT required to keep closing gap from system to ATE.
- EDA must keep up with increasing complexities of designs, integrations, quality requirements.
- Cooperation and bi-directional info exchange across the entire supply chain is a must.
- Standards for data exchange formats and hand-off criteria between supply chain partners need to be agreed.