System Level Design and Simulation for Heterogeneous Integration

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IC Industry – a Brief History

The ITRS was established in 1991to forecast future technology requirements and enable pre-competitive collaboration

- ✓ The participants were integrated circuit manufacturers and their supply chain
- ✓ The focus was on scaling CMOS as the most efficient path to progress
- ✓ The path to progress was
  - Design of integrated circuits
  - Processes and materials needed to manufacture new designs
- ✓ Packaging was a secondary issue

IC Industry – a Brief History

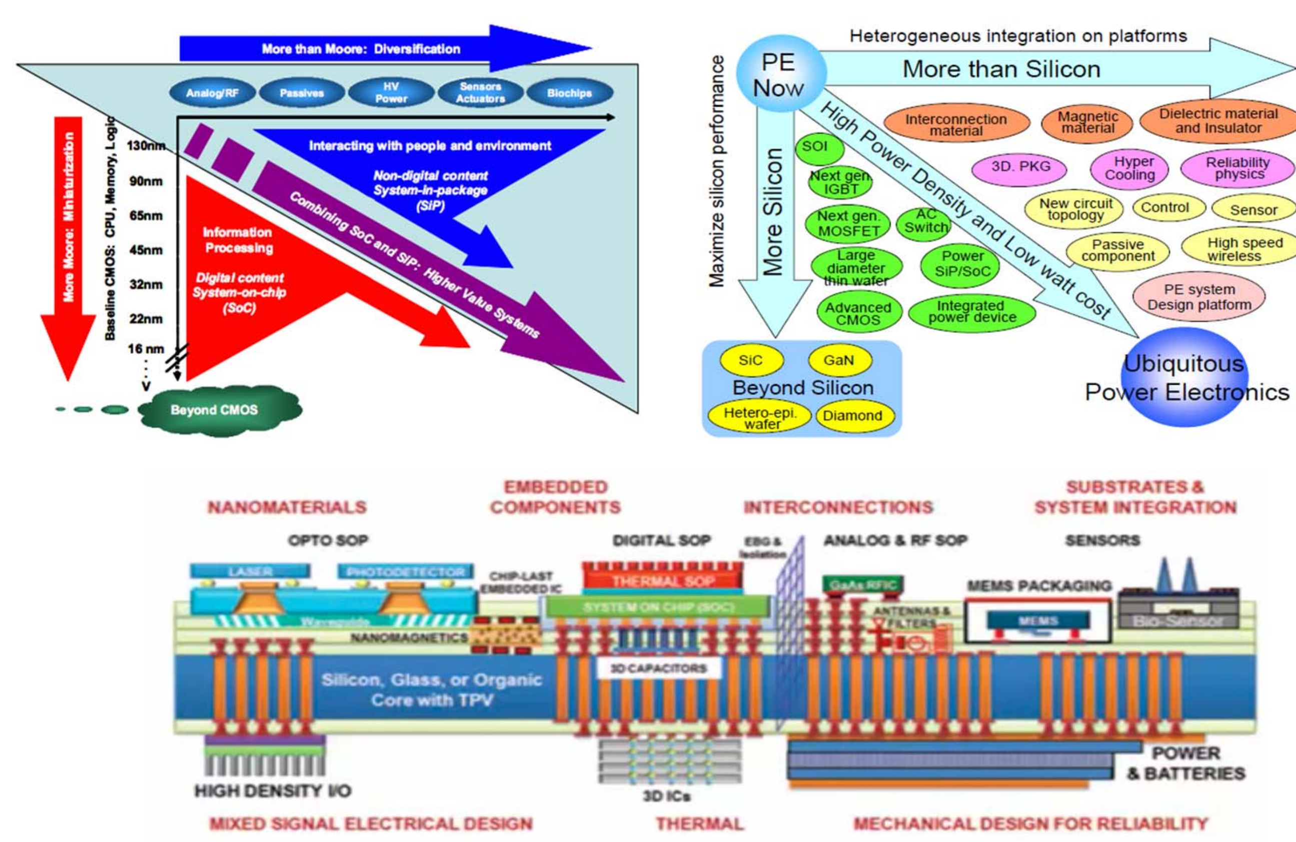
Guided by Moore's Law we knew the challenges well in advance and metrology and characterization tools were available

The path to progress was known, difficult challenges were known and all things were right with the world

26 years later...

….the world has evolved and is changing in ways never imagined.

3D, WLP, Embedding... New Challenges & Opportunities



System Requirements To Support The Future

- ✓ Higher bandwidth density
- ✓ Lower latency
- ✓ Increased performance
- ✓ Lower power
- ✓ Expanded data storage
- ✓ Heterogeneous Integration
- ✓ Ensured reliability
- ✓ Improved security

All at no increase in cost

Potential Solutions To Support This View Of The Future

New Design and Simulation Tools Needed to Integrate these solutions

- ✓ **Higher bandwidth density**

WDM single mode Photonics to the package

- ✓ **Lower latency**

Flat photonic network- replace tree architecture

- ✓ **Increased data processing speed**

Increased parallelism- more cores & software to match

- ✓ **Expanded data storage**

3D memory, new memory devices, hierarchical memory architecture

- ✓ **Ensured reliability in a world where transistors wear out**

Intelligent redundancy

Continuous test while running

Dynamic self repair

Graceful degradation

- ✓ **Improved security while maintaining process speed and latency**

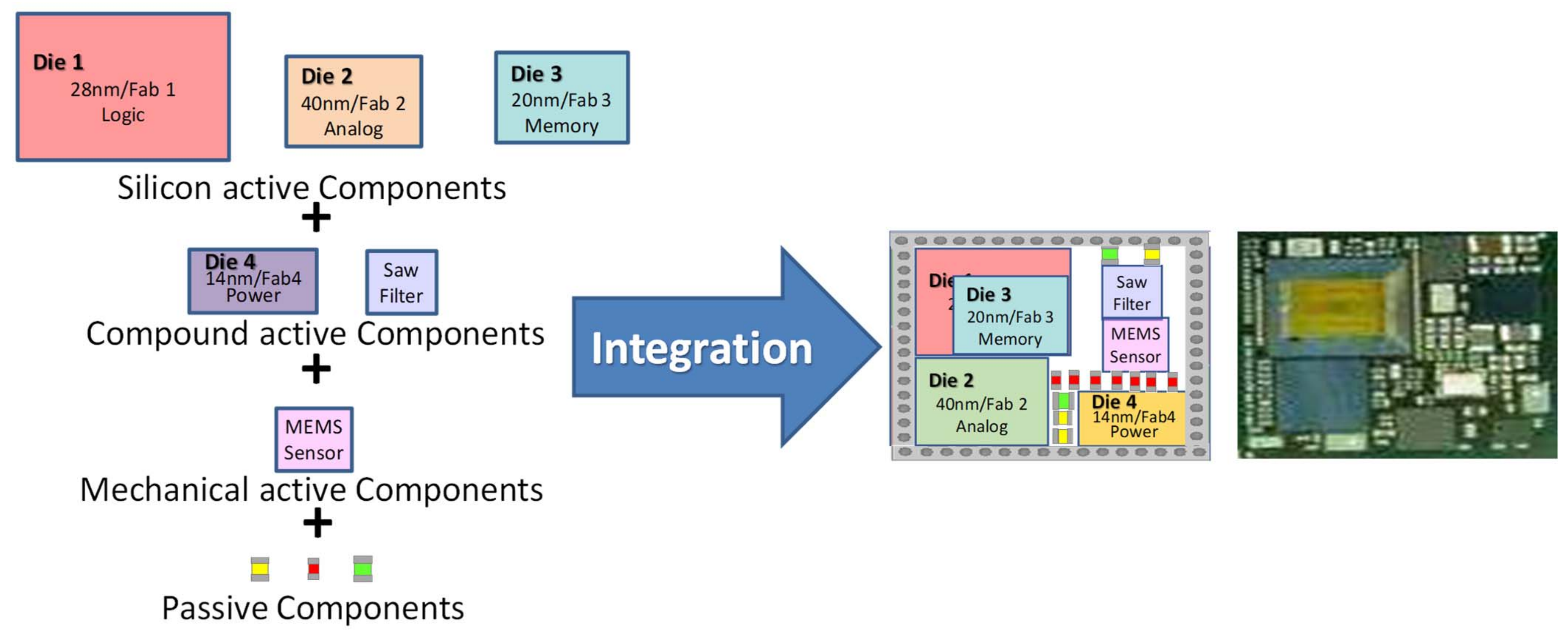
Hardware and software combined-distributed over the global network

New Device and Packaging Architectures Are Needed To Meet Future Market Demand

Emerging Package Architectures

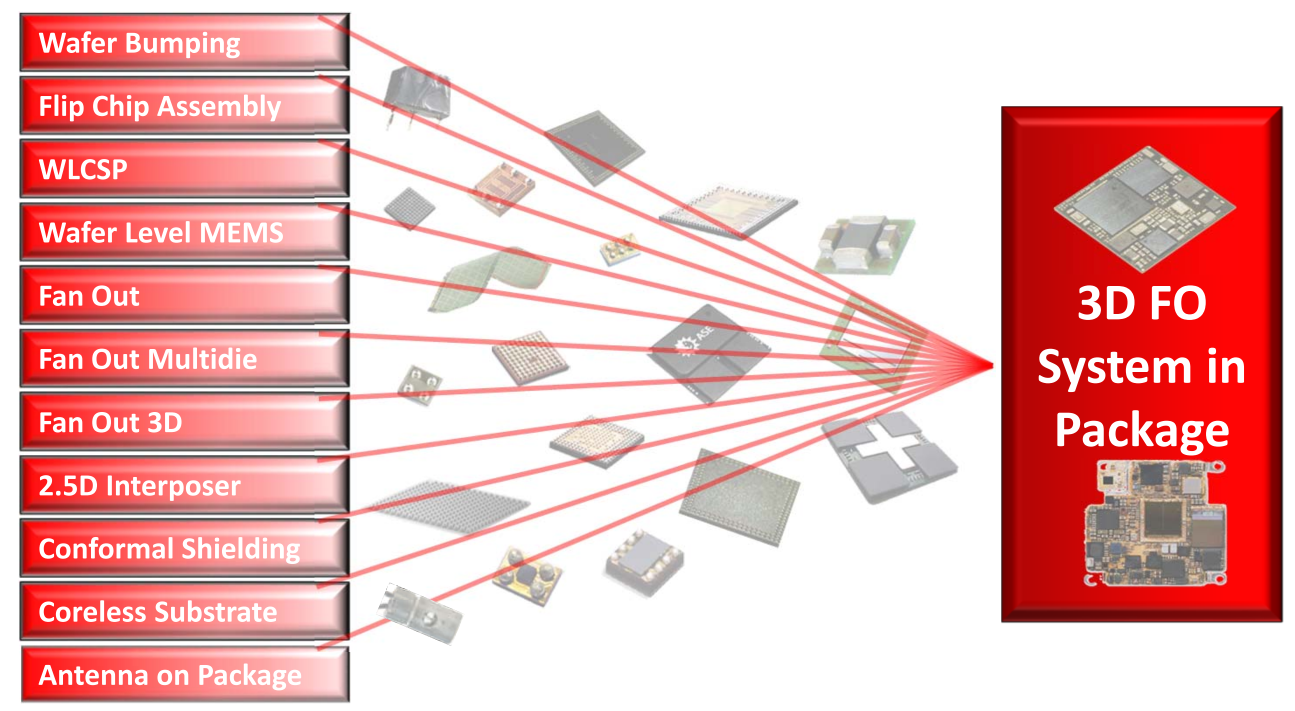
- ✓Heterogeneous System Integration
- ✓Fan-out Wafer Level Packaging
- ✓Embedded Multi-die Integration Bridge
- ✓3D Integration
- ✓System in Package

Heterogeneous System Integration



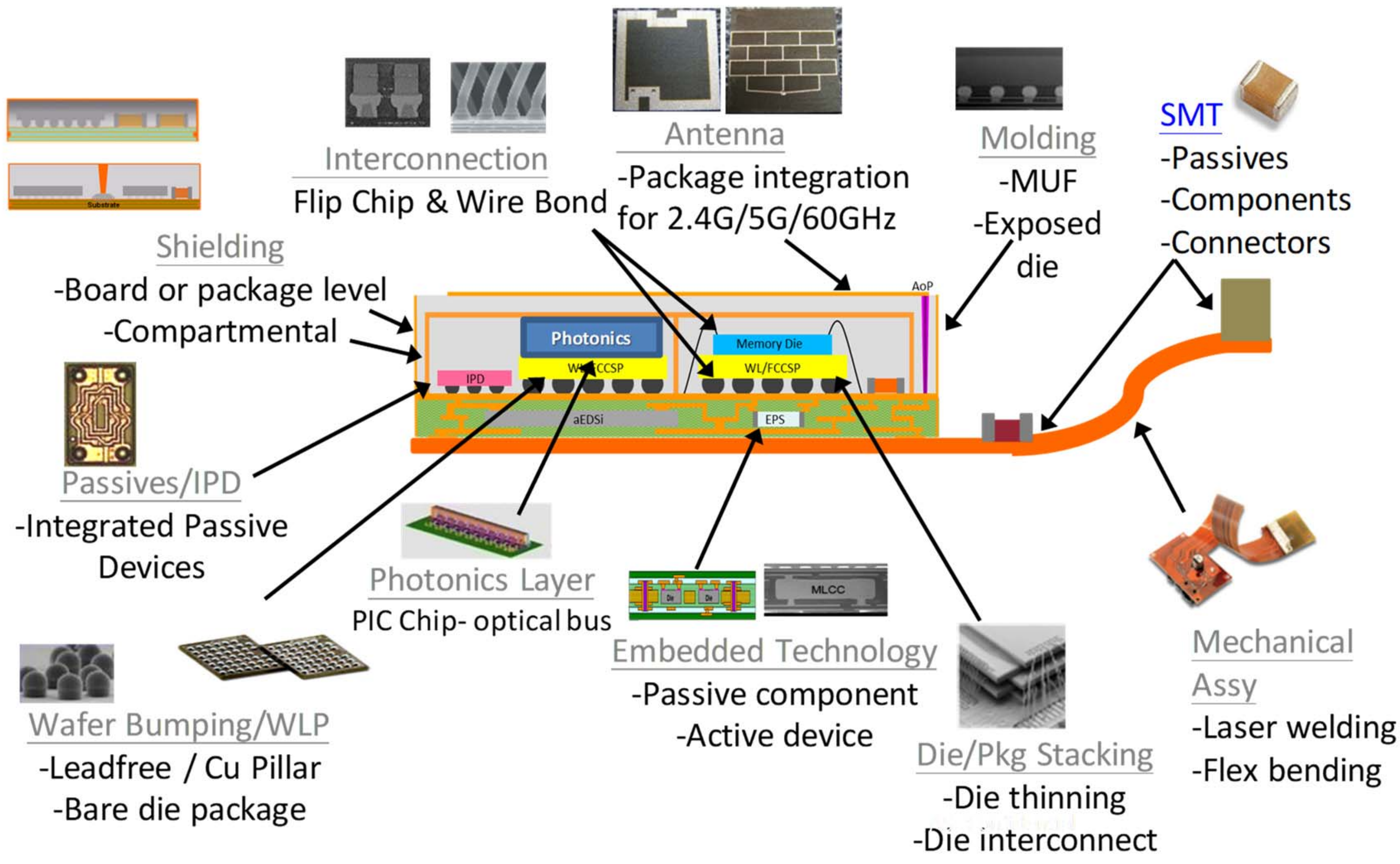
Heterogeneous by material, component type, circuit type, node and bonding/interconnect method

Convergence to 3D SiP



Source: John Hunt, ASE

Electronic/Photonic SiP through Heterogeneous Integration



Source: ASE with additions

The Revolution In Packaging Supporting Heterogeneous Integration And 3D Integration In The Past Two Years

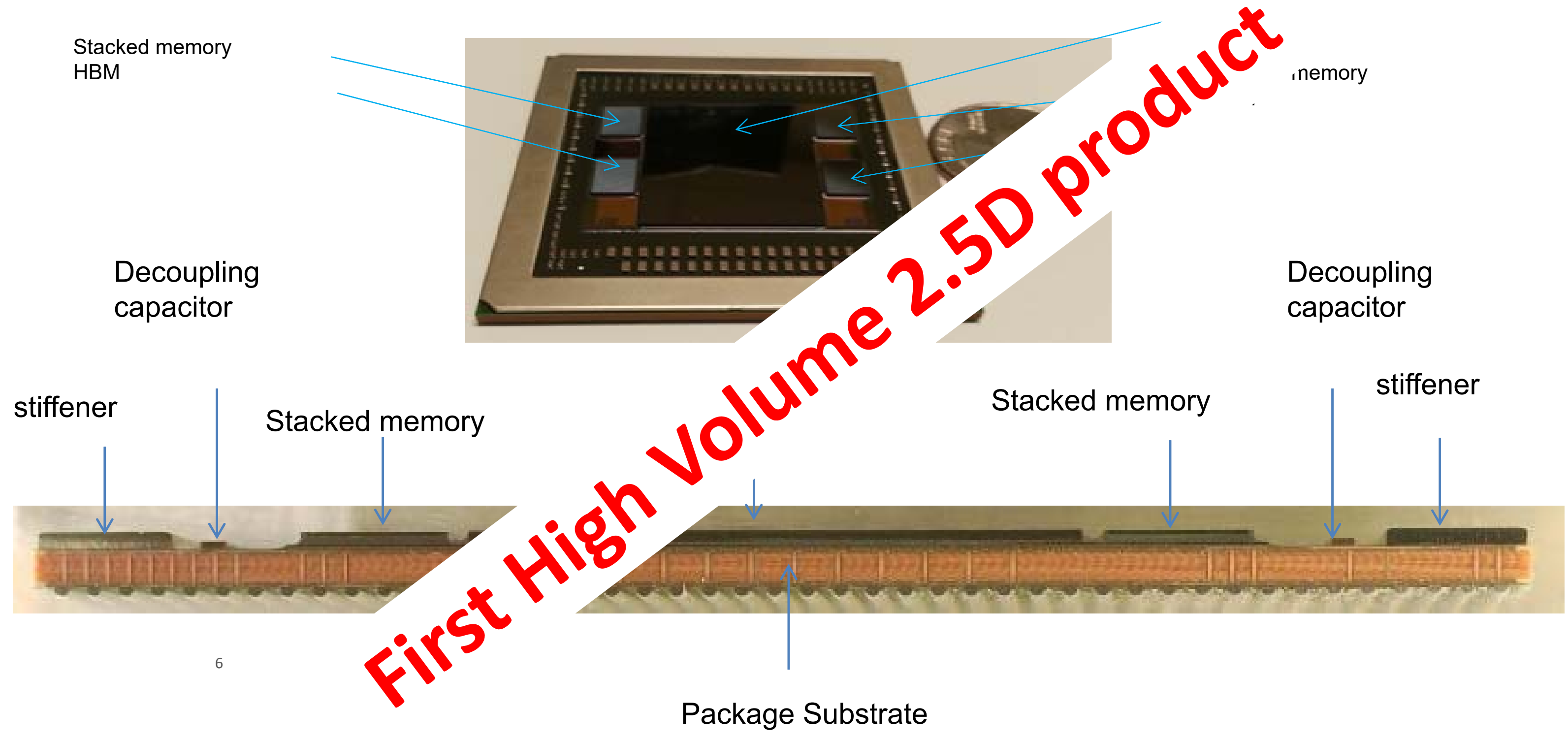
Si Photonic ICs Are In High Volume Production

Intel's Silicon Photonics 100G PSM4 (Parallel Single M
fiber 4-lane) QSFP28 is ***the first*** small formfactor, h
speed, low power consumption Optical Transce

- ✓ Optical links over single-mode fiber.
- ✓ Applications
  - Connectivity for large scale cloud ... prise data centers
  - Ethernet switch, router, and ... telecom interfaces
- ✓ Features
  - Compatibility with ... e fiber connectors
  - Operating tem ... ange: 0 to 70°C
  - 3.5 W max ... ver dissipation
  - Electri ... ce IEEE 802.3bm
  - R ... 2 km

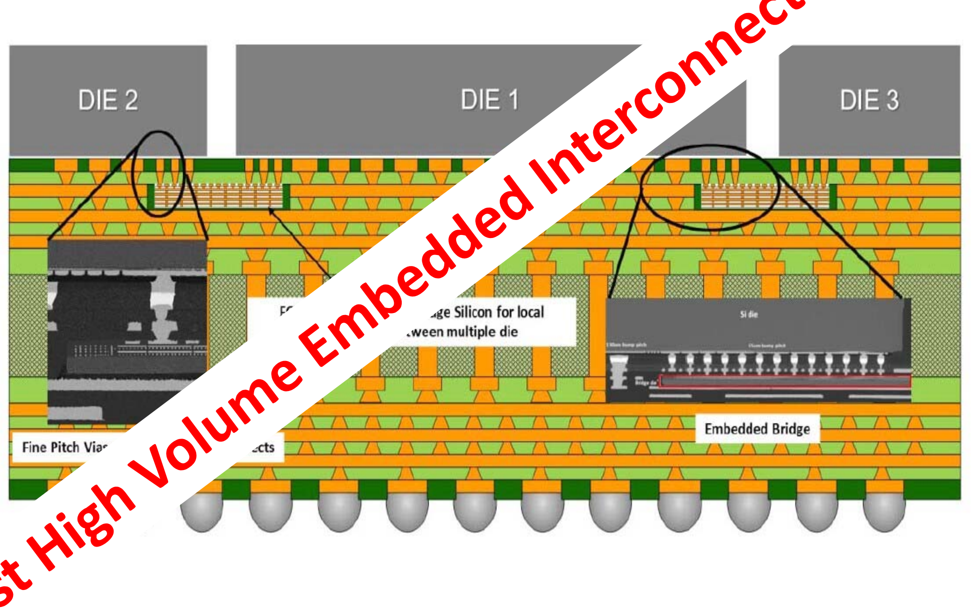
First High Volume Photonic IC Product

AMD Fiji Graphics Processor



Intel Embedded Multi-die Interconnect Bridge

✓ EMIB uses thin pieces of silicon (< 75um) containing fine pitc… …connect (~2um L/S) embedded in an organic substrate to enable dense die … …interconnect between die on the BGA like laminate substrate



First High Volume Embedded Interconnect bridge Product

Apple A10 Fan Out Package

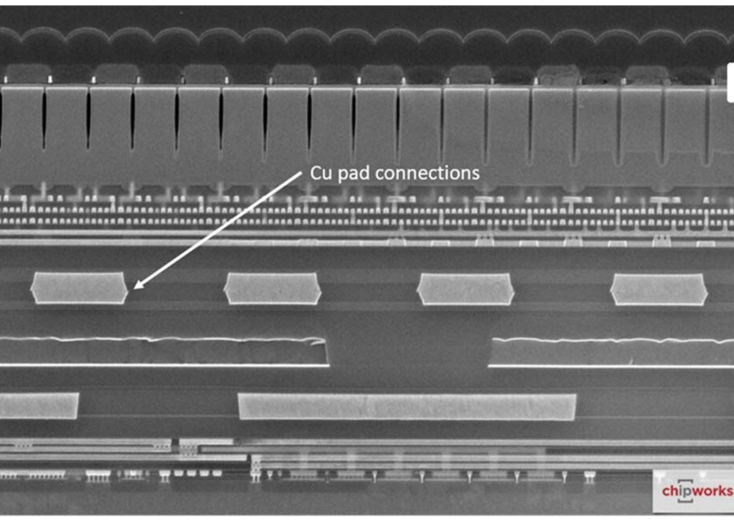
TSMC Info

Direct Bond Interconnect Is Now In High Volume Production

Samsung’s Galaxy S7 is the first high ... use of the Ziptronix’s DBI technol... ...ony CMOS image sensor

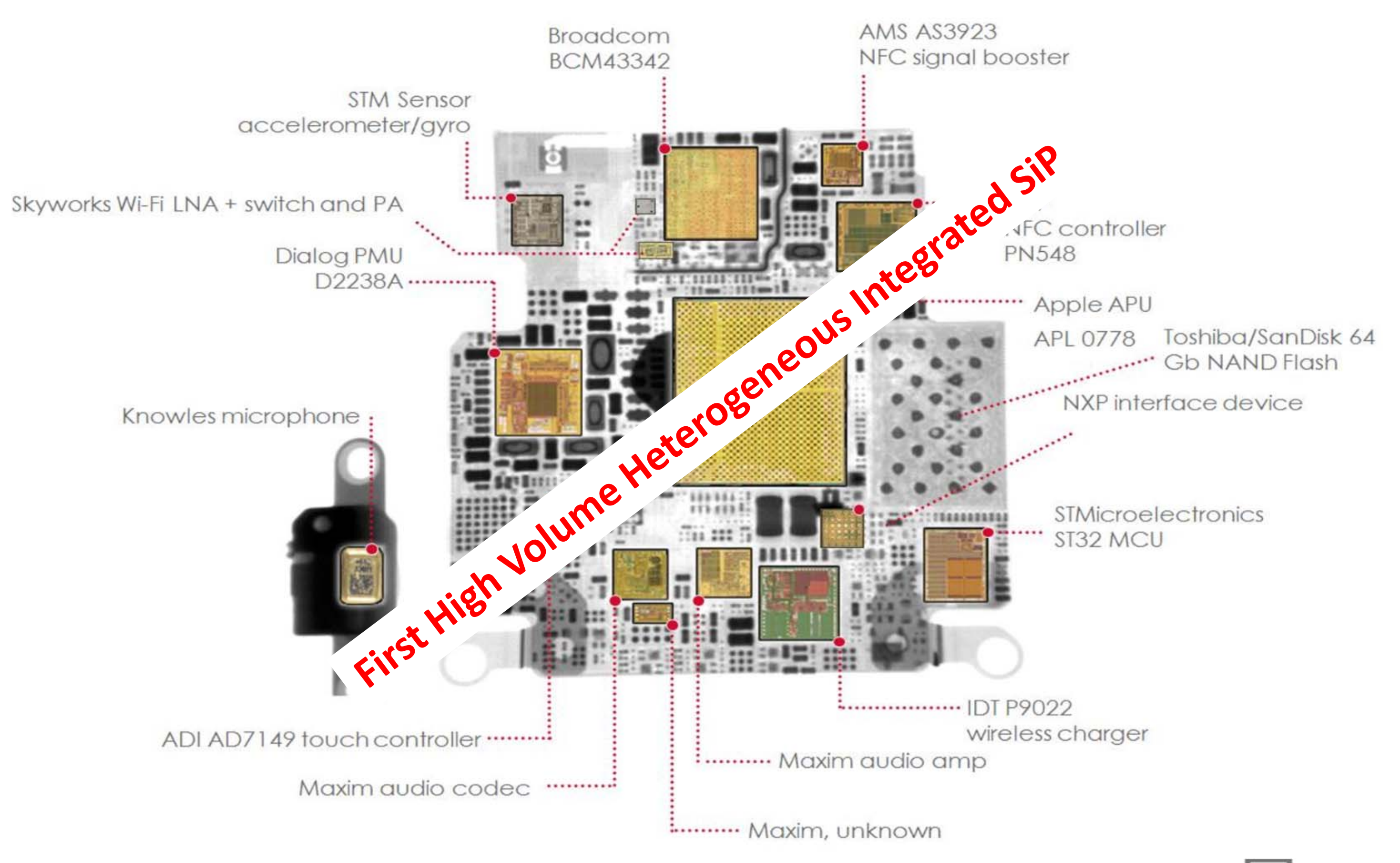
- Bonding force is distribute... ...ectric and conductor interfaces
- Near use case temp... ...ocessing
- No under fill r...

First High Volume DBI 3D Technology Product



Chipwork... ...CMOS image sensor sh... ...per pad connections

Apple Watch S1 (Heterogeneous) SiP



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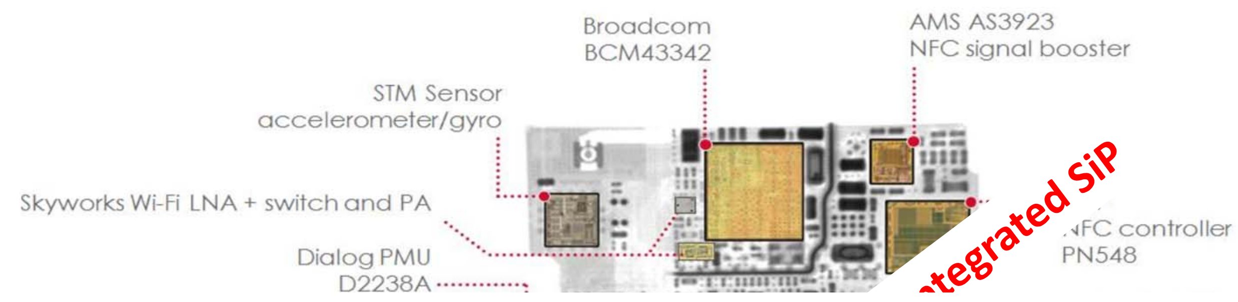
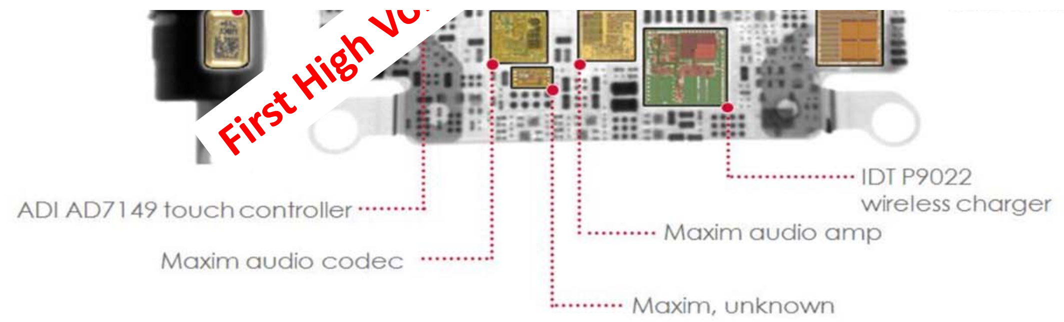


Complex, high performance, low cost and this is just the beginning



Components Incorporated In 3D SiP

Over the next 15 years components incorporated into 3D packages include:

- ✓ Monolithic integrated photonic ICs (photonics, electronics and plasmonics)
- ✓ Other optical components that are not integrated in the SiPh-ICs.
- ✓ Si based logic and memory ICs
- ✓ MEMS devices
- ✓ Sensors
- ✓ GaN power controller circuits
- ✓ RF circuits
- ✓ Compound semiconductor lasers
- ✓ Optical interconnects to and from the outside world
- ✓ Electrical interconnects to and from the outside world
- ✓ Passive components
- ✓ Embedded passives and actives

New devices and new materials that will be developed over next 15 years

Components Incorporated In 3D SiP

Each of these has there own requirements for thermal, mechanical, optical and electronic properties that must co-exist in a single package.

This poses many new challenges for packaging Co-Design and Co-Simulation

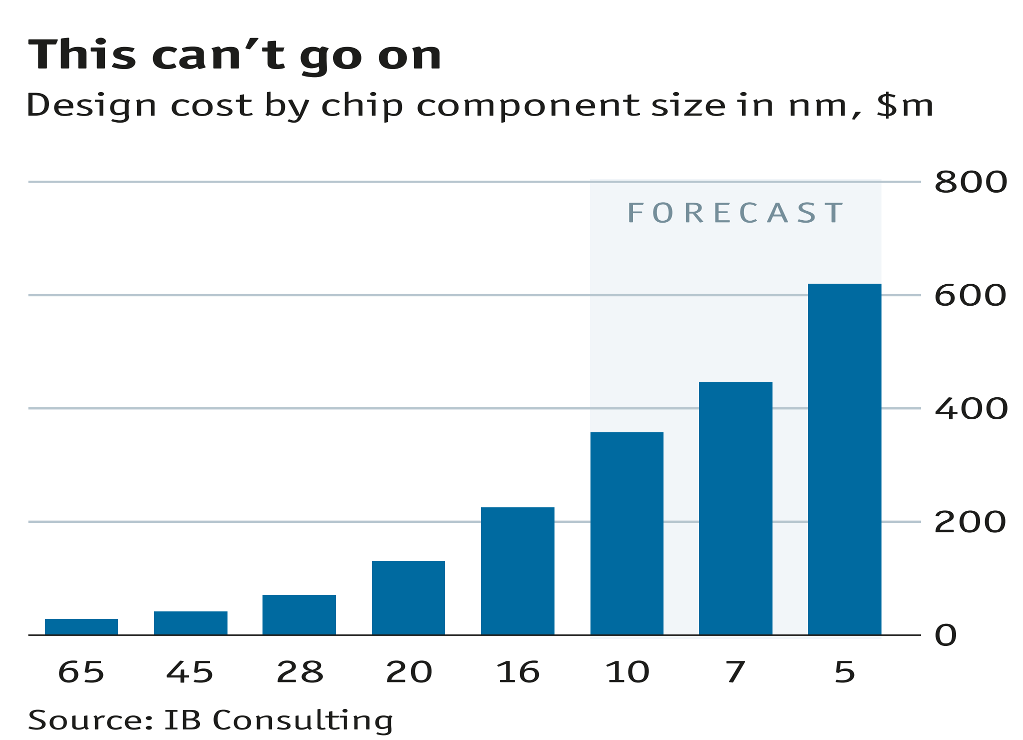
The Most Efficient Path To Progress Has Changed

"For the past 50 years, the cheapest and easiest way to increase complexity was to shrink the feature size and grow the wafer diameter.(That was classic Moore's Law) Now there is a tradeoff. We will do the things that are most economic for the capabilities we want. Some of those will keep us going with smaller and smaller feature sizes almost forever. **But the most economical tradeoff is likely to be a combination of better system engineering, multi-chip packaging, and a whole variety of other techniques to keep advancing the capabilities in the most cost-effective way**." Wally Rhines, Chairman Mentor Graphics.

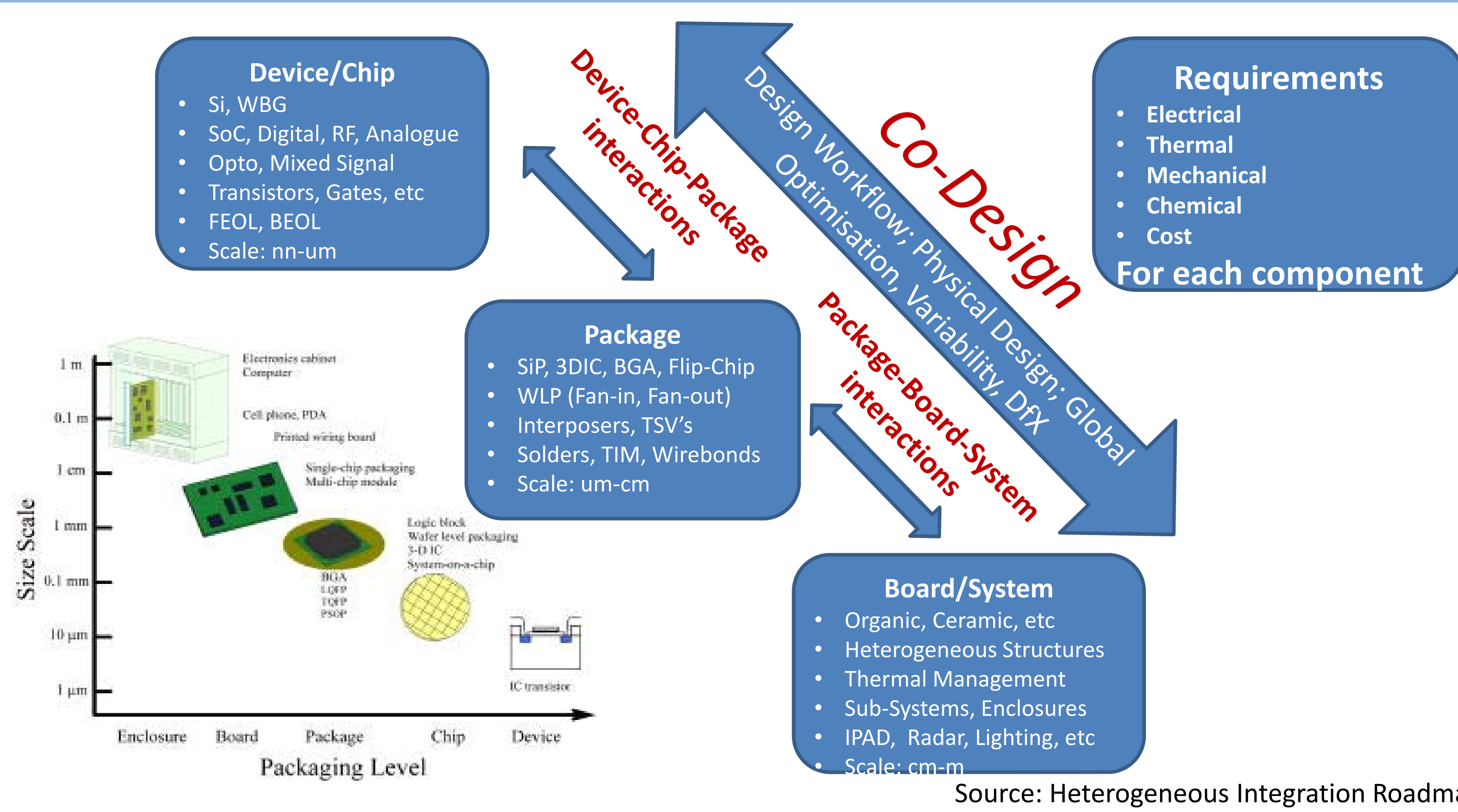
Source: Semiconductor Engineering, Ed Sperling, April 20 2017

Design Cost Escalation May Be The Biggest Challenge

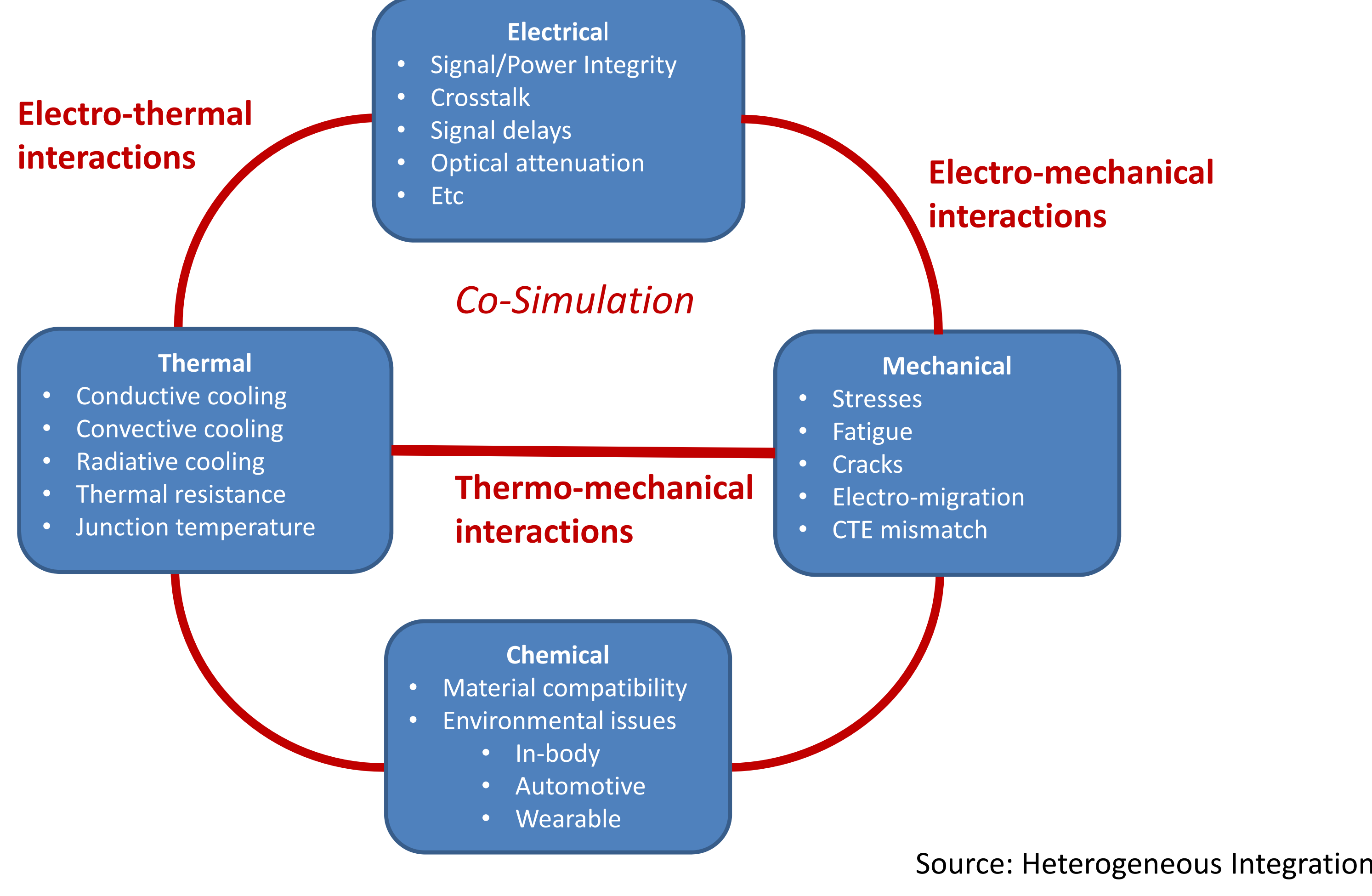
- ✓ Chip Design cost is driven by complexity
- ✓ 3D-SiP Packaging is growing in complexity resulting in NRE including co-design and co-simulation becoming the limiting factor
- ✓ Small volume products cannot support the cost



System Level Co-Design



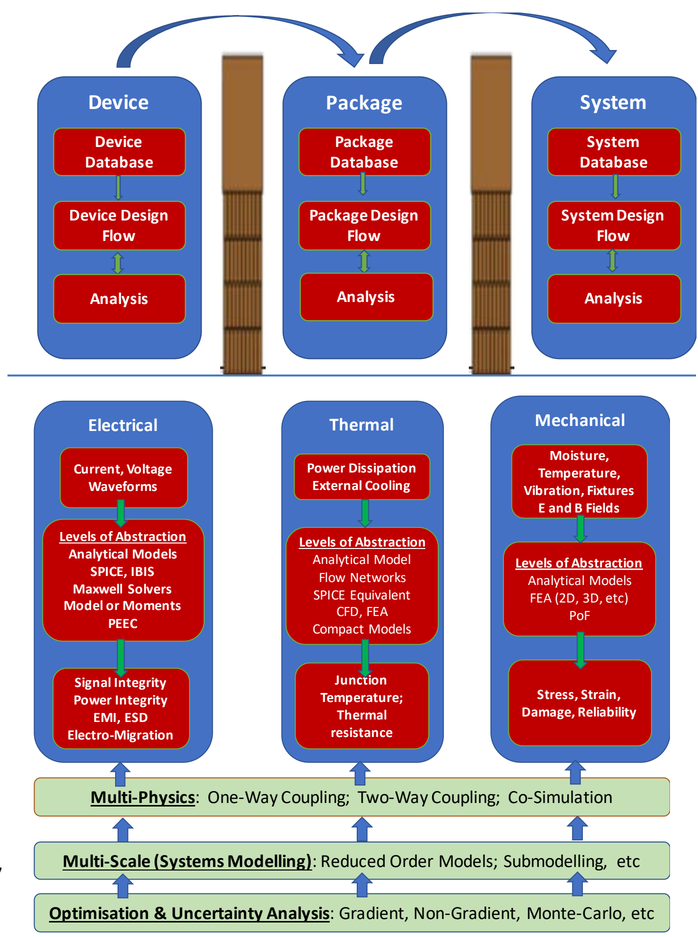
Multi-Physics Co-Simulation



Source: Heterogeneous Integration Roadmap

3D-Design Challenges

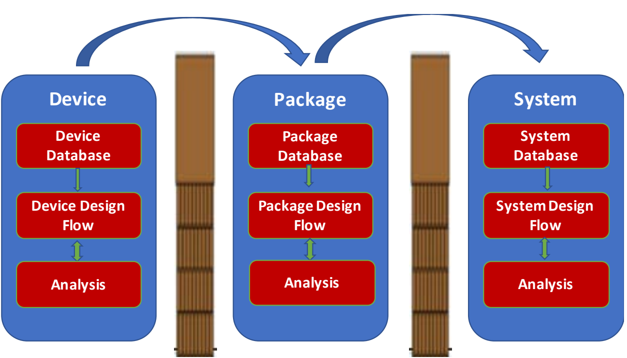
- 3D adds significant complexity
  - Physical design (RDL, Routing, etc)
  - Signal quality, power delivery
  - Thermal behavior (staked dies)
  - New failure modes (TSV's, etc)
- Tools
  - Many point analysis tools
    - Electrical, Thermal, Optical Mechanical
    - Different levels of abstraction
  - Different tools used
    - Device, package, board domains
- Design
  - Design flows disconnected
  - Design data exchange done manually



Source: Heterogeneous Integration Roadmap

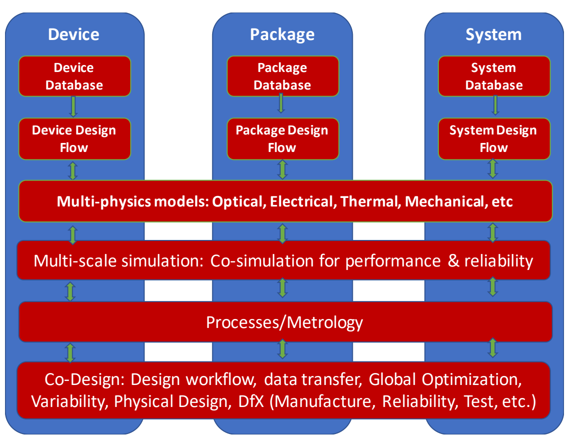
Moving to a new paradigm

Today (Generally)



- ✓ Single Physics
- ✓ Single component
- ✓ Single user
- ✓ Few design points investigated

Future



- Multi-Physics/Scale
  - Processes
  - Performance
  - Reliability/Robustness
- Collaborative
- Design exploration
- System aware design

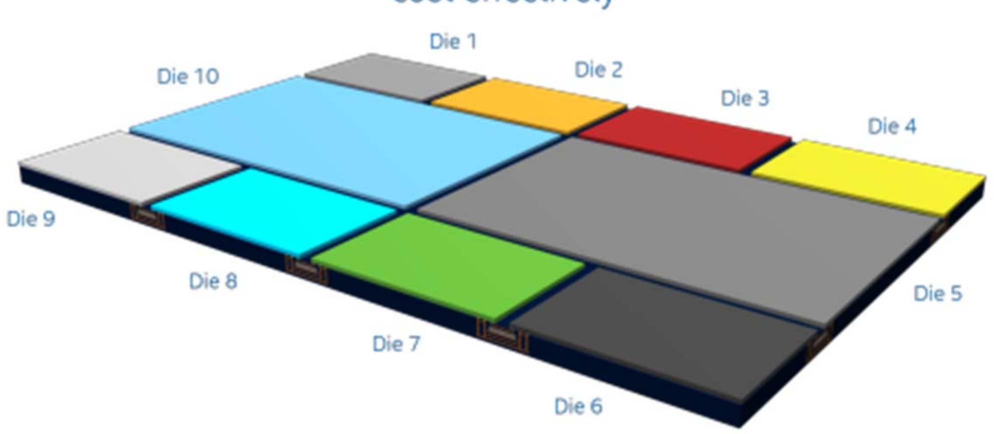
Source: Heterogeneous Integration Roadmap

Intel Embedded Multi-die Interconnect Bridge
The Next Generation of Implementation

Intel Introduced the next generation of EMIB at Hot Chips last week

- ✓ Many die in one piece without large area interposer
- ✓ Components of different nodes in one piece
- ✓ Rapid deployment of advanced nodes
- ✓ Heterogeneous integration

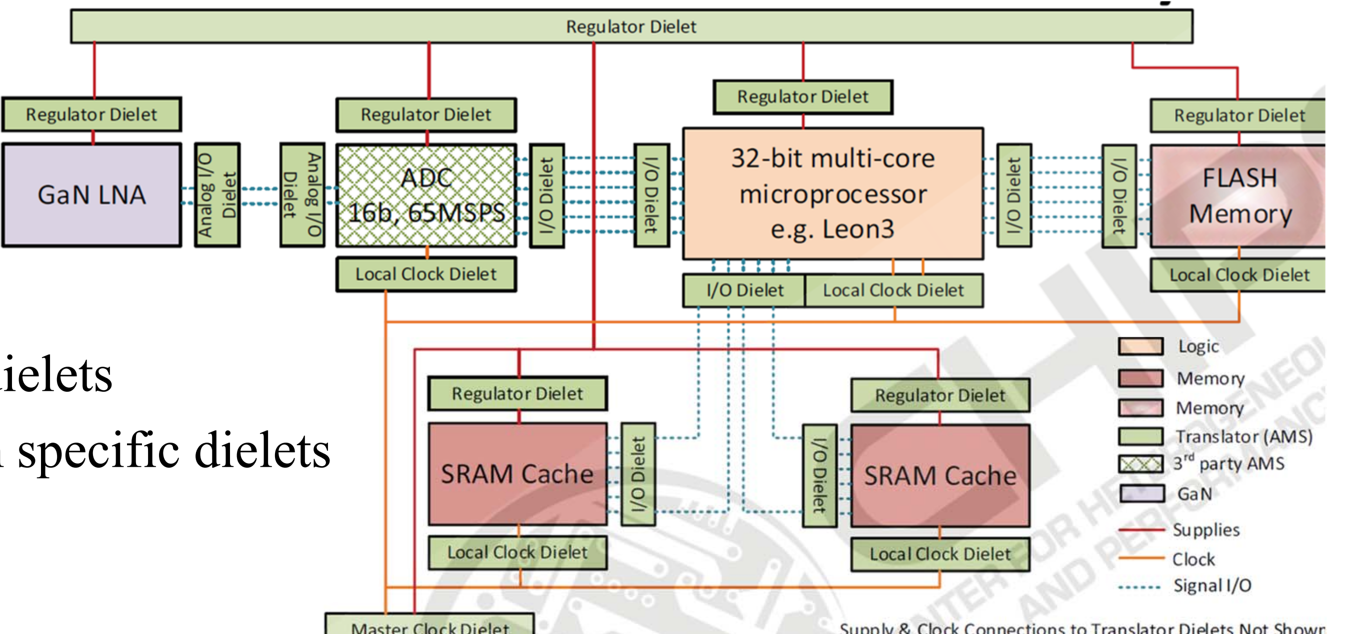
Available to 14nm Foundry Customers now



UCLA's Active Interconnect Fabric
A Plug and Play Dielet Solution

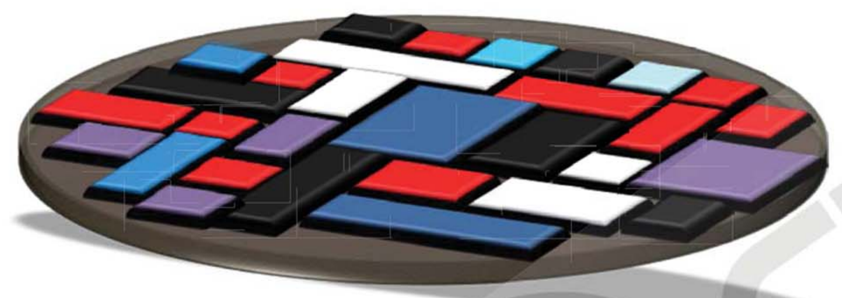
Active Interconnect Fabric

- ✓ Hard IP Library cells available
- ✓ A library of dielets for interface tasks
  - Regulators dielets
  - I/O dielets
  - Clock dielets
  - Test dielets
  - other
- ✓ Green blocks are interface dielets
- ✓ Other blocks are application specific dielets



Source: UCLA Center for Heterogeneous Integration and Performance Scaling

Interconnect Fabric is A Silicon Technology



The "right" interconnect fabric

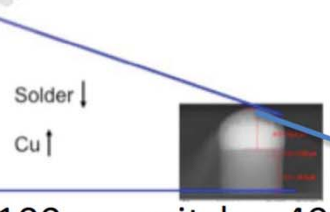
- Mechanically robust (flat, stiff, tough...)
- Capable of fine wiring, fine pitch interconnects
- Thermally conductive
- Can have active and passive built-in components

Silicon Fits the Bill

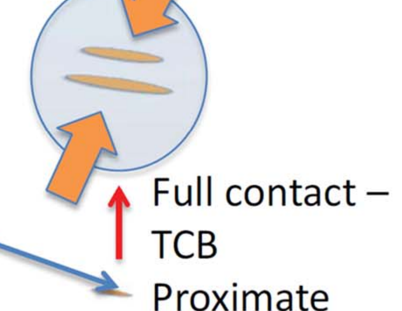
Challenges:

- Warpage
- Topography
- Assembly /Thru'put
- Thermal

>100 µm pitch
Mass reflow



100µm >pitch > 40 µm
Mass re-flow+TCB



2-10µm

Full contact – TCB
Proximate
- Inductive
- Capacitive

Source: UCLA Center for Heterogeneous Integration and Performance Scaling

Target: Push Button System Interconnect Fabric

Standardized Interfaces enabling fast IF-based System Design

- Physical standardization
  - pad/bump sizes, wire pitches
- Electrical standardization
  - voltage/current levels, resistive/capacitive load
- Functional standardization
  - Communication interfaces e.g., multi-Gb/s digital I/O, Z-controlled analog I/O, etc.
  - Dielet health monitor interfaces
    - Temperature, state info, error/mismatch info etc.
    - Facilitate system tuning, self-healing, self-testing
  - Control interfaces
    - Dielet configuration, etc
- Test standardization
  - Continuity tests, JTAG-like infrastructure for BIST

Source: UCLA Center for Heterogeneous Integration and Performance Scaling

CHIPS
CENTER FOR HETEROGENEOUS INTEGRATION
AND PERFORMANCE SCALING

Imec's 3D Interconnect Alternatives Today

- ✓3D adoption was slowed by cost and lack of co-design and simulation tools
- ✓Design and simulation tools were slow due to small perceived market size

This is now rapidly changing

	3D-SIP			3D-SIC	3D-SOC			3D-IC
3D Technology	"PoP"	"Chip last"	"Chip first"	Die stacking	Parallel W2W		Sequential FEOL	
3D-Wiring level	Package I/O	Chip I/O Interposer I/O	Chip I/O	Global	Semi-global	Intermediate	Local	FEOL
				Chip BEOL Wiring Hierarchy				
Partitioning	Functional unit	subsystem	Embedded die	Die	Blocks of standard cells		Standard cells	Transistors
Technology	Package-to Package reflow	Multi-die SIP 3D/2.5D stack	FO-WLP Embedded die	3D D2D, D2W 2.5D Si-interposer	Wafer-to-Wafer bonding Hybrid bonding	Via-last	Active layer transfer or deposition	
2-tier stack Schematic								
Characteristic	Solder ball Stack	• C4, Cu-pillar Si-Organic • Through-Mold-vias	• Bumpless • Si-RDL • Through-Package-vias	• µbump • Si-to-Si • Through-Silicon-Via	BEOL between 2 FEOL layers			FEOL stack
					Overlay 2nd tier defined by W2W alignment/bonding		Overlay 2nd tier defined by litho scanner alignment	
Contact Pitch	400⇒350⇒300µm	120⇒80⇒60µm	60 ⇒40 ⇒20µm	40 ⇒20 ⇒10⇒5µm	5µm ⇒ 1 µm	2 µm ⇒ 0.5 µm	200nm ⇒ 100nm	< 100 nm
Relative density:	1/100⇒1/77⇒1/55	1/9⇒1/4⇒1/2.3	1/2.3⇒ 1 ⇒ 4	1 ⇒ 4 ⇒16⇒ 64	64 ⇒ 1600	400 ⇒ 6400	4 10^4 ⇒ 1.6 10^5	> 1.6 10^5

A new Era view from DARPA’s Bill Chappell

Director of DARPA’s microsystems group

“The next era we're heading into is about progress in lots of variables…hardware/software co-design, new materials and functional blocks, specialization for each app…We’re not out of ideas at all, this is **a wildly interesting time where lots of creativity will make up for the march of scaling**,”

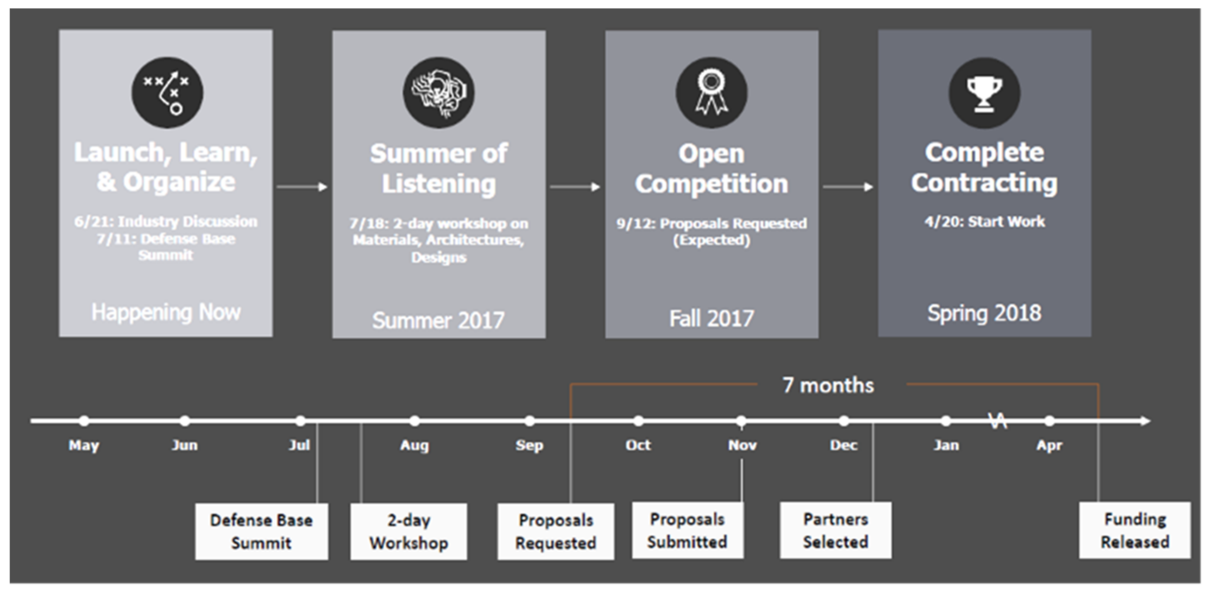
Chappell

Darpa's $200M ERI program has a schedule

Electronics Resurgence Initiative

Supporting a new era of electronics in which advances in performance will be catalyzed not just by continued component miniaturization but also by radically new microsystem materials, designs, and architectures.

Hundreds of people, 45 companies, 10 defense contractors and many universities are already participating



DARPA Heterogeneous Integration Program (CHIPS)

Focused on Advanced Modular SiP

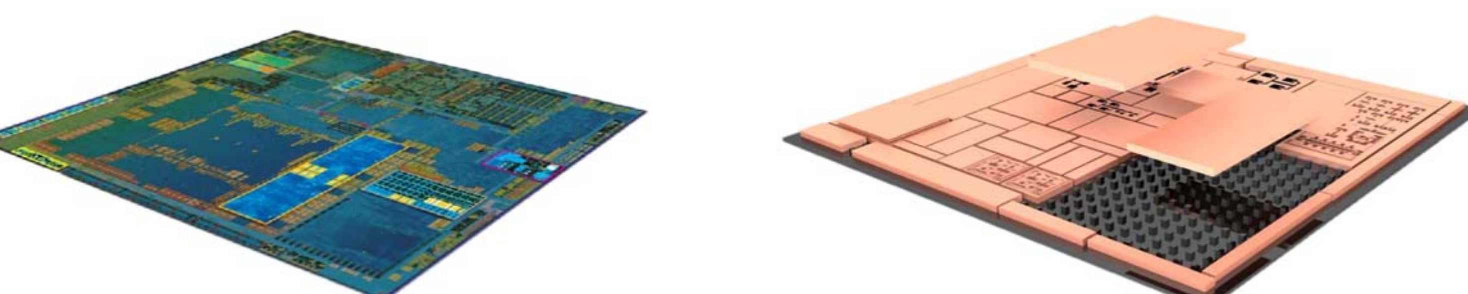
What is CHIPS?

Common Heterogeneous integration and IP reuse Strategies program

CHIPS will develop the **design tools and integration standards** required to demonstrate **modular electronic systems** that can leverage **the best of DoD and commercial** designs and technology.

Today – Monolithic

Tomorrow – Modular



Heterogeneous Integration Program at DARPA

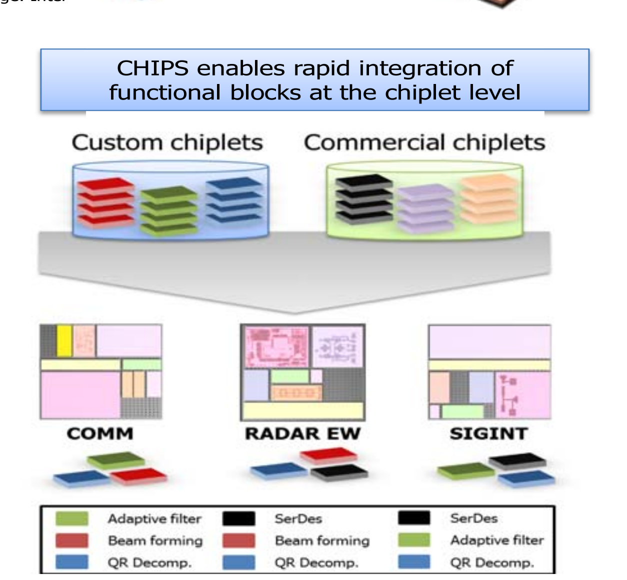
Source: Daniel S. Green - MEPTEC Heterogeneous Integration Roadmap Symposium November 10th 2016 San Jose California

Developing **design tools, integration standards and IP blocks** required to demonstrate **modular electronic systems** that leverage **the best of DoD and commercial** designs and technology

Today – Monolithic

Tomorrow – Modular

Image: Intel

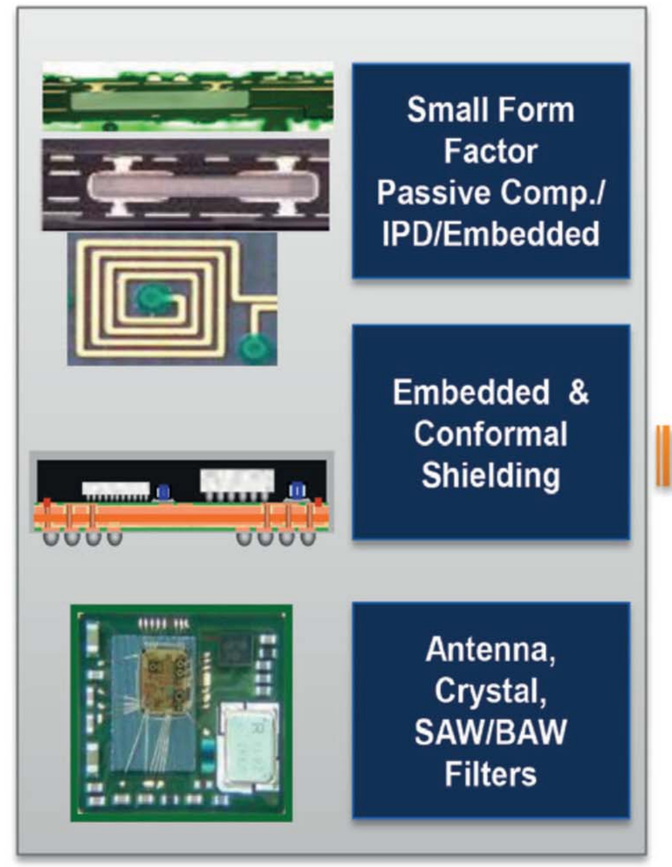


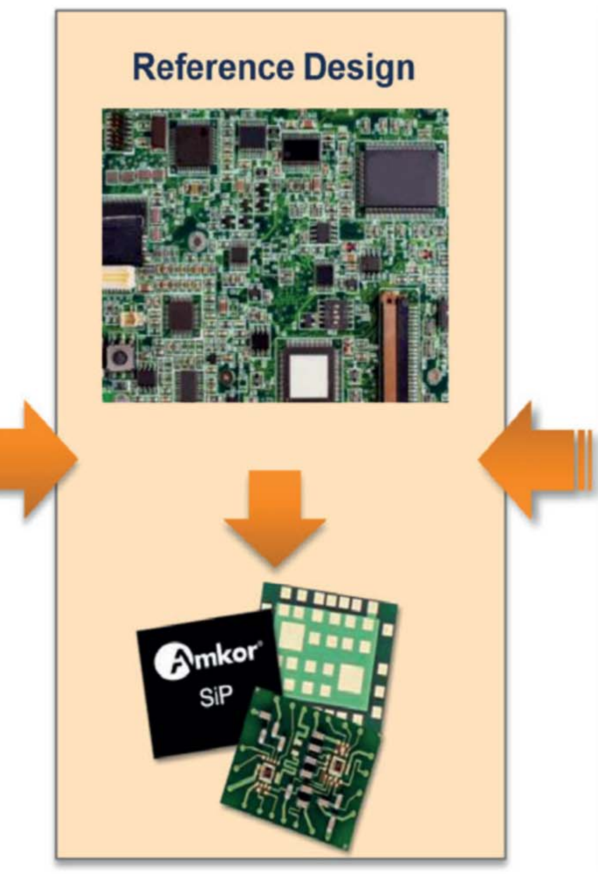
OSATS Are Investing In The Solutions

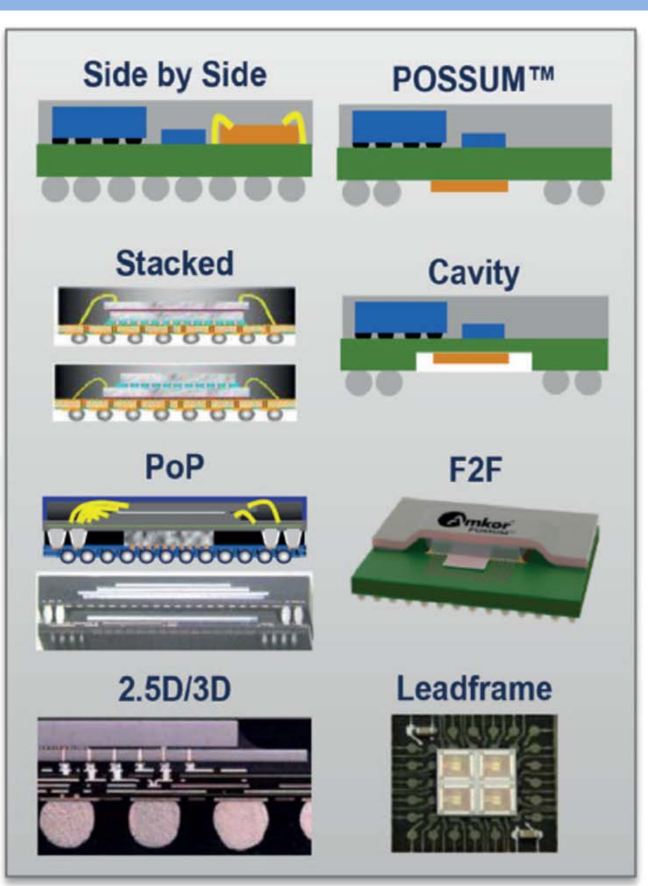
- ✓ Design flows for 3D Heterogeneous integration
- ✓ Reference designs for specific applications
- ✓ Support for
  - 3D
  - FOWLP
  - Panel Processing
  - Photonic Integrated Circuits

Much more is needed for low cost, high throughput Co-Design and Co-Simulation

SiP Reference Design With Standard Components Reduces Design Cost And Drives Higher Volume





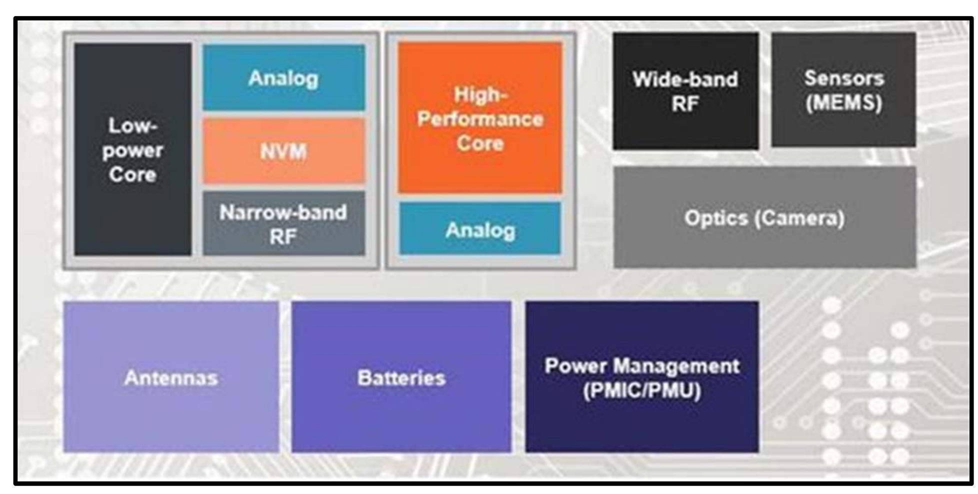


Source: Amkor Technologies, Inc.

The IoT Sensor Hub Must Be A SiP

The sensor hub must combine many functions:

- ✓ Sensors
- ✓ Analog/mixed signal circuits (ADC, etc.)
- ✓ Nonvolatile memory
- ✓ Multi-band RF
- ✓ Antenna
- ✓ Battery/super-capacitor
- ✓ Power management
- ✓ Power scavenger



The IoT Sensor Hub Must Be A SiP

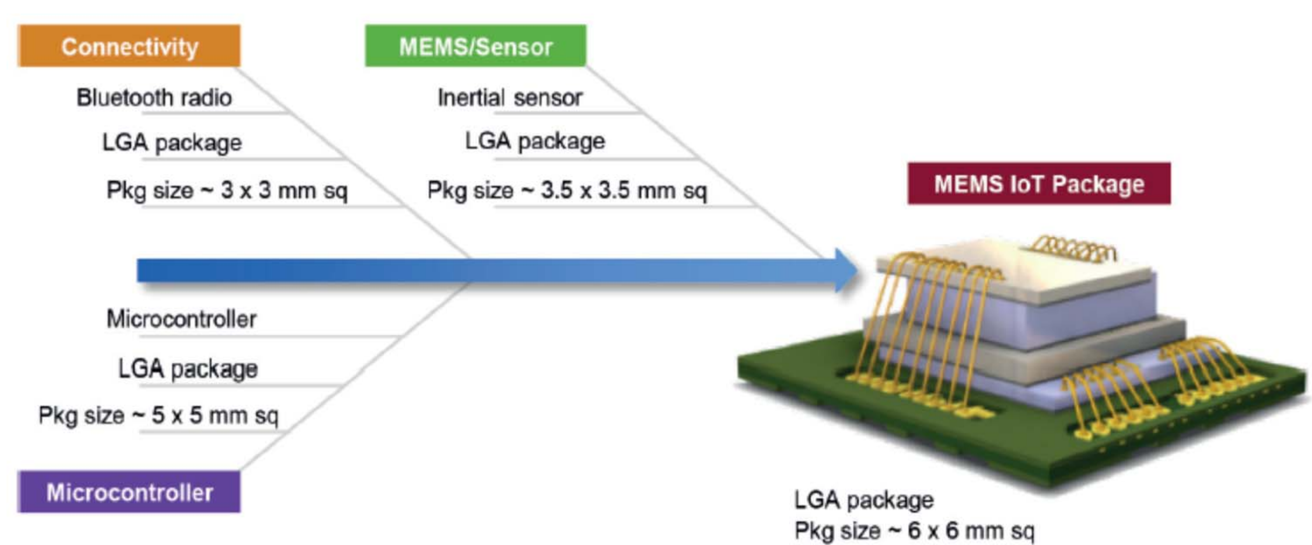
Make it standard for the Hub manufacturer and custom for the final product manufacturer customer

Provide bonding pads for many components with option to populate only what is needed for a specific product design

MEMS Sensor IoT Package

IoT sensor hub components assembled into SiP with all packaged die.

- ✓Blue tooth radio in package
- ✓Microcontroller in package
- ✓MEMS sensor in package



Source: Amkor, Chip Scale Review March-April 2016

The Software Industry is Responding

Value creation is moving to the package from the IC as the “low hanging” fruit to continue the rate of progress

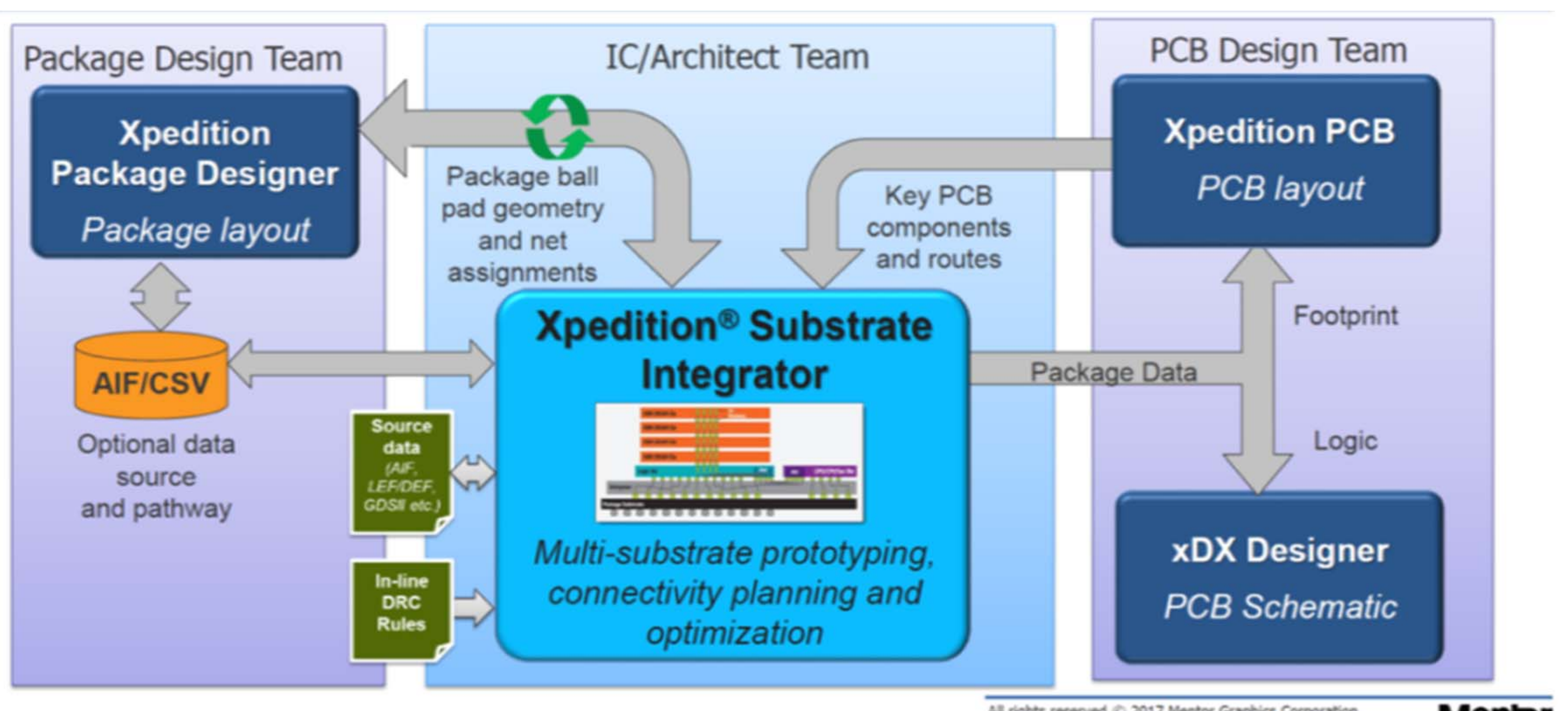
✓ Design and Simulation Tools are coming to address new opportunities and challenges:

- Heterogeneous Integration reducing power but power density increases with increasing 3D functional density.
- Different coefficients of thermal expansion (CTE) of tightly packaged materials cause thermal-mechanical stress and may lead to reliability failures, if not considered during the design process

New flows for co-design, verification and product simulation are coming as the industry recognizes the opportunity associated with the need. But it is just beginning

Mentor's High-Density Advanced Packaging design flow (HDAP)

This June Mentor announced its HDAP design flow and its OSAT Alliance Program



Heterogeneous integration in Design and Production

- ✓Working with OSATs such as Amkor to help drive ecosystem capabilities in support of new HDAP technologies like 2.5D ICs, 3D ICs, and fan-out wafer-level packaging (FOWLP) for customer IC designs.
- ✓Creating certified design kits that help mutual customers speed up IC and advanced package development using Mentor's Tanner® L-Edit AMS design cockpit, Calibre® IC physical verification platform, HyperLynx® SI/PI and HyperLynx full-wave 3D tools, Xpedition® Substrate Integrator, Xpedition Package Designer tools, and newly announced Xpedition HDAP flow.

Source: Mentor web site

What Is needed For Cost and Time To Market

✓Modular EDA components that can interoperate with compatible data base structure or translating wrappers.

✓Standard system component designs (passive and active) that can be interconnected with automated EDA tools.

✓Support for the full spectrum of interconnect technologies (electrical, optical, RF) and processes (3D, 2.5D, EMIB, DBI, wire bond, etc.)

✓System level simulation tools capable of product performance verification enabling optimization in the computer rather than through fab cycles.

✓Modular, open architecture for all design and simulation tools to reduce the cost and time for inserting new materials, processes and architectures.

✓Materials properties for thin layers where interface properties dominate.

Summary

There are many difficult challenges that must be overcome before the needed Co-design and Co-simulation tools are available.

Those that invest successfully in this expertise will be handsomely rewarded

The Design and Simulation capability coming will enable a new generation of information technology and artificial intelligence driving a pace of progress that maintains or exceeds that of Moore's Law for decades to come

Thank You for Your Attention