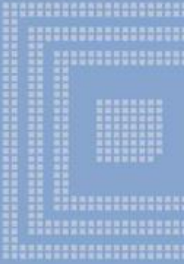

SiP Technology Direction and Design Challenges

CP Hung, Ph.D.

VP of Corporate R&D
ASE Inc.

21 Sep 2017

Contents

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- SEMI Industry Trend
- Industry SiP Interconnection Changes
- Technologies with Max & Min Trend
- Semi Eco-system Triggered Comprehensive SiPs

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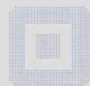
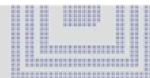

Volume Paradigm Past & Future

Now

Accelerating Devices # > 10x

Aerospace
Thousands Units

Mainframe
Millions Units

PC (PM)
350M+ Units

Cell Phone (PP)
1.8B+ Units

Smart Computing (PMP)
10B+ Units

Internet of Things (IOT) (PMMP)
100B+ Units
Exponential Connectivity & Big Data

Long Tail

1970s 1980s 1990s 2000s 2010s 2020s

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New IC Packaging DNA - TSV

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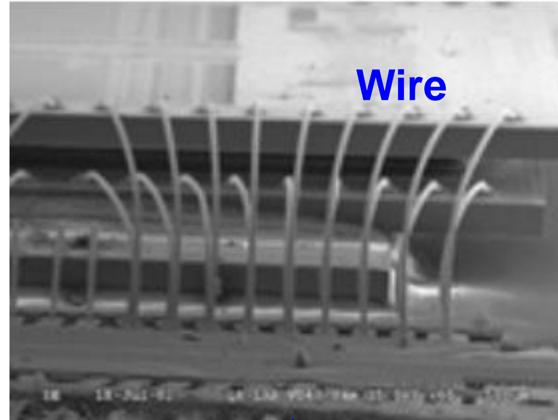
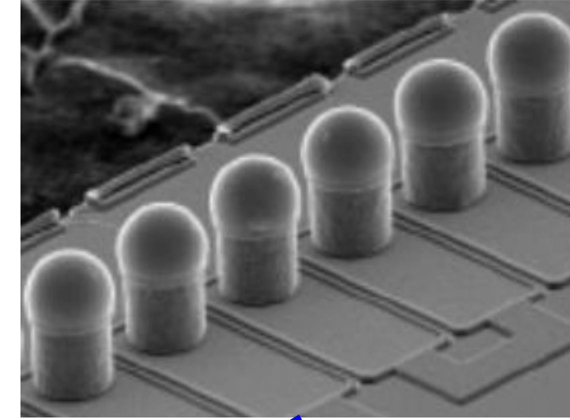
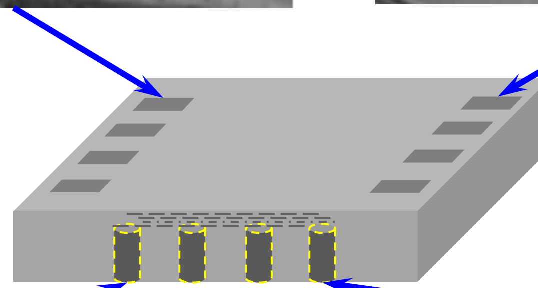
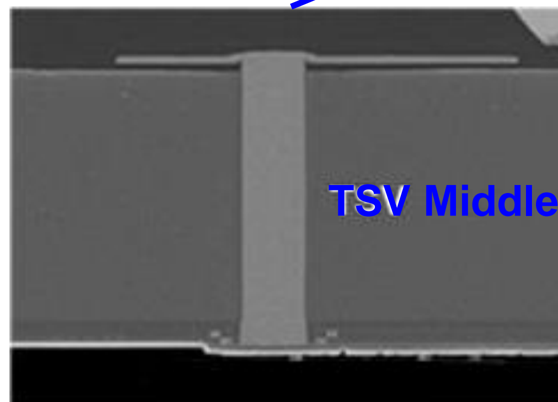
2D Interconnection from Topside of Chip

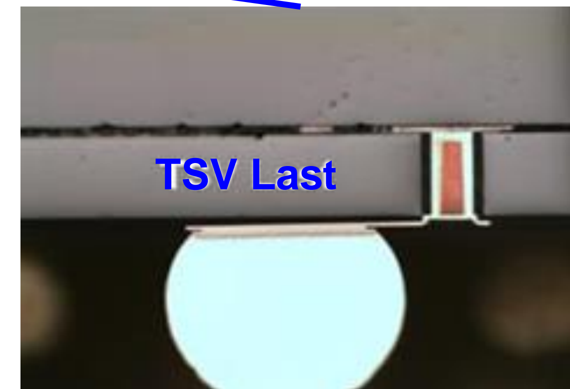


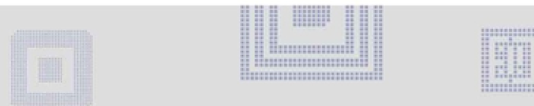




Adding Backside Interconnection → 3D







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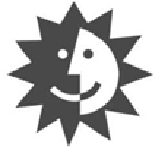
SiP Solutions for “Terminals” & “Cloud”



SiP I/O

FO, 2.5D & 3D IC BGA

Maximizing

Deep Learning

Networking

Compute

FC BGA

Max Limit

BGA

QFP

Die

QFN

WLCSP

3D WL SiP

MEMS

ASIC

XY

Min Limit

Power

Connect

Collect

Z

Embedded SiP

Minimizing

aEASI

FO SiP

SiP Size

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2.5D / 3D IC to FO Packaging Technology

Density of IC Package

2.5D IC FCBGA with Si Interposer

FO (Fanout)

2.nD with Advanced Substrate

3D IC FCBGA

Glass Platform

FCBGA

Current Substrate

Advanced “Substrate”

Silicon Substrate

L/S

10um/10um

1um/1um

Gap Filling

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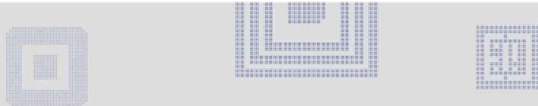

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Thank You

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