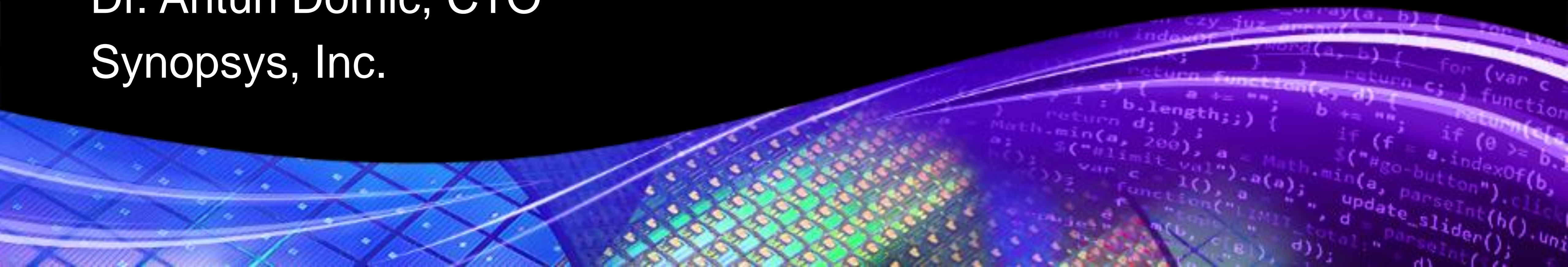
Some Implications Brought In By The Coming Semiconductor Technologies

Dr. Antun Domic, CTO
Synopsys, Inc.



The Rice-And-Chessboard Problem

Once Upon a Time, King Gordon Moore…

1958
1st Integrated Circuit
4 Transistors

2017
State-of-the-Art CPU
19B Transistors
@14nm

2017
State-of-the- Art FPGA
17B Transistors
@ 14nm

1	2	4	8	16	32	64	128
256	512	1024	2048	4096	8192	16384	32768
65536	131072	262144	524288	1048576	2097152	4194304	8388608
16777216	33554432	67108864	1.34E+08	2.68E+08	5.37E+08	1.07E+09	2.15E+09
4.29E+09	8.59E+09	1.72E+10	3.44E+10	6.87E+10	1.37E+11	2.75E+11	5.5E+11
1.1E+12	2.2E+12	4.4E+12	8.8E+12	1.76E+13	3.52E+13	7.04E+13	1.41E+14
2.81E+14	5.63E+14	1.13E+15	2.25E+15	4.5E+15	9.01E+15	1.8E+16	3.6E+16
7.21E+16	1.44E+17	2.88E+17	5.76E+17	1.15E+18	2.31E+18	4.61E+18	9.22E+18

1971
1st CPU
2,300 Transistors
@ 10um

2017
State-of-the-Art GPU
20B Transistors
@ 12nm

2012
State-of-the-Art 128GB DRAM
137B Transistors
@ 30nm

Source: Ibn Khallikān, ca. 1256; M. van den Brink, ASML Investor Day, 2014

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Agenda

- ⇨ Where Do We Stand & What Lies Ahead
- Lithography & Devices

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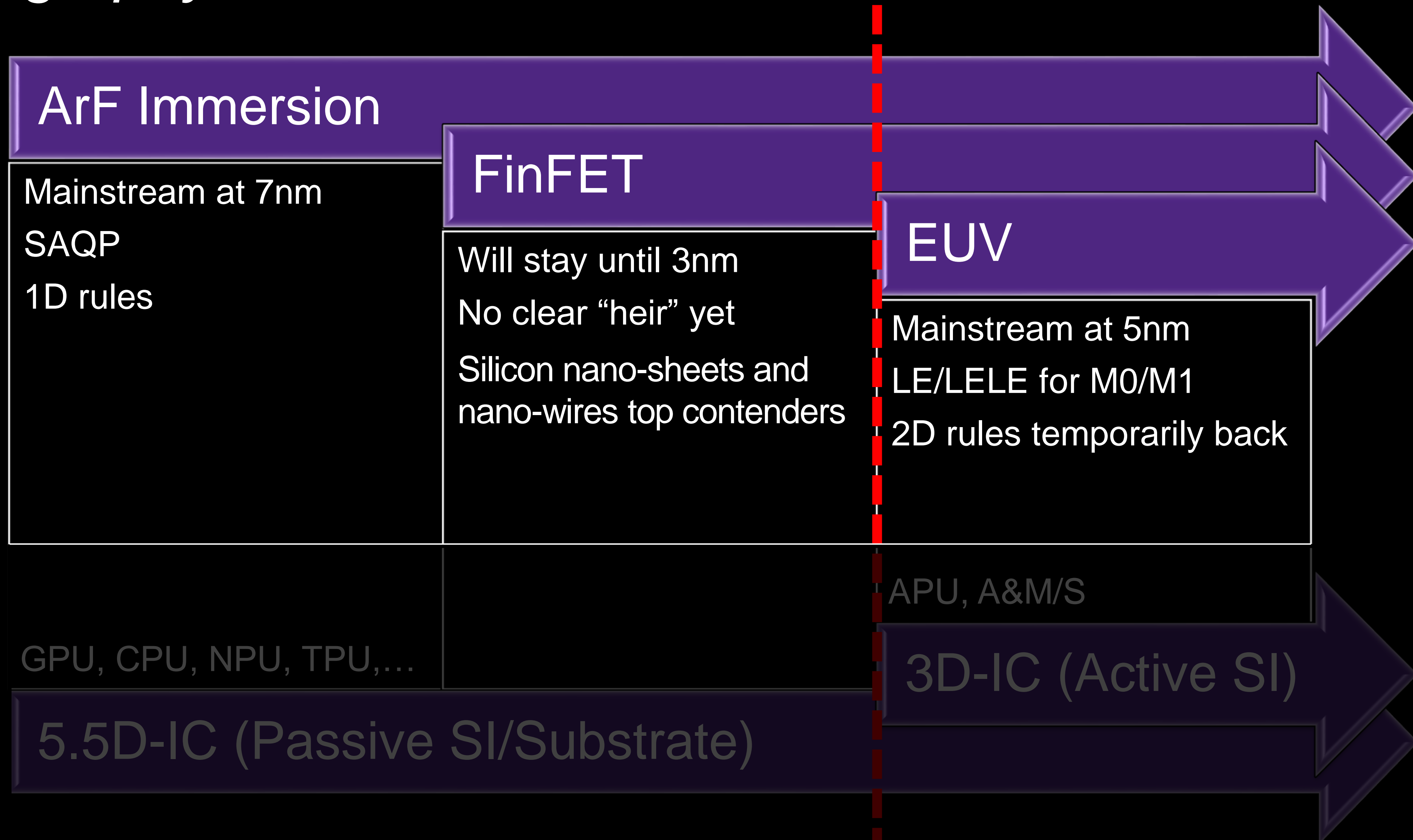
Where Do We Stand ? What Lies Ahead ?

Lithography & Devices



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Lithography Implications – ArFi, EUV, Applications

Different Objectives Lead to Very Different Outcomes !

	Minimum Metal Pitch	Minimum Contacted Pitch	MMP × MCP	MCP / MMP	Most Advanced Lithography
N10 (HP)	36nm	54nm	1,944nm^2	1.5X	**SAQP**
N7	40nm	57nm	2,280nm^2	1.425X	LELELE
N10 LPE	48nm	64nm	3,072nm^2	1.333X	LELELE
N7 LP	40nm	56nm	2,240nm^2	1.4X	LELELE
N7 LPE	36nm	54nm	1,944nm^2	1.5X	**EUV**

Source: Synopsys Research, 2017

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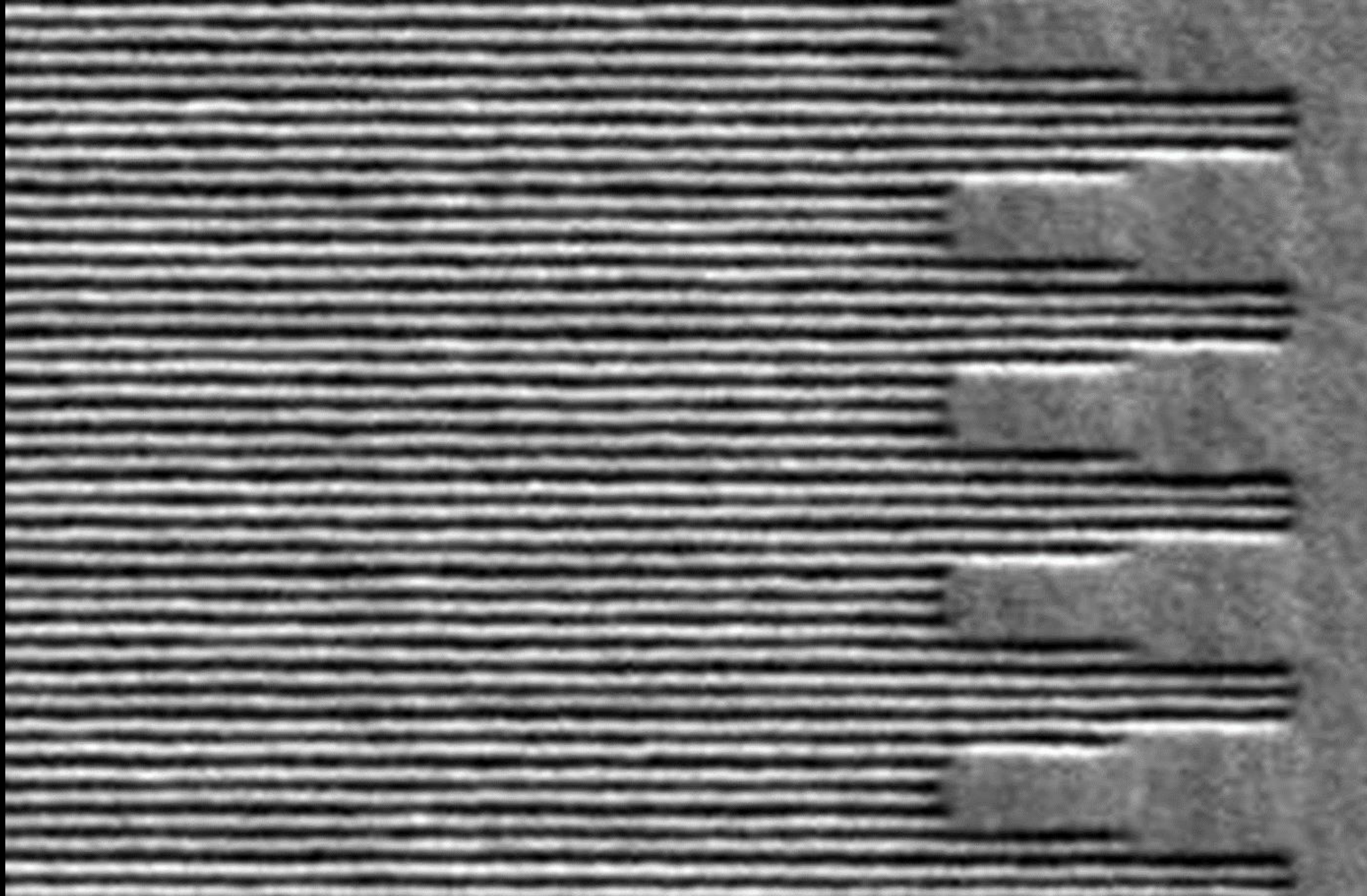
Lithography Implications – ArF Immersion, SAQP

From 2D To 1D Rules, No Jogs, Only One Pitch/Width



24 Nanometer Pitch, ArF Immersion, SAQP; Source: R. Brain et al., Intel, IEDM 2016

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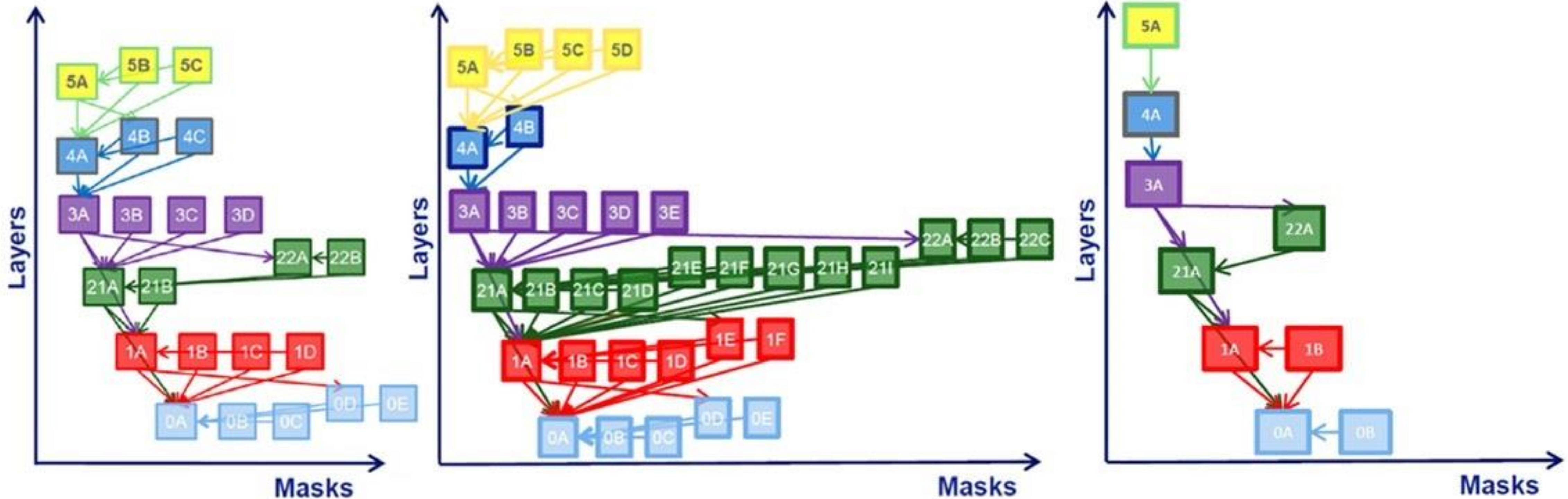
Lithography Implications – ArFi Vs. EUV

# of Critical Lithography & Alignment Overlay Steps



N10	N7 ArFi	N7 EUV
23	34	9
36-40	59-65	12

Source: H. Meiling, ASML Investor Day 2016

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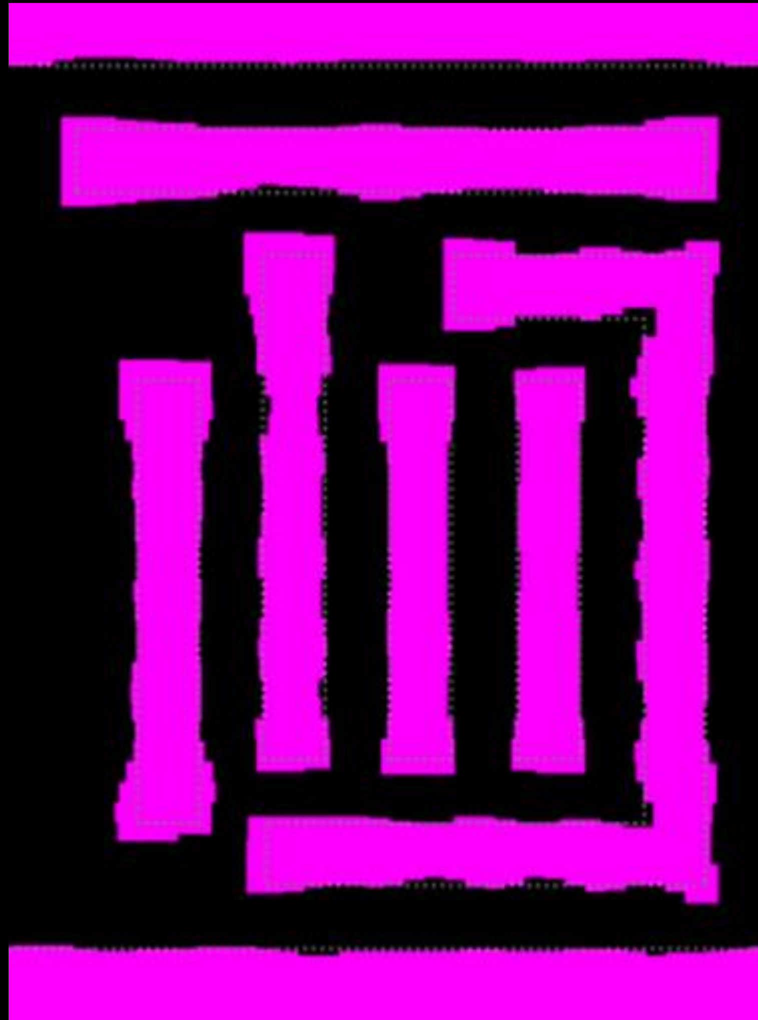
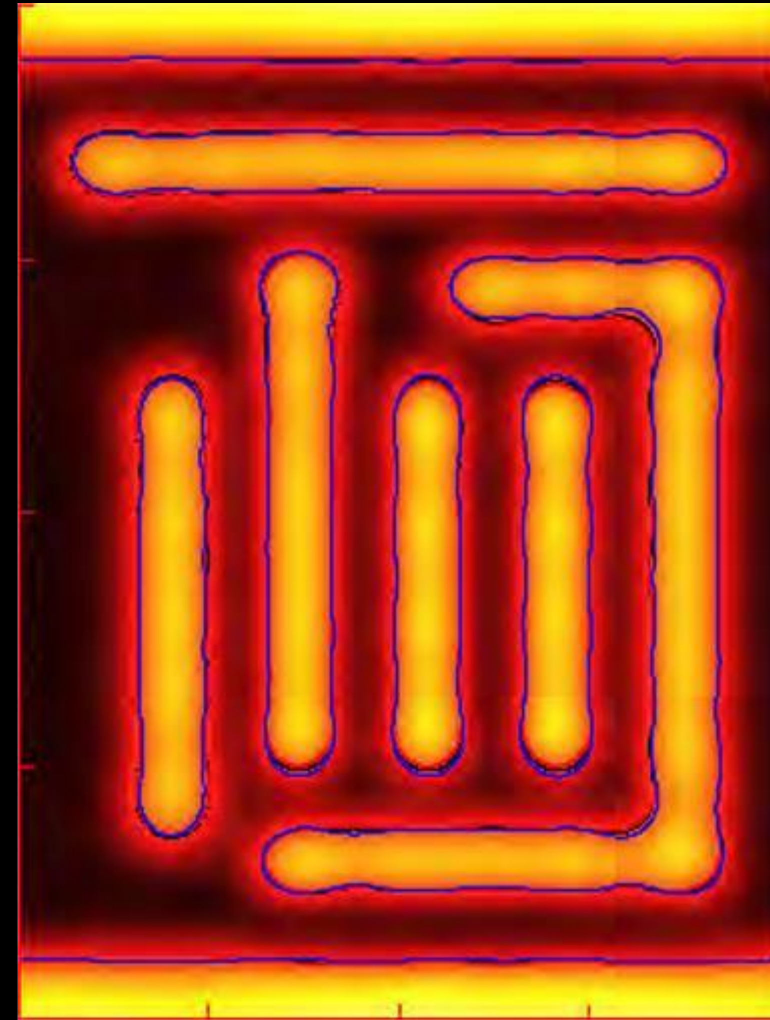
Lithography Implications – EUV

Temporarily Back To 2D Rules At 7 Nanometers ?





11 Nanometer M1 Lines, EUV, SE; Source: J. Miyazaki, ASML, 2015

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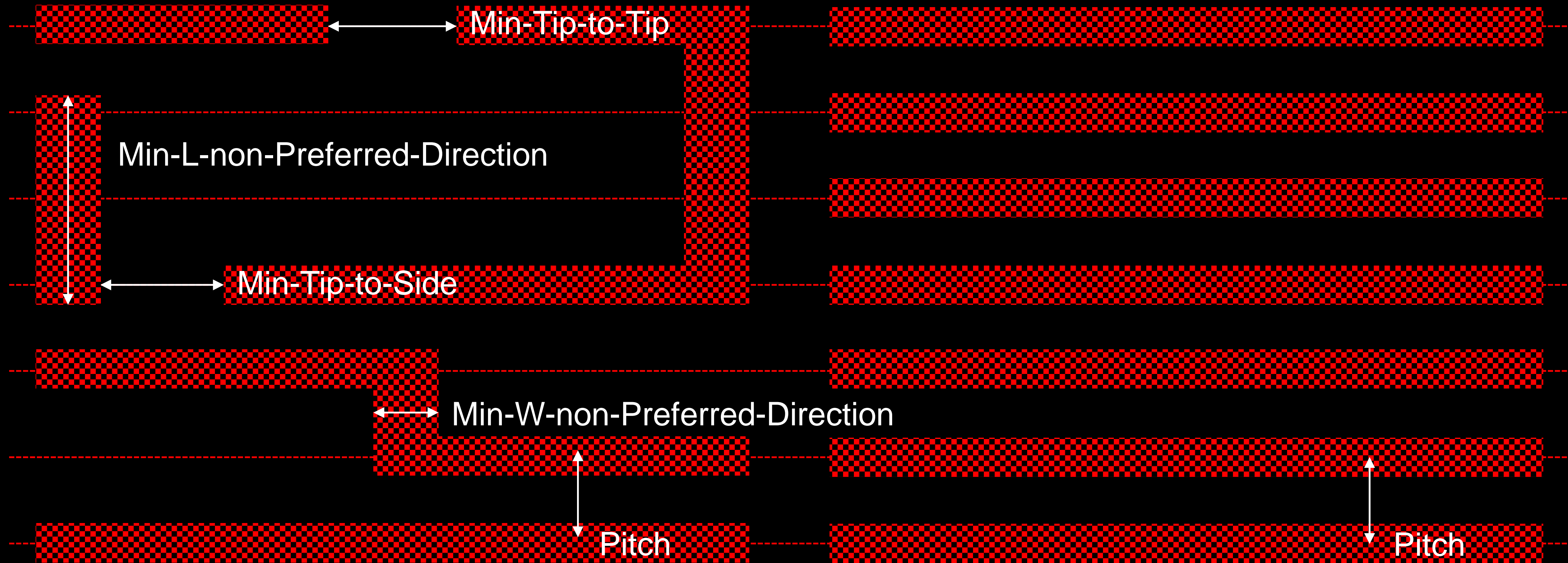
Design Implementation At ≤ 10 Nanometers

From 2D to 1D Routing AND Standard Cells

No More Jogs, Tip-to-Tip, and Tip-to-Side Rules, Only One Pitch/Width



Source: Synopsys Research, 2016

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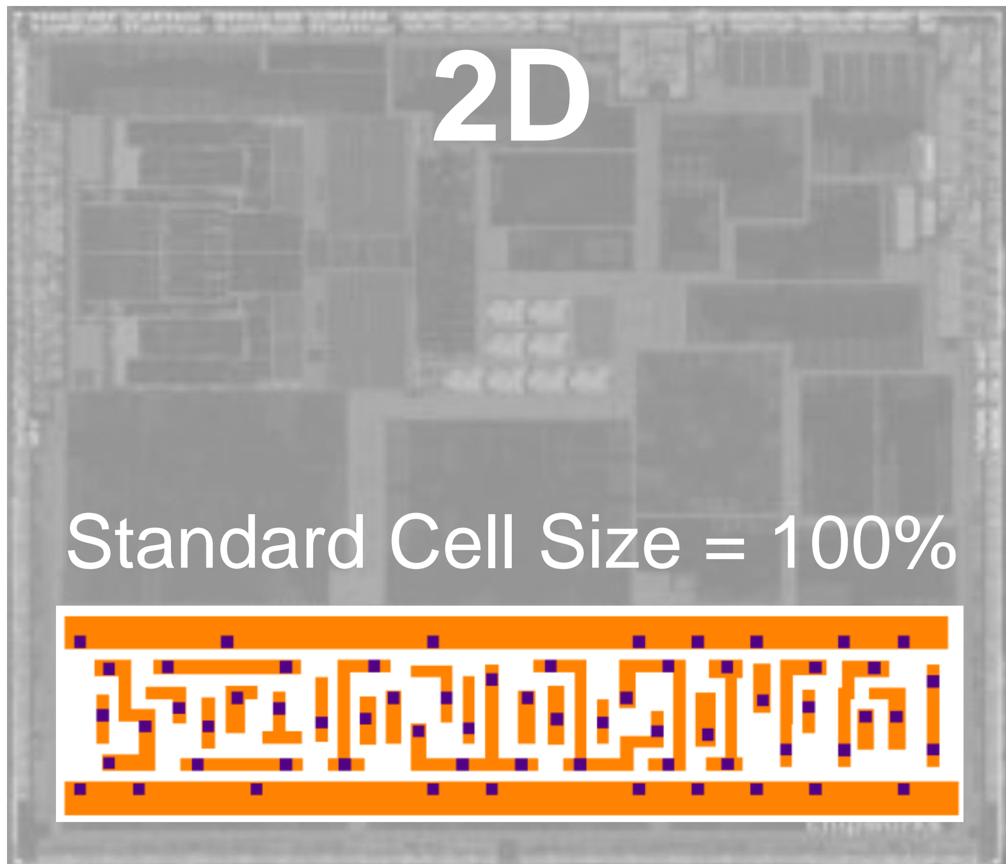
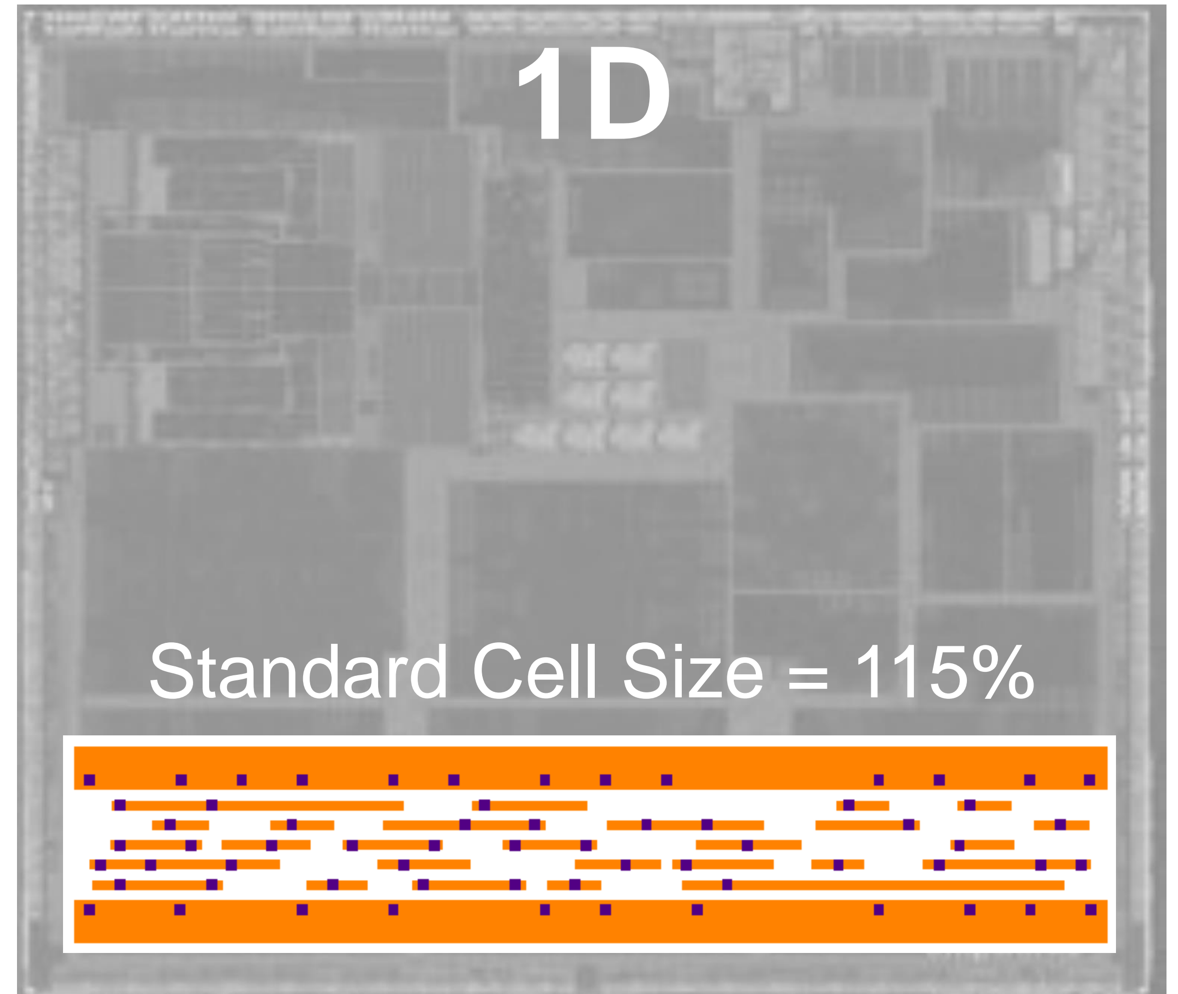
Design Implementation At ≤ 10 Nanometers

From 2D To 1D Routing AND Standard Cells





Source: M. van den Brink, ASML Investor Day 2014

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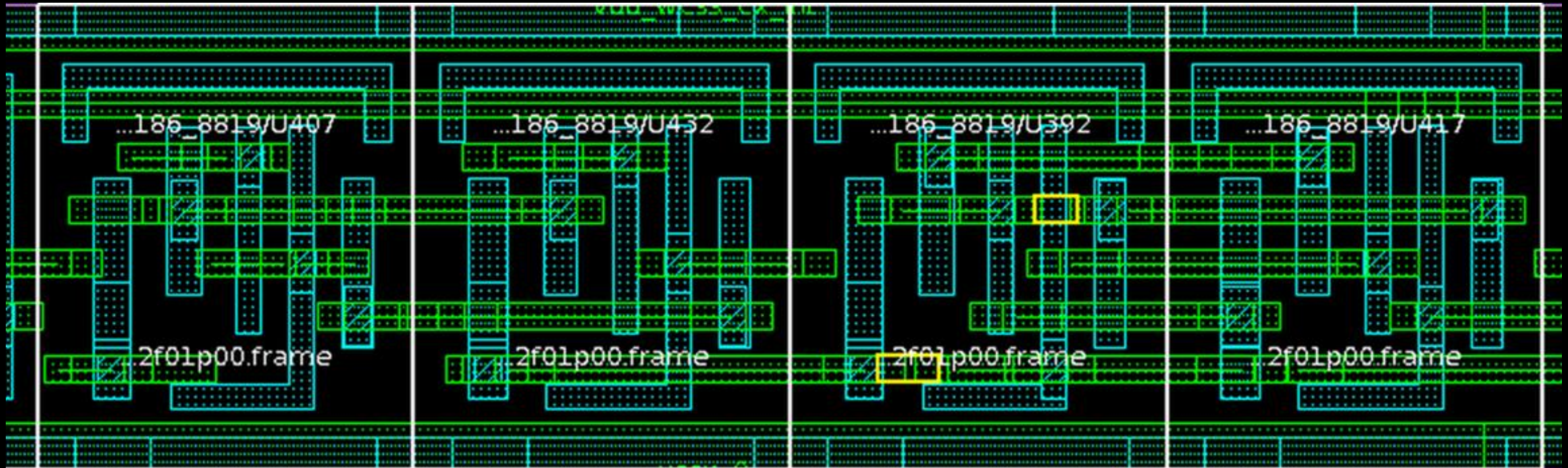
Design Implementation At 7 Nanometers (70 Ångstroms)

End-of-Line Rules Violations at High Pin Count Cell Consecutive Placement Areas
When Pins Are Near Cell Boundary, Wire End Extend Beyond Boundary



Source: Synopsys Research, 2016

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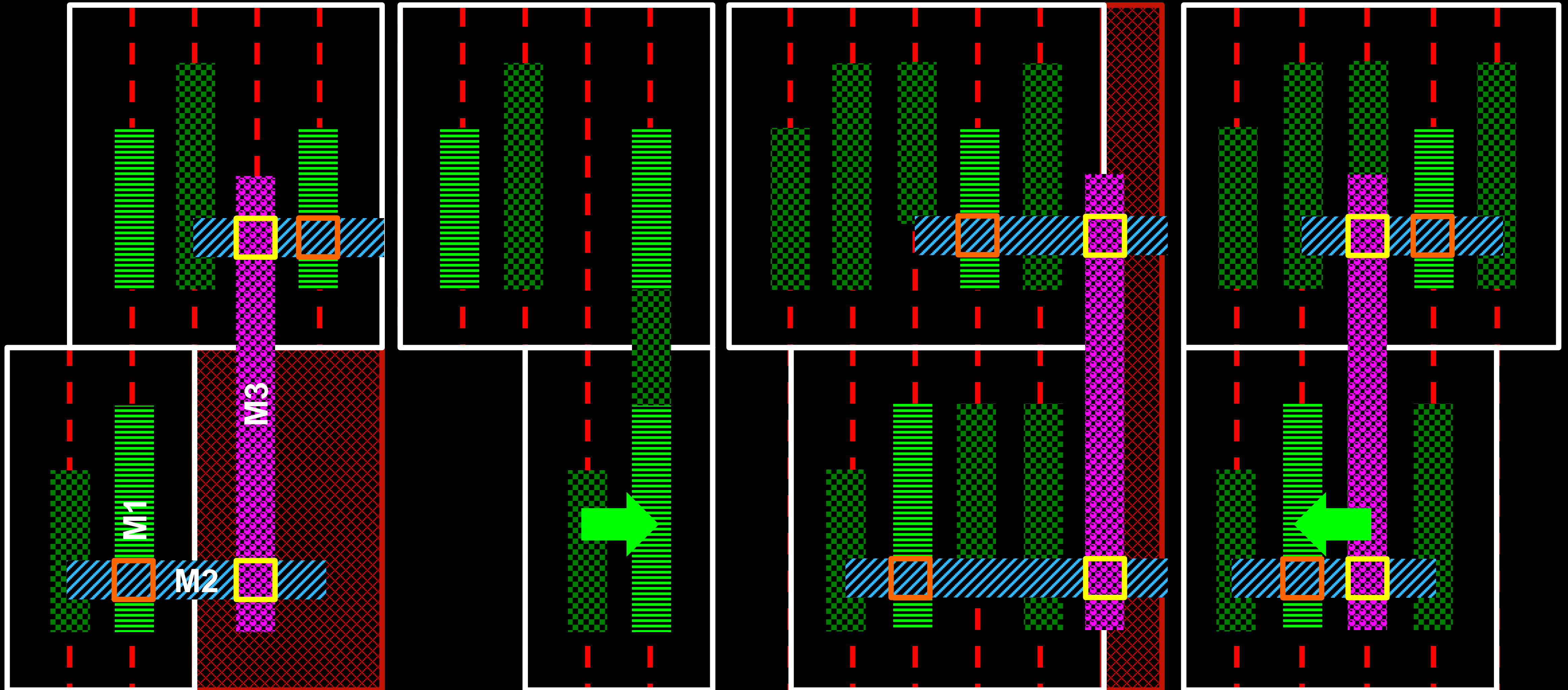
Design Implementation At 7 Nanometers

Placement Must Align Near-by Connected Pins Vertically to Allow Direct Connection on M1, and Avoid Connected Pins in Neighboring Rows Being One Track Off



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Source: Synopsys Research, 2017

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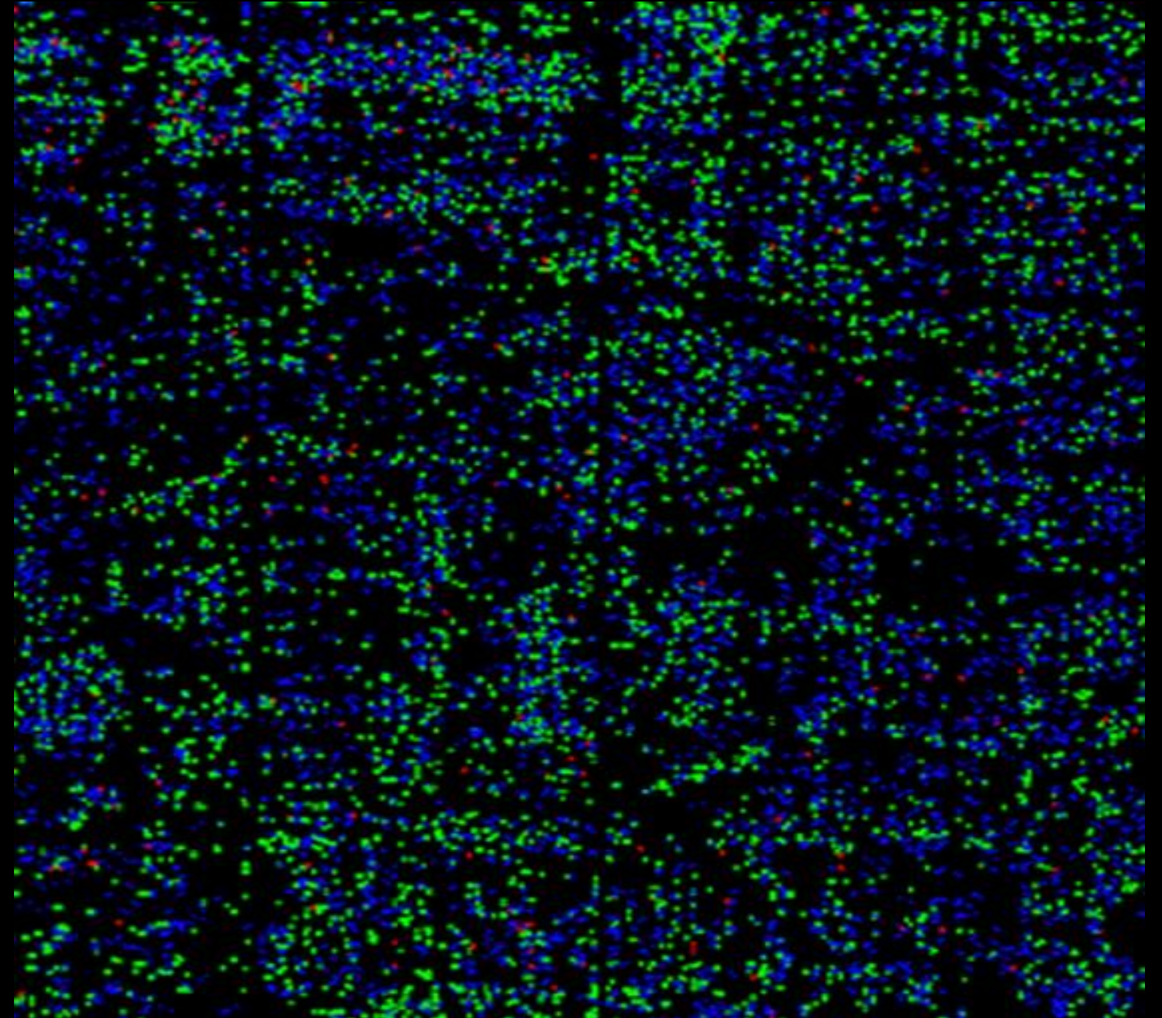
Design Implementation At 7 Nanometers

Vertical Pin Alignment-Aware Placement Reduces Routing Congestion



Source: Synopsys Research, 2017

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Design Implementation At 7 Nanometers

Placement Becomes Increasingly Restricted
More and More White Space Is Required to Achieve Legality

Source: Synopsys Research, 2017

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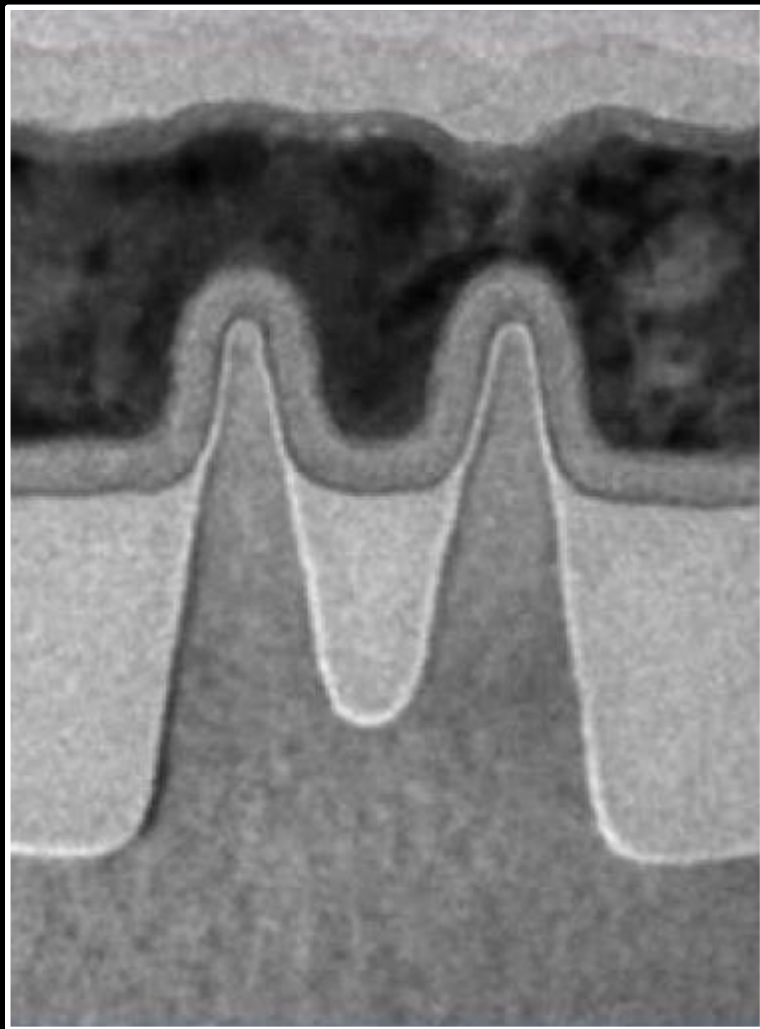
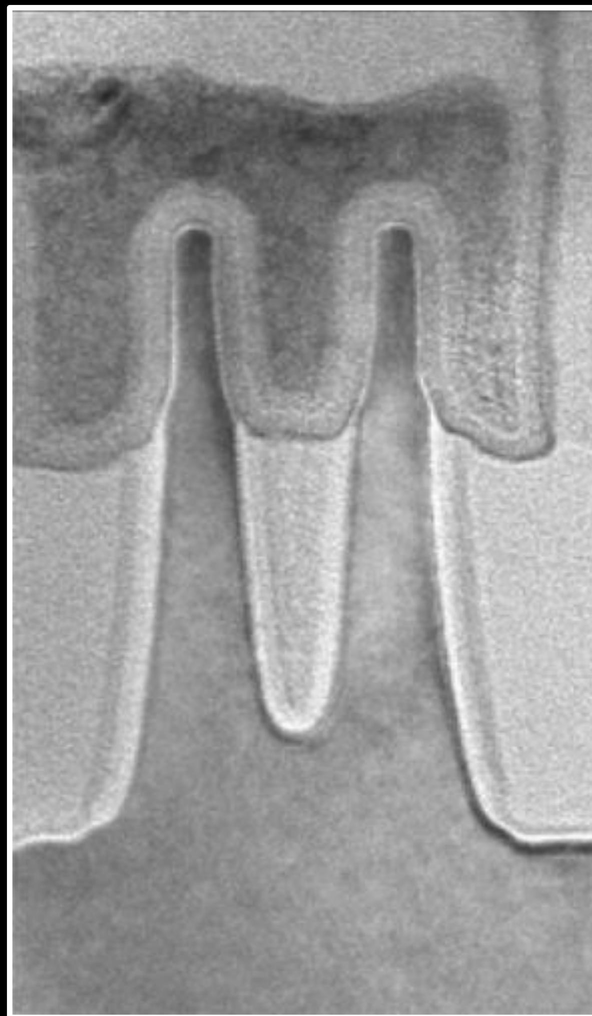
Device Implications – FinFET Prolonged Life Span

Taller/Closer Fins (Height/Pitch) : 34/60 ⇨ 42/42 ⇨ 53/34

22, 14 & 10 Nanometer FinFET; Source: K. Mistry, Intel Technology & Manufacturing Day, 2017

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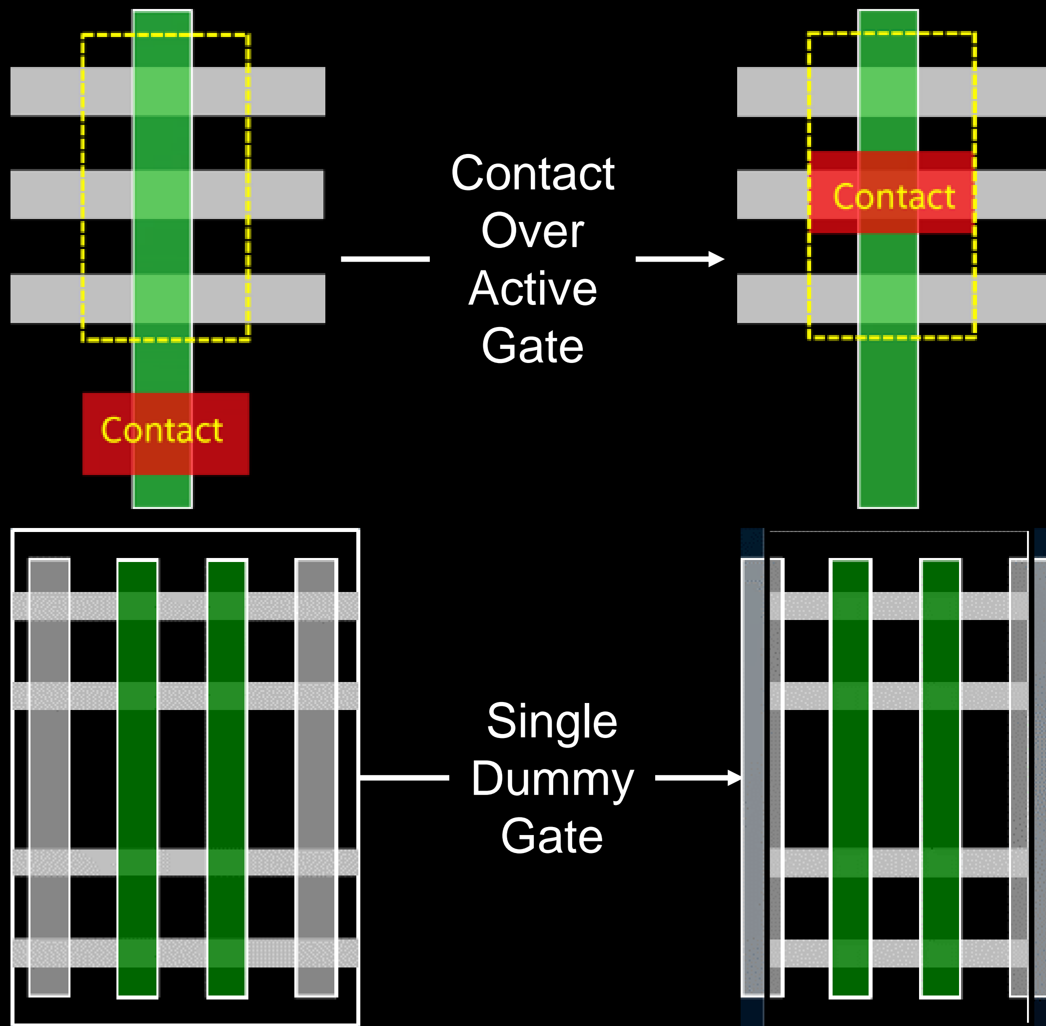
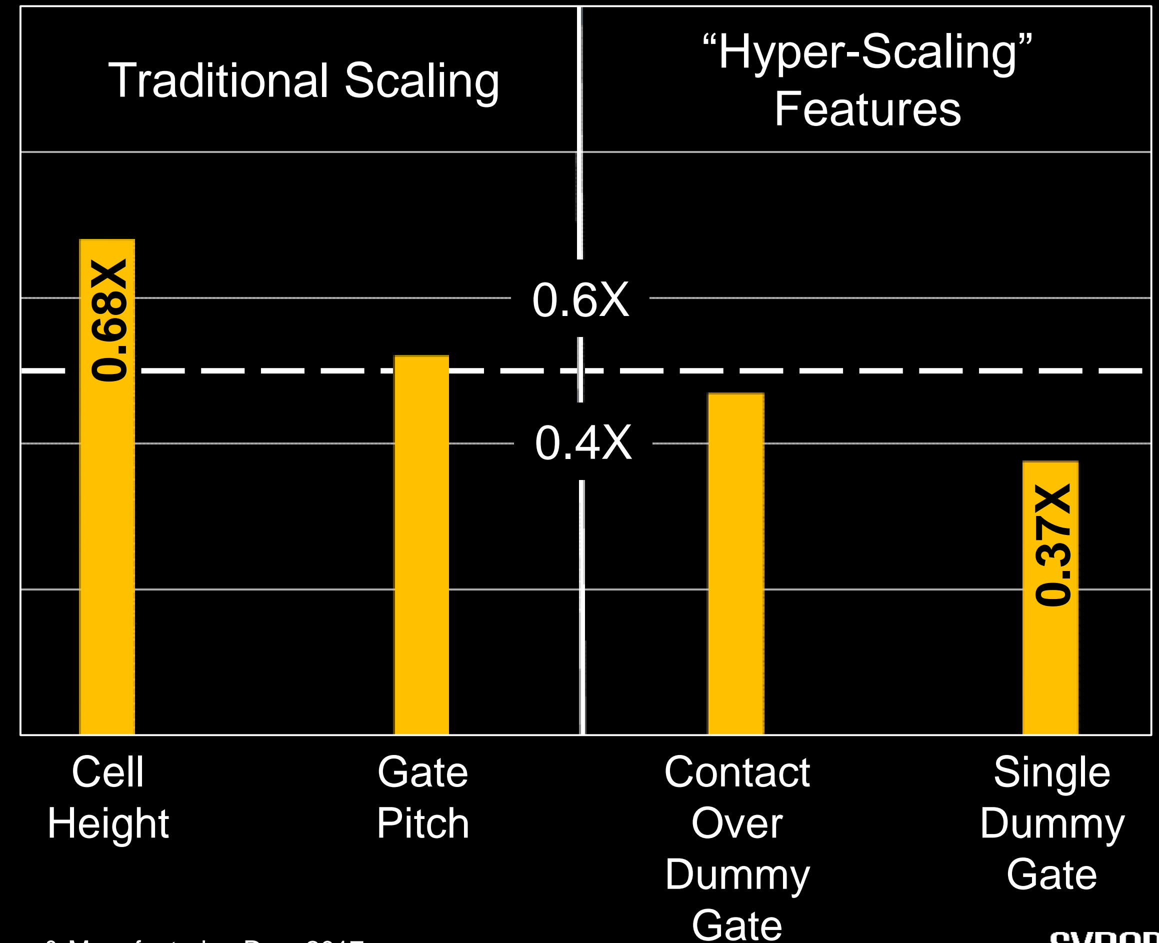
Design Implementation At ≤ 10 Nanometers

Moore's Law Is Fueled by Single Bullet Weapons





Source: M. Bohr, Intel Technology & Manufacturing Day, 2017

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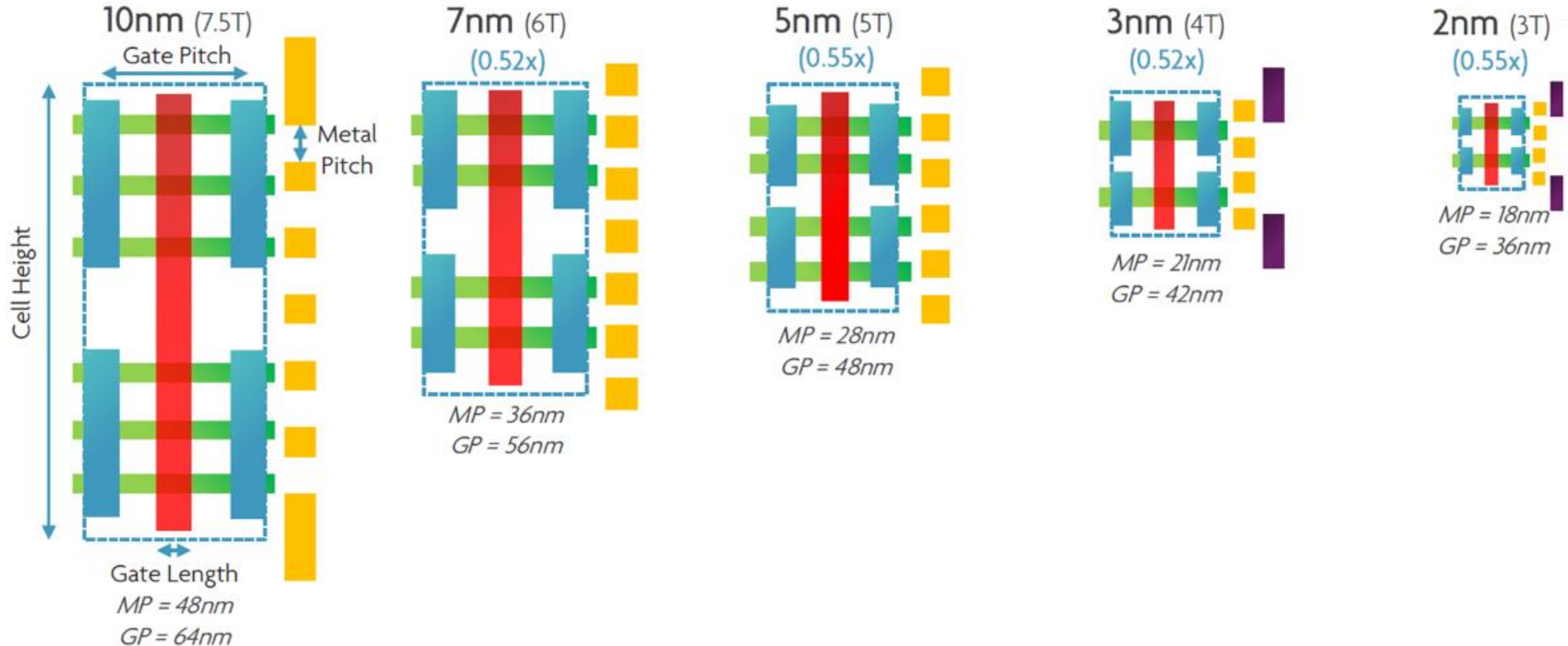
Design Implementation At ≤ 10 Nanometers

Caveat: Standard Cells Shrink, # of Pins Remain the Same



Source: IMEC Technology Forum, 2017

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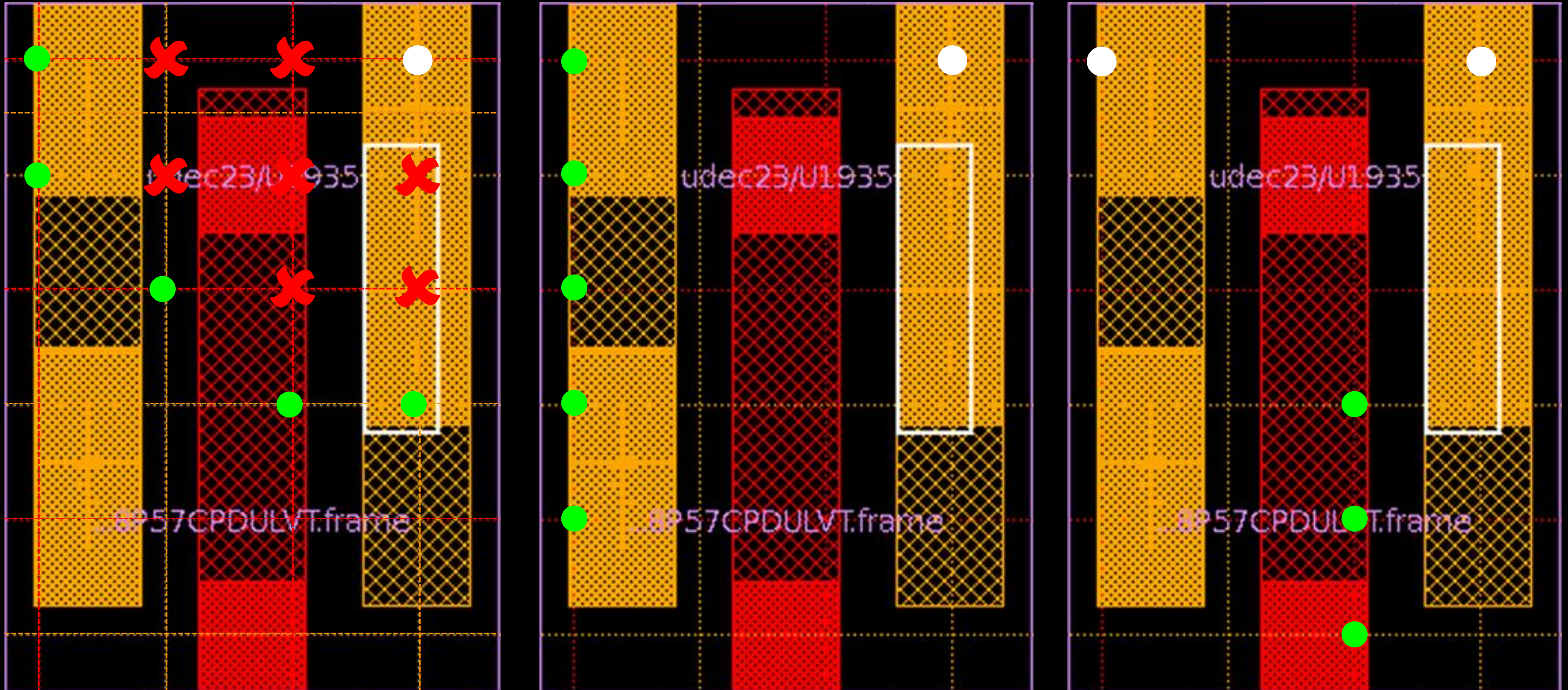
Design Implementation At 7 Nanometers

A Nanometer… Tic-Tac-Toe: a 4x6 Grid, P&R Must Route 3 Pins, But… There Are Only 4 Simultaneous Legal Access Points (Via Spacing Rule $\geq 2\sqrt{2}$ Grids)



Source: Synopsys Research, 2016

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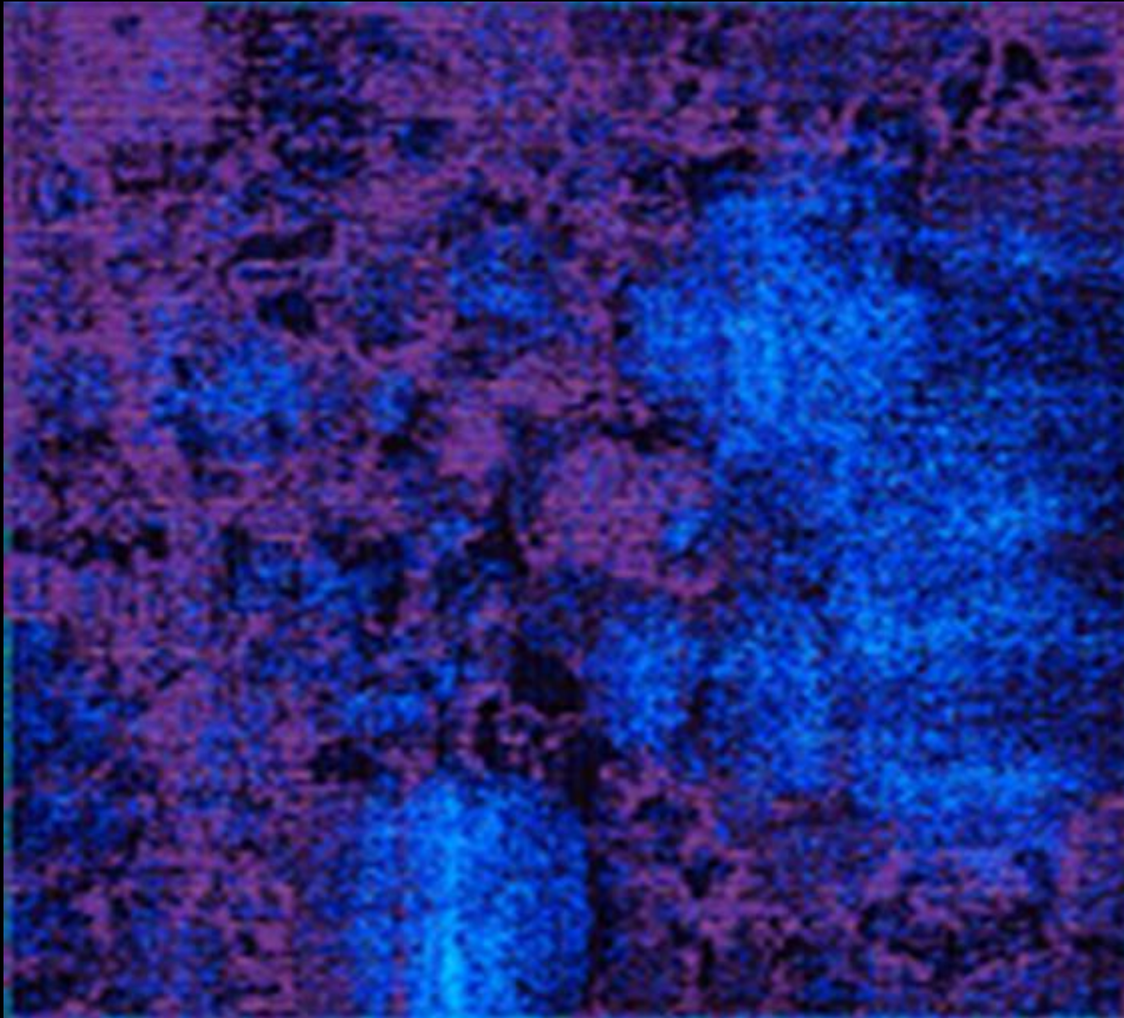
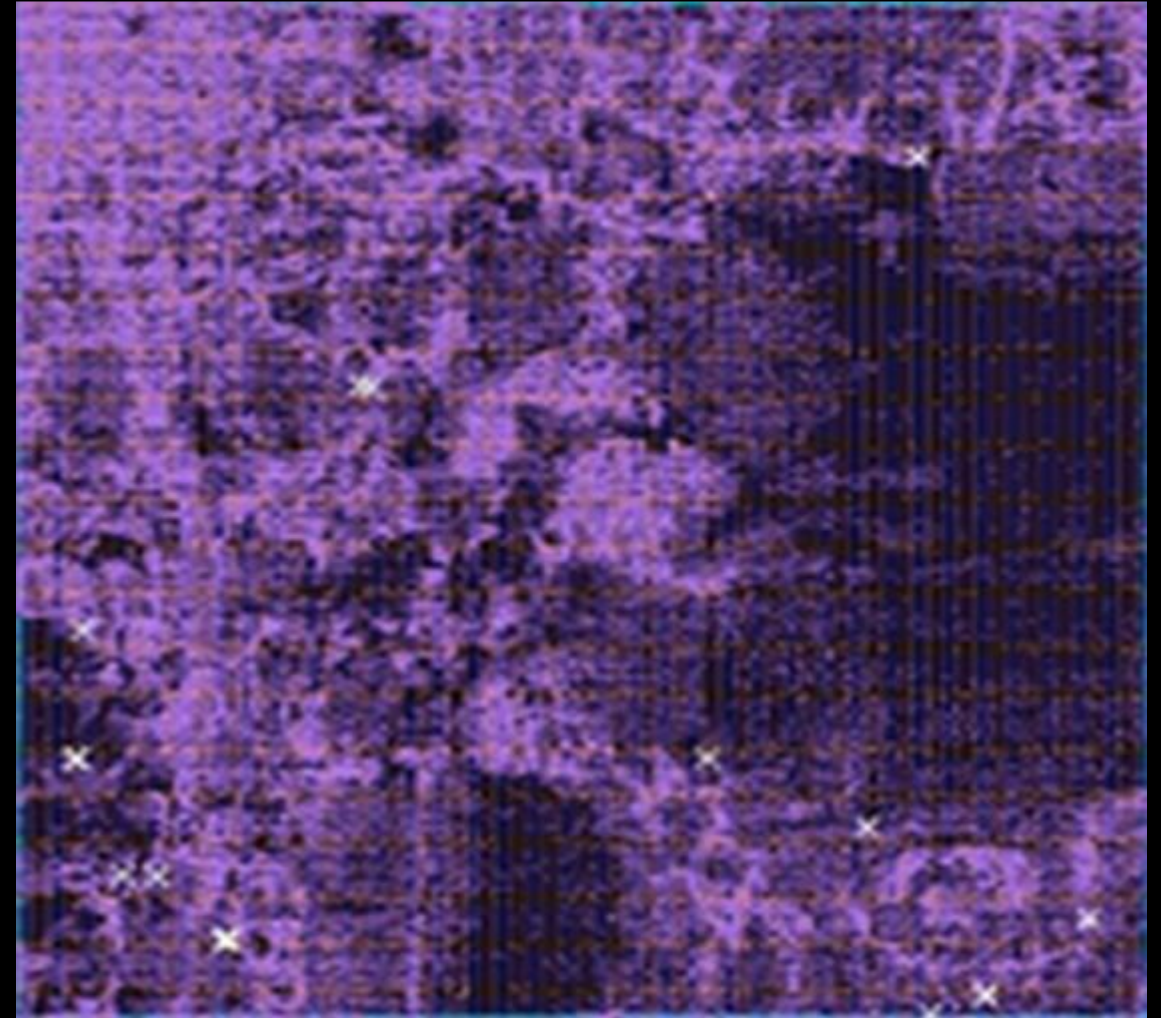
Design Implementation At 7 Nanometers

Pins Density & Accessibility-Aware Placement Addresses/Mitigates Pins Density/Accessibility, and Routing Congestion Issues





Source: Synopsys Research, 2016

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Shrink Scenarios For Logic Devices

No End in Sight

Bulk CMOS

Partially Depleted SOI

Fully Depleted SOI

Bulk FinFET

SOI FinFET, III-V

GAA

Source: M. van den Brink, ASML Investor Day 2014

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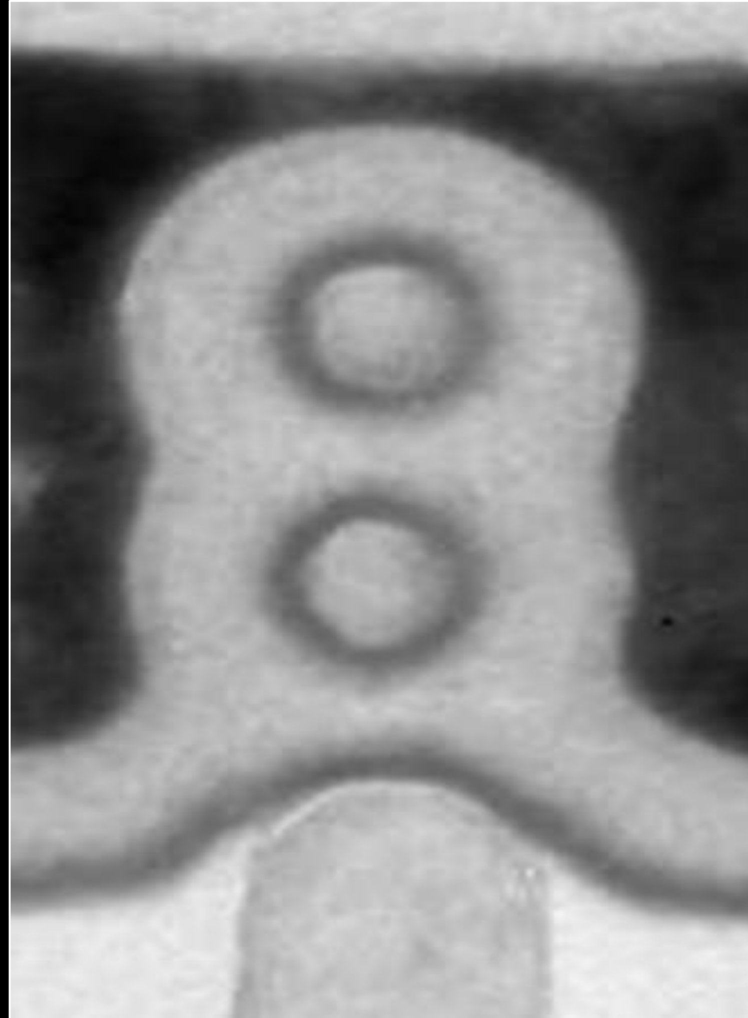
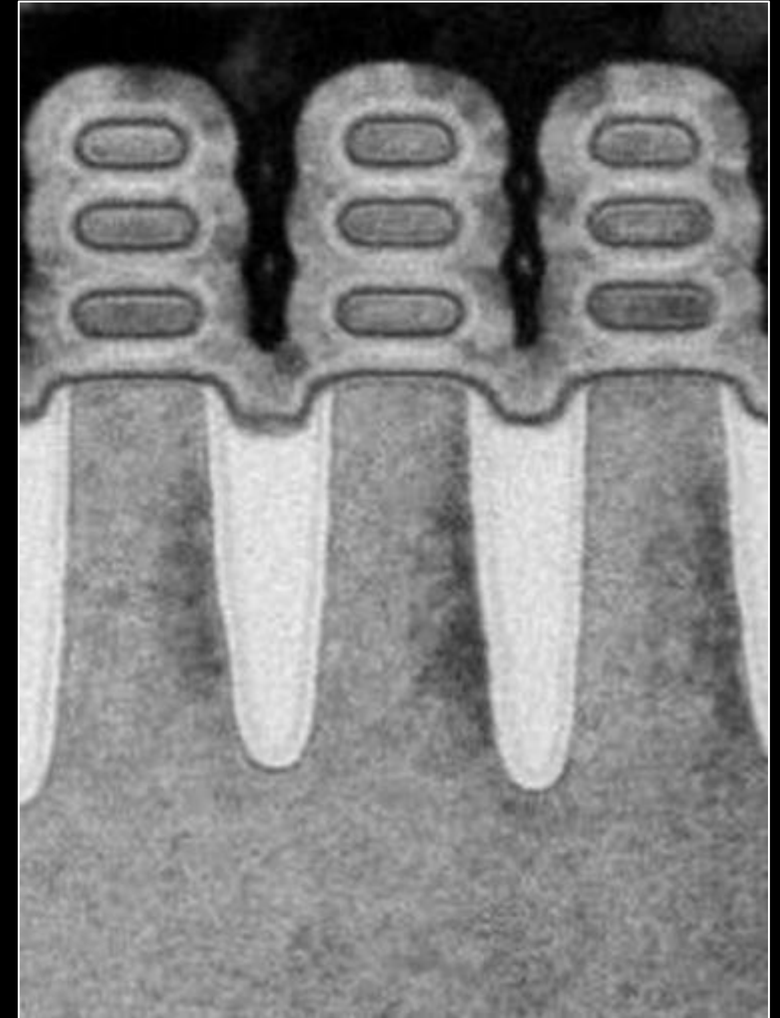
Device Implications – Beyond FinFET (At 3 Nanometers)

[Stacked] Nano-Wires, and Nano-Sheets





Source: K. Mistry, Intel Technology & Manufacturing Day, 2017; IMEC Technology Forum, 2017; IBM, 2017

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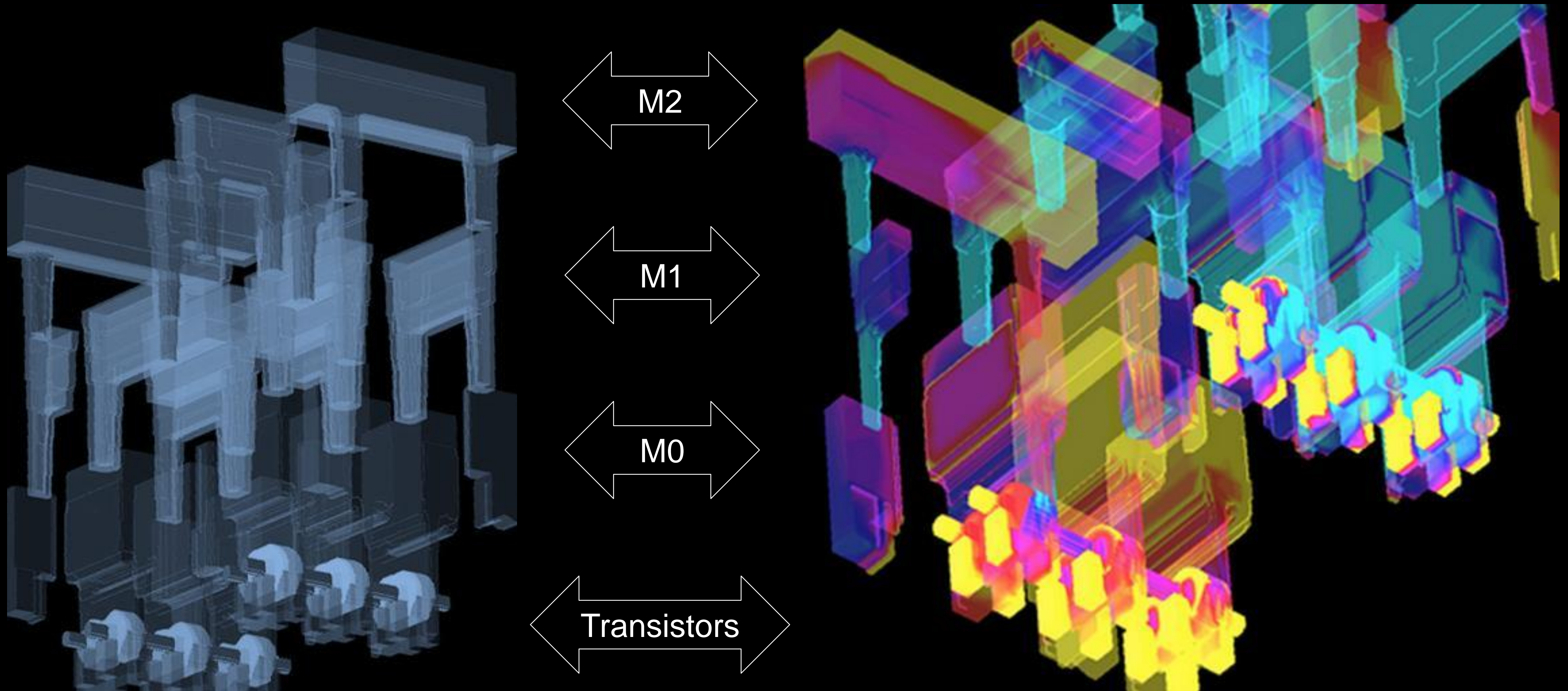
Process Exploration At 5 Nanometers (50 Ångstroms)

2-Input NAND 3D Structure, and Current Flows



Source: V. Moroz, Synopsys, ISPD 2016

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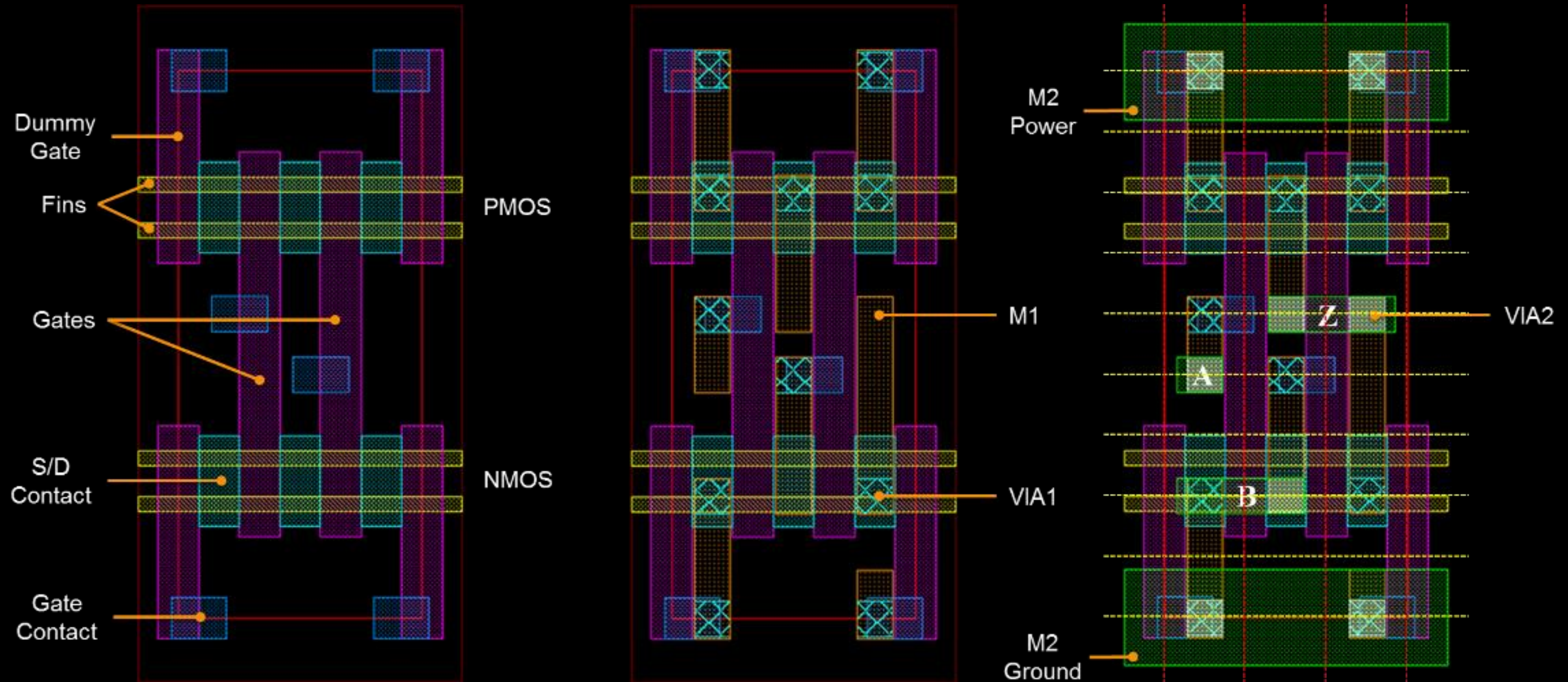
IP Exploration At 5 Nanometers

9-Track 2-Input NAND Layout

Gate Pitch = 32nm, M1 Pitch = 24nm, Fins Pitch = 18nm



Source: V. Moroz, Synopsys, ISPD 2016

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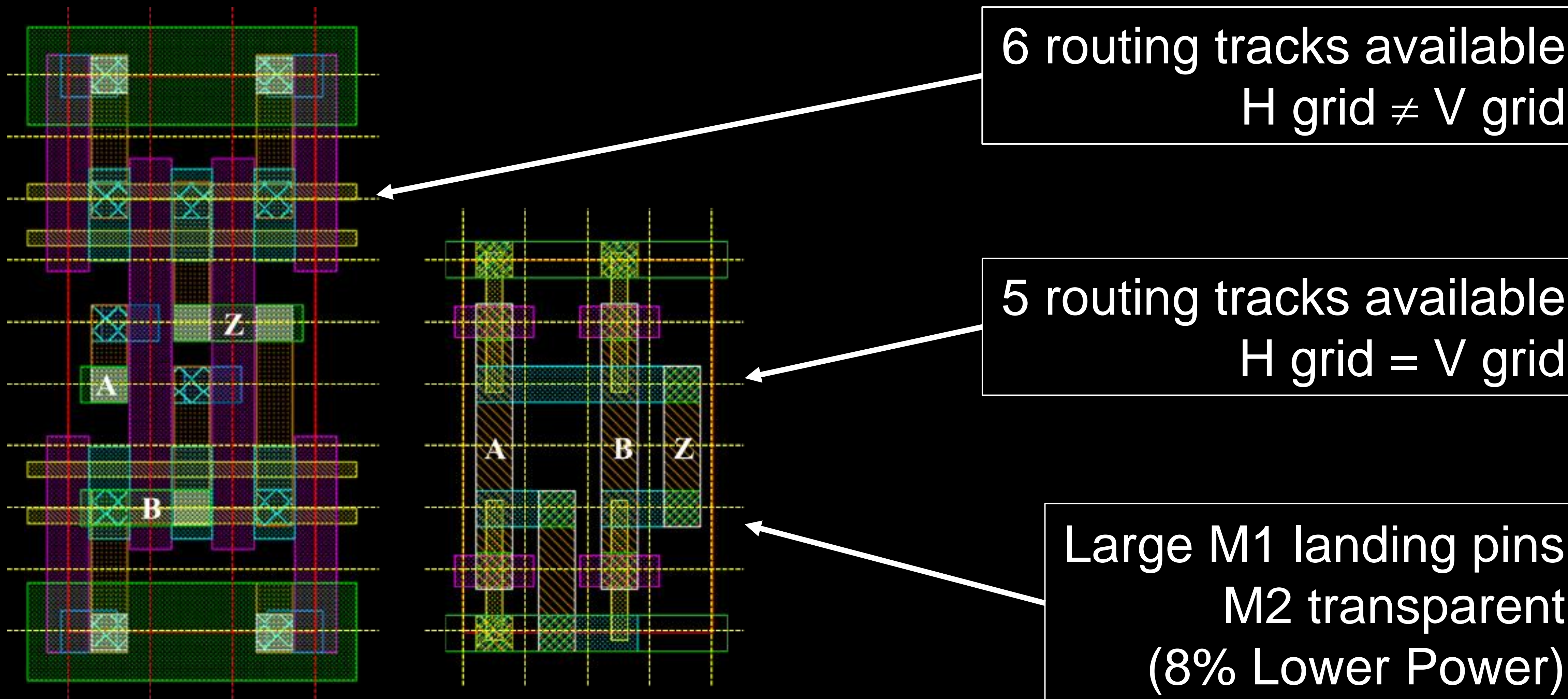
IP Exploration At 5 Nanometers

What If We Rotate The Fins ? 9-Track vs. 6-Track 2-Input NAND Layout
Gate Pitch = 48nm, M1 Pitch = 24nm, Fins Pitch = 48nm



Source: V. Moroz, Synopsys, ISPD 2016

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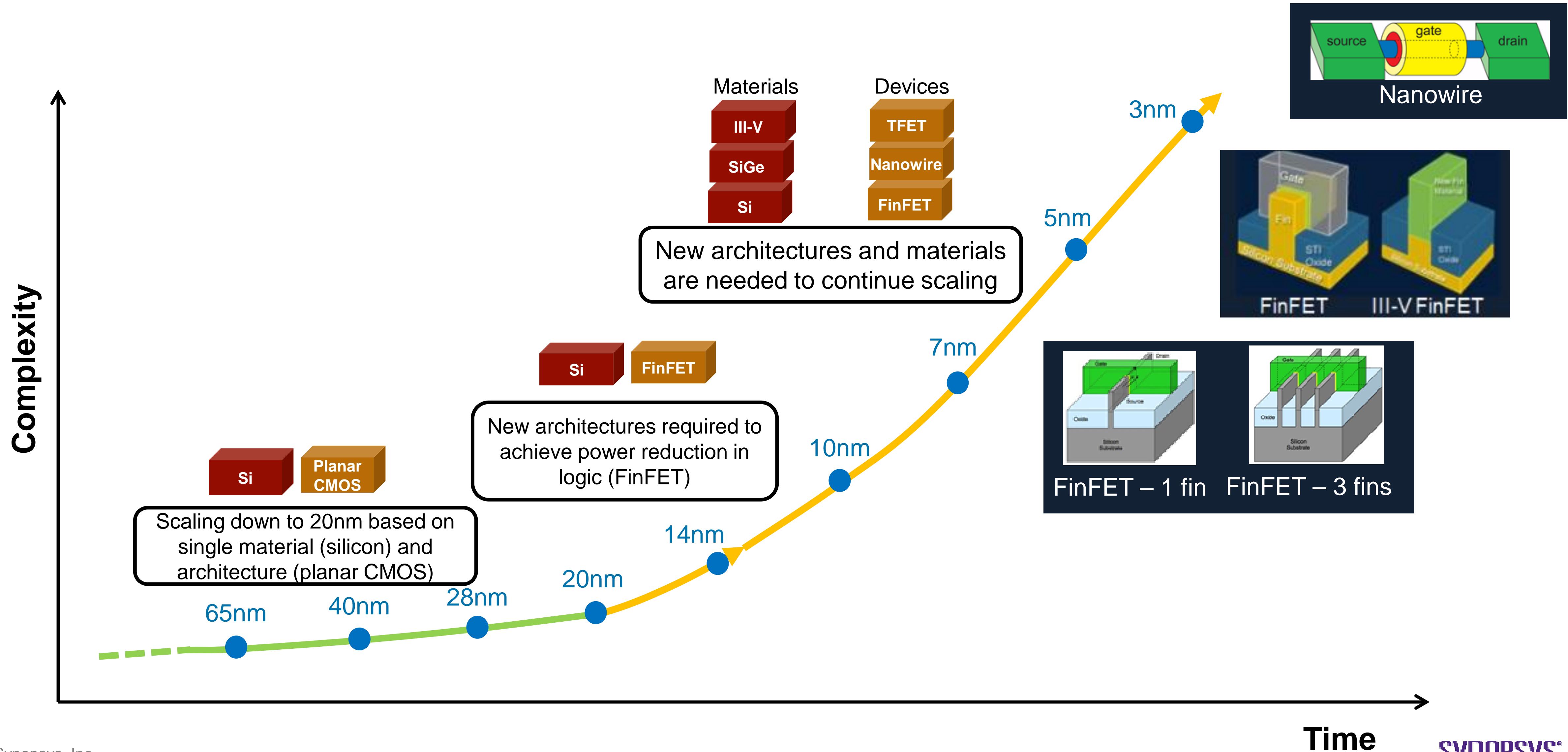
The Number Of Material And Device Options Increases

Selection Of Optimal Solution Threatens Schedule



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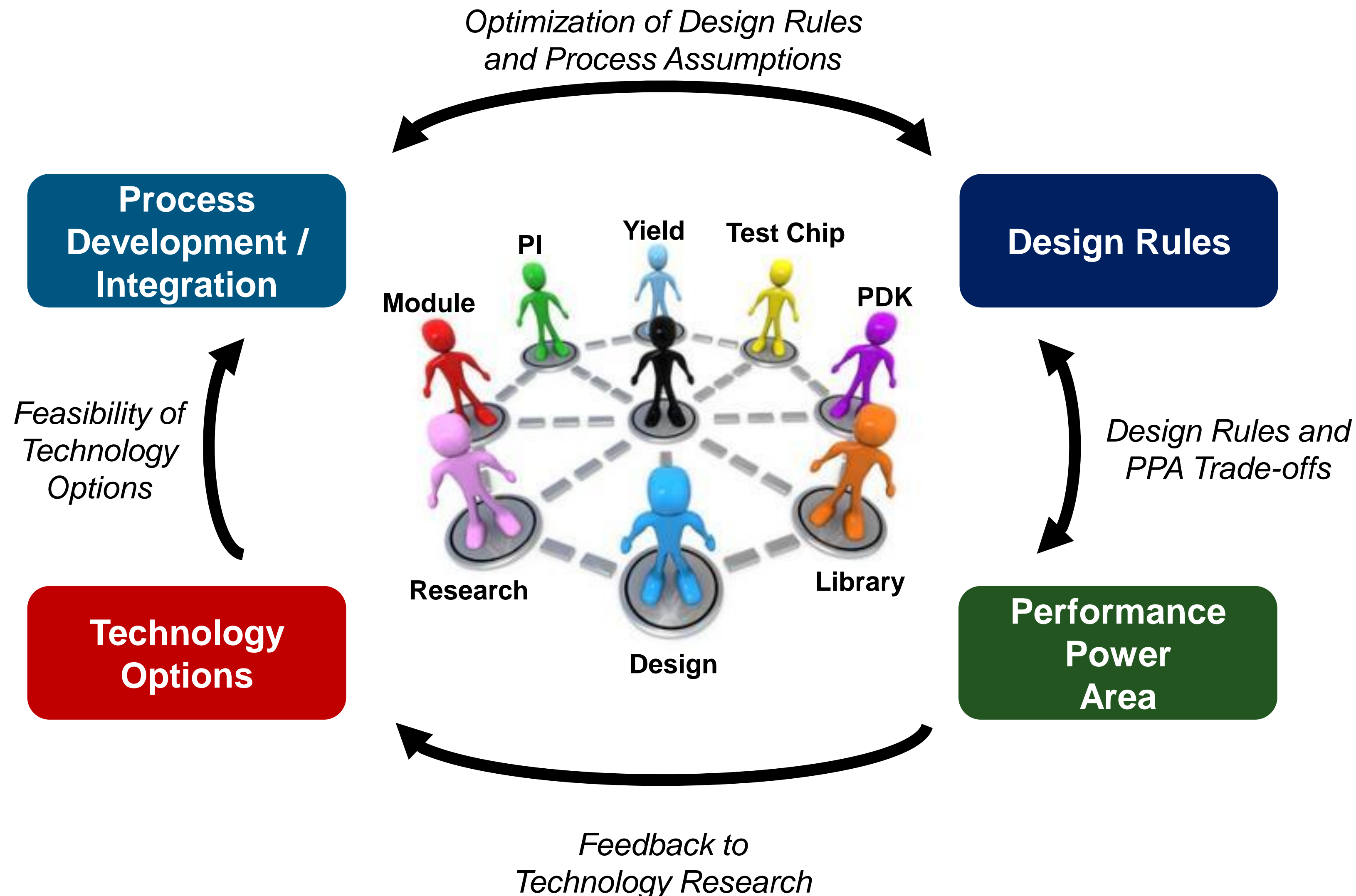
DTCO Enables Landscape Exploration

Introduces Use of Larger Circuits for Technology Assessment



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Agenda

- ⇨ Where Do We Stand & What Lies Ahead
- Lithography & Devices
- ⇨ DTCO: Design And [Process] Technology Co-Optimization

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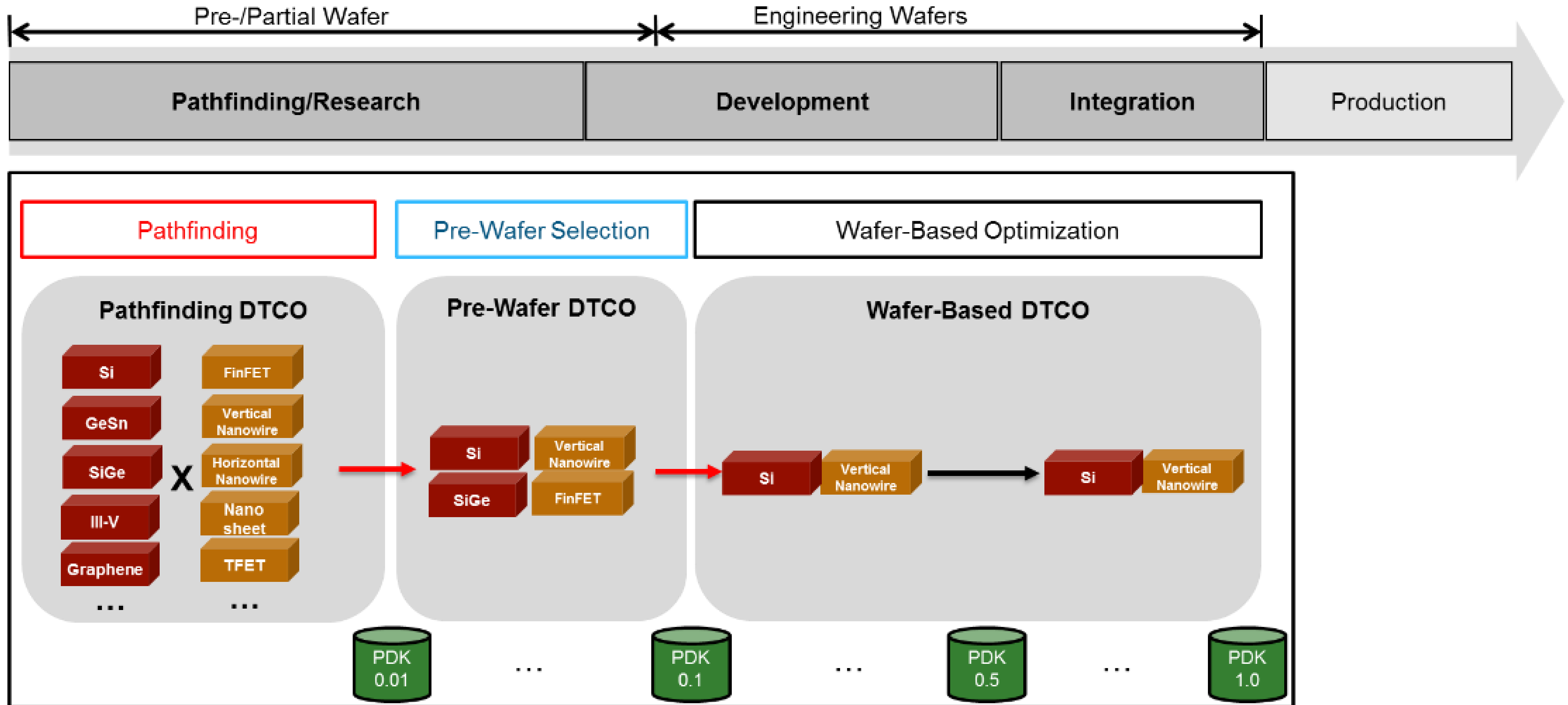
Evaluate Multiple Options

Deliver a Competitive Technology as Quickly as Possible



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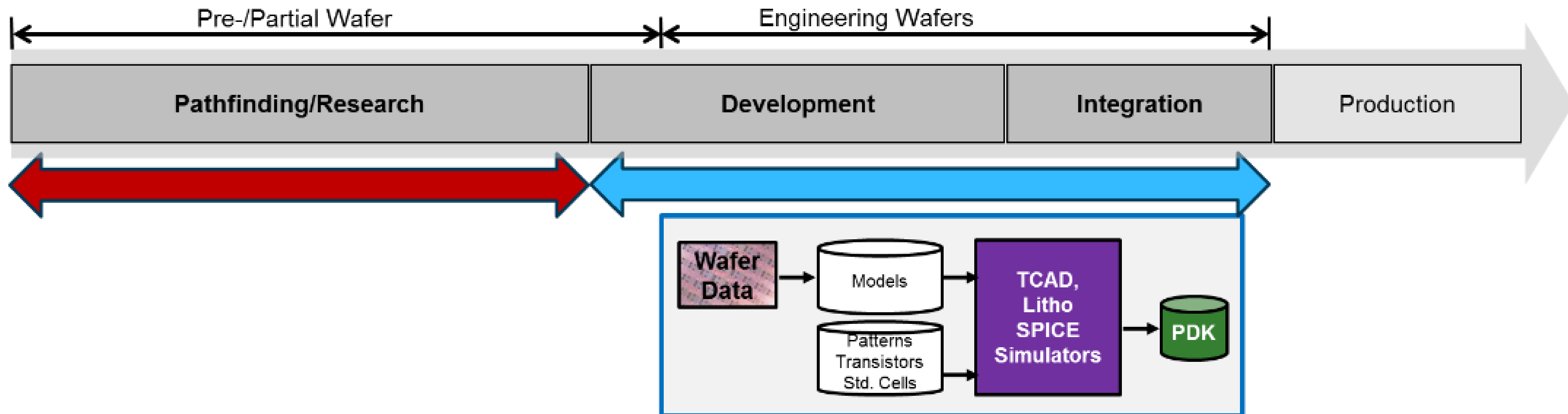
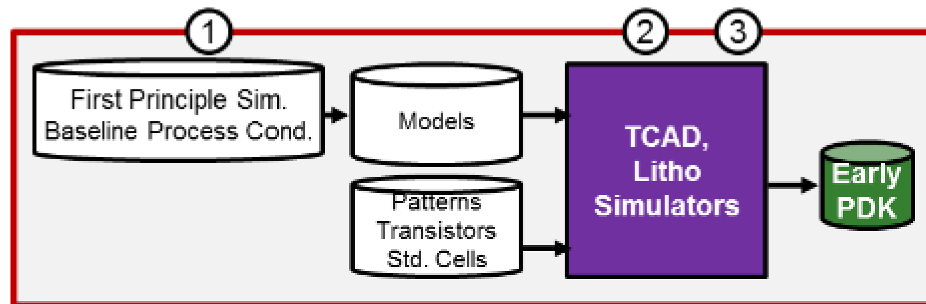
Reduce Process Technology Development Time

By Enabling Selection through Early Process, Design Rules & IP Co-Development





<u>Research phase selection and evaluation enabled by</u>:

1. First Principle Simulators and Baseline Process Conditions to create models for TCAD and litho simulation
2. Automated TCAD-to-SPICE model creation for PPA evaluation of full circuits
3. TCAD, lithography, SPICE simulation to achieve early maturity in litho/OPC and design rules, and analyze/optimize performance, power, area, yield of transistors, patterns, and circuits

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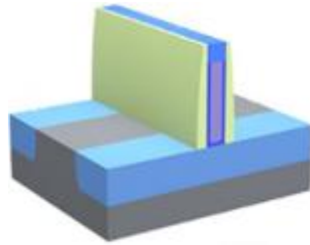
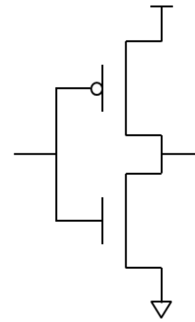
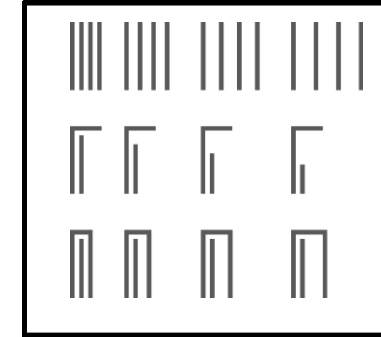
Traditionally, Small Structures Are Used To Develop And Evaluate Devices/Process

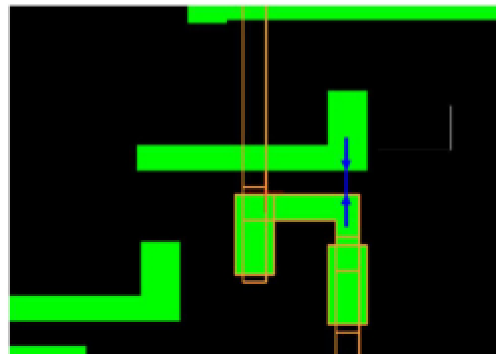
- Single transistors
- Simple logic (inverter)
- Metal patterns for lithography
- Etc.

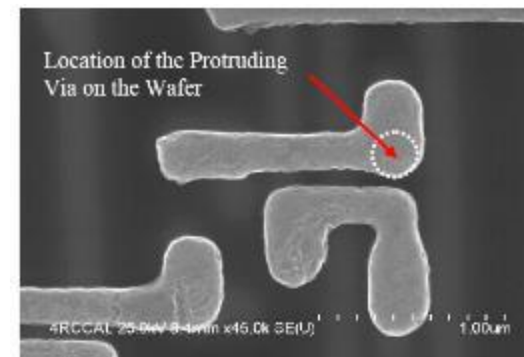






- Problem: Complicated, actual designs often reveal fundamental problems after the process is delivered to production
  – For example: A particular layout pattern causes systematic yield loss





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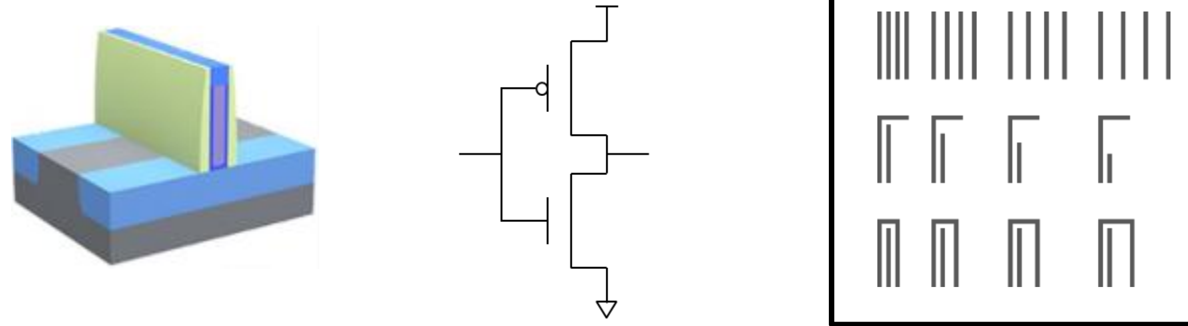
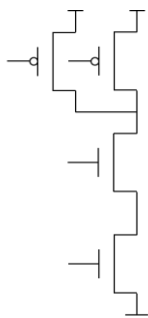
DTCO: Early Use Of Larger Circuits For The Evaluation Of Technology Options Minimizes Late Surprises

- Single transistors
- Simple logic (inverter)
- Metal patterns for lithography
- Etc.

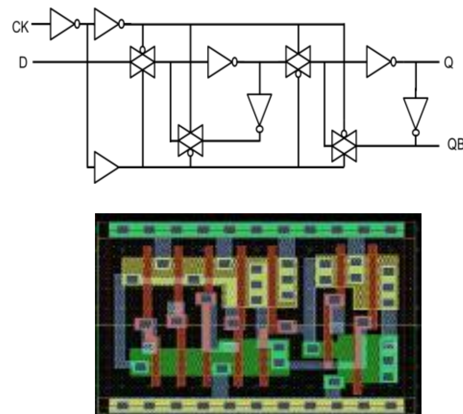


- **DTCO**: Use larger, more realistic test cases earlier in development to better evaluate how well the device/process options meet the requirements of real designs

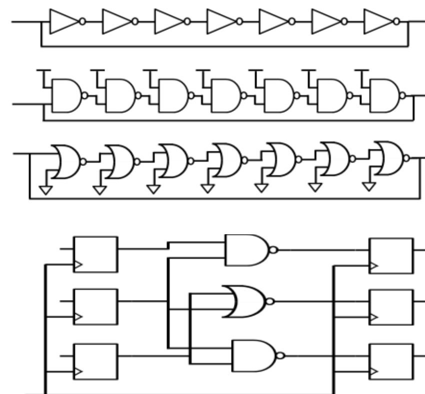
Simple Std. Cells



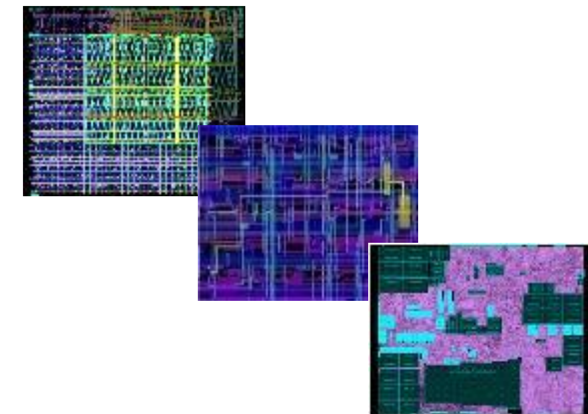
Complex Std. Cells



Test Circuits



Customer Blocks



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Fast Process Simulation, Automatic Generation of SPICE Models & Early PDK Enables Use Of Larger Test Cases

Test Cases	Cells		
	Pathfinding	**Pre-Wafer**	**Wafer-Based**
Size	~10T	~40T to ~200T	~40T to 100K Gates
Number	~5	~100	~1000
Examples	Transistor, Inverter, NAND, SRAM	+ MUX, Flip-Flop,… Ring Osc USB Logic	+ Full Std. Cell Lib. Customer Blocks

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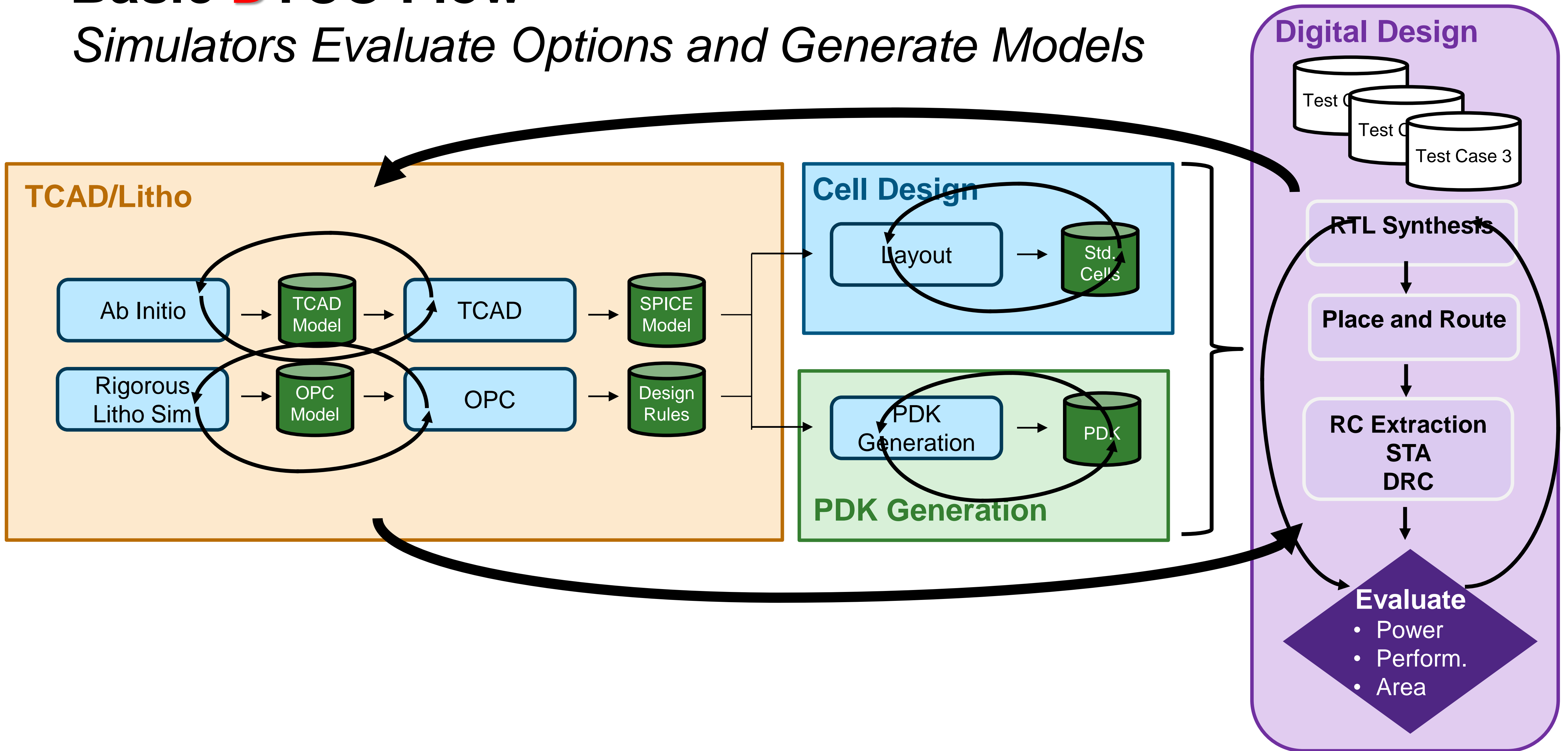
Basic DTCO Flow

Simulators Evaluate Options and Generate Models



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Agenda

- ⇨ Where Do We Stand & What Lies Ahead
- Lithography & Devices
- ⇨ DTCO: Design And [Process] Technology Co-Optimization
- ⇨ Back To… The Future !
- [Heterogeneous] Integration

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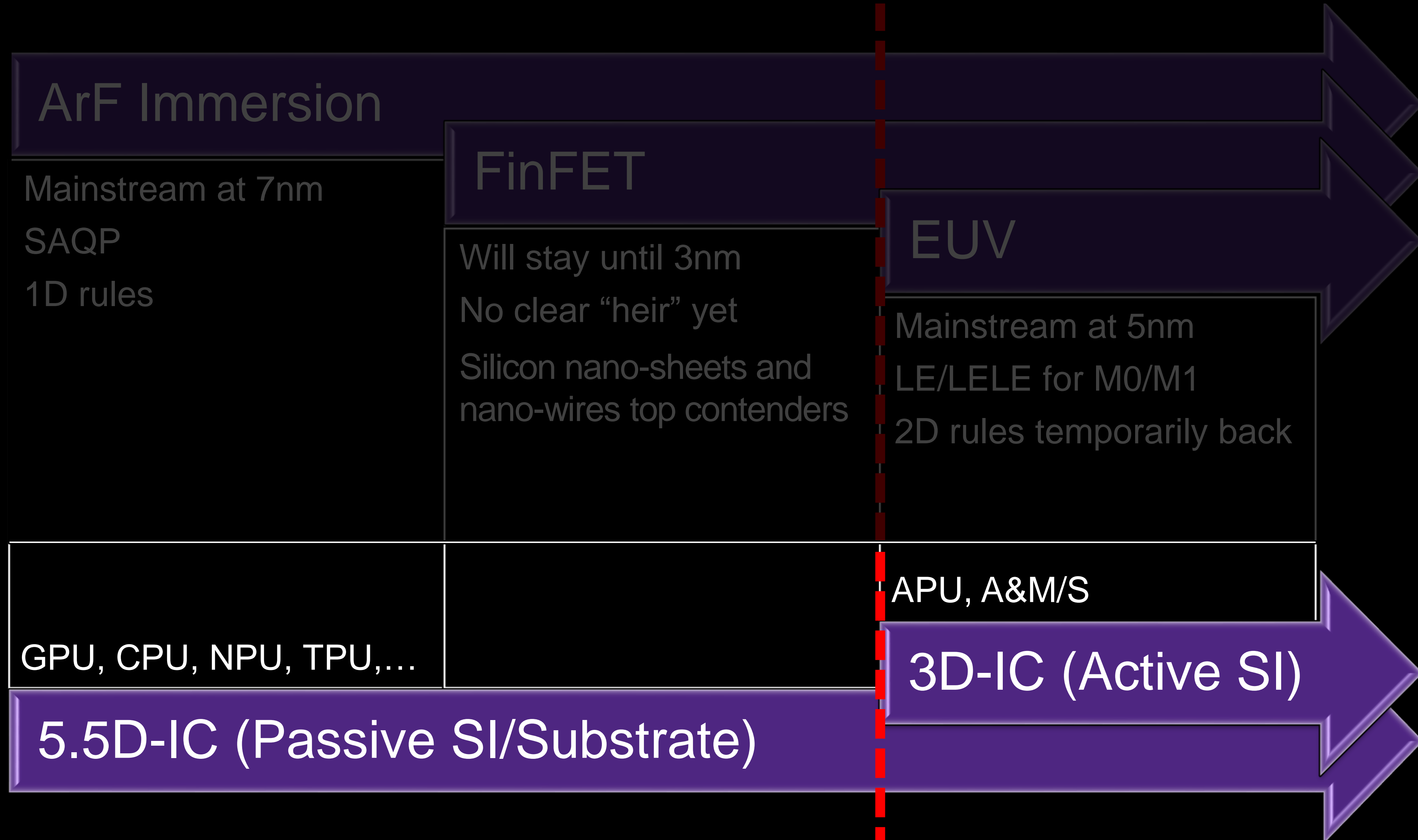
Where Do We Stand ? What Lies Ahead ?

Heterogeneous Integration



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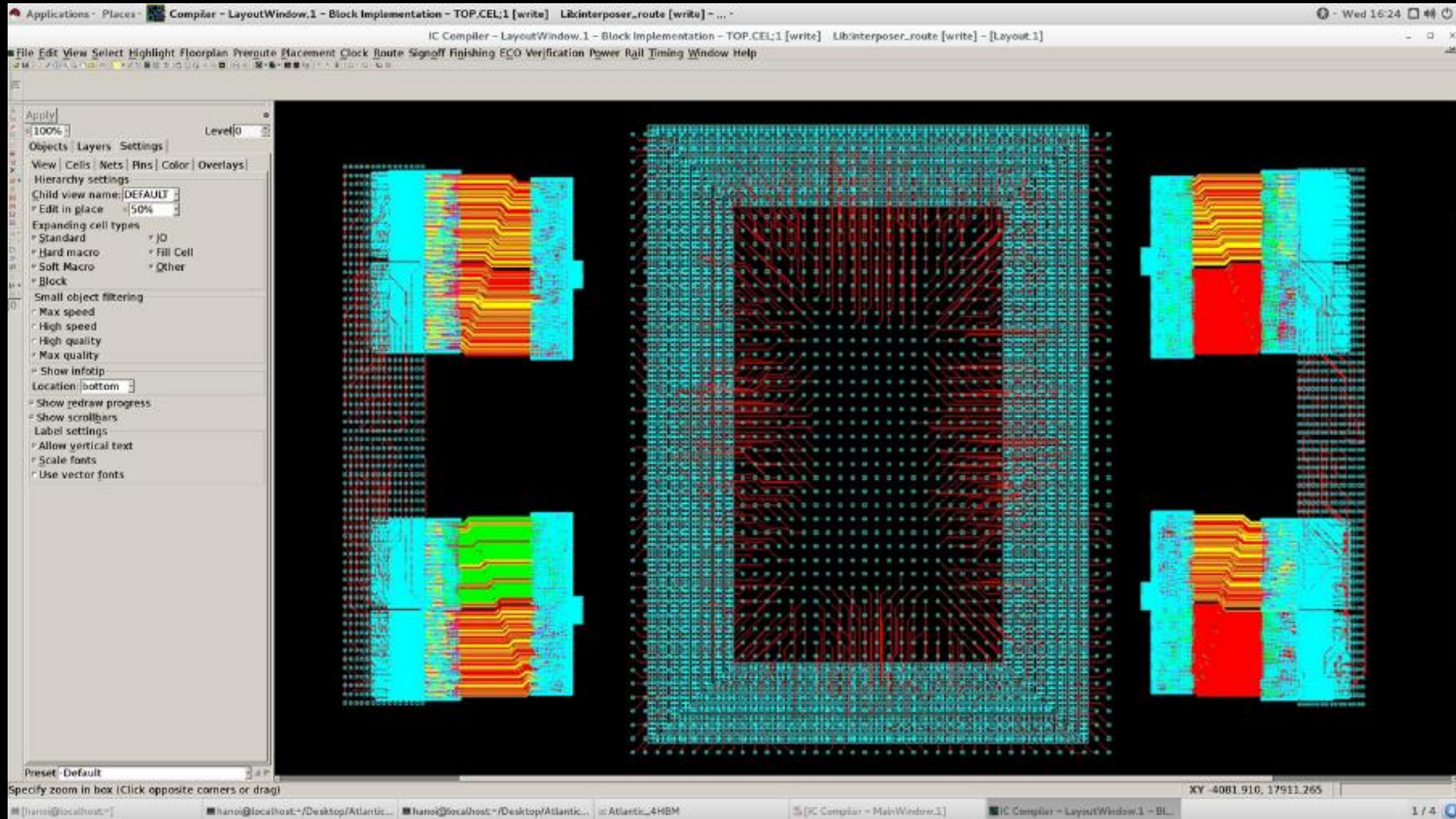
Integration Implications – Beyond The Die

Multiple Die/Stacks Onto Multiple Silicon Interposers



Source: Synopsys Research, 2017

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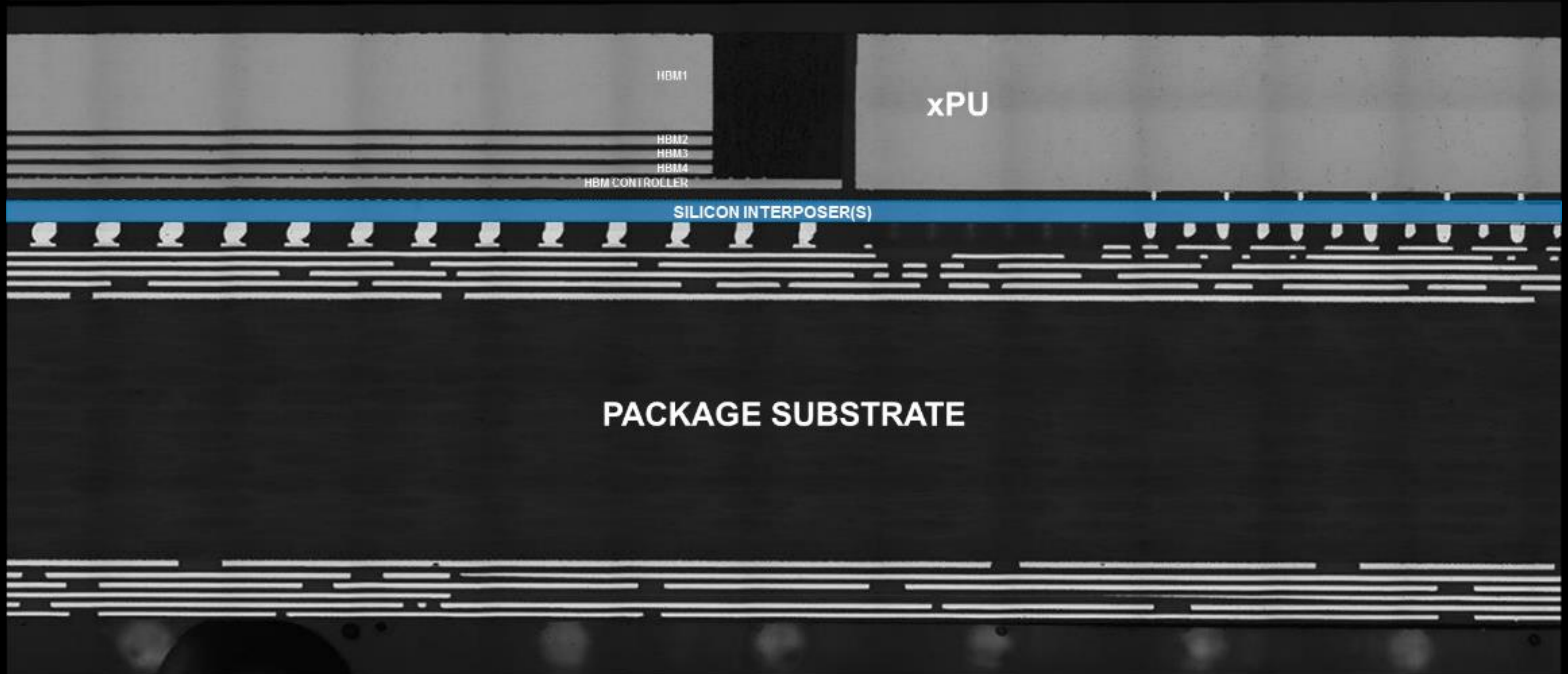
Integration Implications – 2.5D-IC

Multiple Die/Stacks Onto Multiple Silicon Interposers



“Pascal” 5.5D-IC (3D + 2.5D) Integration; Source: L. Nyland, et al., NVIDIA, GPU Technology Conference 2016

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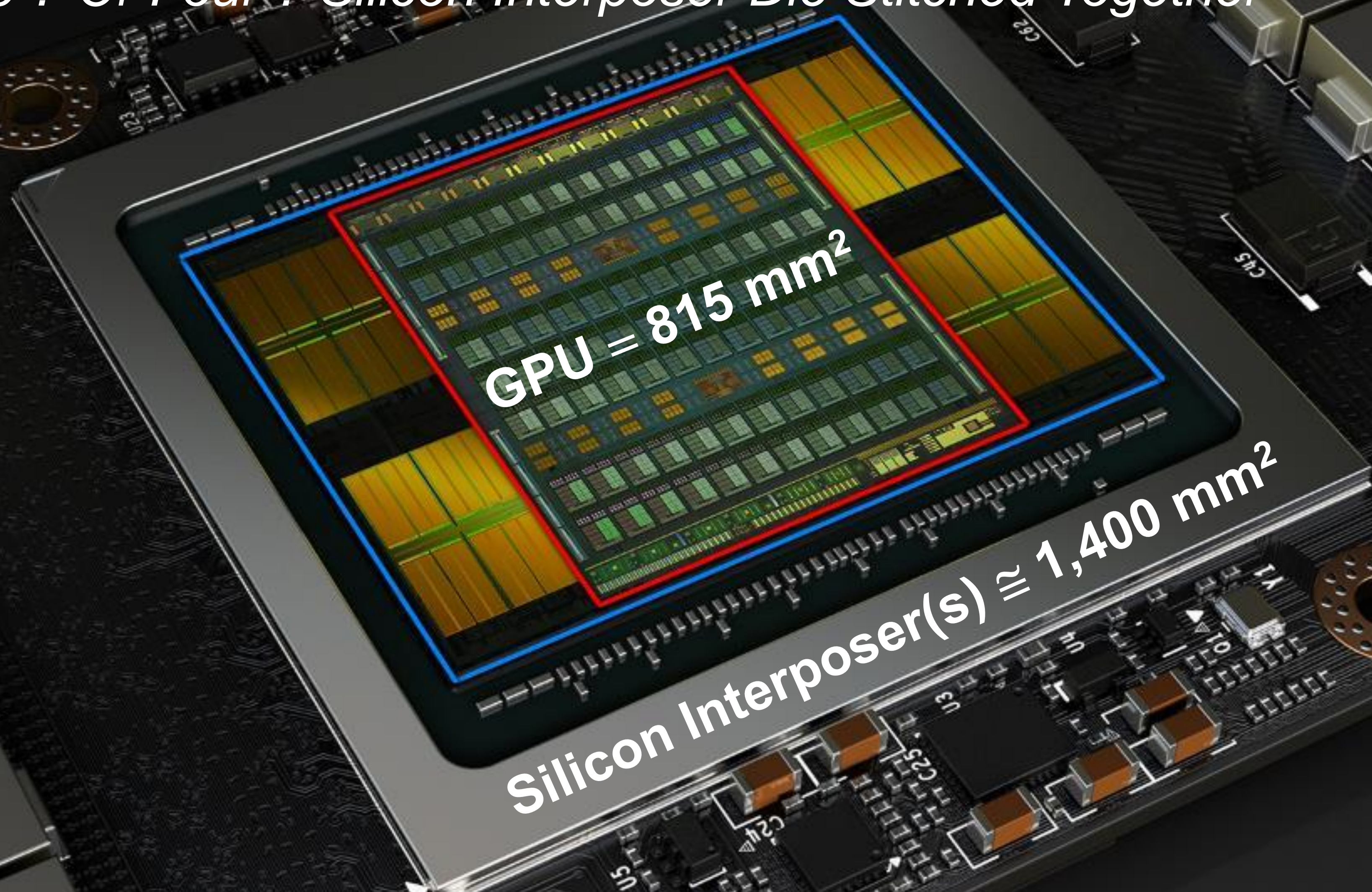
Typical 5.5D-IC (3D + 2.5D) HBM-Based Application

GPU Die (21B Transistors @ 12 Nanometers) + 4 HBM2 Stacks (4 × 4GB) Onto Two ? Three ? Or Four ? Silicon Interposer Die Stitched Together

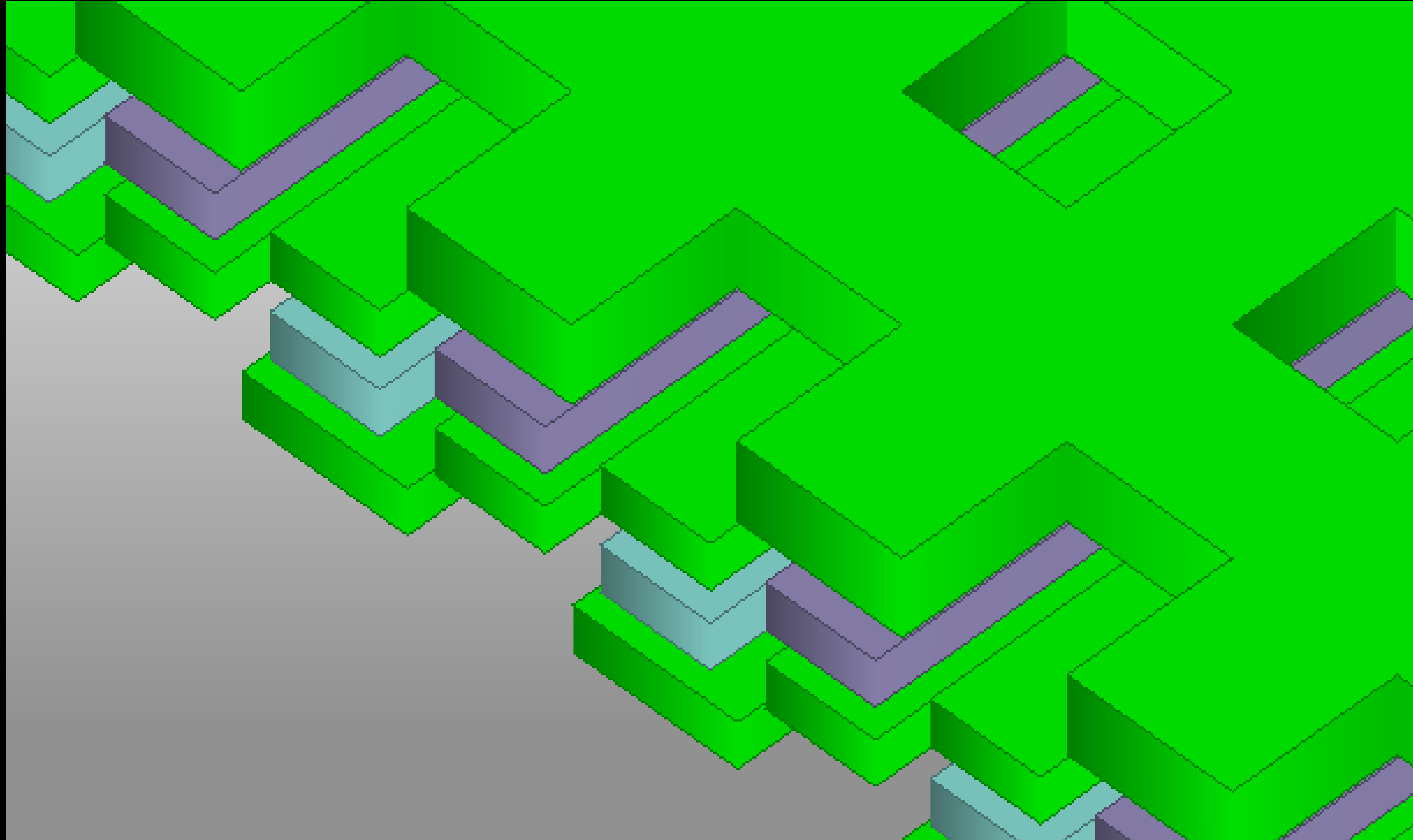


"Volta" 5.5D-IC (3D + 2.5D) Integration; Source: J.-H. Huang, et al., NVIDIA, GPU Technology Conference 2017

HBM2 Die-To-Die Routing Onto The Silicon Interposer

Signals Routed on M2 & M3, Offset by One Track, Run Between VSS Routes

VSS Mesh Provided on M4 (AP) and M1 for M3 & M2 Shielding, Respectively



Source: Synopsys Research, 2016 *(Provisional Patent Application Filed on December 6th, 2016)*

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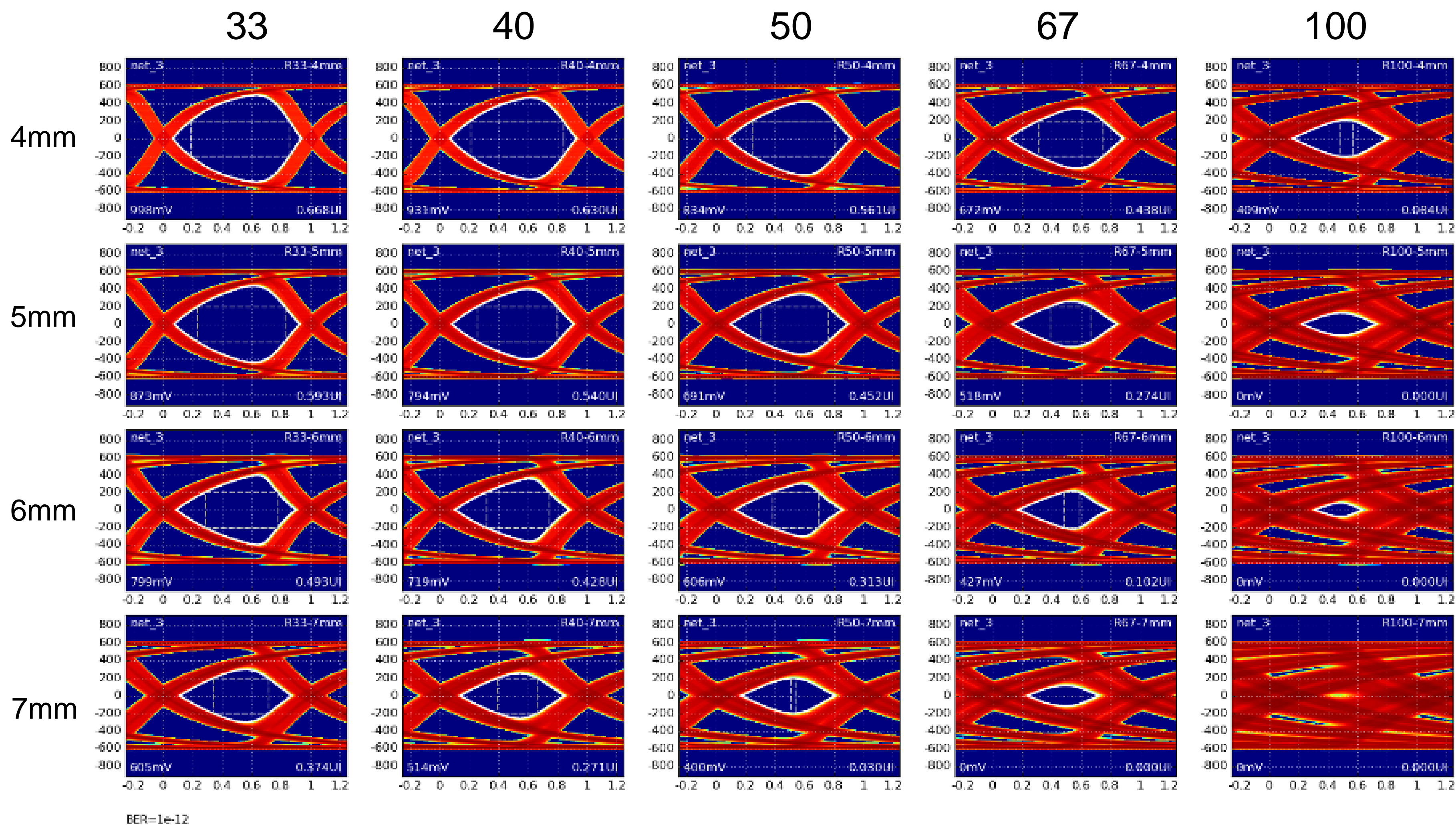
HBM2 Die-To-Die Routing Solution Space

Driving Strength (33, 40, 50, 67, 100 Ω) and Channel Length (4, 5, 6, 7 mm)



- Assuming Linear Ideal IO model at 2.4Gbps speed
- VDD=1.2
- Cpad@PHY = 0.4pF
- Cpad@DRAM = 0.4pF
- TX Jitter = 0.1UI UDJ
- Expected RX metric (FOM) = 0.5UI
- 4mm and 5mm will pass the FOM with some driver strength(s)

Source: Synopsys Research, 2017 *(Provisional Patent Application Filed on December 6th, 2016)*

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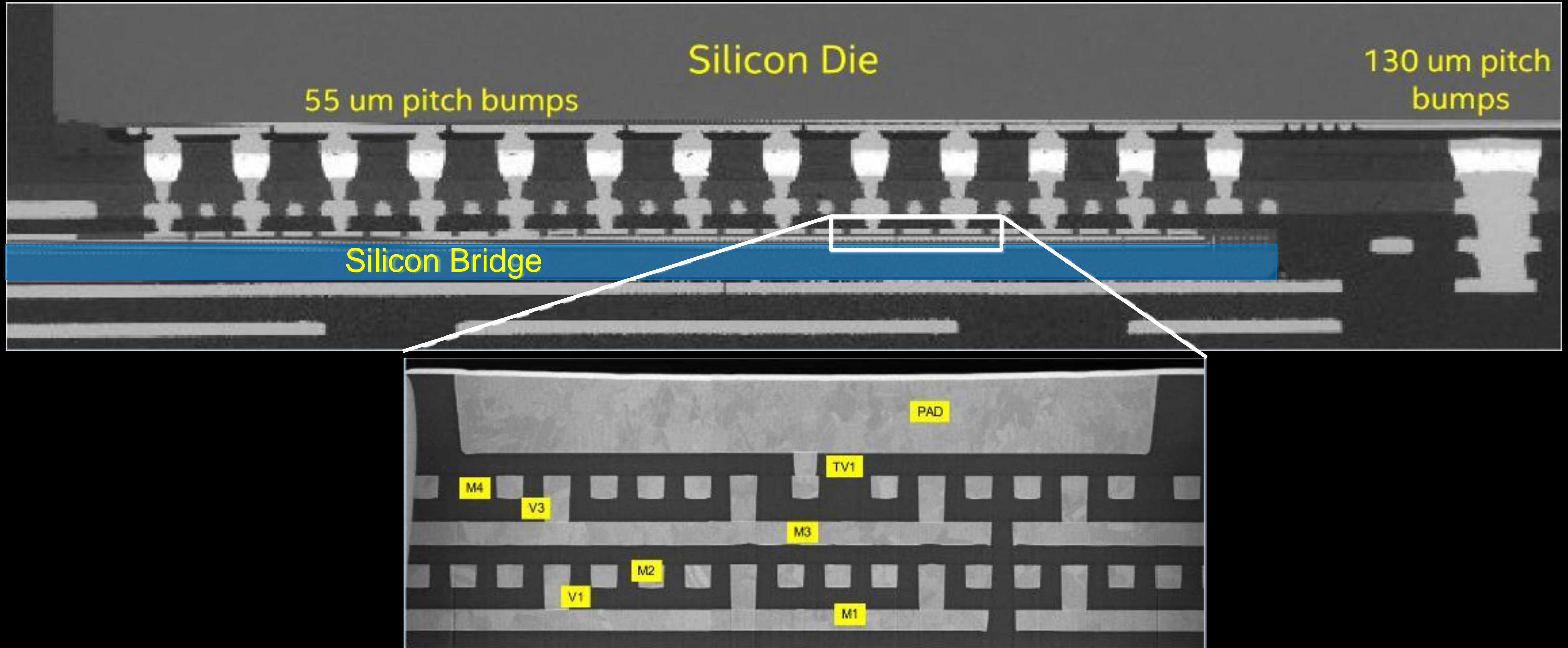
Integration Implications – 2.5D-IC

Multiple Die/Stacks Onto a Package Substrate with EMIB



10 Nanometer EMIB; Source: M. Bohr, Technology & Manufacturing Day 2017

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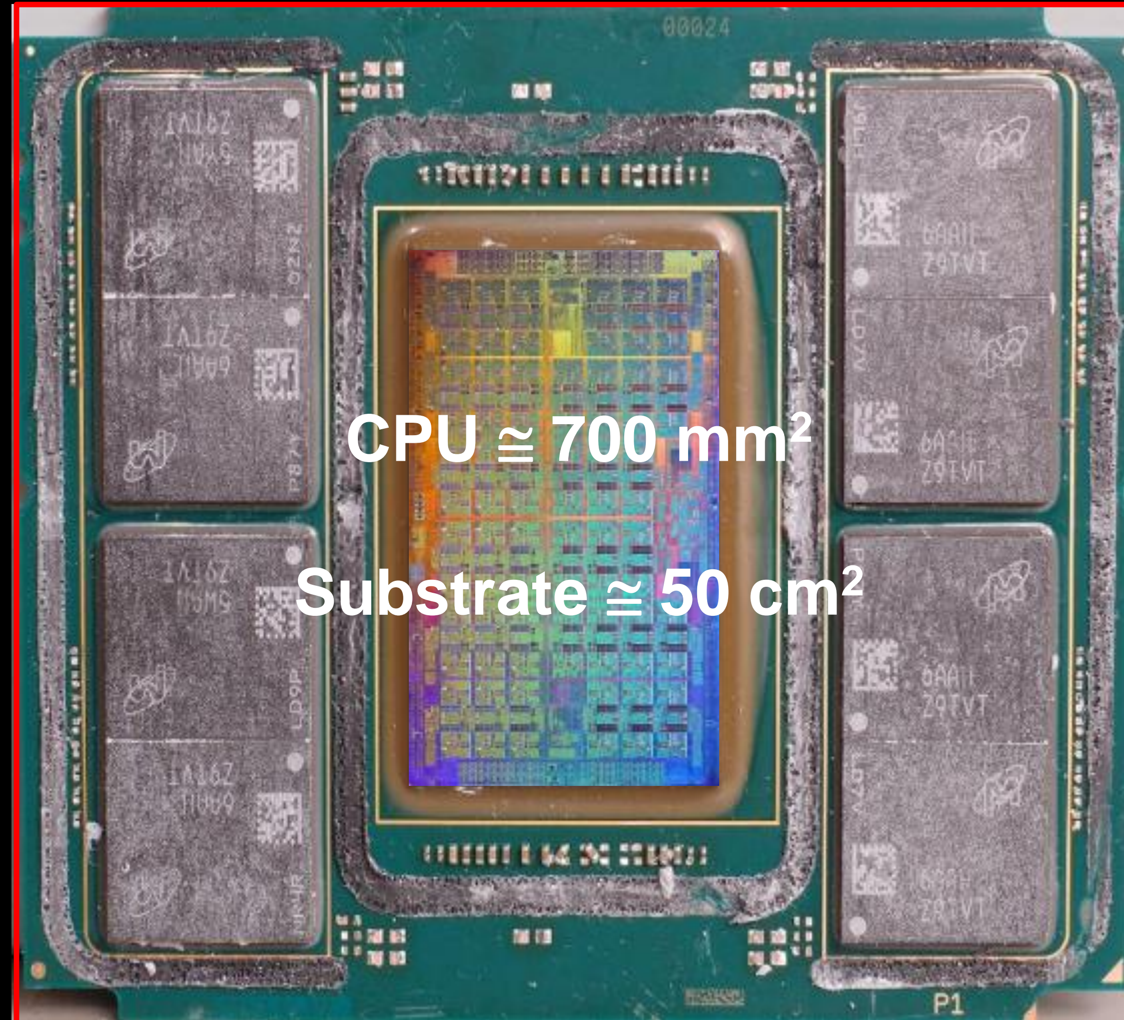
Typical 5.5D-IC (3D + 2.5D) Application

CPU Die + 8 HBM1 Stacks (8 × 2GB) Onto a Package Substrate with Intel Embedded Multi-Die Interconnect Bridge (EMIB)



"Knights Landing" Xeon Phi 5.5D-IC (3D + 2.5D) Integration; Source: Intel 2016 ; Synopsys Research 2017

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Agenda

- ⇨ Where Do We Stand & What Lies Ahead
- Lithography & Devices
- ⇨ Design And [Process] Technology Co-Optimization
- ⇨ Back To… The Future !
- Integration
- ⇨ Closing Remarks

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Closing Remarks

- Our ability to etch taller/thinner fins went the extra-mile, thus extending FinFET lifespan beyond the most optimistic forecasts
  - GAA expected to replace finFETs at 7nm, but managed to push finFET down to 5nm
- EUV is finally here, and will be introduced at some point for 7nm
  - There are still drawbacks to be solved, such as power source degradation, mirrors, pellicles, resists, wafer planarization, metrology, etc
- EUV is not the panacea some dreamt about
  - EUV is actually a very expensive etchnology
  - Multi-patterning will be back at 5nm
- 3D-IC, attractive because of memory and bandwith requirements, now being used in many applications: CPU, GPU, TPU, Network Processors (NPU)

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Closing Remarks

- A lot of the challenges of the coming technologies fall on physical design
  - Sheer complexity remains the #1 challenge:
    - 1T transistors at 3nm (30Å) translate into 100B placeable instances
    - # of polygons & LRC values may exceed 1P = 10^{15} = 50 bits
    - Significantly more complex placement rules
  - Lithography changing balances
    - Transistors shrink much faster (30% linear, 50% area) than interconnect (20%)
    - Number of pins/gate stays equal, less tracks per cell, so routability is the key problem
  - Rule complexity, both placement and routing, and "special" cells – e.g. via ladders, impact the physical side of synthesis. Increasing dependence on placement, global routing, track assignment, and possibly even further
  - IC integration brings challenges beyond the die
    - Partitioning before place & route

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The BUCK STOPS here!

Some Implications Brought In By The Coming Semiconductor Technologies

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