

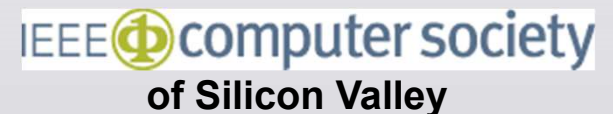


Welcome to EDPS 2017

Electronic Design Process Symposium

www.ieee-edps.org

Shishpal Rawat
General Chair





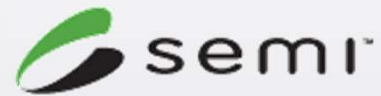
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EDPS – A new beginning in Silicon Valley

Bringing Design, Test & Manufacturing together - Application of new techniques across silos


Closer to home – reduce travel & time away from work

Closer interaction with academia – Mutually beneficial interaction



Great Line-up in store for you

<p>Antun Domic CTO, Synopsys Exploit close relationship of design & manufacturing to accelerate product intro</p>	<p>Zoe Conroy Sr. Manager, Cisco Using System level testing as a conduit to HVM</p>	<p>Jim Hogan Private Investor EDA industry's participation in cognitive age: The fourth industrial revolution</p>	<p>Pankaj Mehra VP, Western Digital Getting EDA ready for the data centric architecture</p>
<p>Design Acceleration Rajesh Gupta, John Lee, CP Hung, Bill Bottoms</p>		<p>Driving to Higher Yield Keith Arnold, Asim Salim, Gerard John, Juan Rey</p>	
<p>Accelerating Debug & Validation Gajinder Panesar, Cynthia Cook, Al Czamara, Vikas Kumar</p>		<p>Machine Learning Paul Franzon, David White, Rob Aitken, Jeff Dyke, Abhijit Chatterjee</p>	



EDPS 2017

- 20+ Speakers; 70 attendees
- Attendees
 - Approx. 70% (50) new to EDPS
 - Diverse representation: Intel (9), Synopsys (4), Keysight (4), Mentor (3), Cadence (3) + others.....
- 4 keynotes
- Great Food and Banquet at Embassy Suites (6:30 PM – Thu)



Your EDPS Committee

Aparna Dey

Camille Kokozaki

Darshan Patra

Dwight Hill

Herb Reiter


John Swan

Naresh Sehgal

Shishpal Rawat

Steve Grout

Vivek Joshi



Thank you for coming Have a great symposium

- Please silence your alerts - Our speakers will appreciate that
- Please (as much as practically possible) occupy the back seats if you are taking notes on the laptop.
- Let a committee member know if we can help you with something.
- And most of all - Ask Questions, Provide Feedback to organizers and Network with colleagues