Amkor
Technology®

Amkor Advanced Packaging Technology

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Agenda

- About Amkor
- Advanced Packages
- Architectures

About Amkor Technology

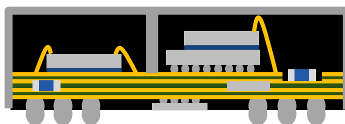
- Amkor Is A Leading Out Sourced Assembly & Test Provider to the Semiconductor Industry
  - Turn-key semiconductor packaging & test services
  - Supports all package technologies across every major semiconductor product segment such as mobile, memory, MEMS, sensors, automotive, power, etc.
  - Technology leader in semiconductor packaging
- Founded in 1968
- 26,700+ employees
- 8,000,000 Sq. Ft. of manufacturing floor space w/ +20 sites
- Presence in 10+ countries
- $3.70B net sales

Common Advanced Packages

WLP

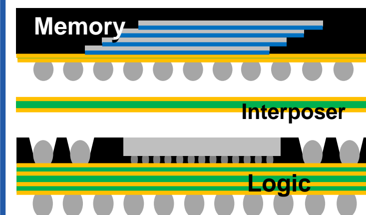
- Low cost
- BLR
- High I/O & large die
- Multi die and passive integration
- 3D structure
- Fine pitch RDL & low cure temp. polymer
- 5s mold
- Profile

SiP



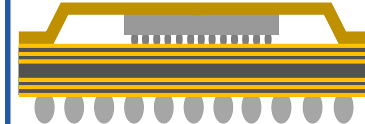
- Low cost
- Active and passive integration
- EMI shield – conformal and compartment shield
- High I/O
- POSSUM™
- Profile

PoP



- Low cost
- Profile
- High I/O and fine pitch interface & BGA
- Fine pitch chip bonding interconnect
- Advanced substrate
- Interposer PoP
- Warpage and memory stacking

Large Flip Chip

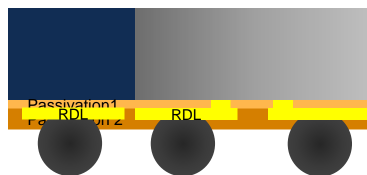


- Large body and die
- Fine pitch bump interconnect
- Reliability
- Co-planarity
- Thinner substrate
- 2.5D integration
- HBM integration
- Low cost

Amkor's Advanced Fan-Out Packages

WLFO

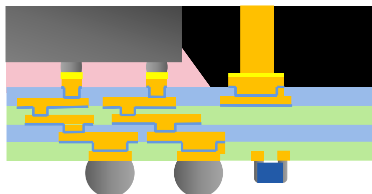
Wafer Level Fan-Out



- Single or multi-die
- 6~12 µm L/S RDL
- Die-RDL-BGA

SWIFT™

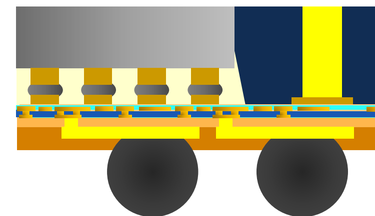
Silicon Wafer Integrated Fan-Out Technology



- Single or multi-die, SoC partition, 3D-POP compatible
- Fine L/S RDL 2~5 µm
- RDL-µbump-Die-BGA
- Small form-factor

SLIM™

Silicon-Less Integrated Module

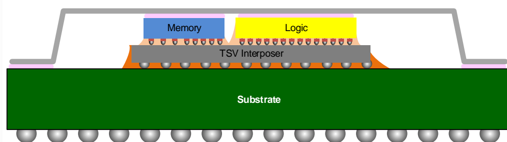


- Multi-die, SoC partition, 3D-POP compatible
- Foundry BEOL with < 2 µm L/S
- BEOL-RDL-µbump-Die-BGA

Amkor's TSV Packaging Capability

2.5D FCBGA

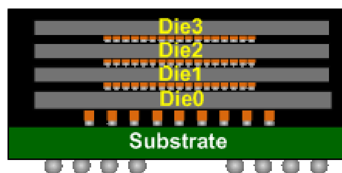
2.5D TSV Flip Chip BGA



- Homogenous & heterogeneous die integration
- Multi-die, side by side
- < 2 µm L/S D2D
- Bare Die, Overmold, Lidded

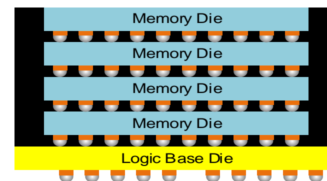
3D-TSV FCCSP

3D TSV Flip Chip CSP



- Memory/Memory, Logic-Logic, and Logic/Memory Configurations
- Tier-to-tier stacking
- Overmold and Exposed Die

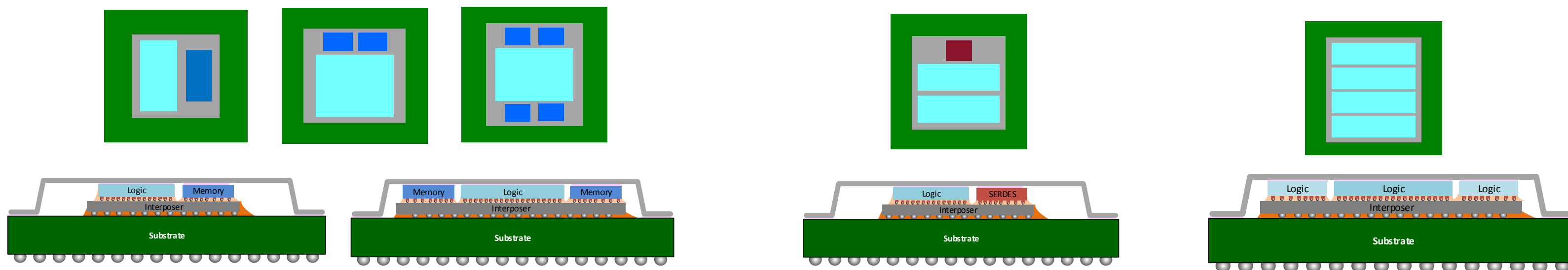
TSV WLCSP

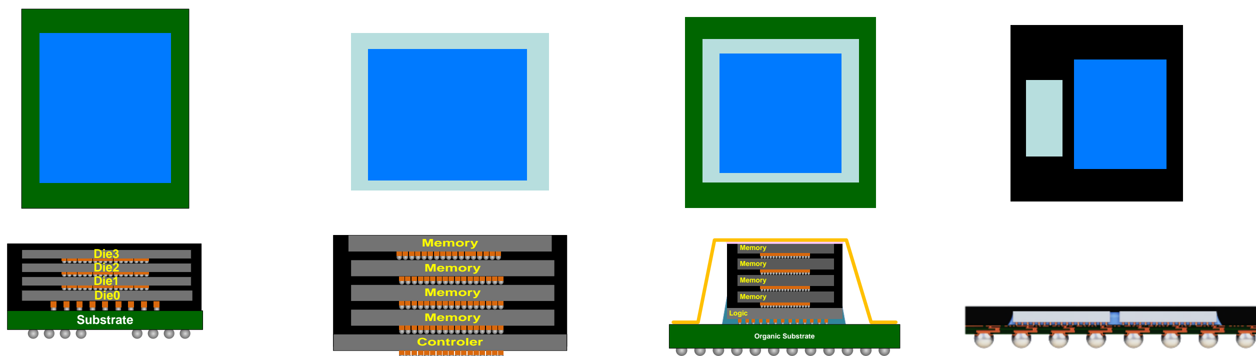


- 2.5D & 3D configurations
- Multi-die, side-by-side (2.5D) and tier/tier stacking (3D)
- Foundry logic & BEOL with TSV integration
- Bare die & Exposed die assm.

Architectures

- Common architectures for logic and memory integration





Thank You