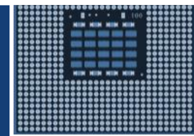
Open-Silicon.com

490 N. McCarthy Blvd, #220
Milpitas, CA 95035
408 240-5700
HQ

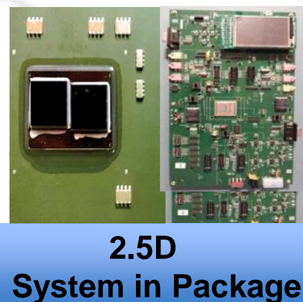


CONFIDENTIAL

Multi-Die ASIC SiP (System in Package) Manufacturing

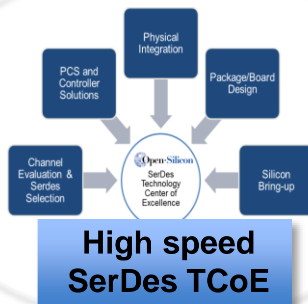
Open-Silicon

Spec2Chip

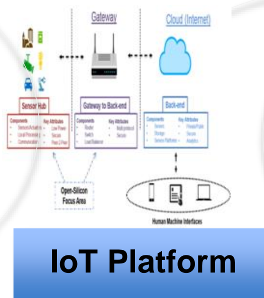


2.5D System in Package

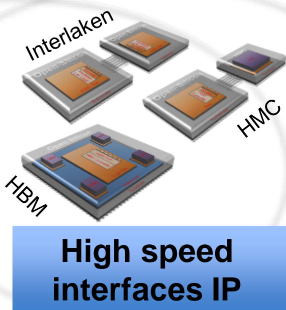
ARM TCoE



High speed SerDes TCoE



IoT Platform

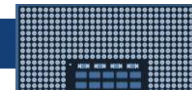


High speed interfaces IP

Asim Salim

VP Mfg. Operations

- 20+ experience is Semiconductor Operations Engineering (Product Engineering, Device Physics, Reliability, Supply Chain)
- Early adopter of SiPs – shipped >5M mobile graphics processors with DDR KGD memories in 1999



Multi-Die ASIC SiP (System in Package) Overview

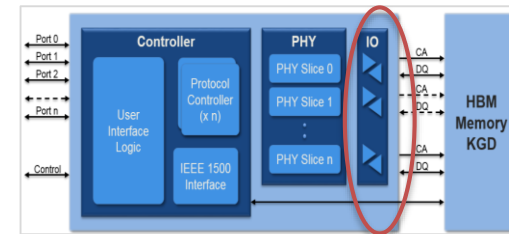
First ASIC-vendor to bring 2.5D to prototype silicon (Avatar)
Awarded best chip-design at ARM TechCon 2013,Santa Clara

Why 2.5D has a future → Memory Wall

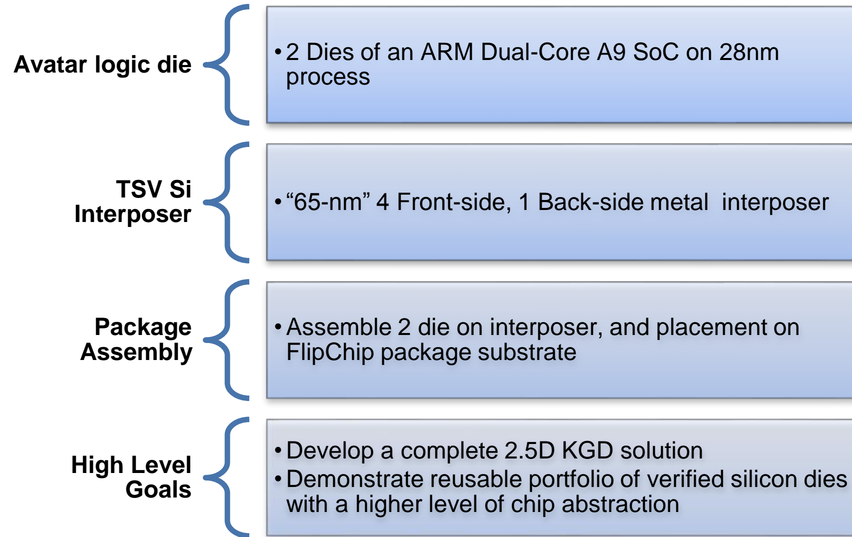
- Processing can see 50-75% idle times
- CPU performance is increasing 4x-8x compared to memory performance
- Power is a big issue
  - HBM uses wide-IO to reduce frequency → lower power
- IO space is limited (packaging)
  - Memory cannot become wider
- Faster data
  - USB, PCIe, SATA, all are faster now
  - Multiple interfaces vie for same DRAM
  - Larger on-chip storage is needed
  - <u>Video/graphics is the biggest contributor</u>

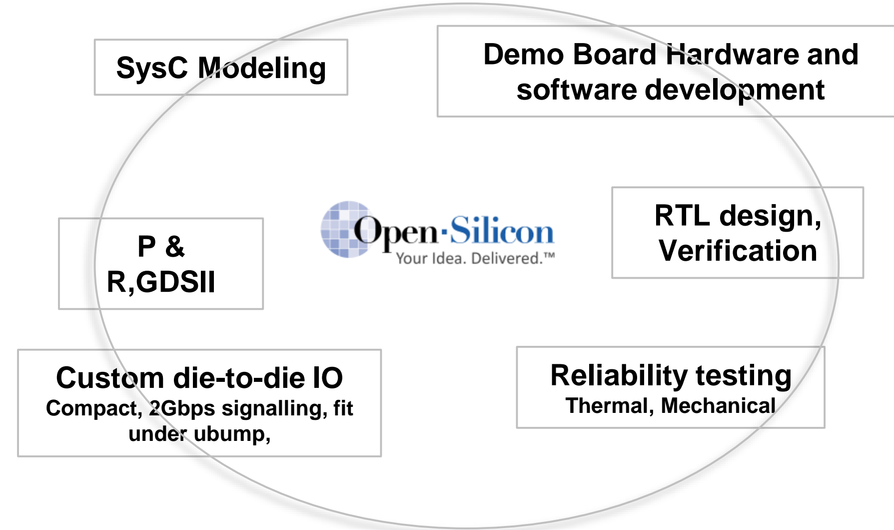
High Bandwidth Memory

- *In-house design, Hard-IP*
- *Leveraging 2.5D die2die "channel" experience from Avatar*
- *e.g. on Interposer interconnect electricals, ESD, DfT, etc.*
- *CMOS IO driver, 1GHz/2Gbps DDR with light output loading (1 – 8mm interposer trace)*
- *Electrically compatible with JEDEC HBM DRAM spec*
- *TSMC 16FF-GL Implementation*

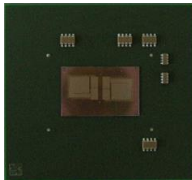


Avatar 2.5D Solution Demonstration

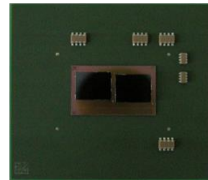




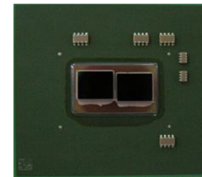
Interposer + Cap



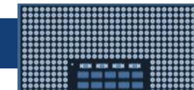
w/AVATAR



w/Underfill

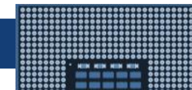


Lid attach



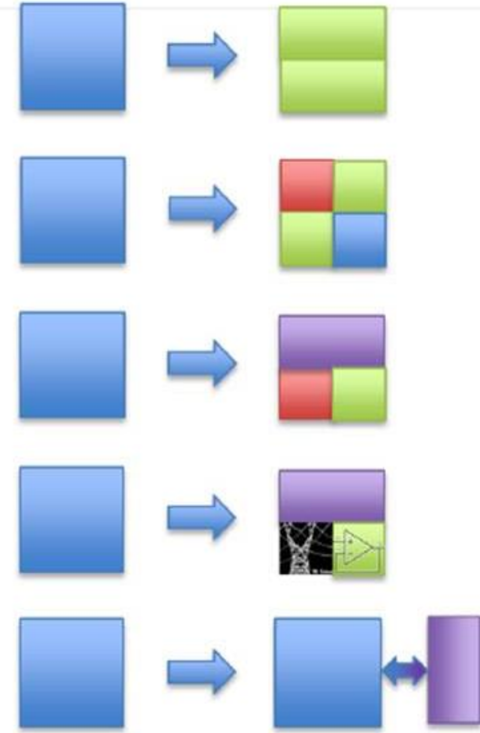
Building the Ecosystem

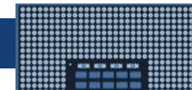
Foundries	Interposer Foundries	OSATs	Semi's IP Houses Standard. Committees	KGD vendors	DFT/Test	EDA
Collaboration with assembly houses (OSATs) for TSV/Interposer construction	Traditional Fabs: TSMC, GF, UMC	ESD guidance	Interposer optimized D2D interfaces	**Memory** High Bandwidth DRAM Stack KGD	e.g. IEEE P1838 Working Group	Area-IO floor planning, die P&R, integration, and verification
Models and PDK for Interposer silicon process e.g. for P&R, extraction and physical verification	Specialized Fabs: Innotera, Tezzaron	Test tooling, e.g. Microbump wafer probing	Wide-IO and HBM memory controllers, etc.	**Specialized IP** High speed SERDES	Fine-pitch probe technology for probing micro-bumps	Power, EM, thermal modeling, and ESD analysis
TSMC ,Global Foundries	Organic Interposer: Kyocera	Detailed package reliability				2.5D ATPG



Additional Benefits Of 2.5D Based Design

- Yield Improvement for large SoC die
- Overall power improvement by mixing slow and fast parts
- Risk and Cost improvement due to process node mix
- Die partitioning and optimization for analog, performance, power management, etc.
- Integrating High Bandwidth Memory, flash, or other memory technologies





Challenges

Foundries
- Microbumping,
- > Interposers exceeding reticle size
- Reliability
- Cost

Interposer Foundries
- Keep Costs Low
- Optimize Number of Metal Layers
- Integrate passives

OSATs
- Low ESD environment
- Wafer level processing techniques
- Large stacked package reliability
- Costs

Semi's
IP Houses
Standard. Committees
- New additions and requirements (D2D IOs, ESD)
- new players

KGD vendors
- Standards across suppliers on Test/DFT, delivery metrics

DFT/Test
- Probing Microbumps
- Testing out at many different levels
- High-speed testing at probe

EDA
- Integrated tools connecting core die to interposer, package substrates