XILINX
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Integrated Silicon and Package Solutions

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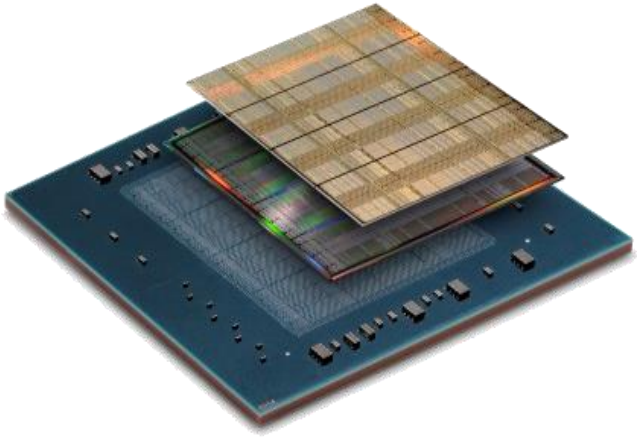
Stacked Silicon Interposer Strategies

- **Motives for adopting silicon interposer technologies include Performance Gain, Miniaturization, Integration of Disparate Silicon Technologies and Cost Reduction.**
- **Xilinx introduced SSIT (Stacked Silicon Interposer Technology) with TSV (Through Silicon Vias) to reduce the cost of creating high end FPGA's**
- **Recent advances are allowing even larger devices to be created.**

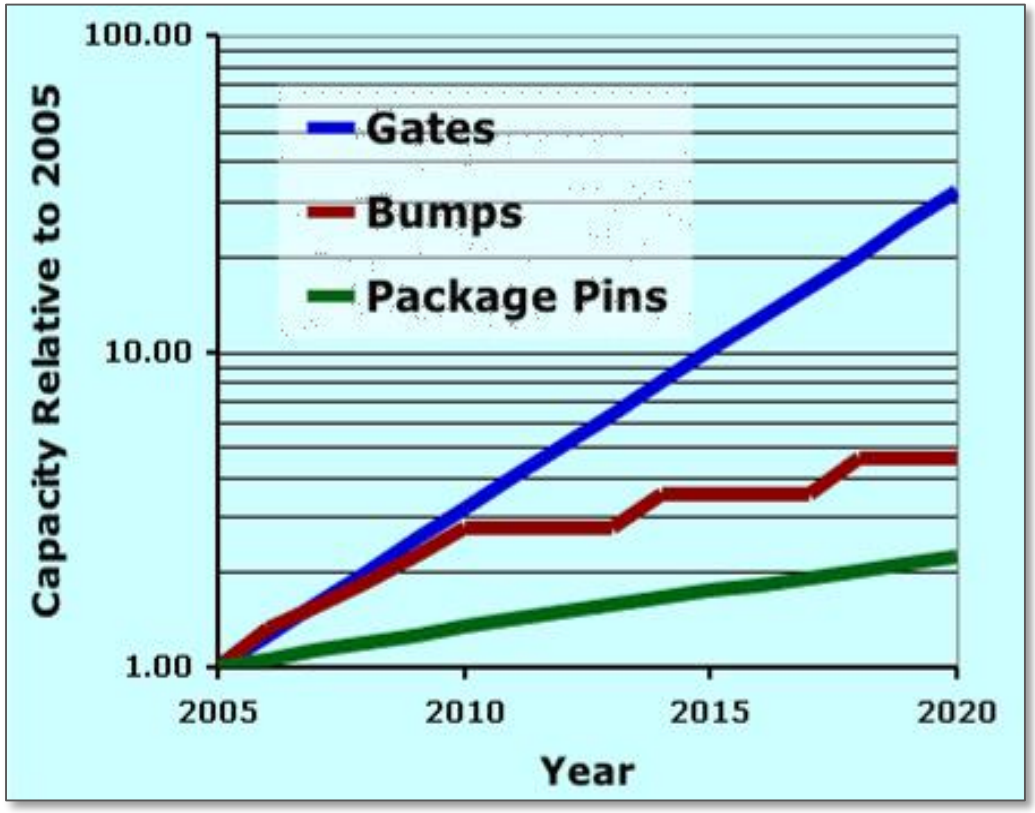
Economics of Xilinx SSIT (2.5D)Entry Point



The Case for Integrated Silicon and Package Solutions

- **It has been observed that the density of die to package interconnect scale more slowly than gate counts and PCB densities improve at an even slower rate.**

- **The continuing demand for more bandwidth and emerging IOT computational demands may accelerate the volume of data being processed.**
- **The "End of Moore's Law" makes the case for integrated silicon and package solutions more compelling.**



The Case for Integrated Silicon and Package Solutions

- **SSIT changes the die interconnect road map from 180/150/130u bump pitch to 45/40/30u micro bump pitch.**
  - Micro bump roadmaps lead to 5 – 10u pitch
  - Radical technologies such as Hybrid Bonding or Capacitive Coupling can eliminate die to die underfills and reduce interconnect pitch to below 5u
- **Integrated HBM eliminates the need for memory buses to and from the package.**
- **Innovative extensions of Interposer technology such as "larger than reticle" interposers and SLIT further reduce cost and increase platform utility.**
- **Integrated platforms eliminate IO drivers and line losses reducing power.**
- **Challenges are Power Density and Cost Reduction**

Summary - Integrated Silicon and Package Solutions

- **SSIT technology was introduced to reduce the cost of large die.**
  - The approach has been extended to facilitate heterogeneous integration on a large silicon platform.
- **A silicon platform closes the IO/package density gap and can eliminate many package/board connections.**
- **Industry Challenges such as Power, Performance, The End of Moore's Law and the IOT Edge Computing are opportunities for Integrated Silicon and Package Platforms.**
- **Power Density and Cost Reduction are the major challenges for Integrated Silicon and package Solutions.**